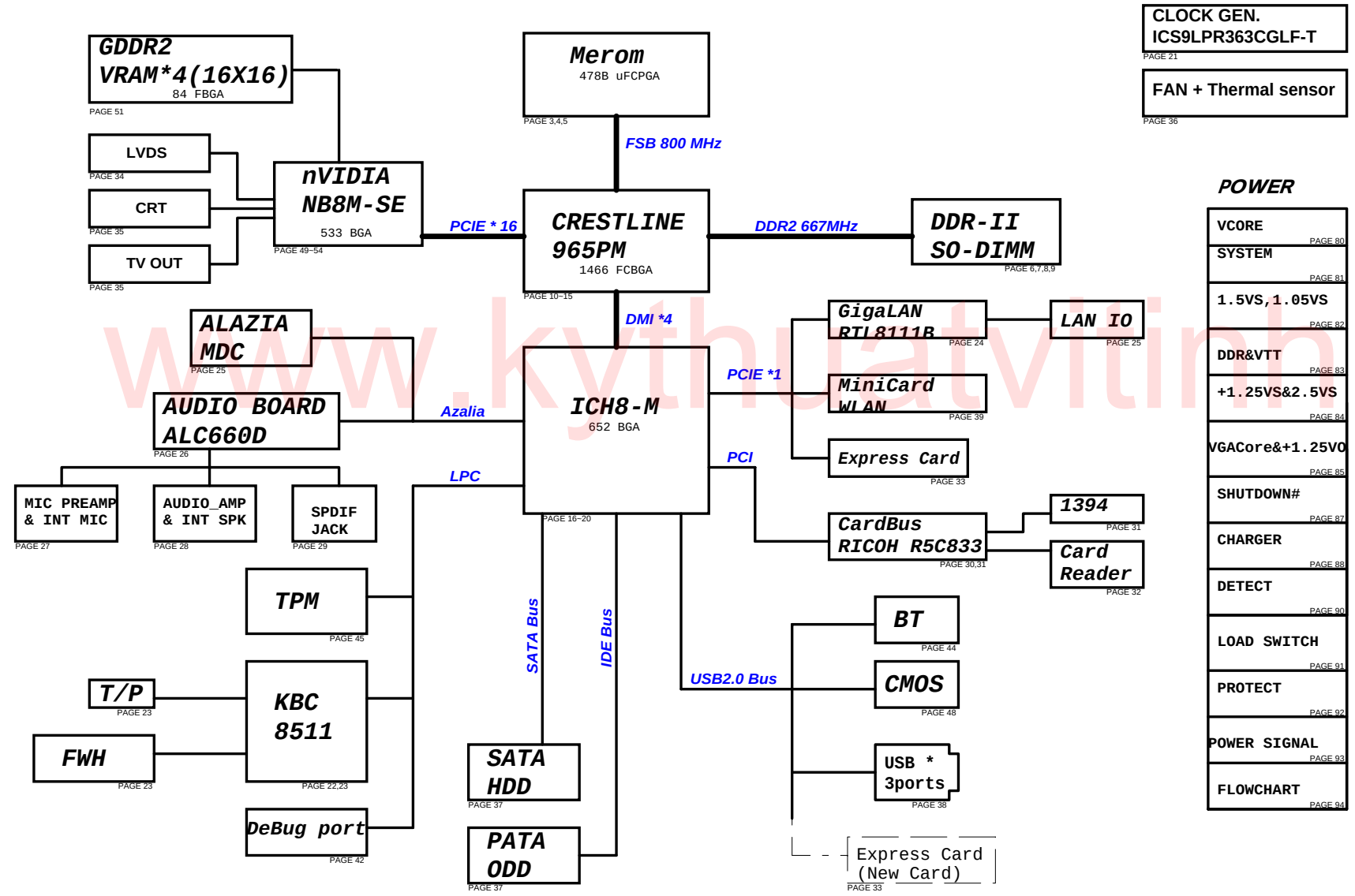
T76S: MEROM/965-PM/ICH8-M/NB8M-SE BLOCK DIAGRAM

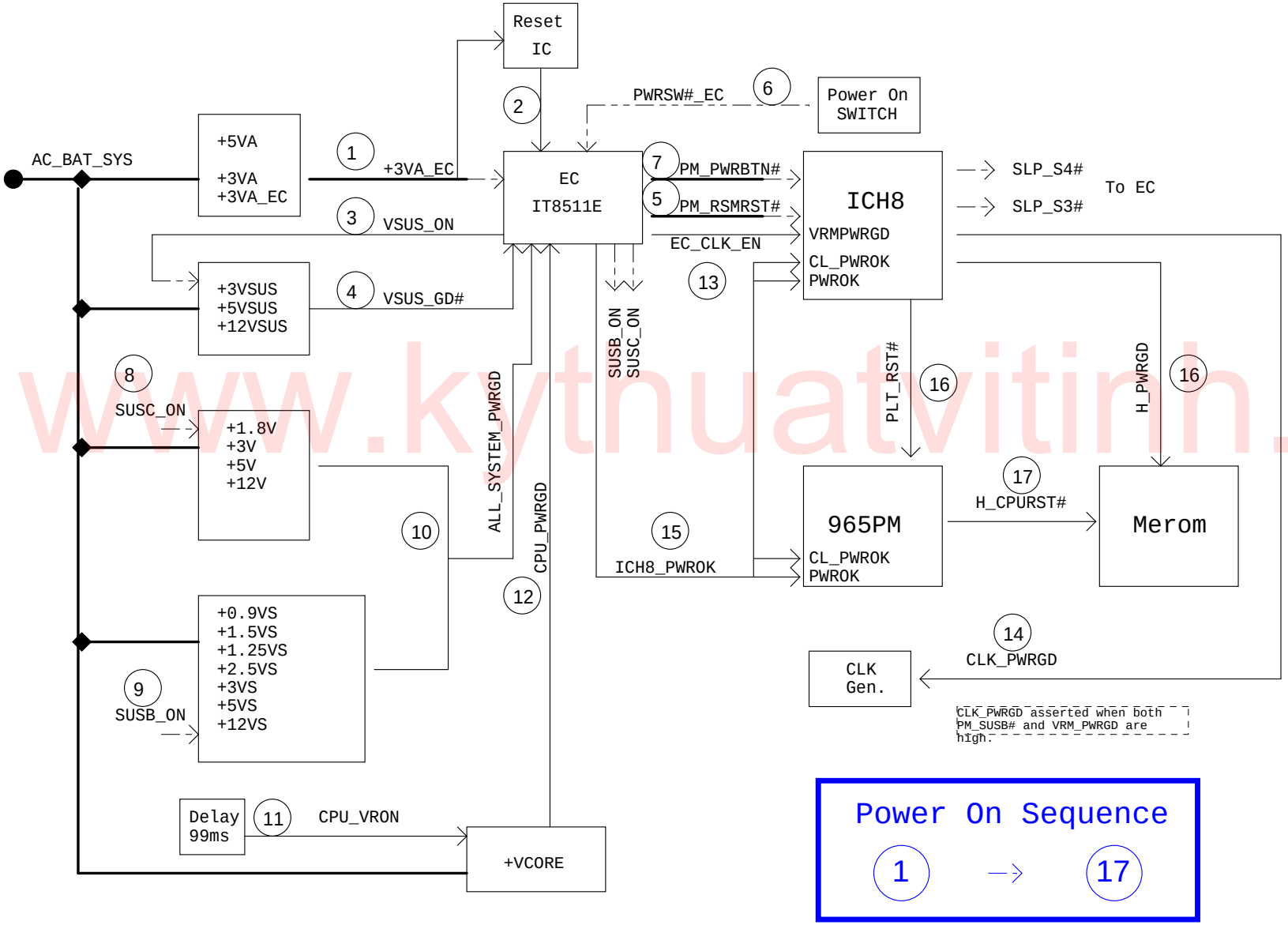


ASUSTeK COMPUTER INC

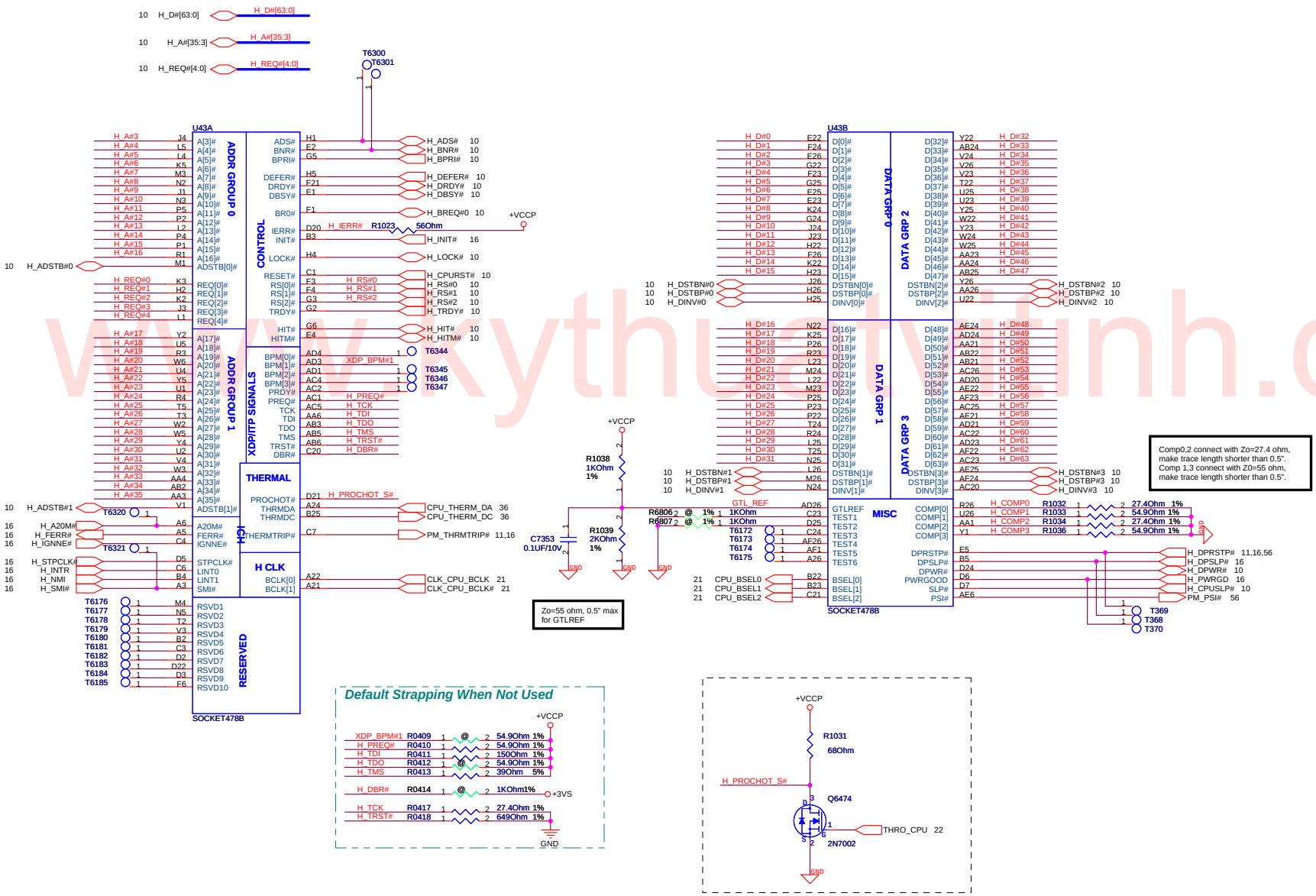
Title : BLOCK DIAGRAM
Engineer: Lorentz_Chang

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 1 of 70



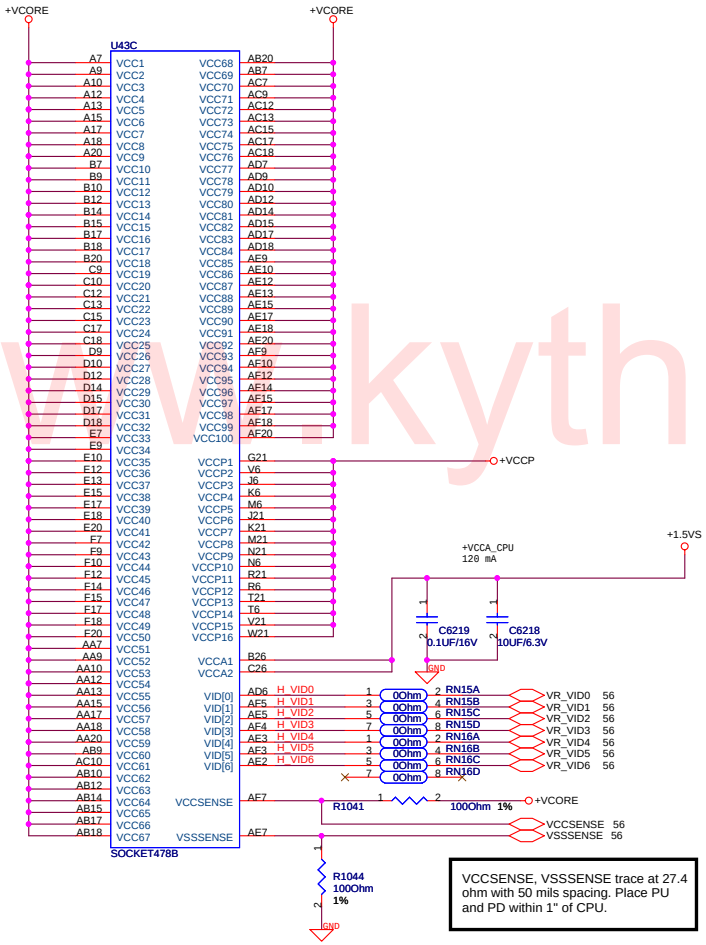
ASUSTeK COMPUTER INC	Title : PowerOn sequence	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 2 of 70	

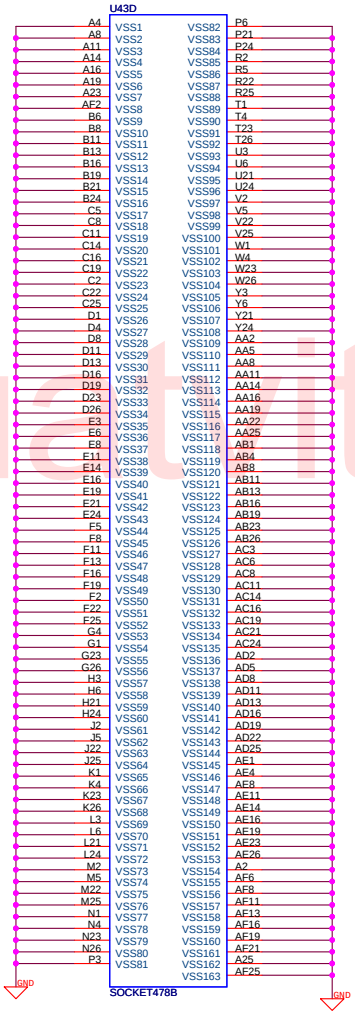


ASUSTeK COMPUTER INC	Title : MEROM CPU (1)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 3 of 70		

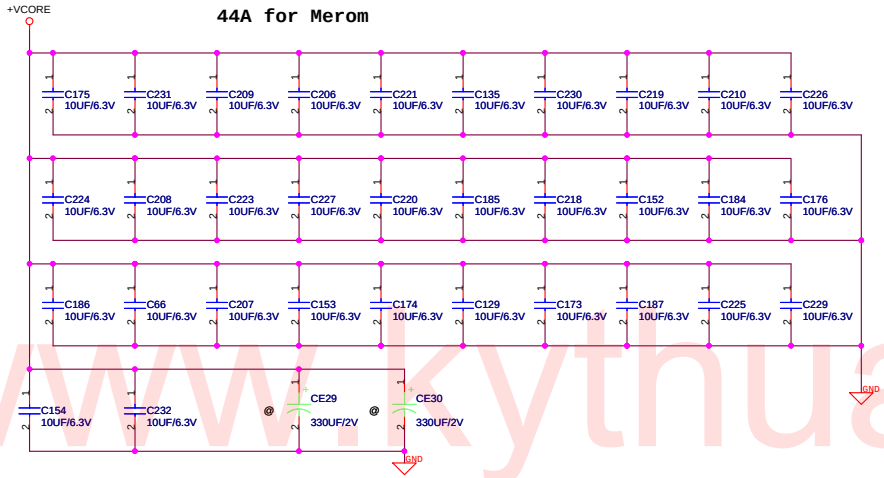
MEROM FSB800 Vcore			
	LFM	TYP	HFM
VCC	0.75V		1.325V
ICC	30.4A		41A

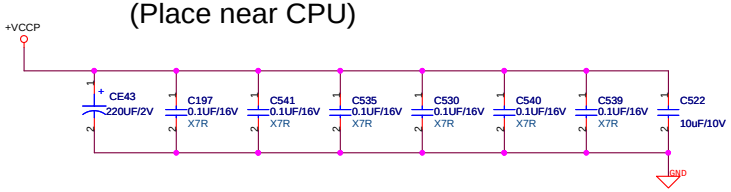
MEROM FSB800 Vcore			
	Min	Typ	Max
VCCP	1.0V	1.05V	1.1V
	Min	Typ	Max
ICCP			2.5A





ASUSTeK COMPUTER INC	Title : MEROM CPU (2)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 4 of 70	





Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	270uF	* 1pcs for CPU

Decoupling for W7S

VCORE	10uF/6.3V	* 32pcs
	330uF/2V	* 2pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

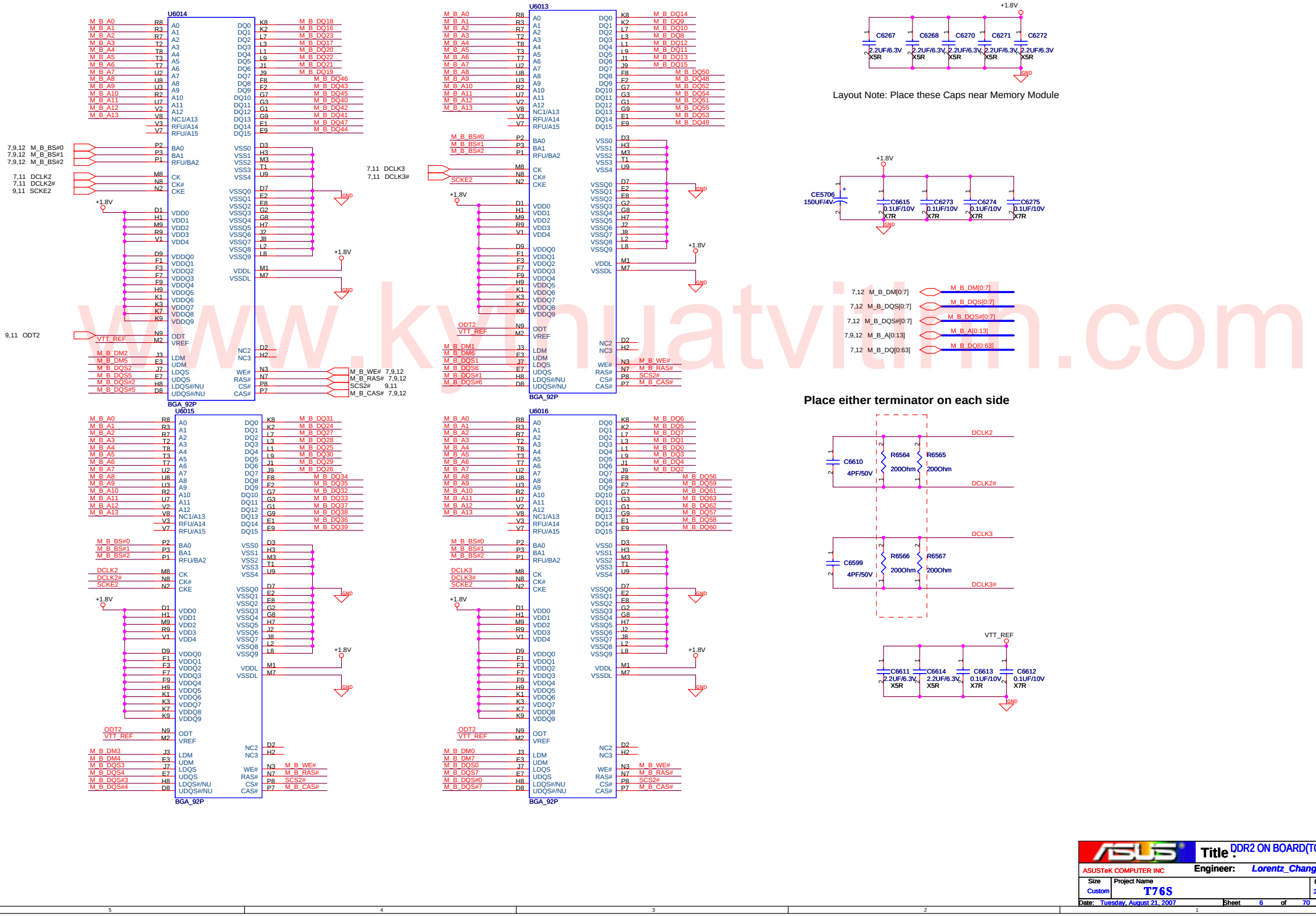
ASUSTeK COMPUTER INC

Title : CPU CAP

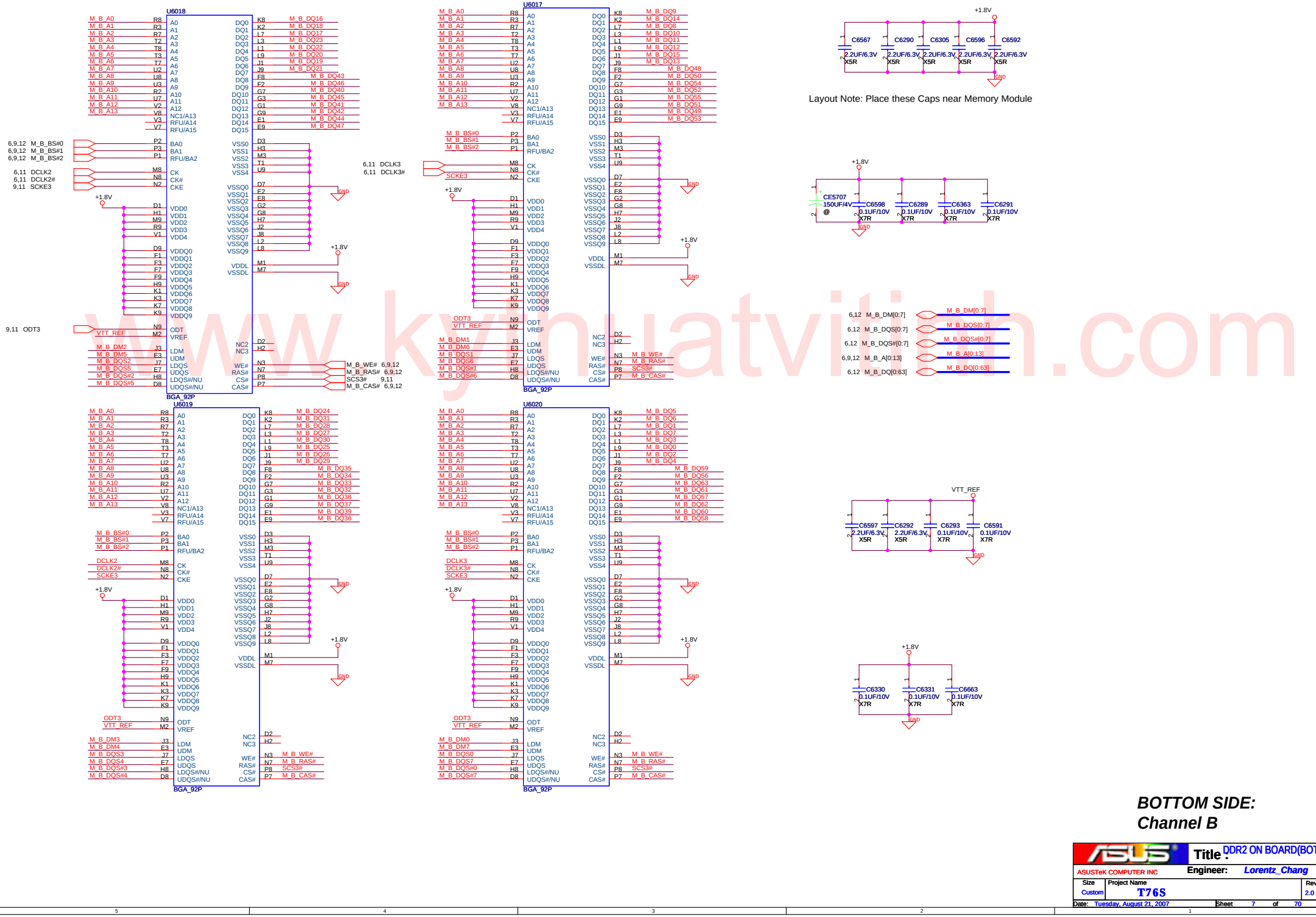
Engineer: Lorentz_Chang

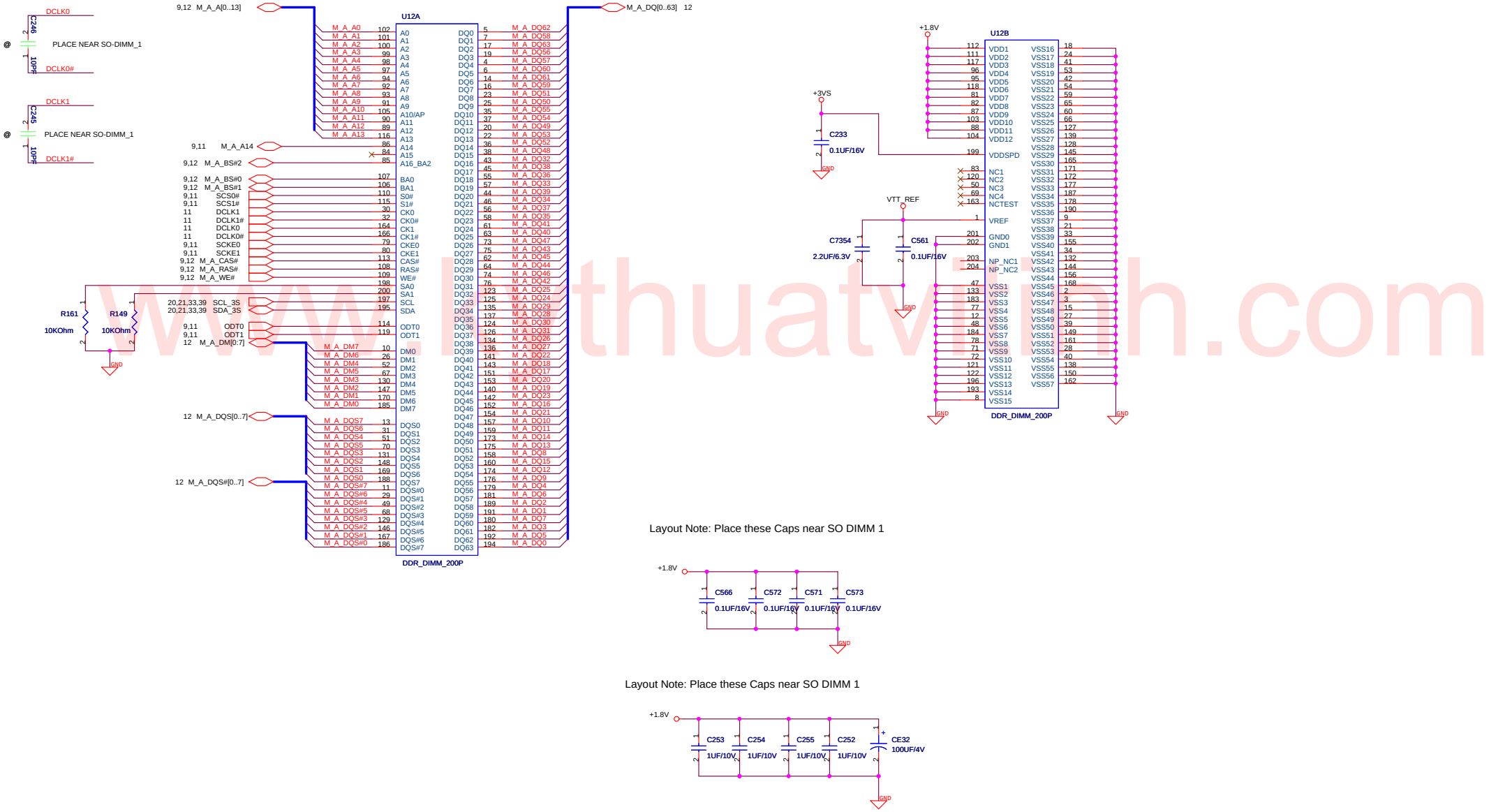
Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 5 of 70



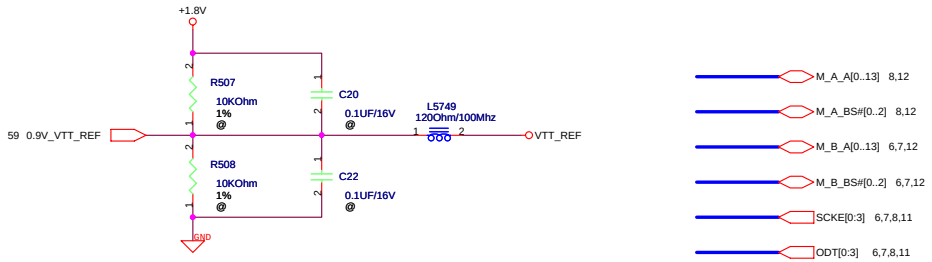
ASUSTeK COMPUTER INC	Title : DDR2 ON BOARD(TOP)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 6 of 70	



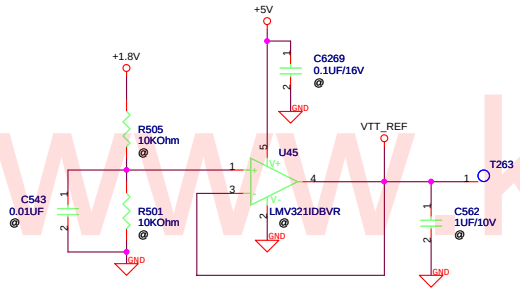


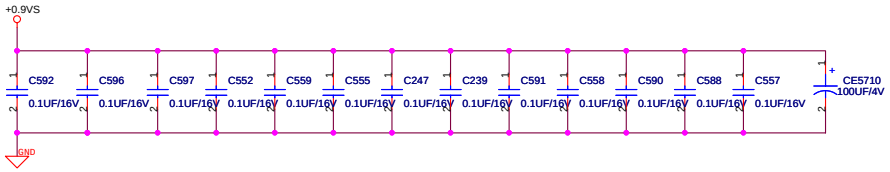
TOP SIDE:
Channel A

ASUSTeK COMPUTER INC	Title : DDR SO-DIMM		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 8 of 70		

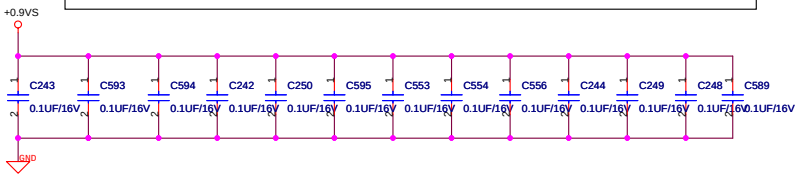


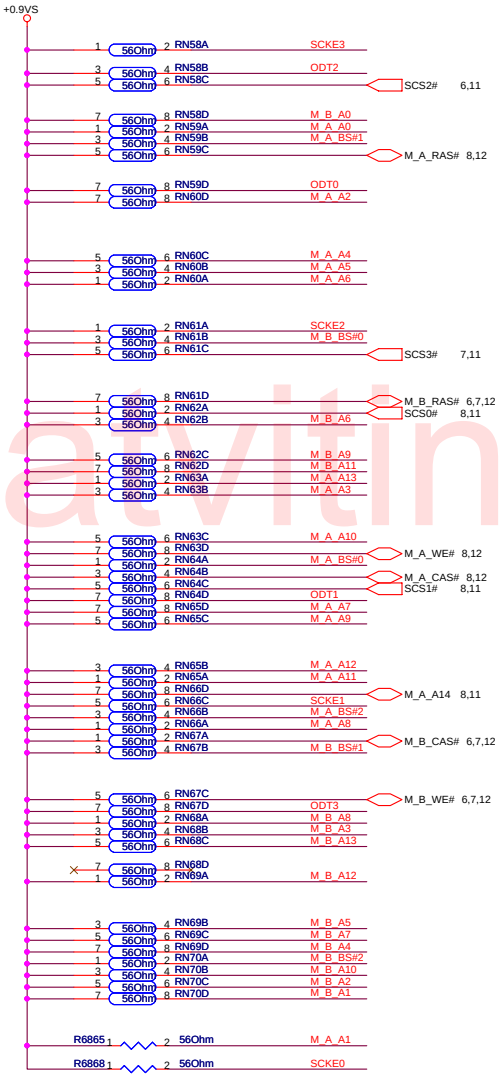
M_A_A[0..13] 8,12
M_A_BS#[0..2] 8,12
M_B_A[0..13] 6,7,12
M_B_BS#[0..2] 6,7,12
SCKE[0:3] 6,7,8,11
ODT[0:3] 6,7,8,11





Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





ASUSTeK COMPUTER INC

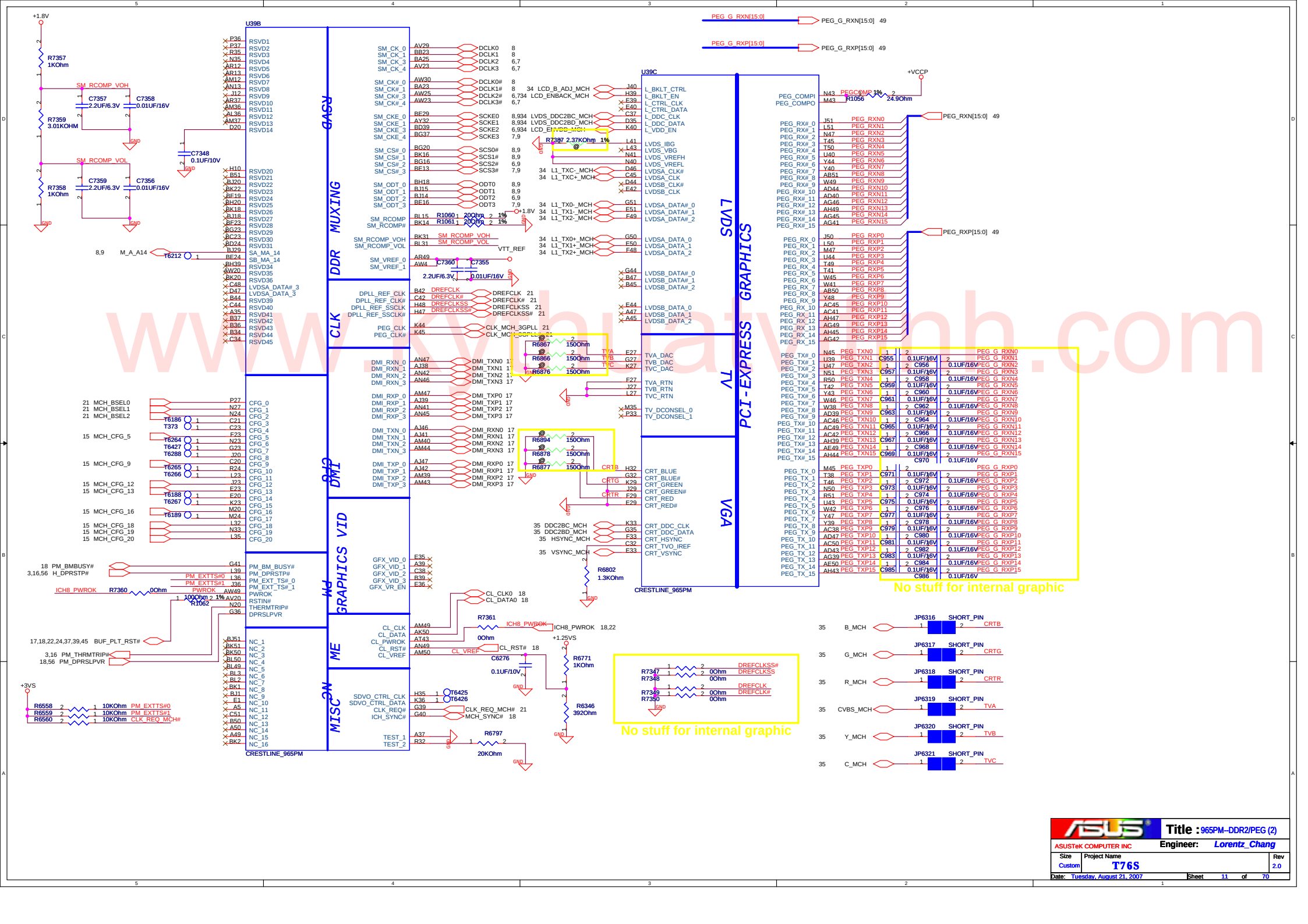
Title : DDR2 ADDR TERM

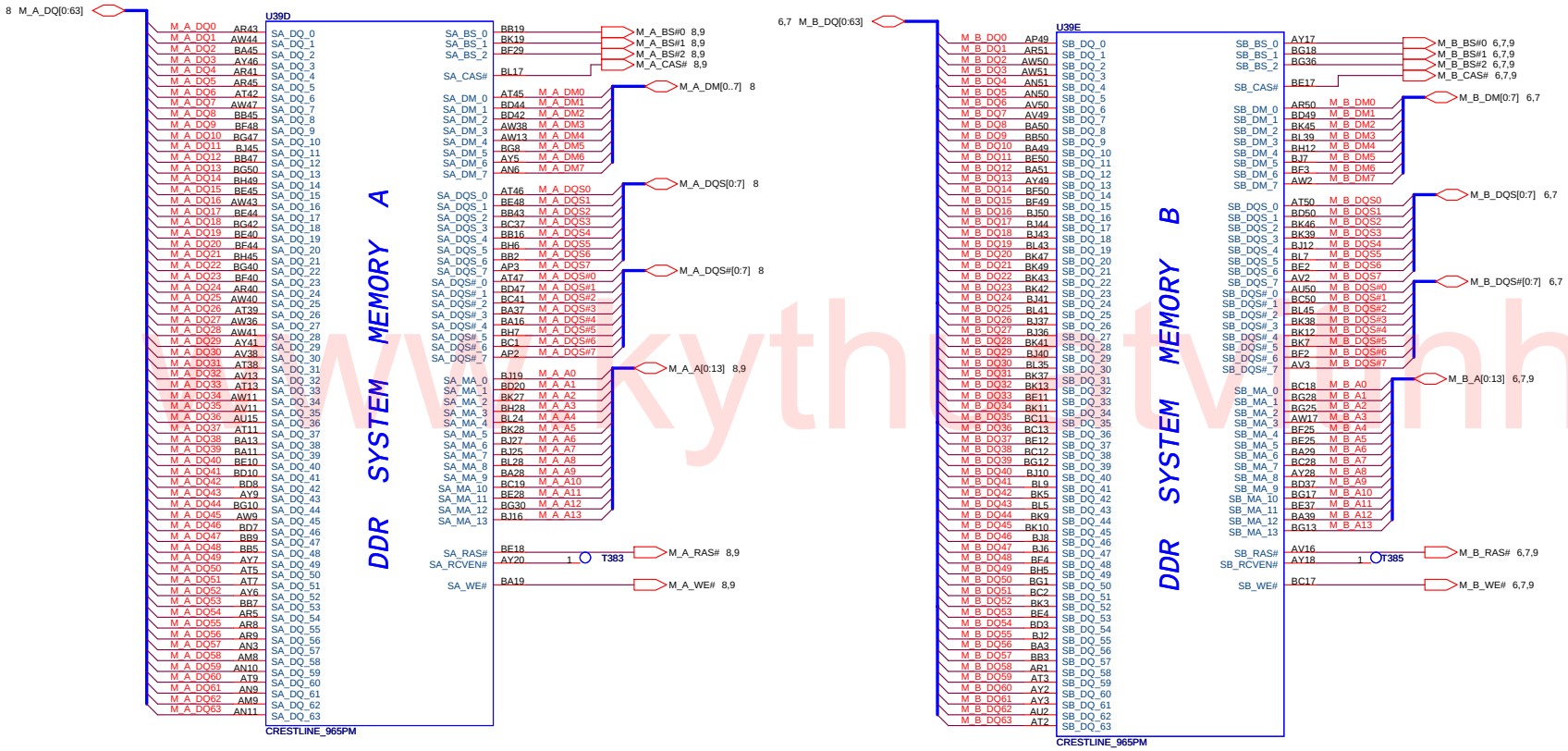
Engineer: Lorentz_Chang

Size	Project Name	Rev
Custom	T76S	2.0

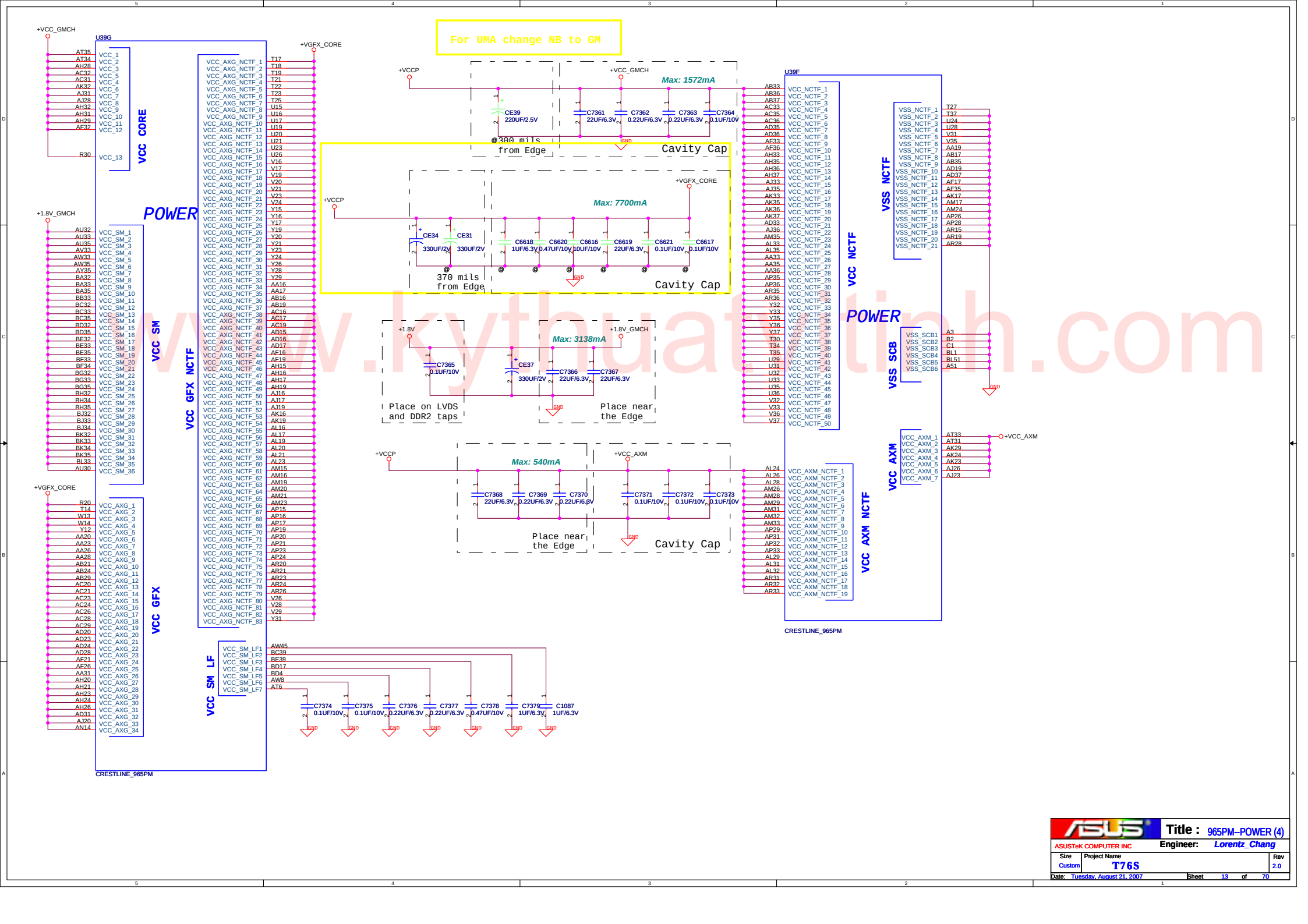
Date: Tuesday, August 21, 2007 Sheet 9 of 70

ASUSTeK COMPUTER INC	Title : 965PM – CPU (1)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 10 of 70		

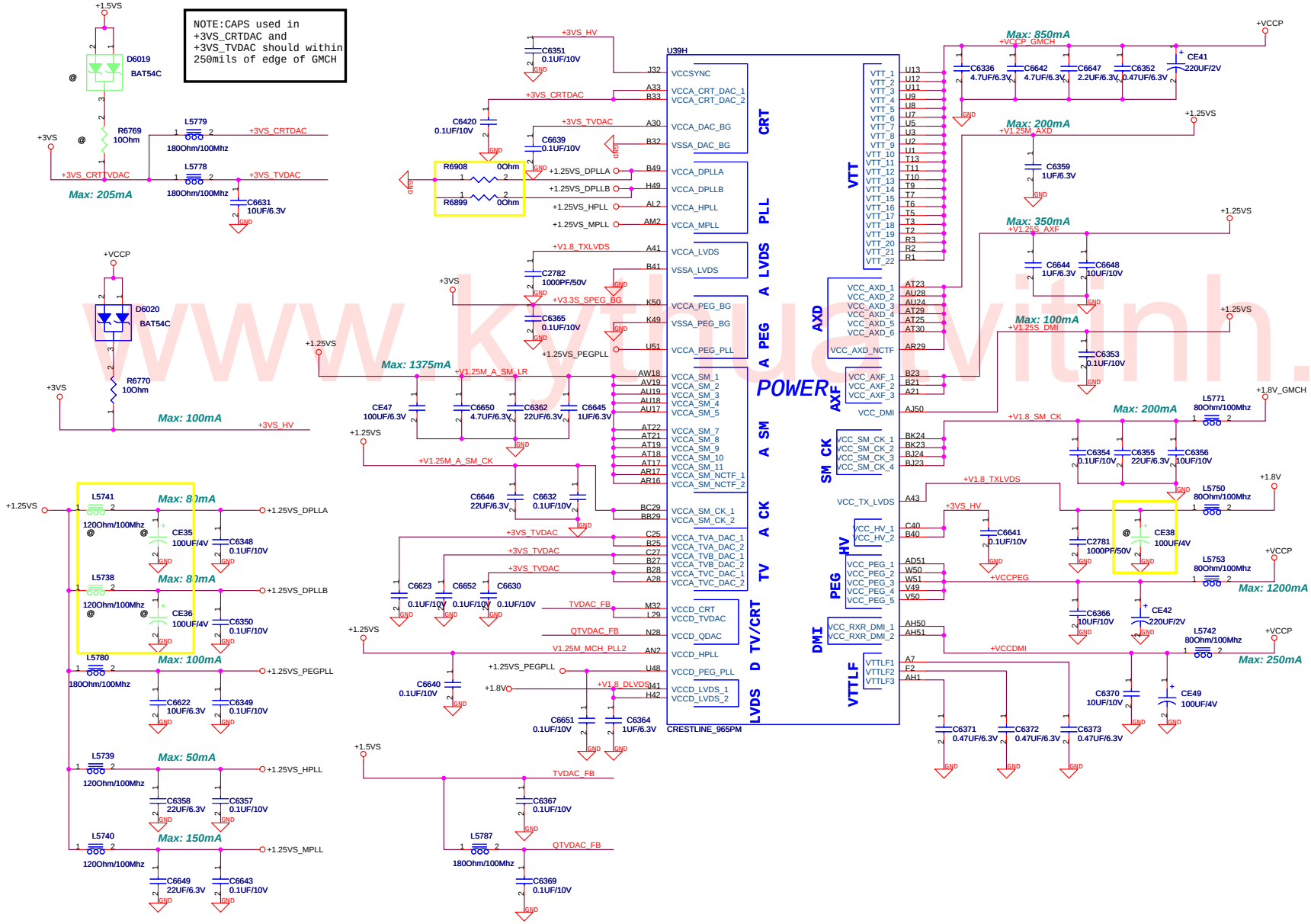

U39B
U39C
RSVD
DDR MUXING
CLK
DMI
GRAPHICS VID
PM
MISC
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CRESTLINE_965PM
No stuff for internal graphic
No stuff for internal graphic
Title : 965PM-DDR2/PEG (2)
ASUSTeK COMPUTER INC
Engineer: Lorentz_Chang
Size Custom
Project Name T76S
Rev 2.0
Date: Tuesday, August 21, 2007
Sheet 11 of 70



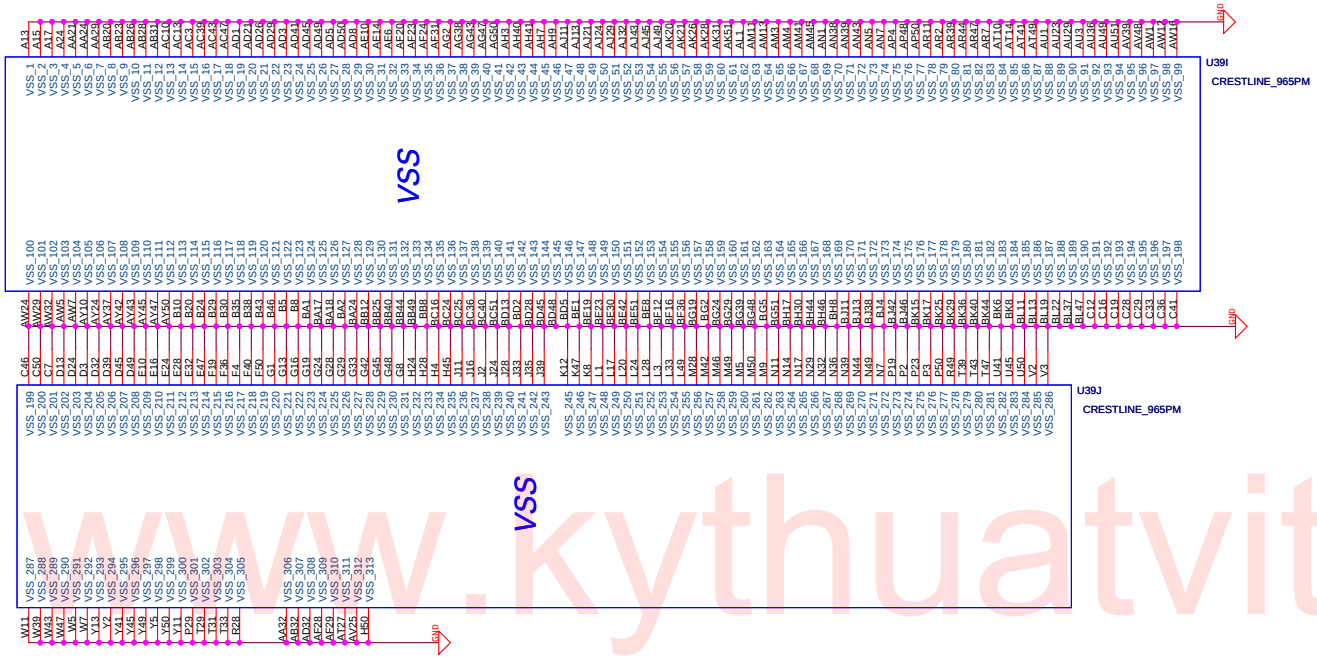
ASUSTeK COMPUTER INC	Title : 965PM–DDR2 bus (3)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 12 of 70		



ASUSTeK COMPUTER INC	Title : 965PM--POWER (4)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 13 of 70	



ASUSTeK COMPUTER INC	Title : 965PM--POWER (5)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 14 of 70	



11 MCH_CFG_5

R7338 4.02KOHM

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

11 MCH_CFG_9

R7339 4.02KOHM

CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE

HIGH = Normal Operation (Default)

No stuff for UMA

11 MCH_CFG_16

R7340 4.02KOHM

CFG16 : Dynamic ODT STRAP

Low = Dynamic ODT Disabled

HIGH = Dyanamic ODT Enabled (default)

+3VS

R7341 4.02KOHM

11 MCH_CFG_18

CFG18 : VCC select

LOW = 1.05V (default)

HIGH = 1.5V

+3VS

R7342 4.02KOHM

11 MCH_CFG_19

CFG19 : DMI LANE REVERSAL

LOW = NORMAL (default)

HIGH = LANES REVERSED

+3VS

R7343 4.02KOHM

11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

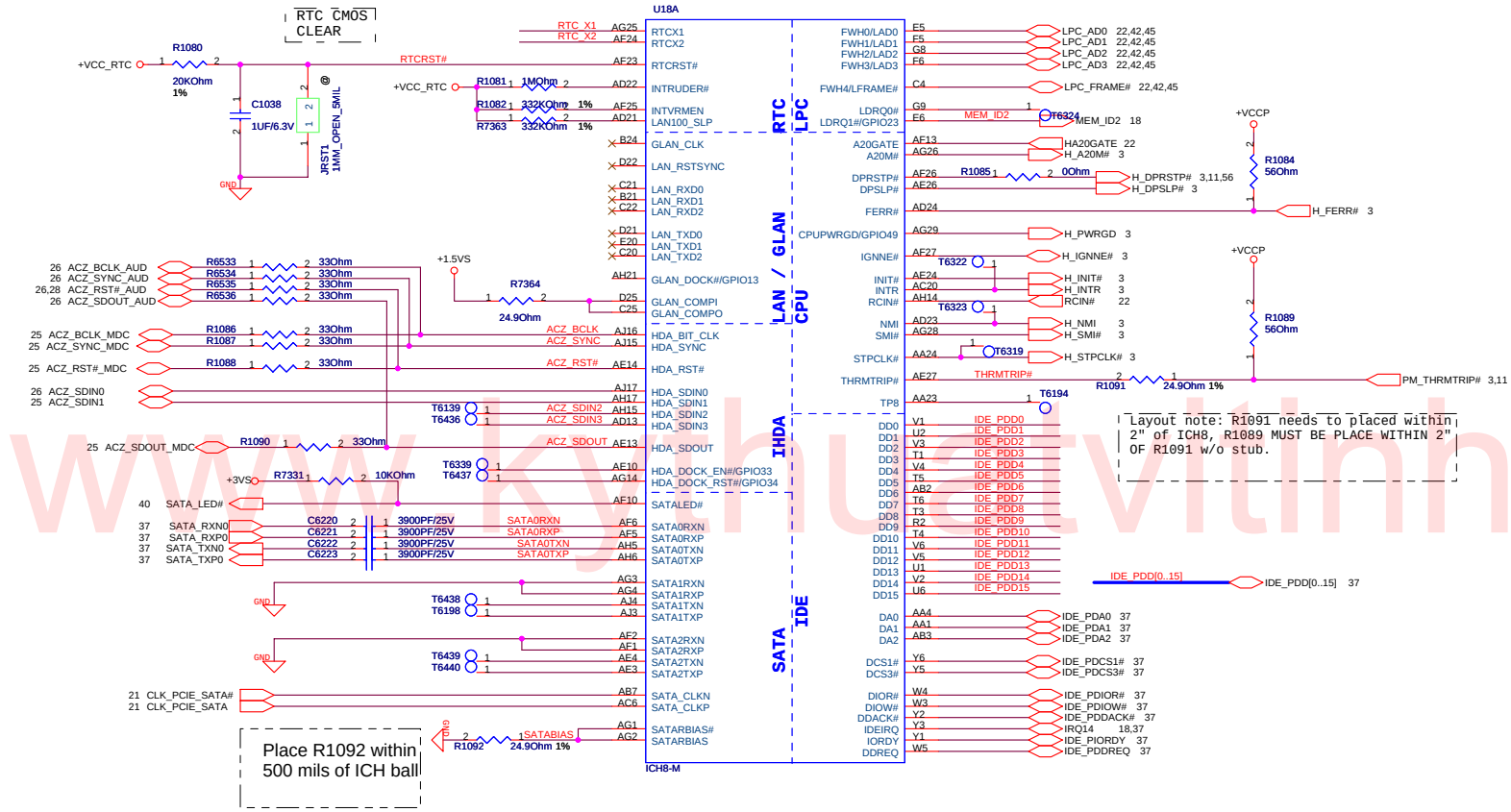
11 MCH_CFG_12

11 MCH_CFG_13

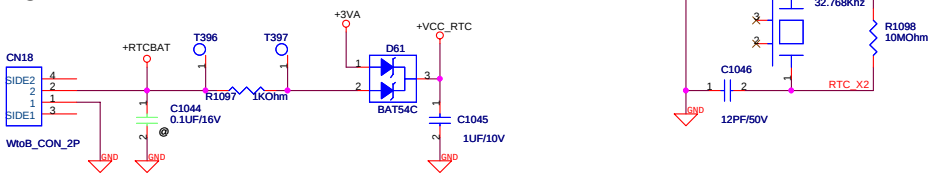
R7344 4.02KOHM

R7345 4.02KOHM

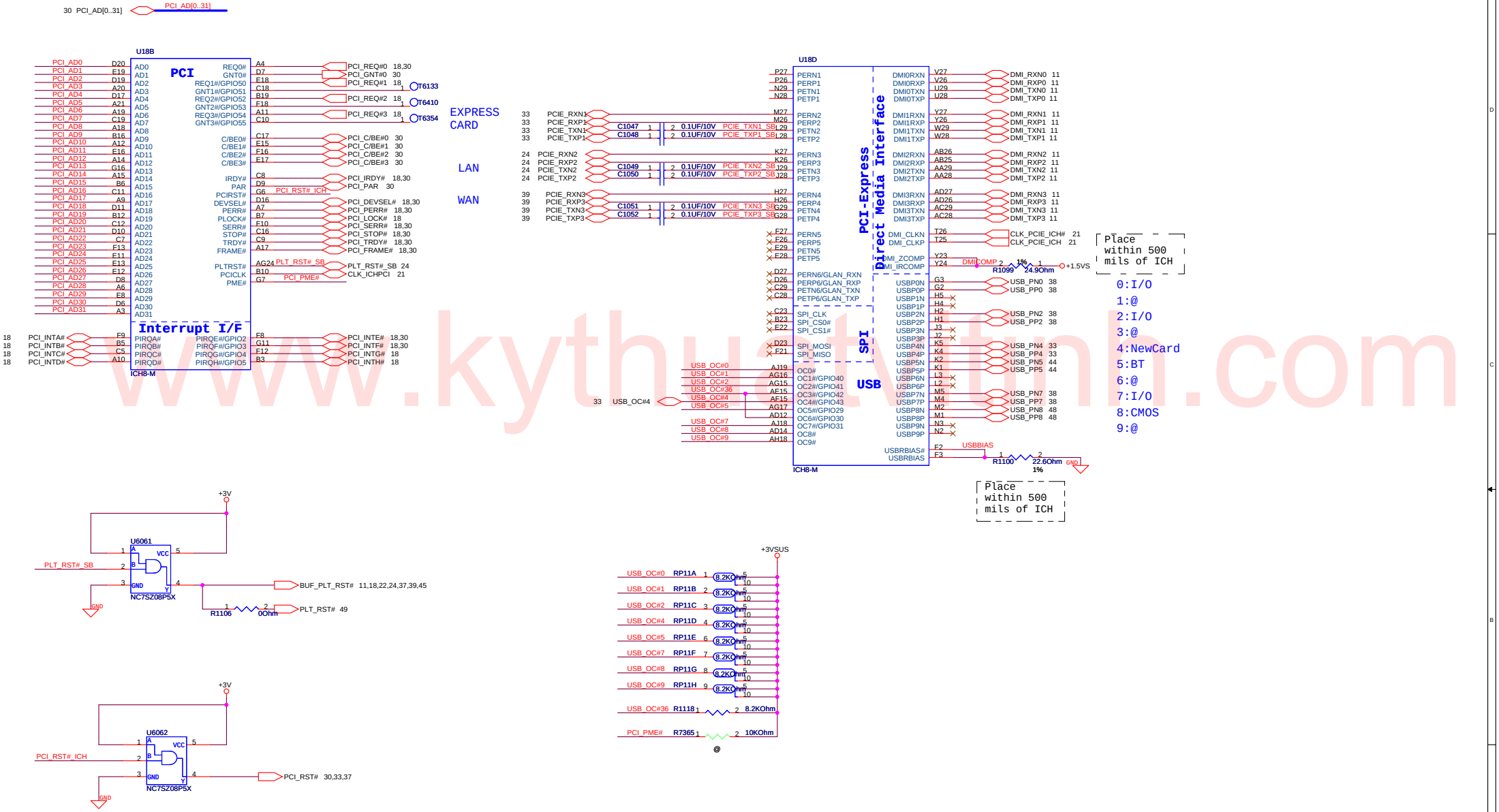
Title : GND/Strapping (6)			
ASUSTeK COMPUTER INC	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 15 of 70		



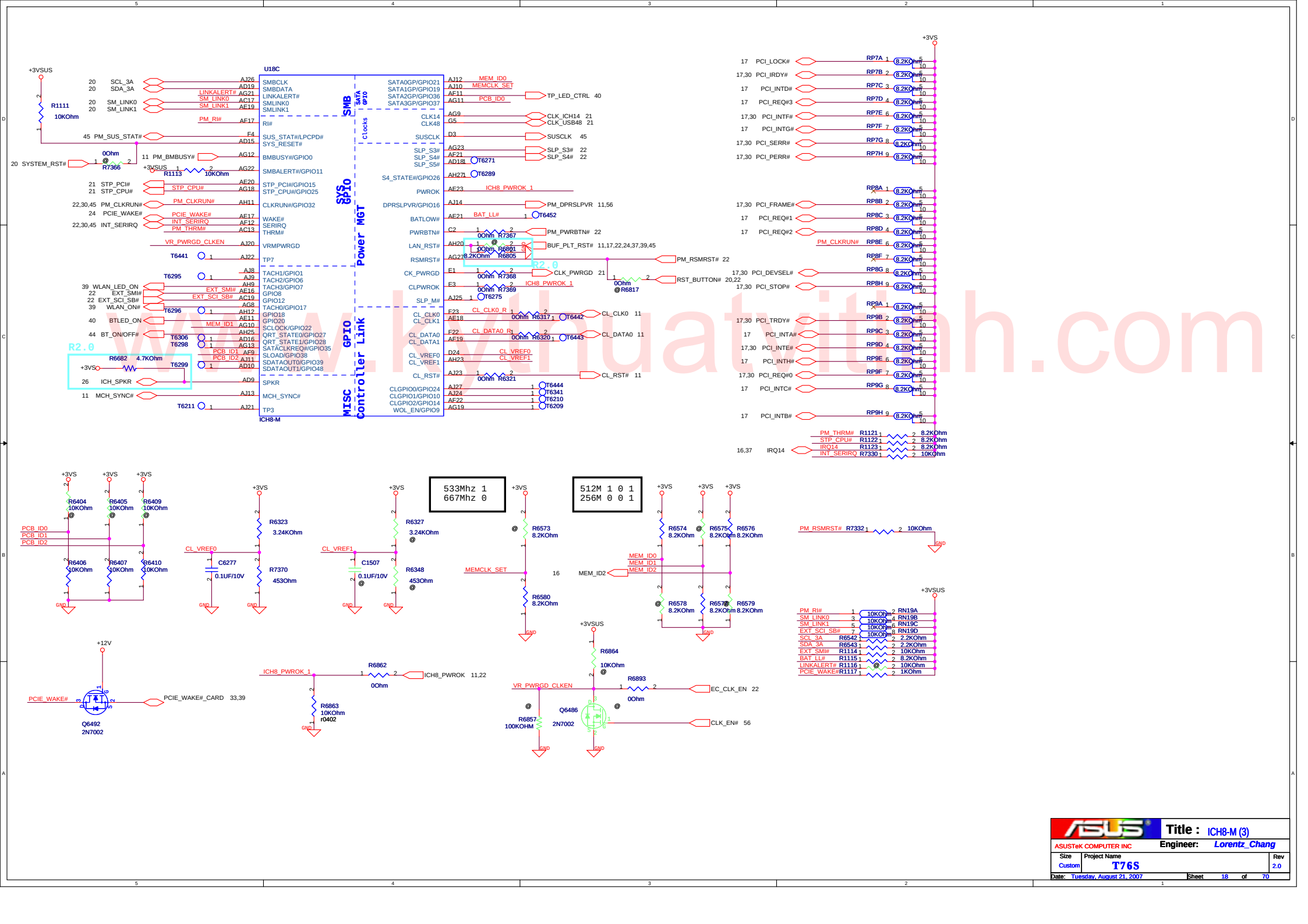
RTC BAT



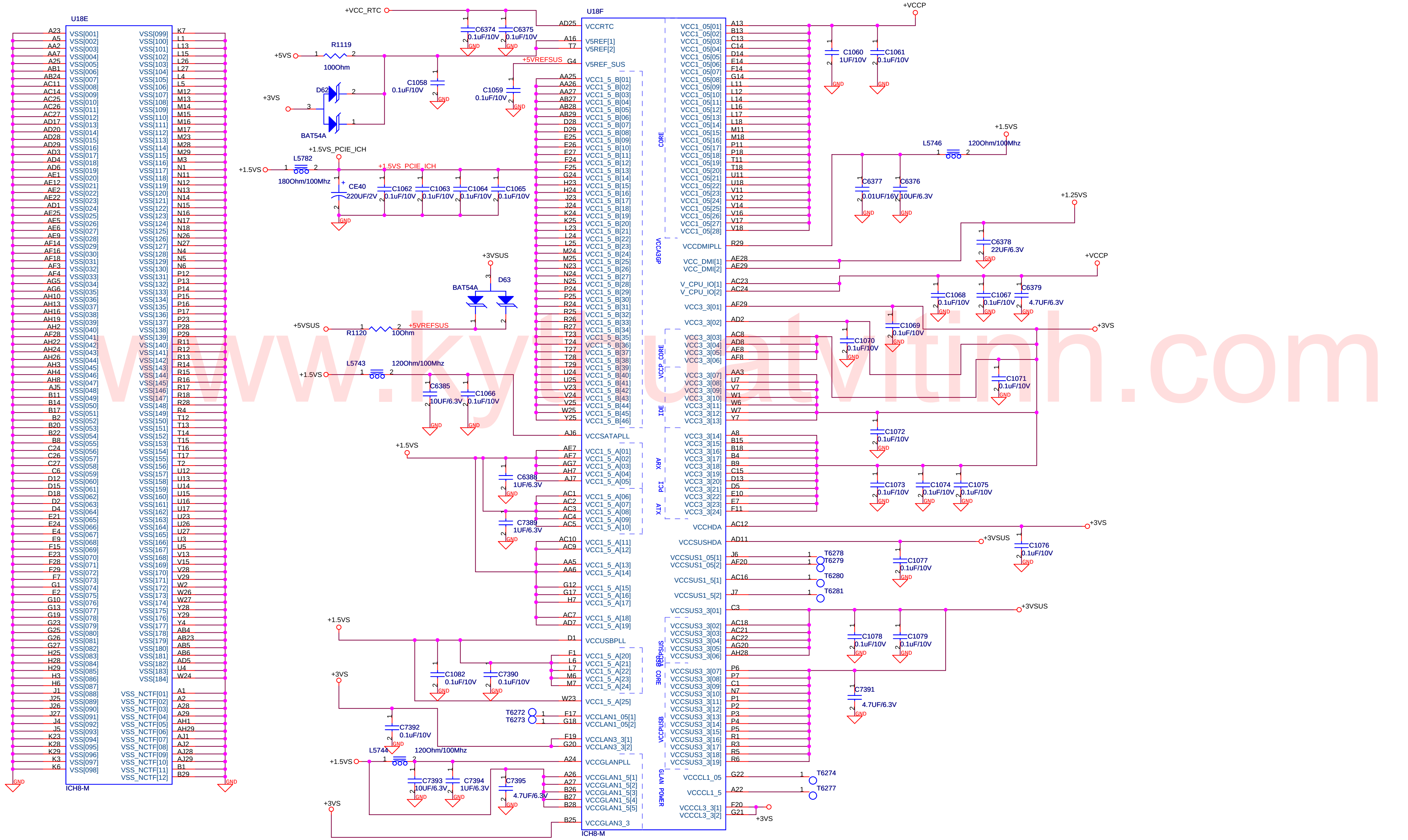
ASUSTeK COMPUTER INC	Title : ICH8-M (1)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 16 of 70		



ASUSTeK COMPUTER INC	Title : ICH8-M (2)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 17 of 70	



ASUSTeK COMPUTER INC	Title : ICH8-M (3)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 18 of 70	



ASUSTeK COMPUTER INC

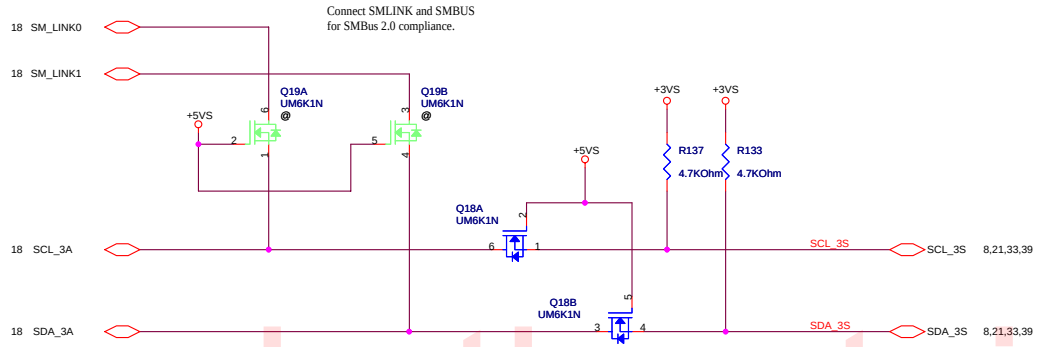
Title : ICH8-M (4)

Engineer: Lorentz_Chang

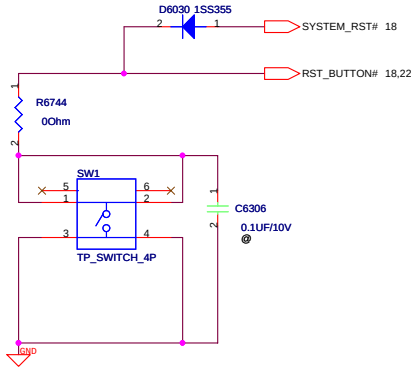
Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 19 of 70

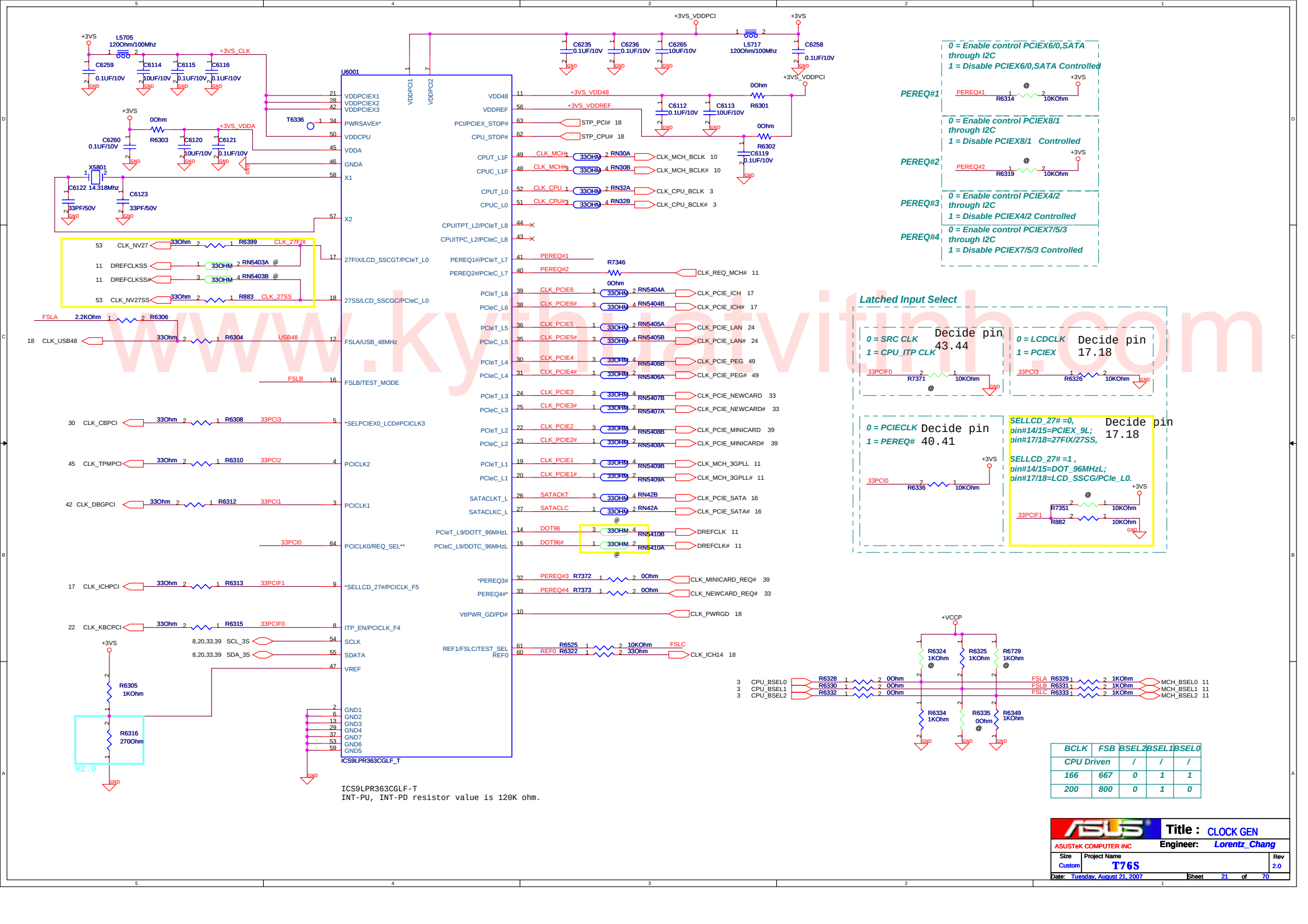
ICH8-M

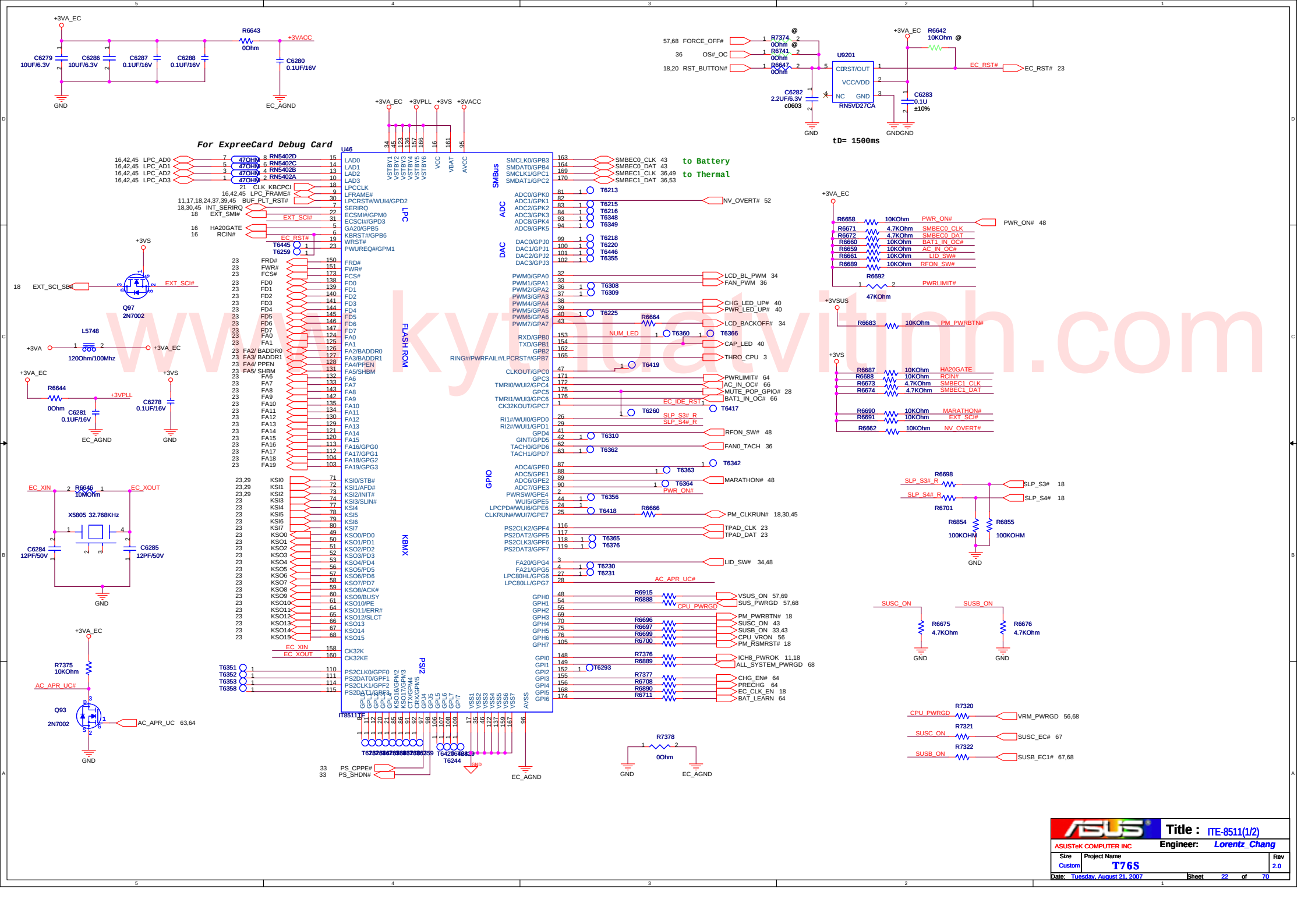


ICH8-M

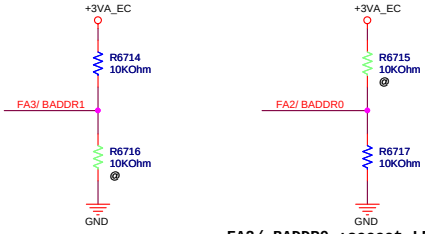


ASUSTeK COMPUTER INC	Title : ICH8M--Other	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 20 of 70	



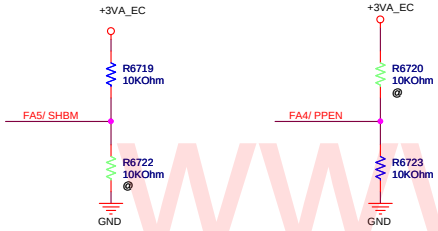

For ExpreeCard Debug Card
U46
IT8511TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
tD= 1500ms
Title : ITE-8511(1/2)
ASUSTeK COMPUTER INC
Engineer: Lorentz_Chang
Project Name T76S
Size Custom
Rev 2.0
Date: Tuesday, August 21, 2007
Sheet 22 of 70

10:Determined by EC



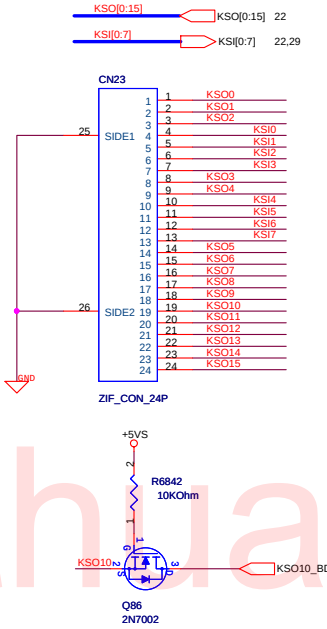
FA3/ BADDR1:secect LPC address: 4E/4F

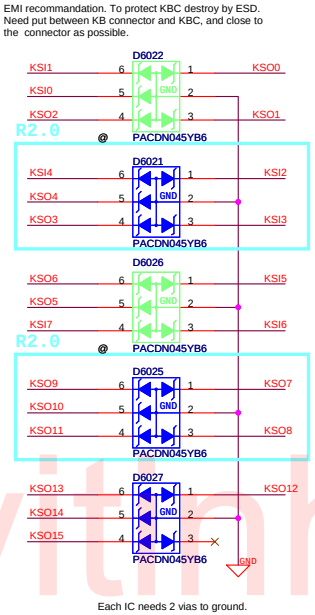
FA2/ BADDR0 :secect LPC address:2E/2F



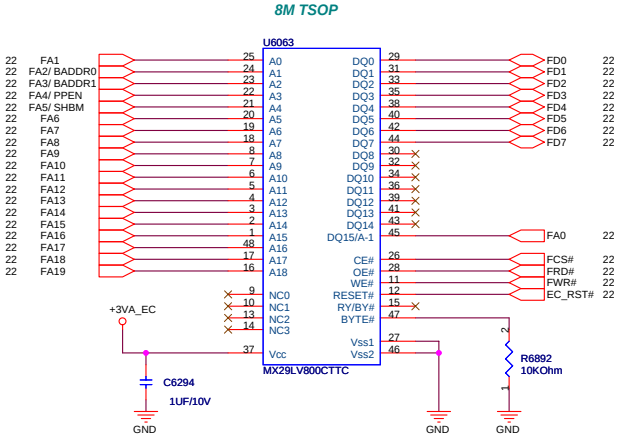
FA5/ SHBM:share BIOS mode enable.

FA4/ PPEN:enable in-system program via parallel port interface.(KBS down)

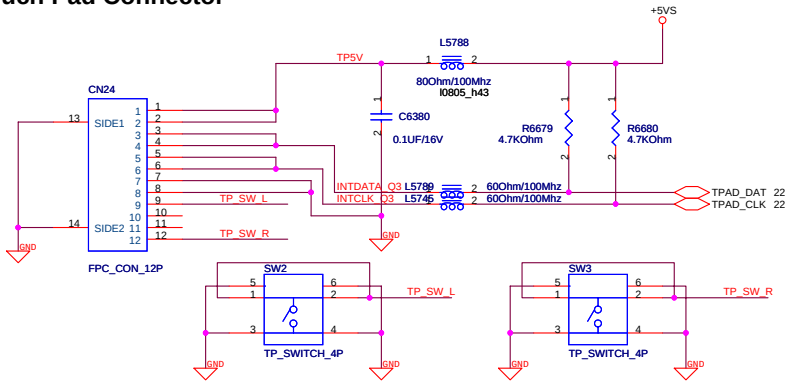




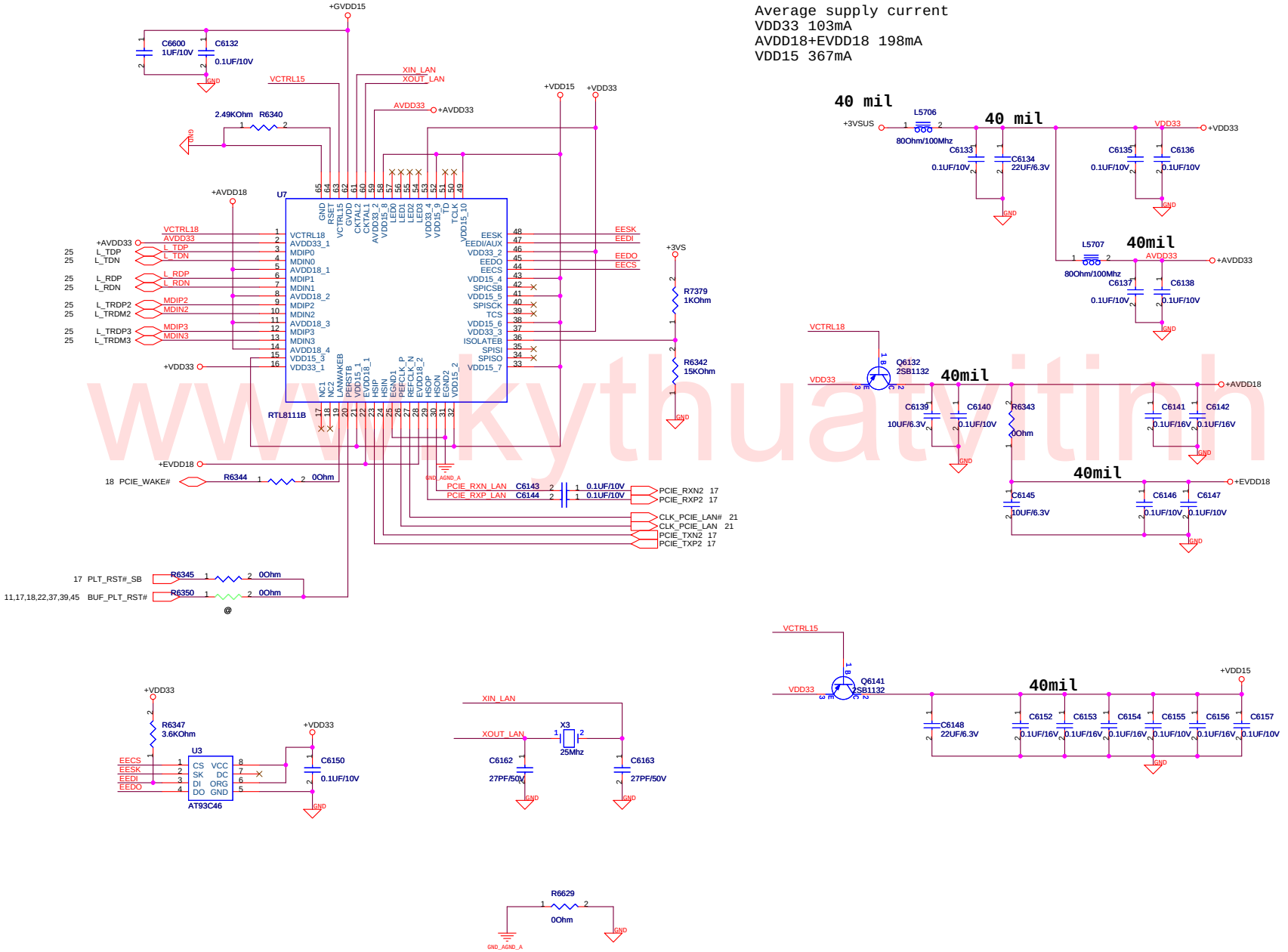
8M-ROM

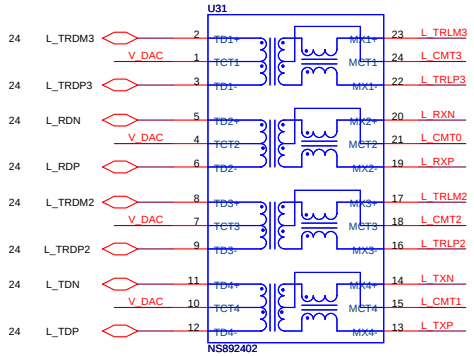


Touch Pad Connector

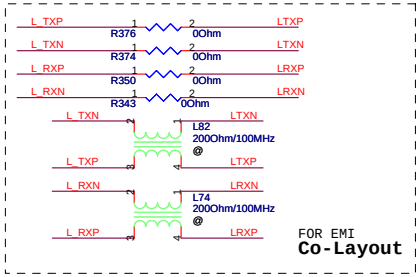


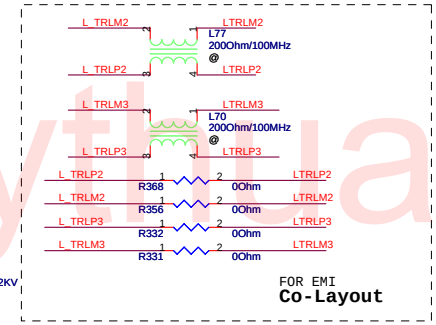
ASUSTeK COMPUTER INC	Title : ITE-8511(2/2)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 23 of 70	

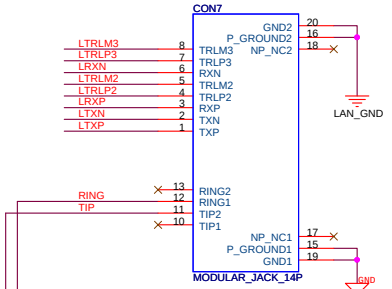


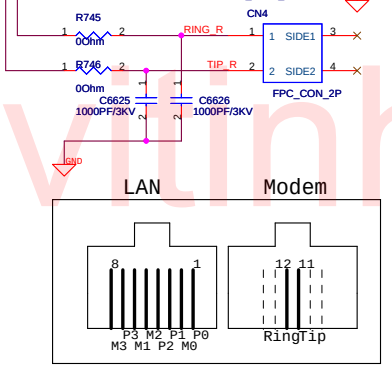


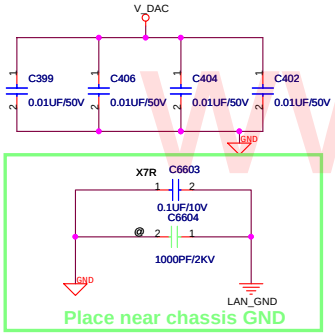
Transformer close CON7

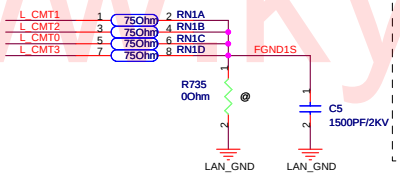




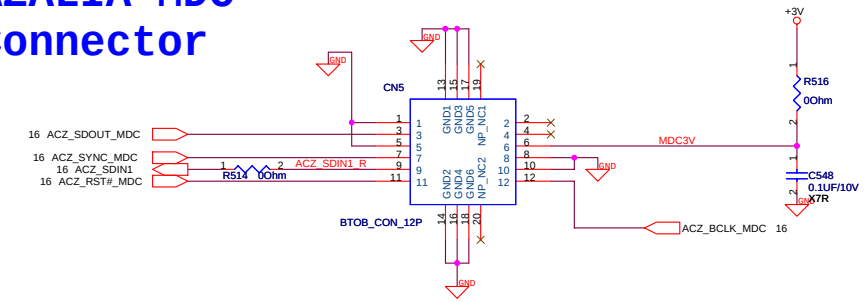




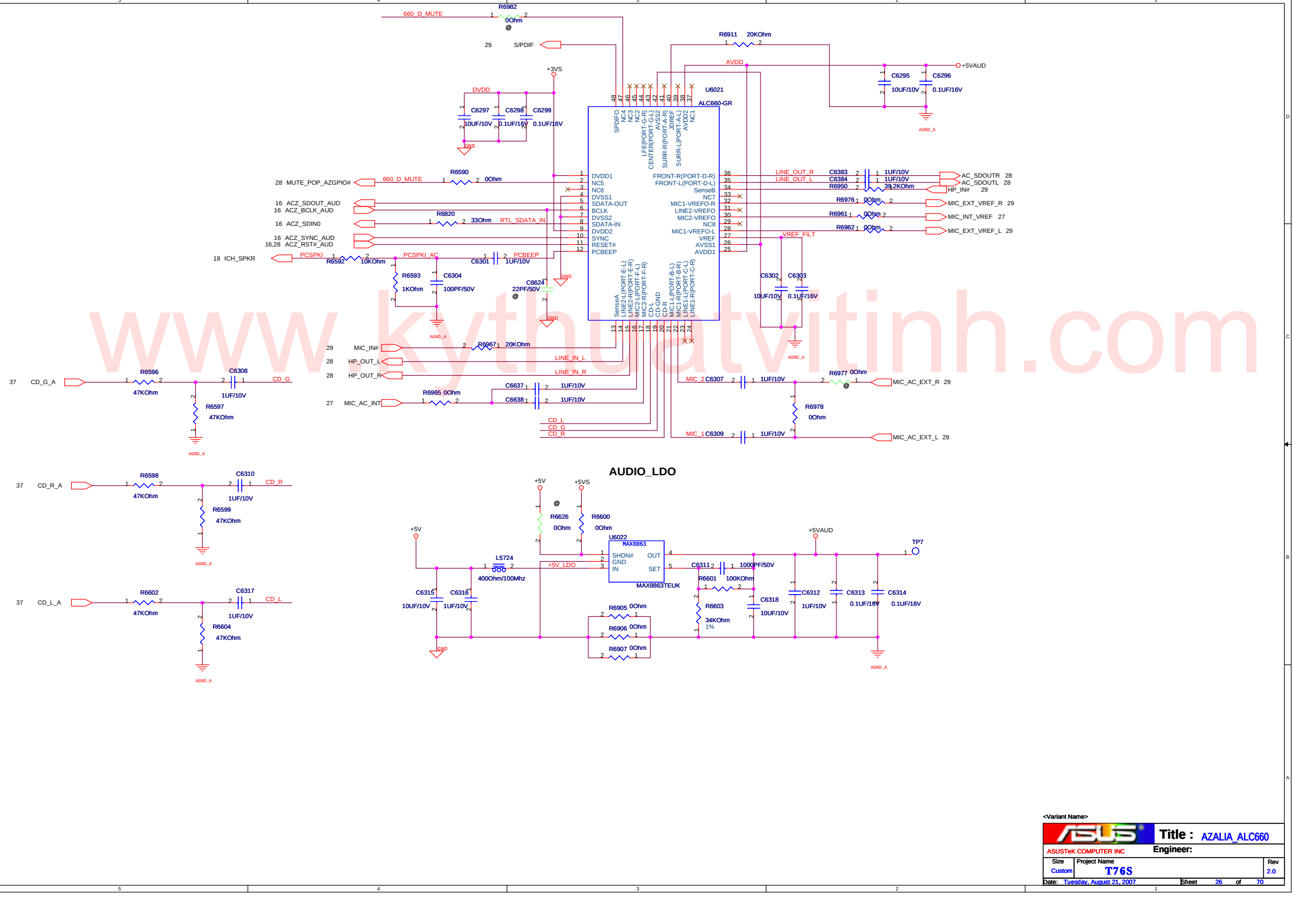




AZALIA MDC Connector



ASUSTeK COMPUTER INC	Title : RJ11+45 , MDC	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 25 of 70	



<Variant Name>

ASUSTeK COMPUTER INC

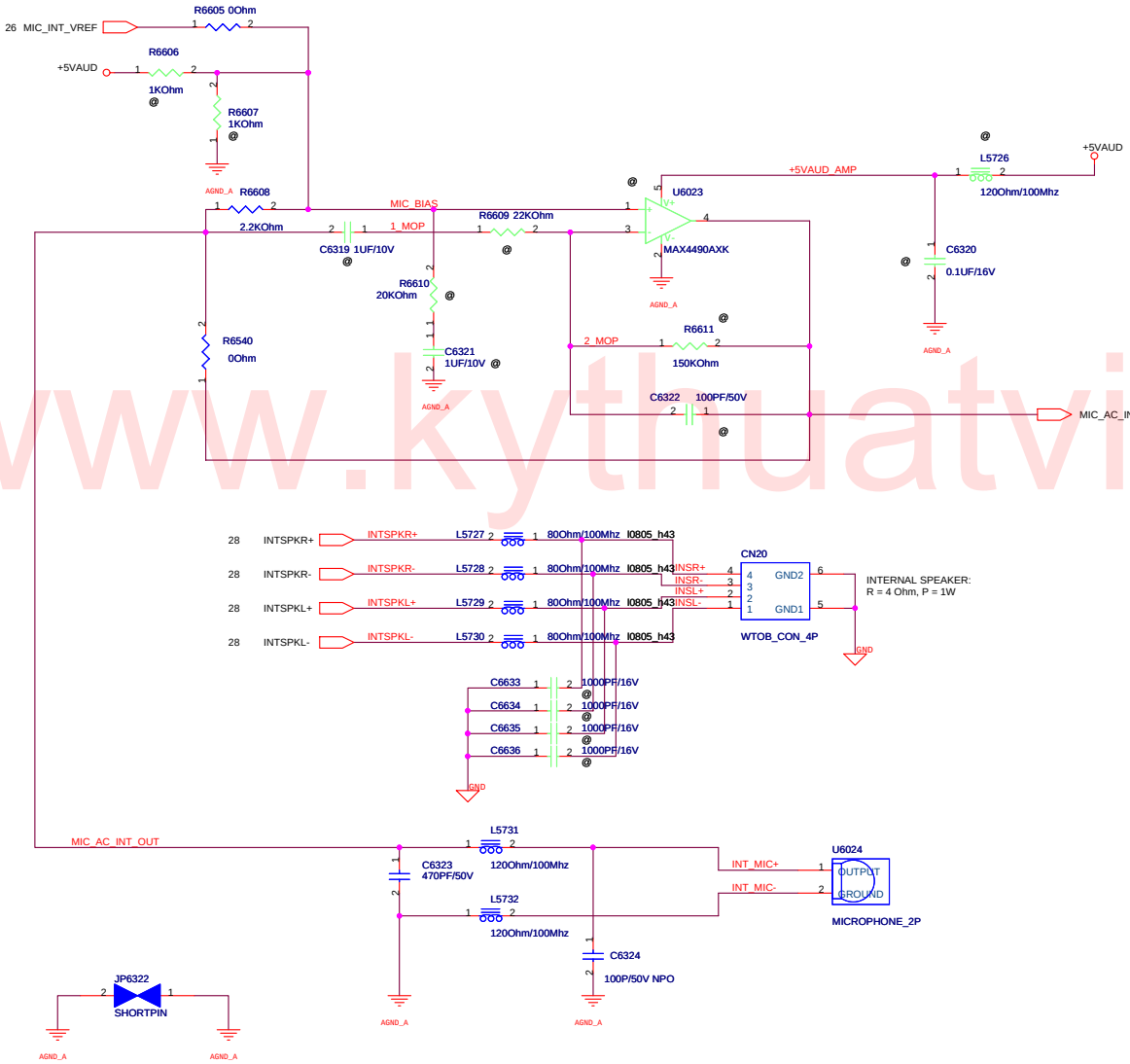
Title : AZALIA_ALC660

Engineer:

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 26 of 70

MIC PreAmp & Mic Jack



<Variant Name>

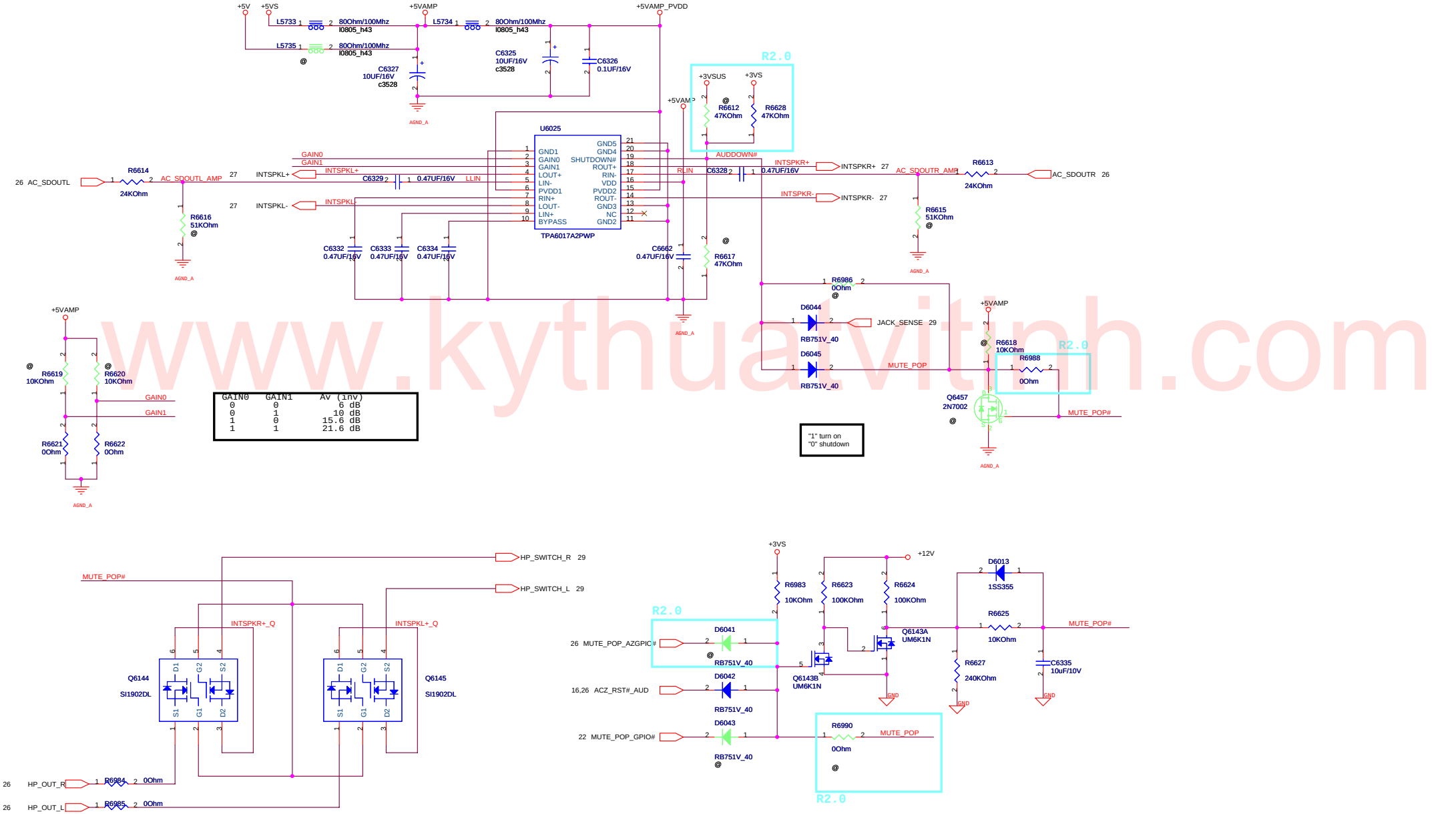
Title : MIC PREAMP & INT MIC

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 27 of 70



<Variant Name>

Title : AUDIO_AMP & INT SPK

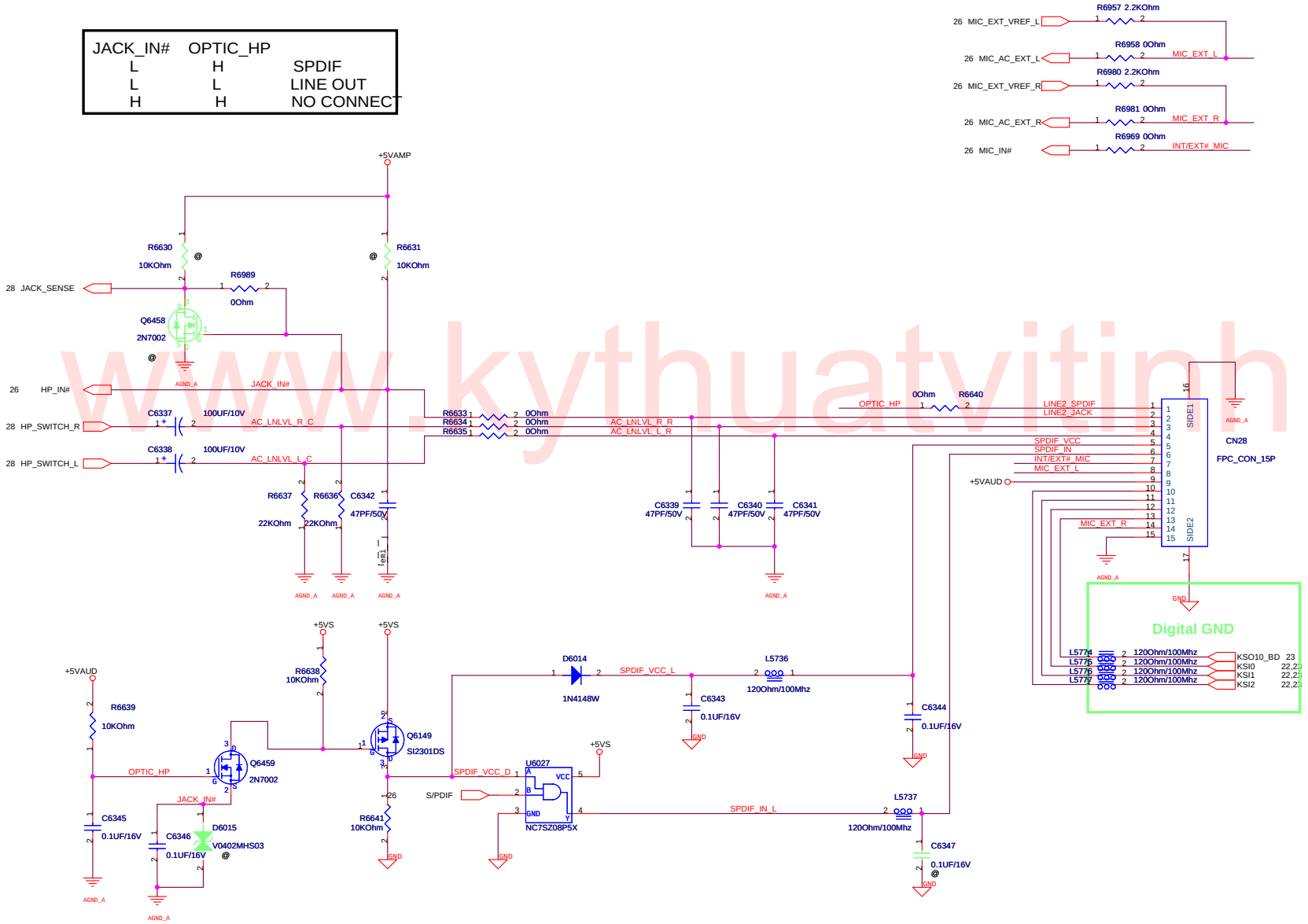
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 28 of 70

JACK_IN#	OPTIC_HP	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT



<Variant Name>

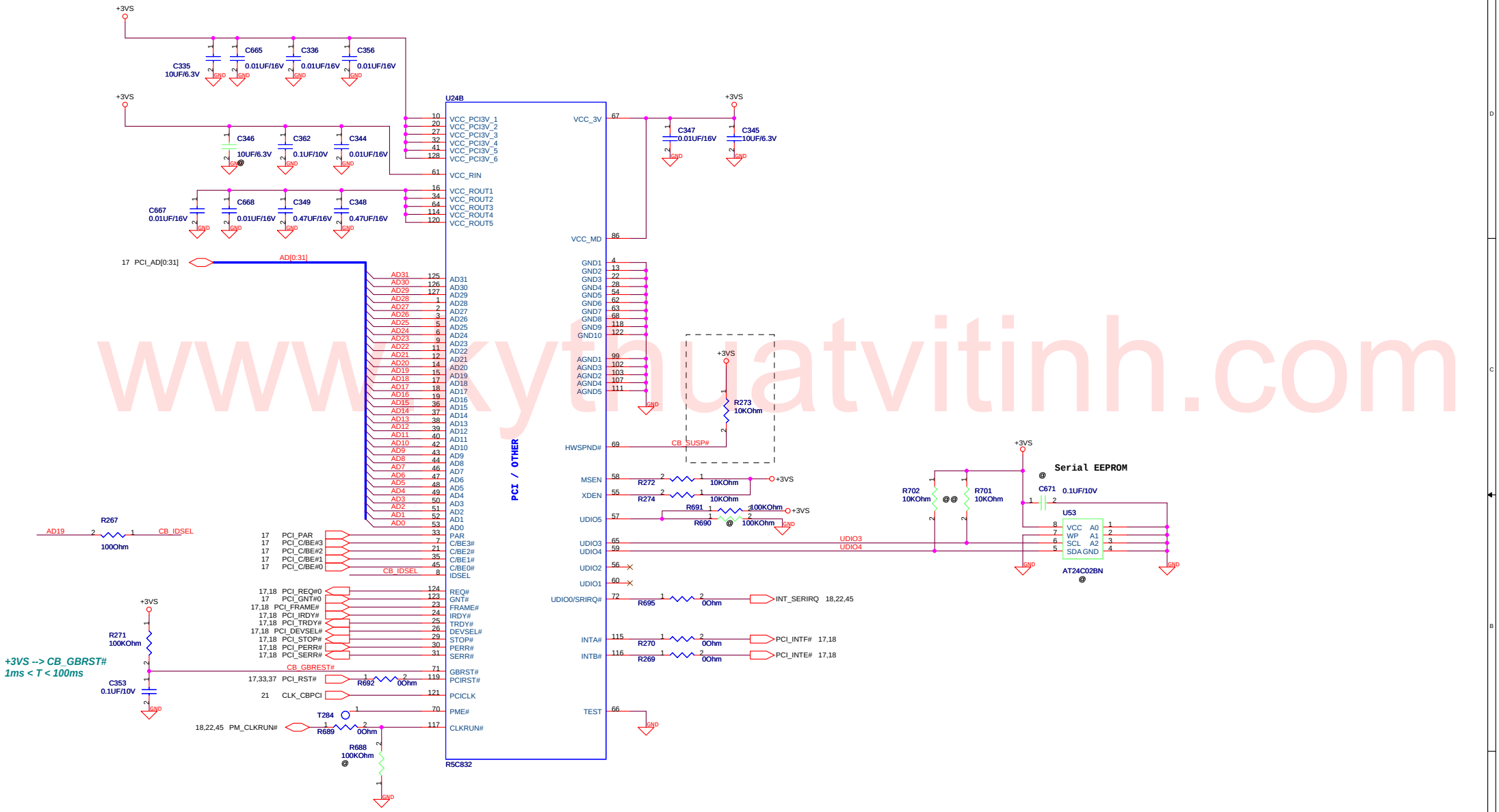
ASUSTeK COMPUTER INC

Title : SPDIF JACK

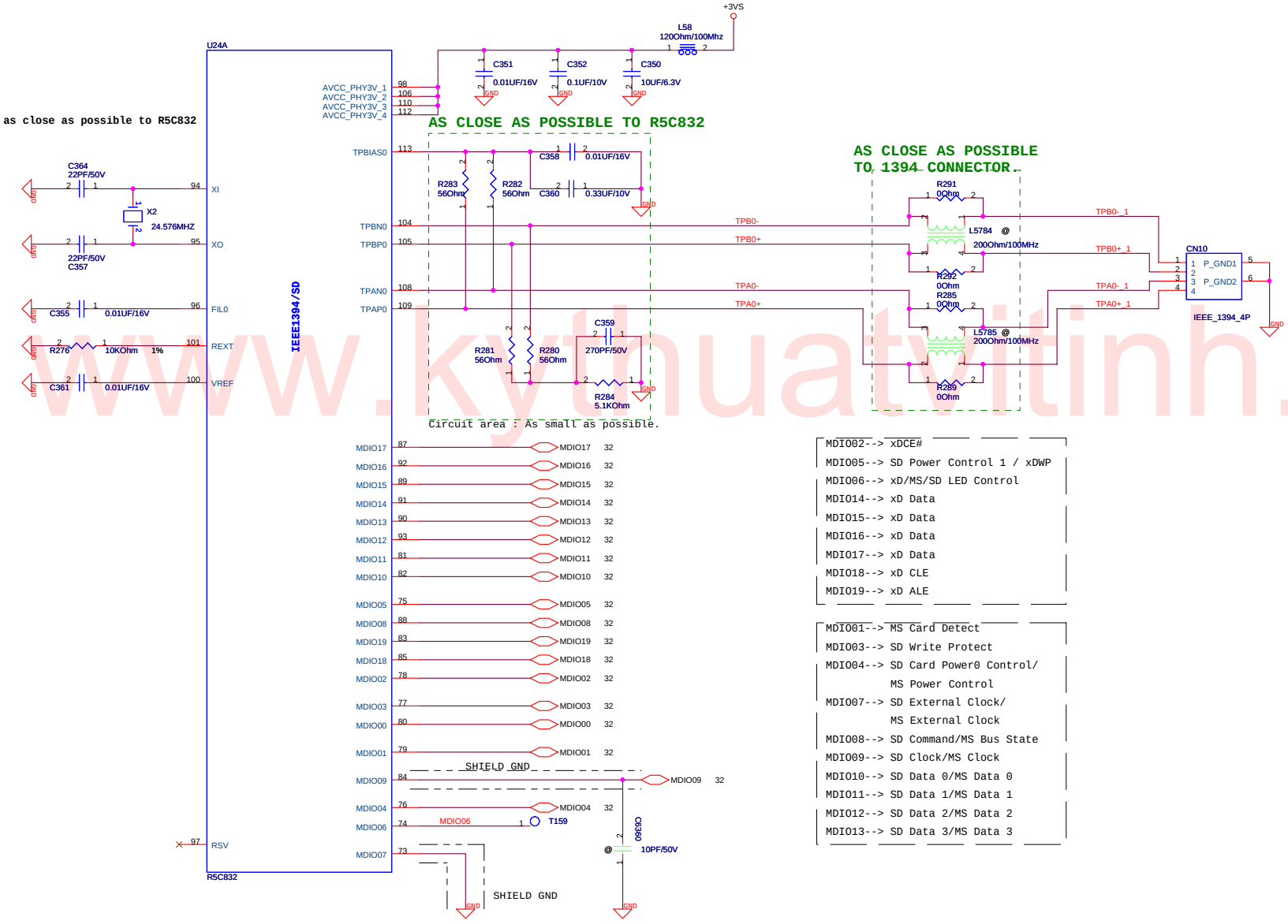
Engineer:

Size	Project Name	Rev
Custom	T76S	2.0

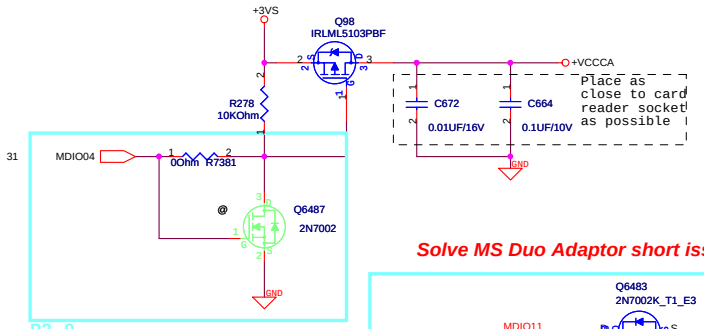
Date: Tuesday, August 21, 2007 Sheet 29 of 70



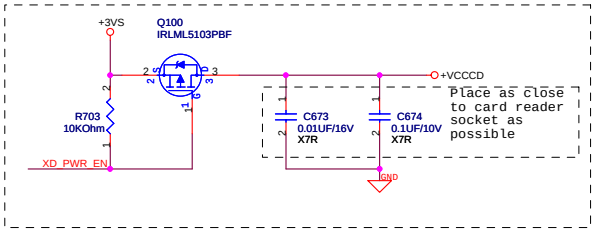
ASUSTeK COMPUTER INC	Title : RICOH R5C832/PCI_B	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 30 of 70	



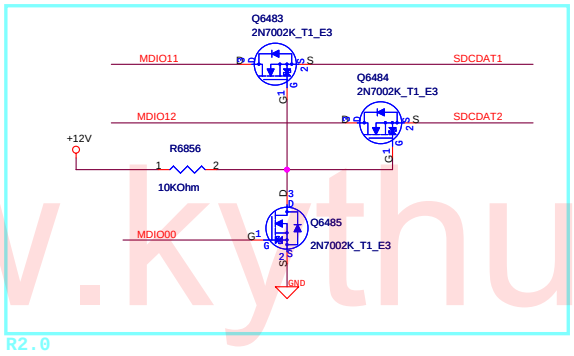
ASUSTeK COMPUTER INC	Title : RICOH R5C832/PCI_A	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 31 of 70	



To correct the problem when MS Duo adaptor is in use.

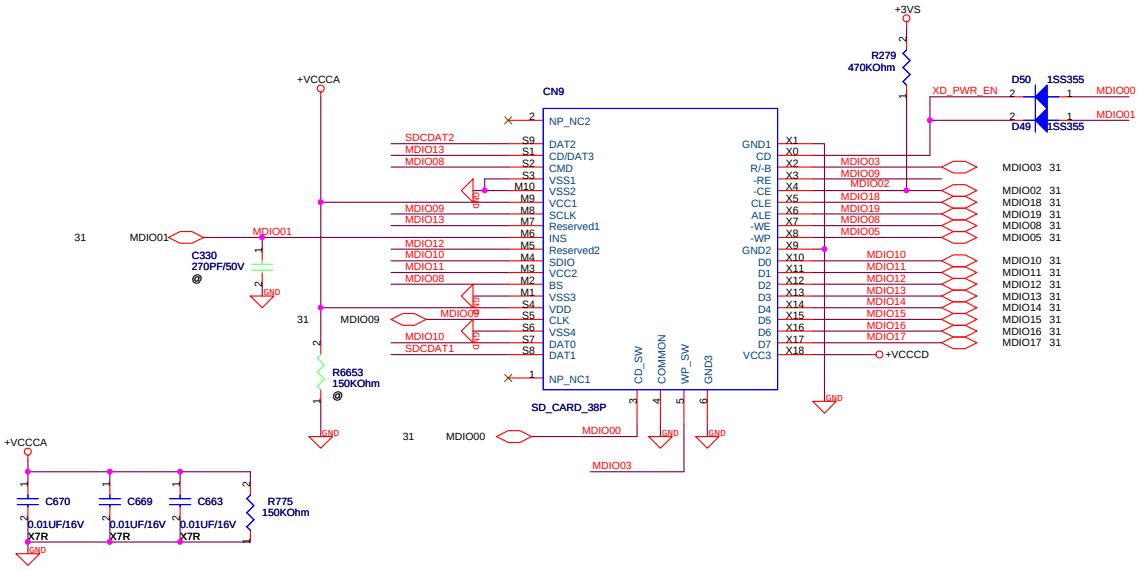


Solve MS Duo Adaptor short issue.

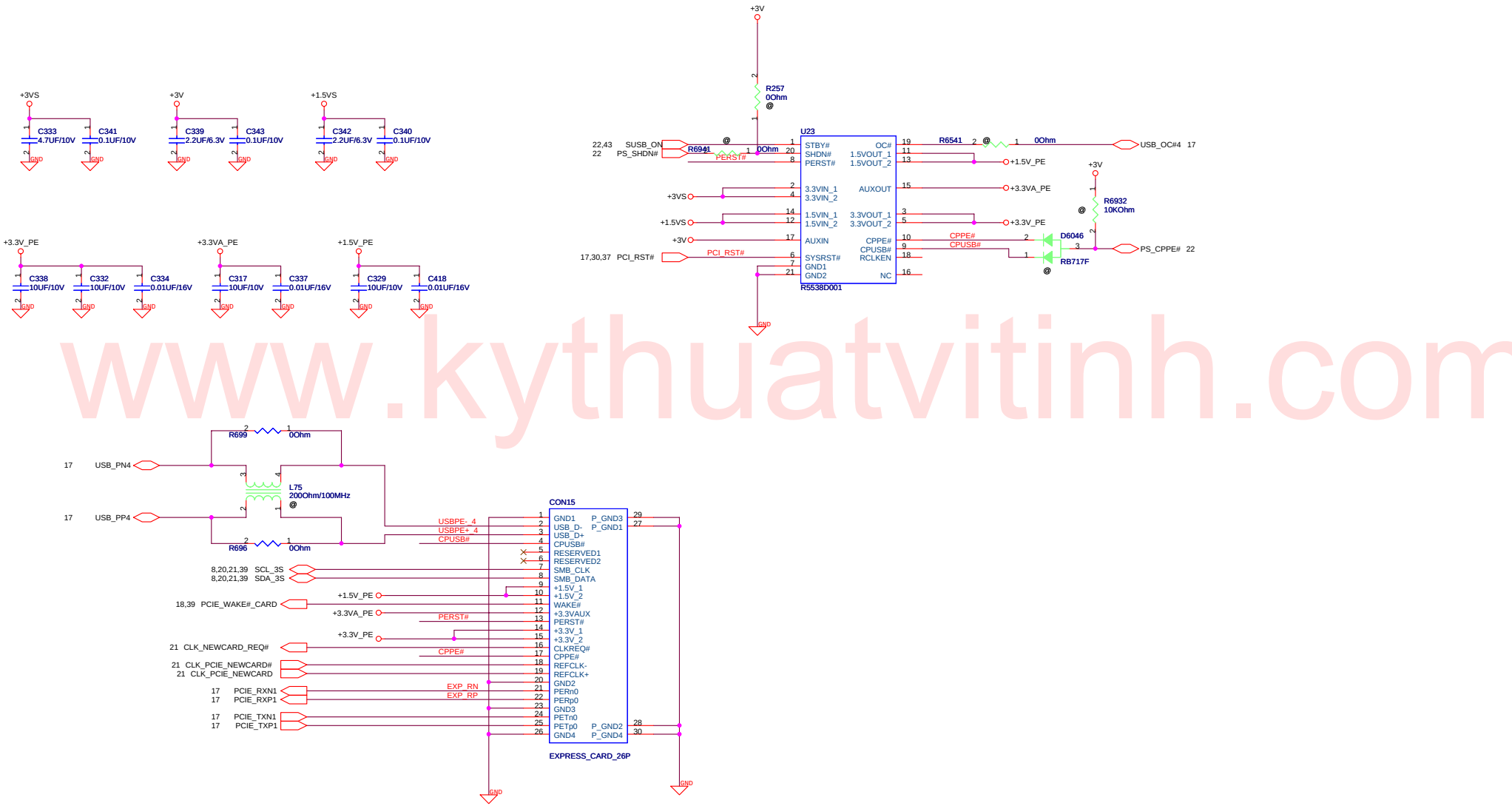



```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

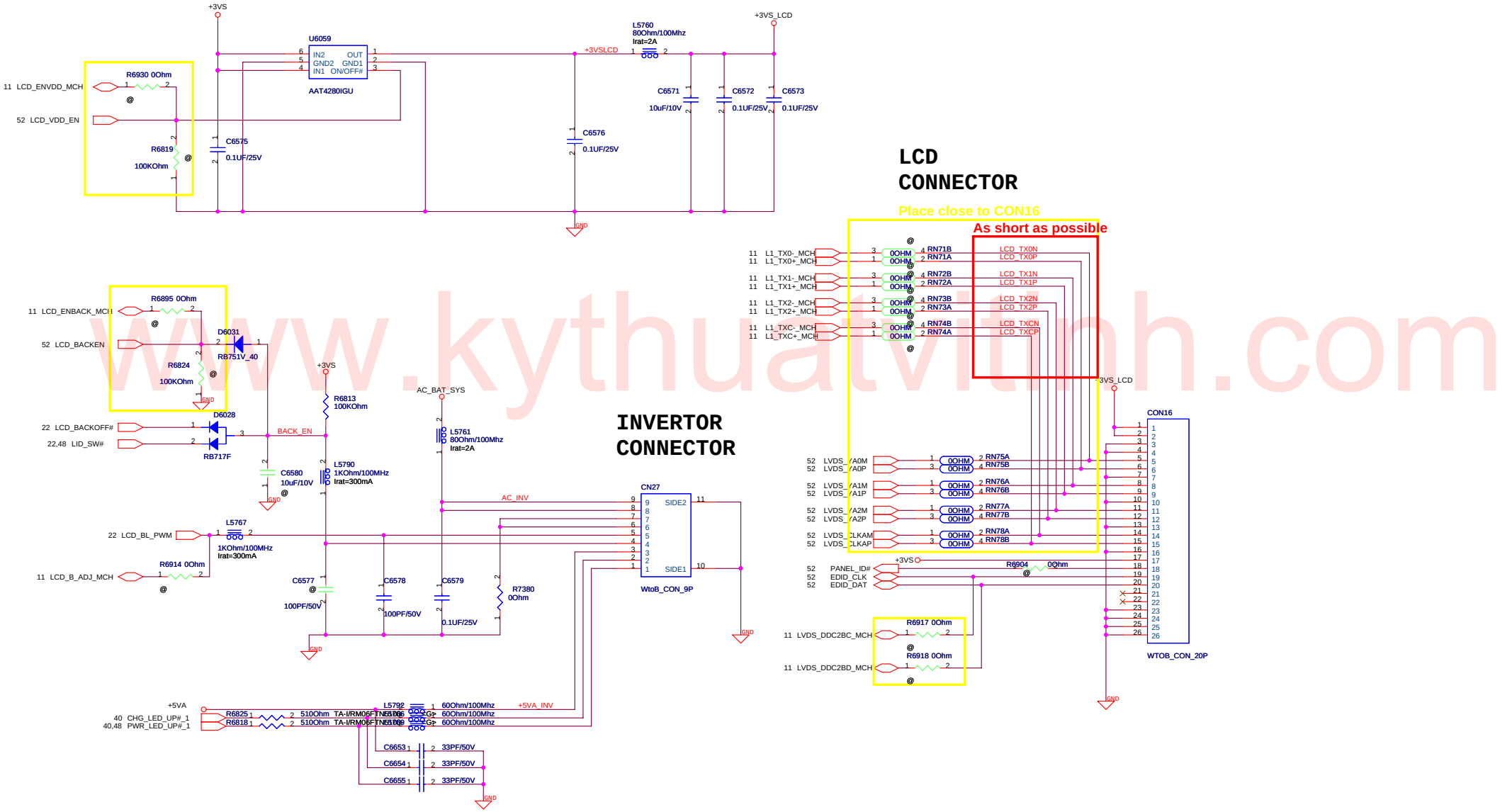
```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```



ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 32 of 70	

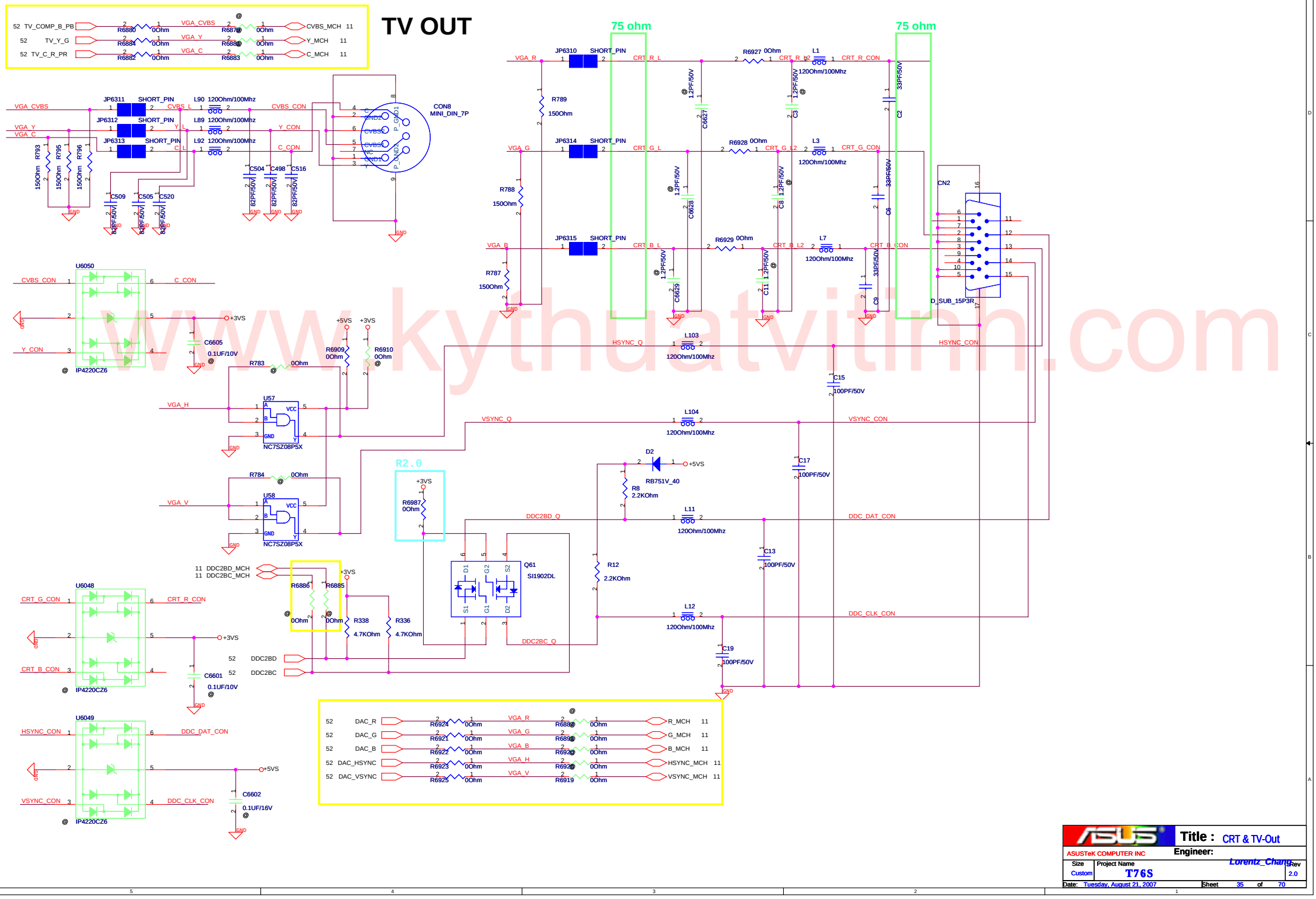


ASUSTeK COMPUTER INC	Title : Express Card	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 33 of 70	



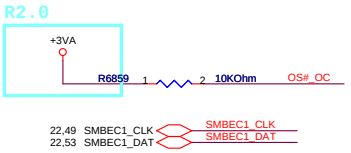
ASUSTeK COMPUTER INC	Title : LVDS & Inverter	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 34 of 70	

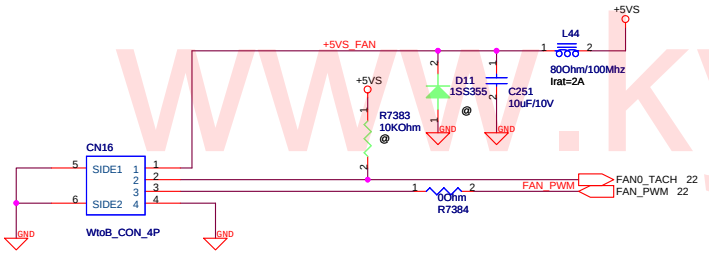
TV OUT

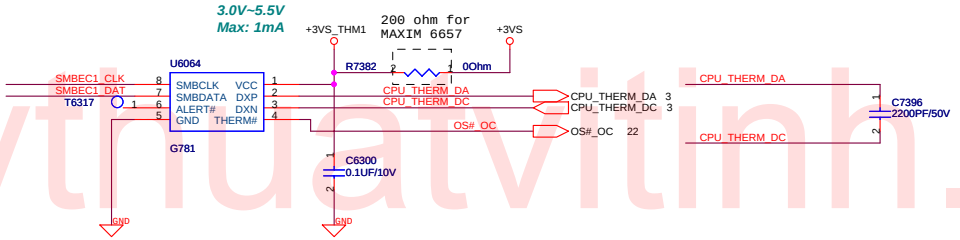


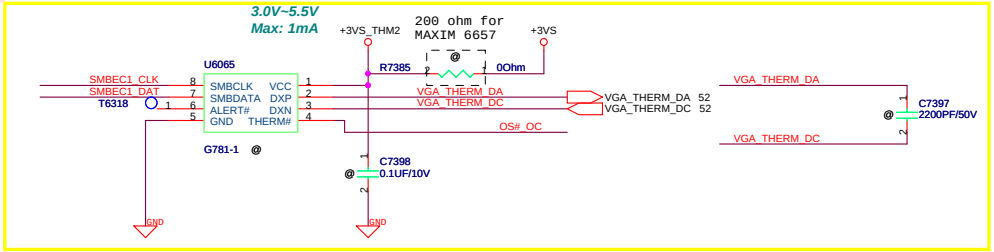
Title :	CRT & TV-Out
ASUSTeK COMPUTER INC	Engineer: Lorentz_Chang
Size: Custom	Project Name: T76S
Rev: 2.0	
Date: Tuesday, August 21, 2007	Sheet 35 of 70

FAN & THERMAL CONTROLLER



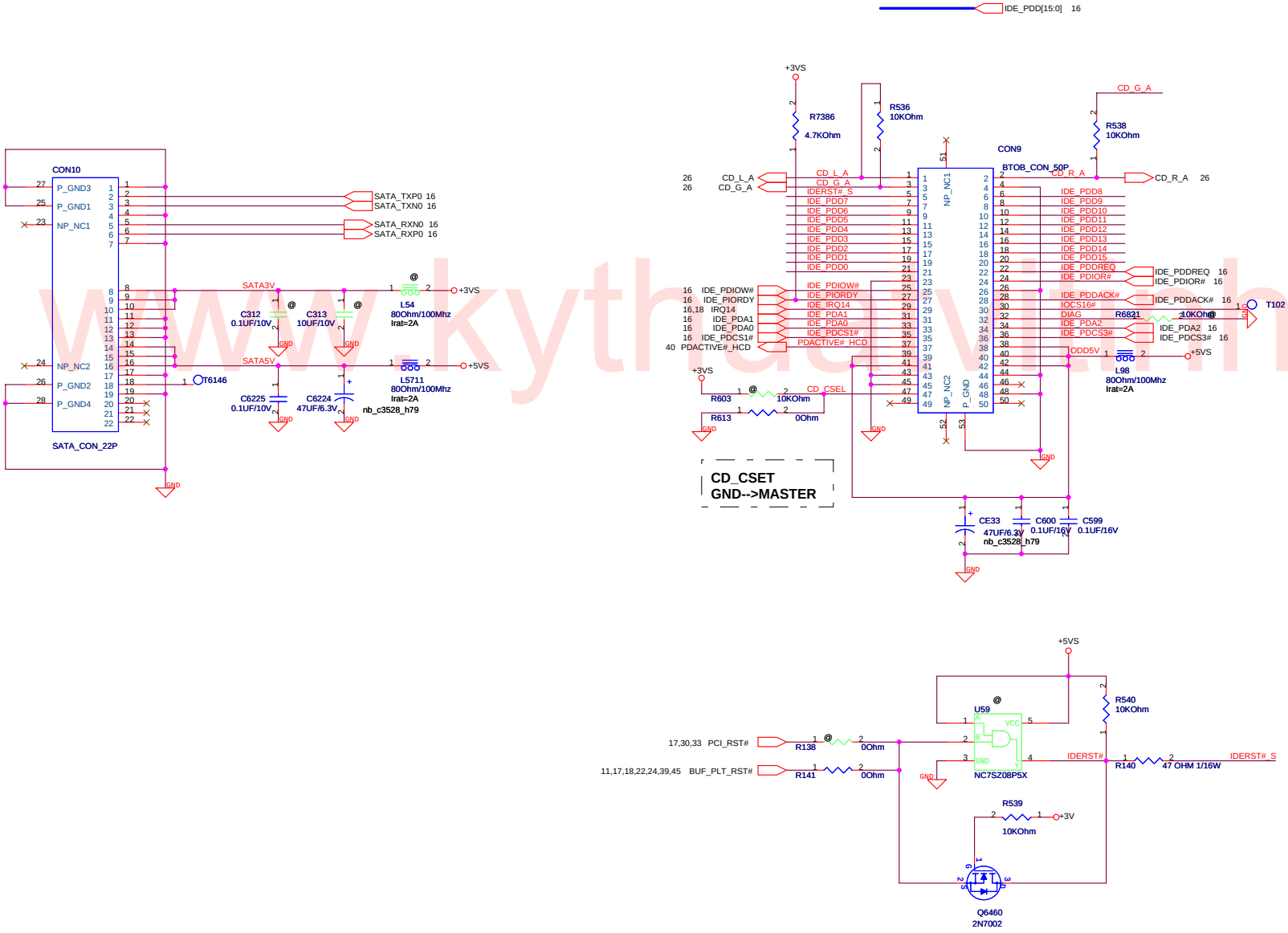




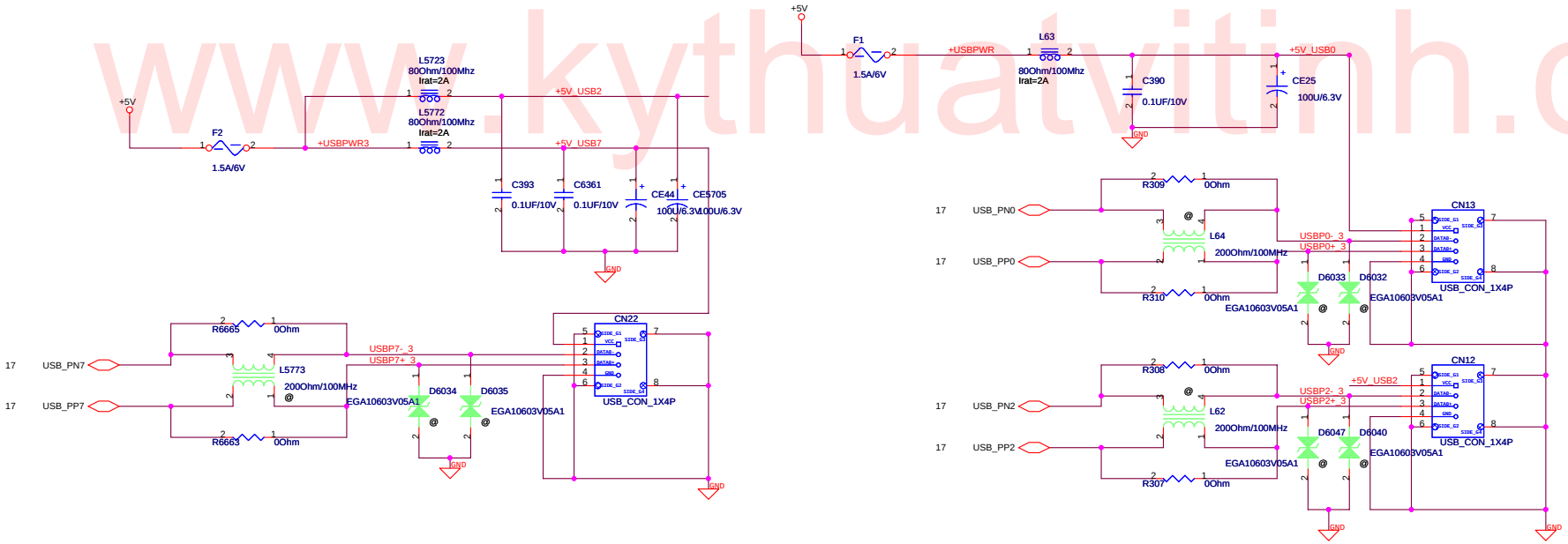


No stuff for UMA

ASUSTeK COMPUTER INC	Title : FAN	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 36 of 70	

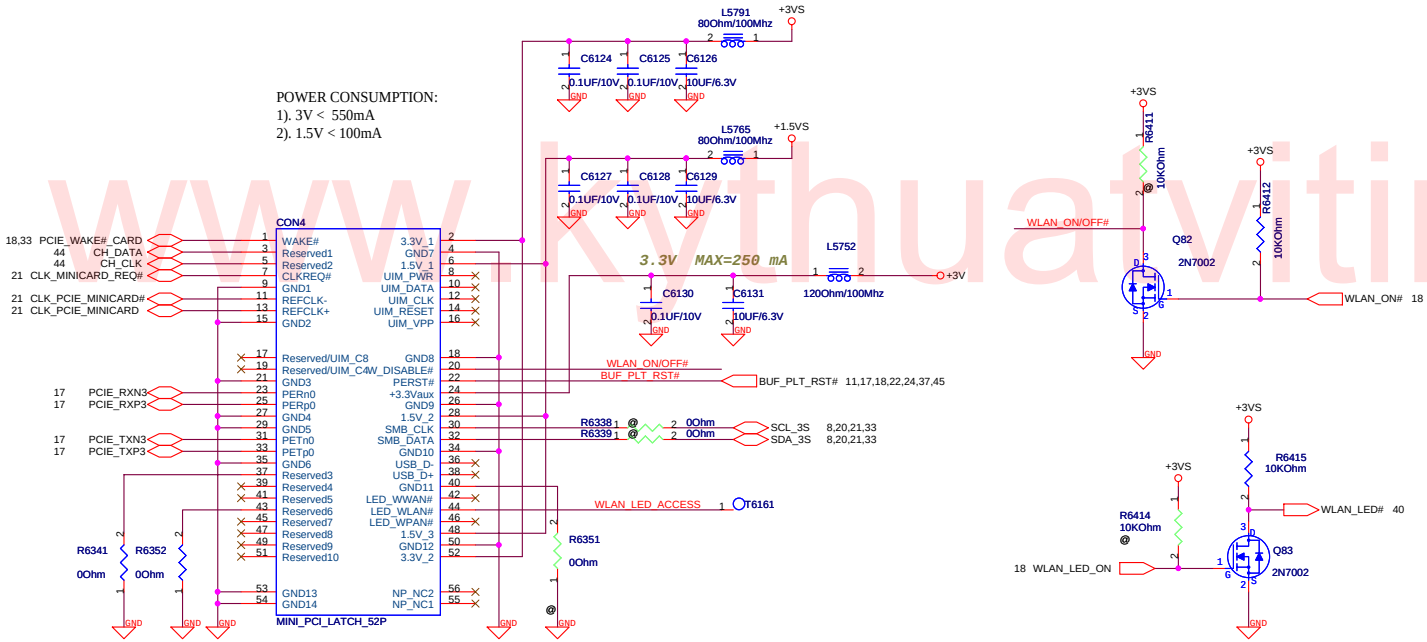


ASUSTeK COMPUTER INC	Title : HD+ODD	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 37 of 70	



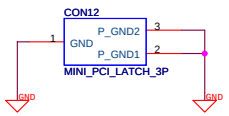
ASUSTeK COMPUTER INC	Title : USB CON* 3	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 38 of 70	

WLAN CON



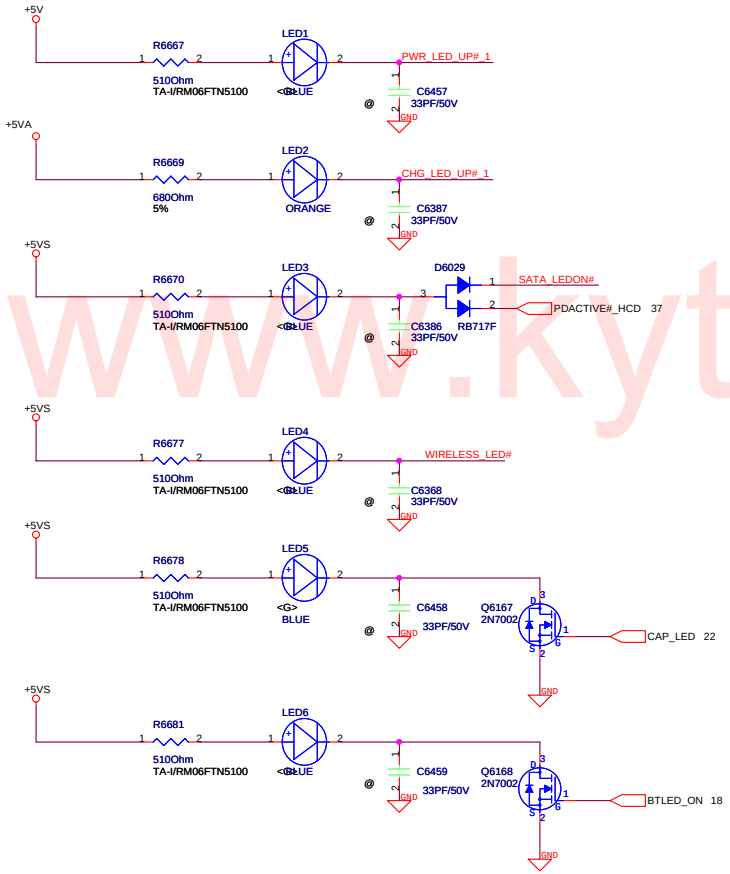
PCB Height =0mm

Mini Card Latch

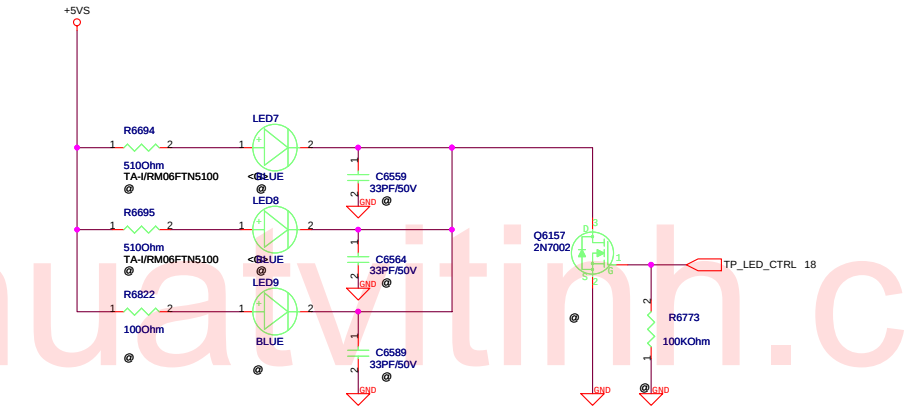


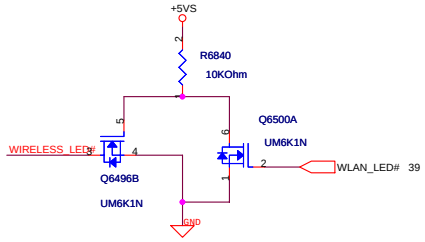
ASUSTeK COMPUTER INC	Title : MINICARD	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 39 of 70	

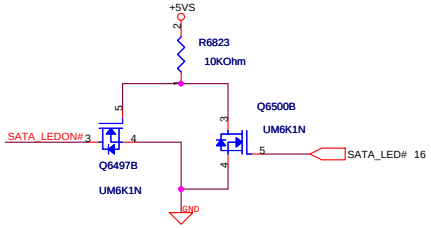
MB/LEDs

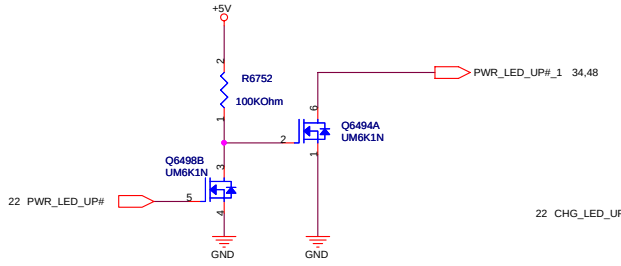


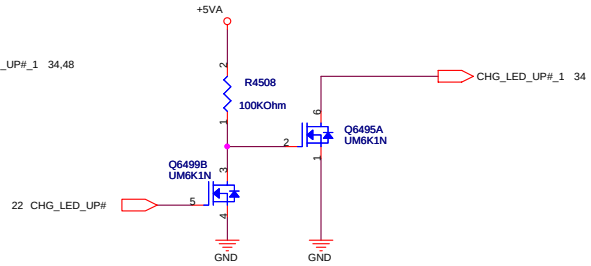
Touch Pad LED





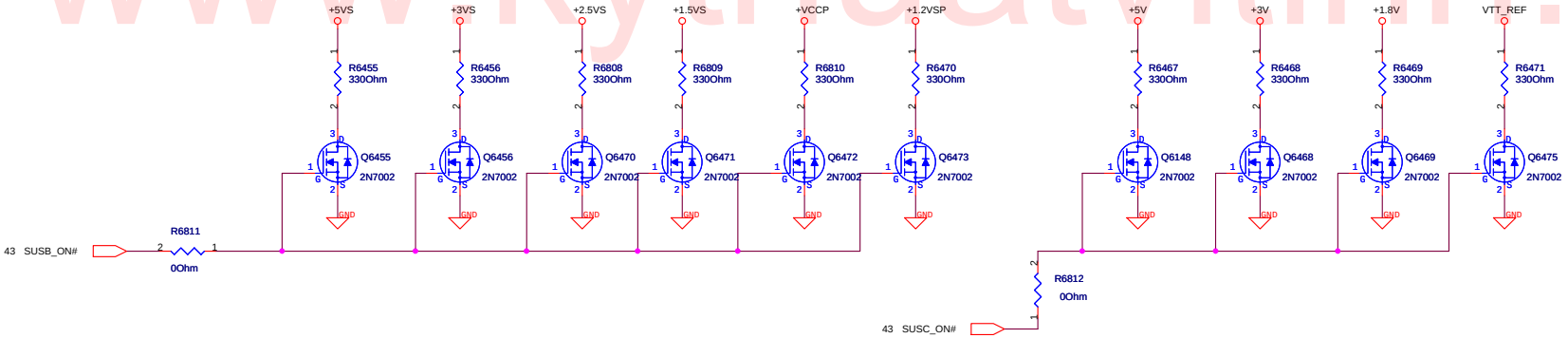






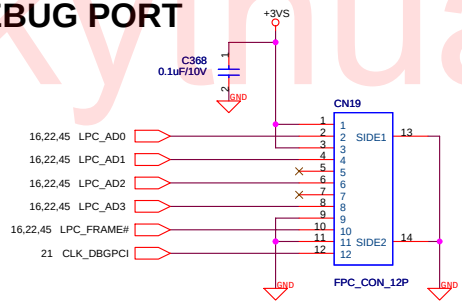
ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 40 of 70	

Discharge Circuit



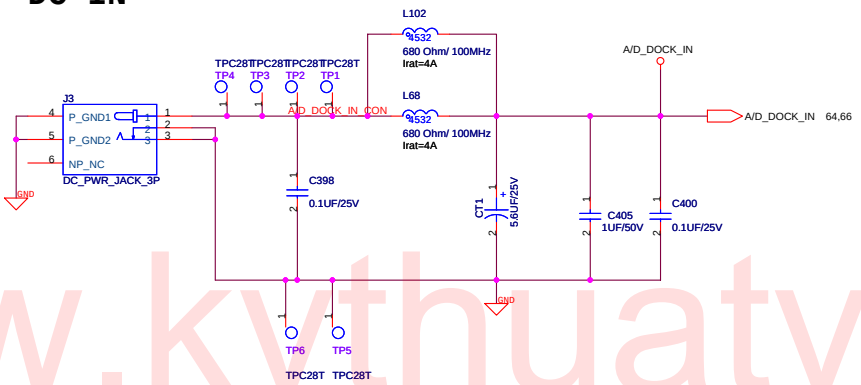
ASUSTeK COMPUTER INC	Title : Discharge	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 41 of 70	

LPC DEBUG PORT

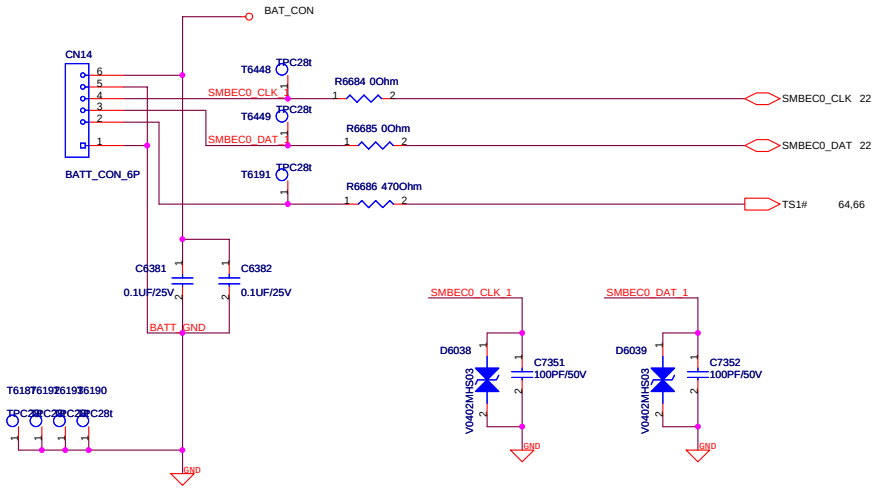


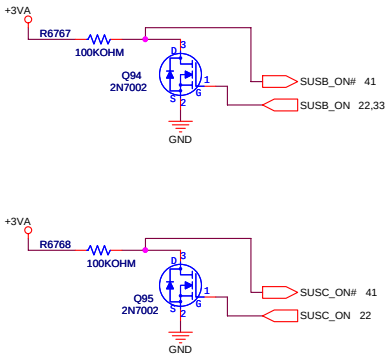
ASUSTeK COMPUTER INC	Title : Debug Port	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 42 of 70	

DC-IN



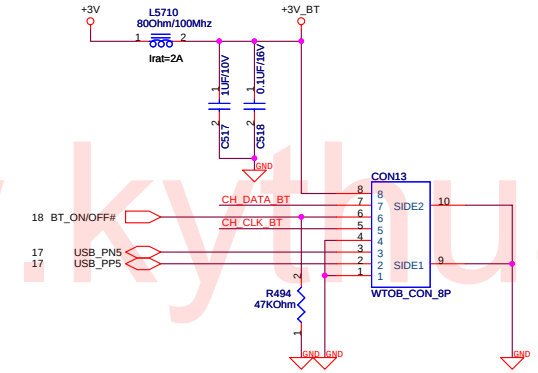
Battery Connector

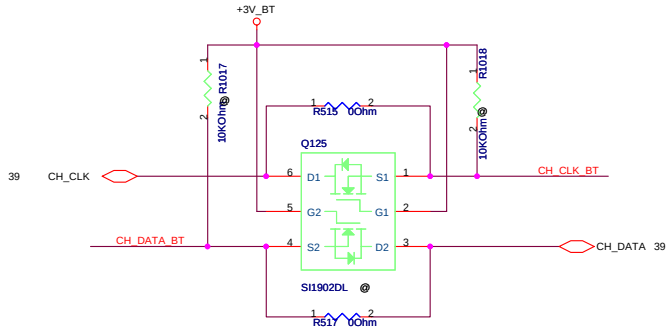




ASUSTeK COMPUTER INC	Title : DC-in / BAT con	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 43 of 70	

Bluetooth Module
Connector

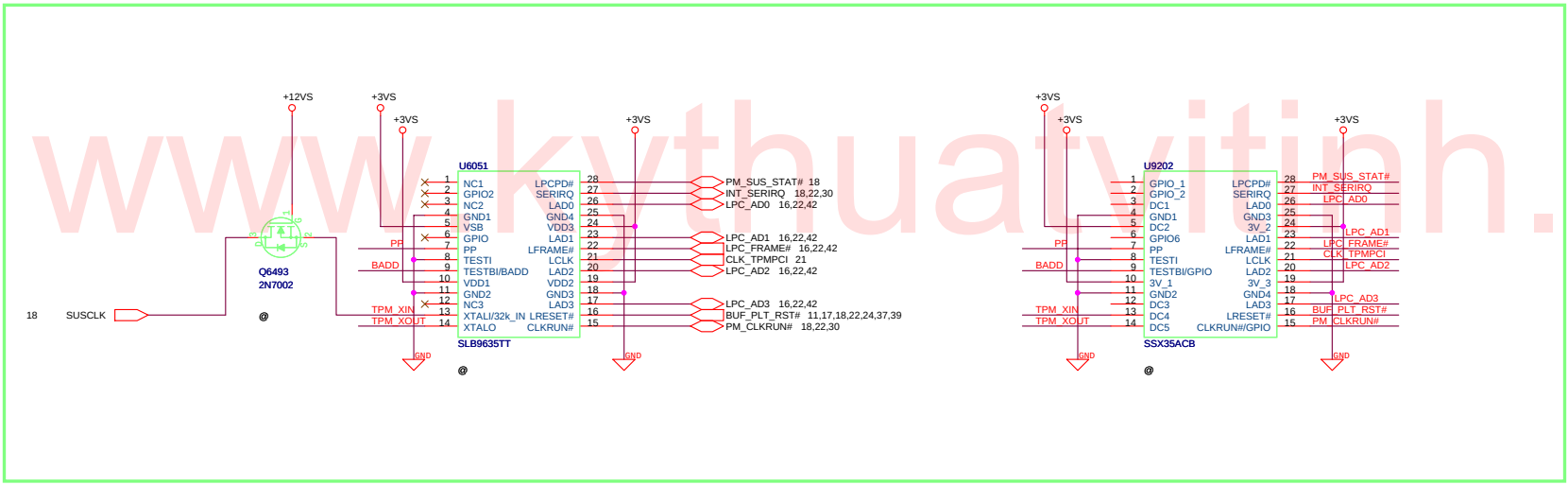


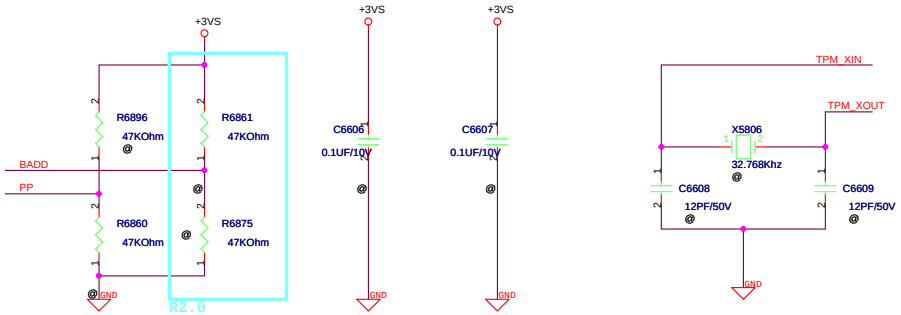


ASUSTeK COMPUTER INC	Title : BT	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 44 of 70	

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.

CO-LAYOUT





ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 45 of 70	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
VGA	AD16		A
LAN	AD16	0	B
CARD READER	AD17	1	B
CARDBUS	AD19	1	C
1394	AD17	1	D
MINIPCI 2 (802.11)	AD17	3	D,C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor (CPU)	1001100x (98)
Thermal Sensor (VGA)	1001101x (9A)

ICH8-M GPIO	W7S
GPIO 0	PM_BMBUSY#
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 7	WLAN_LED_ON
GPIO 8	EXT_SMI#
GPIO 11	SMBALERT#
GPIO 12	EXT_SCI_SB#
GPIO 15	STP_PCI#
GPIO 16	DPRSLPVR
GPIO 17	WLAN_ON#
GPIO 19	MEM_ID1
GPIO 20	BTLED_ON
GPIO 21	MEM_ID0
GPIO 22	MEMCLK_SET
GPIO 25	STP_CPU#
GPIO 27	BT_ON/OFF#
GPIO 29	USB_OC#5
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 36	MEM_ID2
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 40	USB_OC#1
GPIO 41	USB_OC#2
GPIO 43	USB_OC#4
GPIO 49	CPUPWRGD
GPIO 50	PCI_REQ#1
GPIO 52	PCI_REQ#2
GPIO 54	PCI_REQ#3

ITE8511 GPIO	W7S
GPA0	LCD_BL_PWM
GPA1	FAN_PWN
GPA4	CHG_LED_UP#
GPA5	PWR_LED_UP#
GPA7	LCD_BACKOFF#
GPB1	CAP_LED
GPB2	TP_LED_CTRL
GPB3	SMBEC0_CLK
GPB4	SMBEC0_DAT
GPB5	A20GATE
GPB6	RC_IN#
GPB7	THRO_CPU
GPC1	SMBEC1_CLK
GPC2	SMBEC1_DAT
GPC4	ACIN_OC#
GPC5	MUTE_POP_GPIO#
GPC6	BAT_IN_OC#
GPD0	SLP_S3#_R
GPD1	SLP_S4#_R
GPD2	BUF_PLT_RST#
GPD3	EXT_SCI#
GPD4	RFON_SW#
GPD6	FAN0_TACH
GPE2	MARATHON#
GPE4	PWR_ON#
GPE7	PM_CLKRUN#
GPF4	TPAD_CLK
GPF5	TPAD_DAT
GPG0	FA16
GPG1	FA17
GPG2	FA18
GPG3	FA19
GPG4	LID_SW#
GPG7	AC_APR_UC#
GPH0	VSUS_ON
GPH1	SUS_PWRGD
GPH2	CPU_PWRGD
GPH3	PM_PWRBTN#
GPH4	SUSC_ON
GPH5	SUSB_ON
GPH6	CPU_VRON
GPH7	PM_RSMRST#
GPI0	ICH8_PWROK
GPI1	ALL_SYSTEM_PWRGD
GPI3	CHG_EN#
GPI4	PRECHG
GPI5	EC_CLK_EN
GPI6	BAT_LEARN
GPJ4	PS_CPPE#
GPJ5	PS_SHDN#
GPM0	EXT_SMI#

ASUSTeK COMPUTER INC

Title : System Resource

Engineer: Lorentz_Chang

Size	Project Name	Rev
Custom	T76S	2.0

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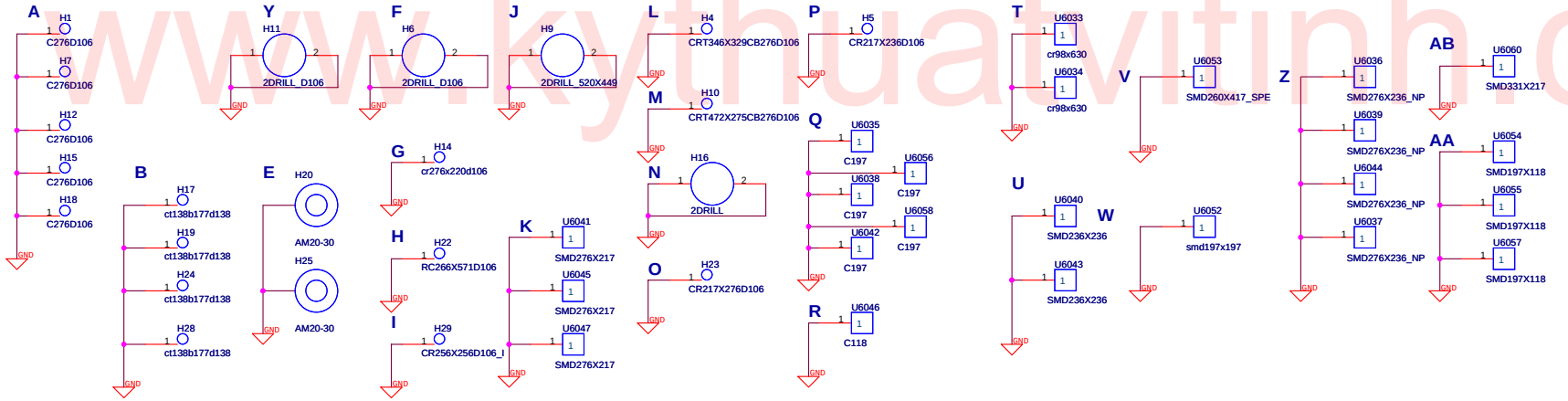
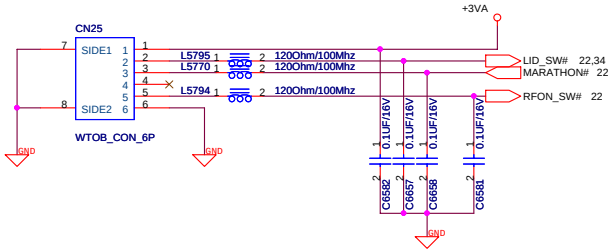
SCREW HOLE



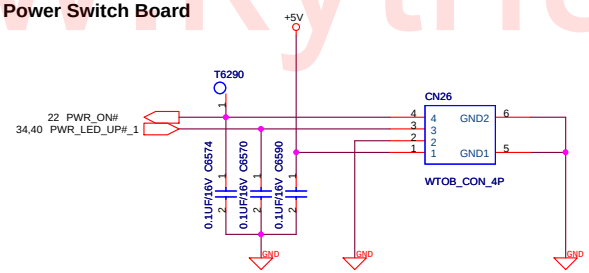
ASUSTeK COMPUTER INC	Title : ME	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 47 of 70	

LID_SW_Board

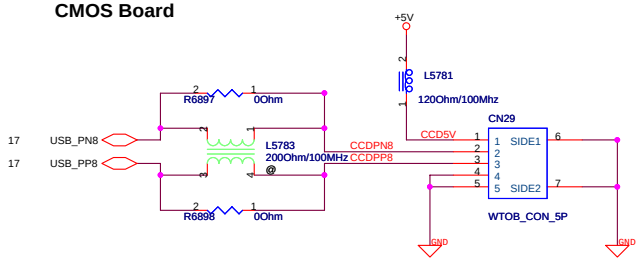



```
RFON_SW#(RF OFF)
----------------------------
right off --->  high
left  on  --->  low
```

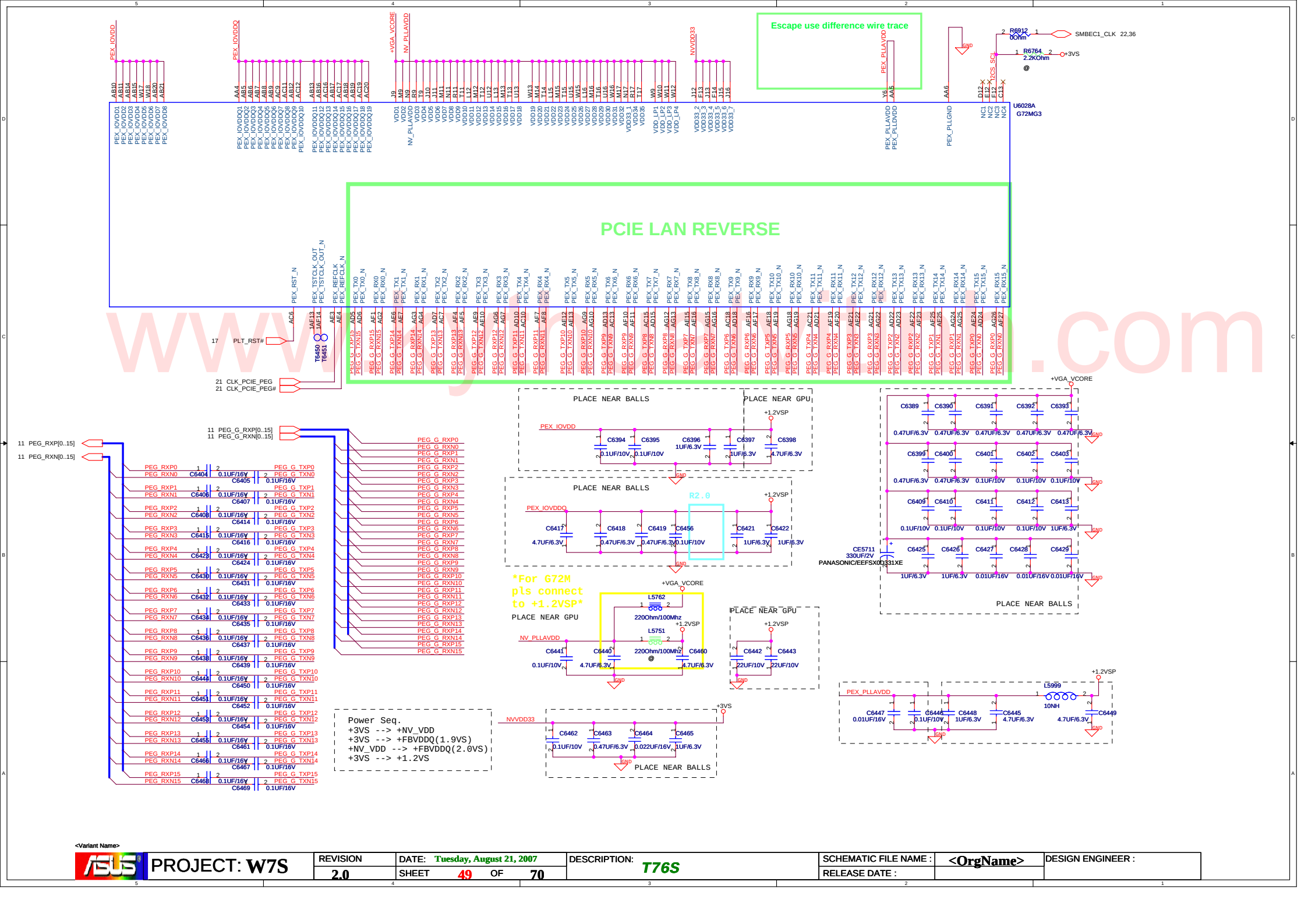

Power Switch Board

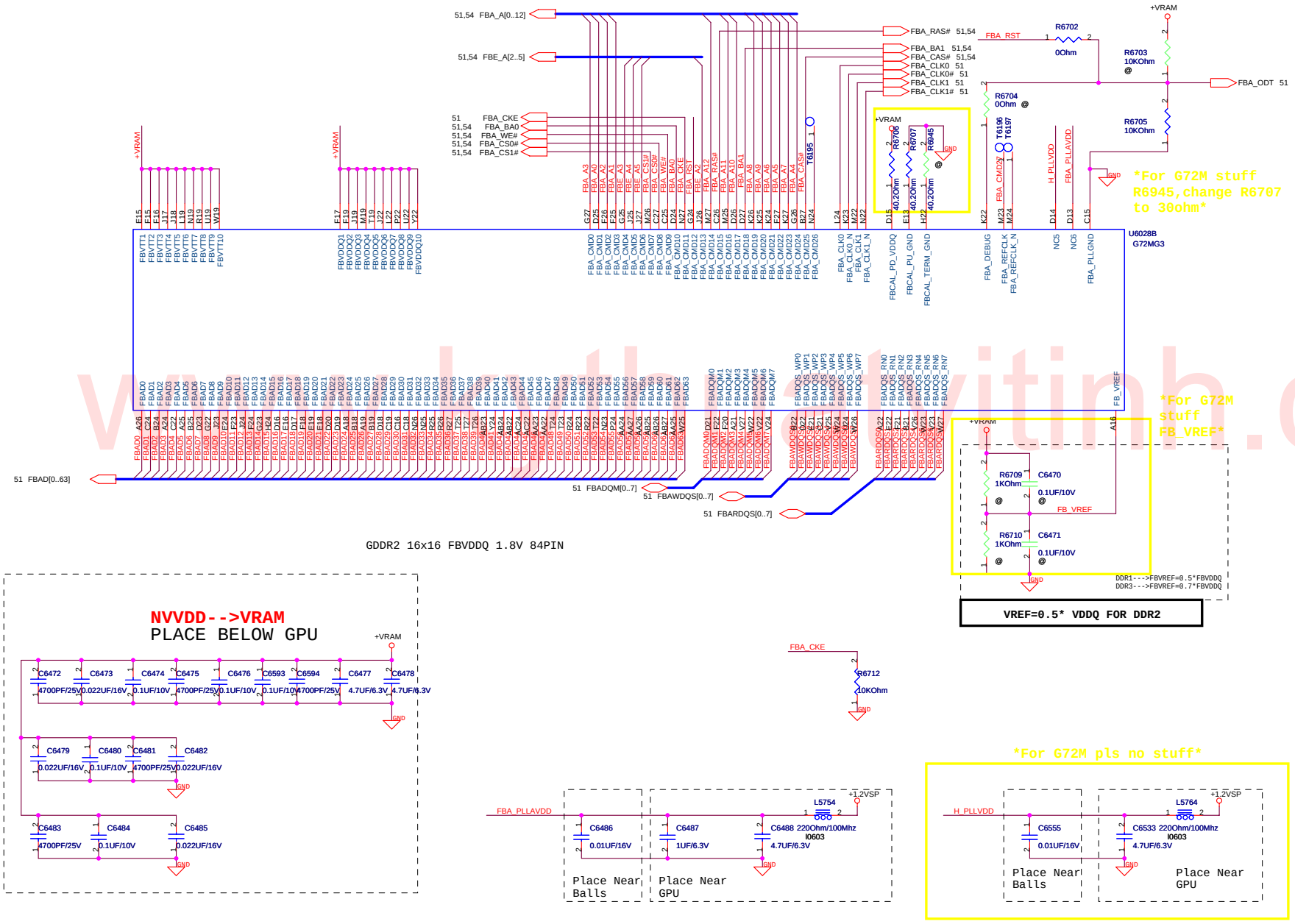


CMOS Board



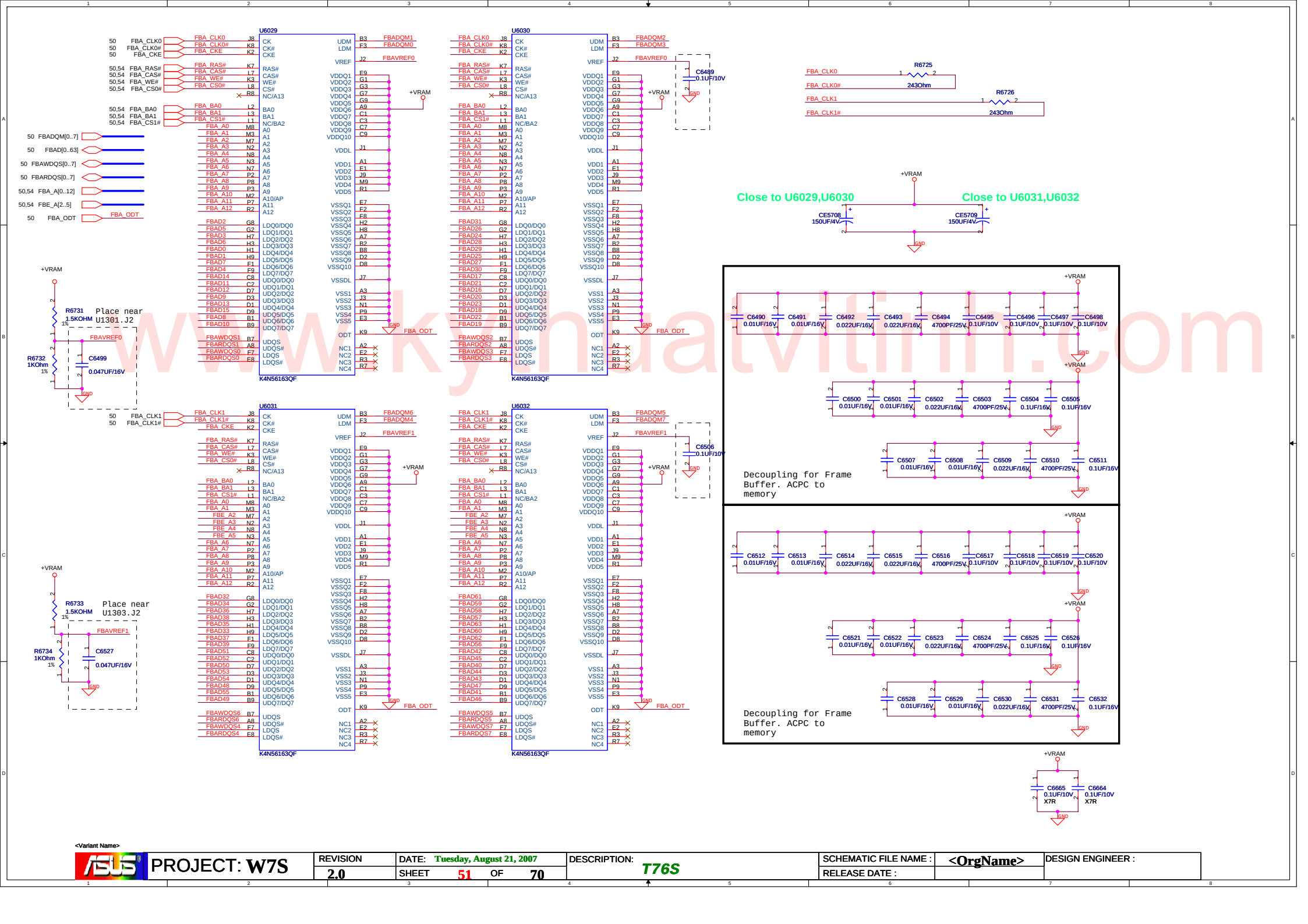
ASUSTeK COMPUTER INC	Title : Sub_Board		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 48 of 70		


Escape use difference wire trace
PCIE LAN REVERSE
U6028A
G72MG3
PLACE NEAR BALLS
PLACE NEAR GPU
*For G72M
pls connect
to +1.2VSP*
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS
PROJECT: W7S
REVISION
2.0
DATE: Tuesday, August 21, 2007
SHEET 49 OF 70
DESCRIPTION: T76S
SCHEMATIC FILE NAME :
RELEASE DATE :
<OrgName>
DESIGN ENGINEER :



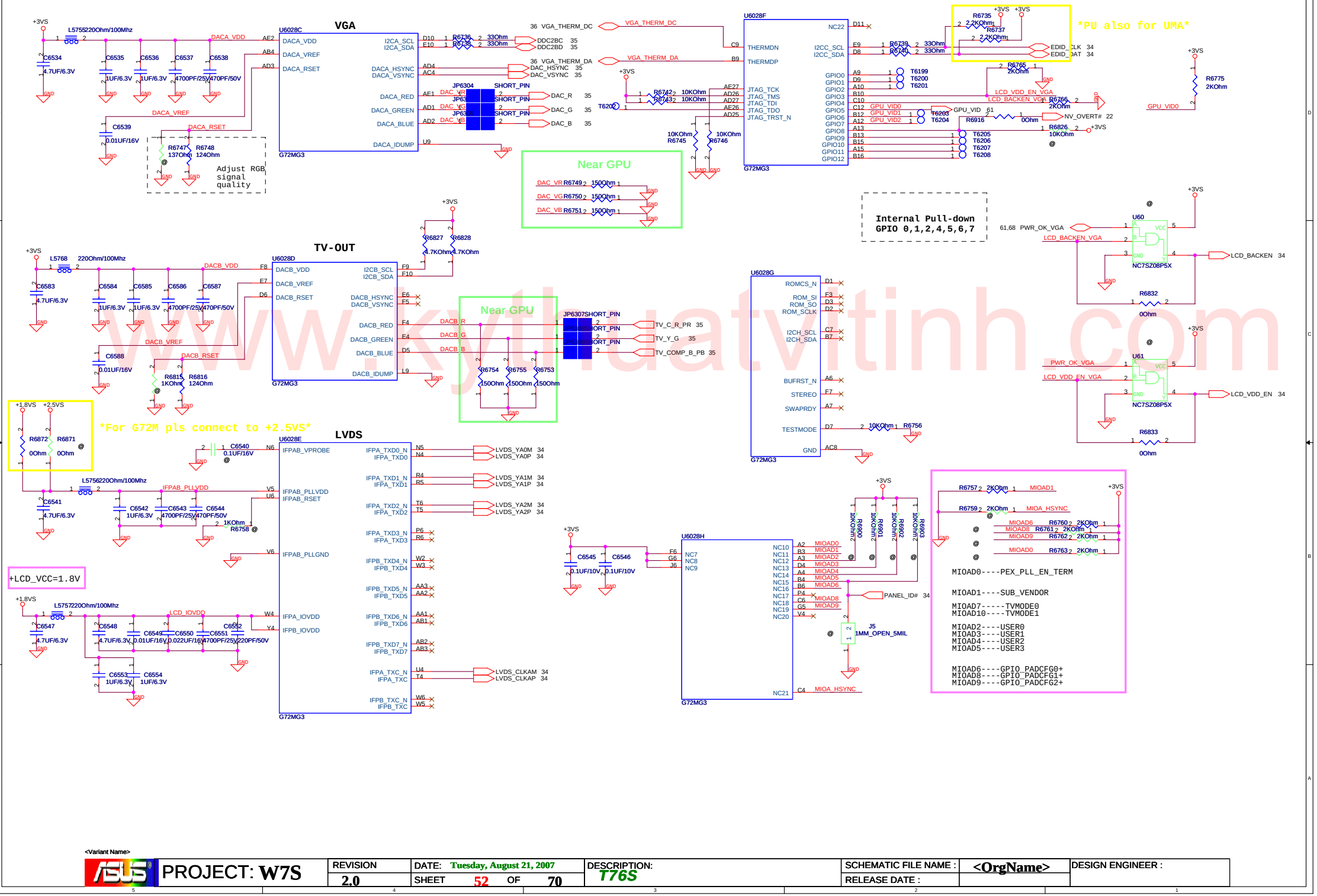
<Variant Name>

PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007 SHEET 50 OF 70	DESCRIPTION: T76S	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName> DESIGN ENGINEER :



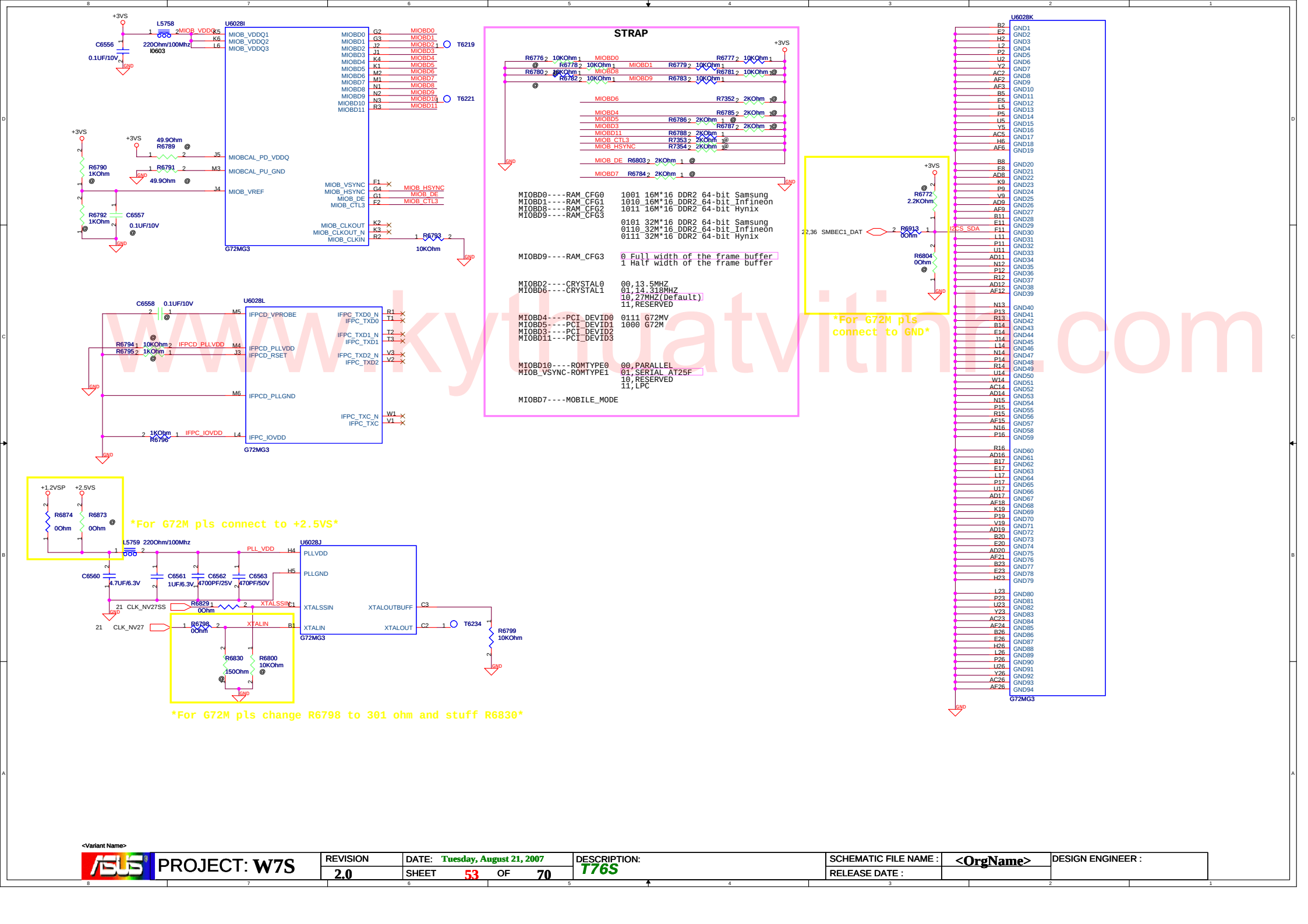
<Variant Name>

PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007	DESCRIPTION: T76S	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 51 OF 70		RELEASE DATE :		



<Variant Name>

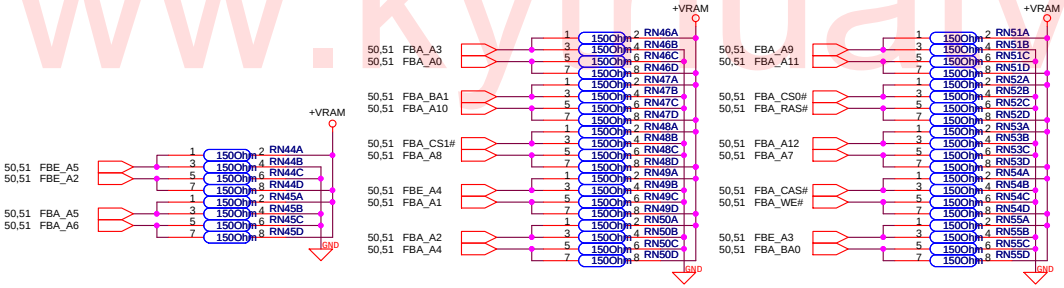
PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007	DESCRIPTION: T76S	SCHEMATIC FILE NAME :	<OrgName>
		SHEET 52 OF 70		RELEASE DATE :	DESIGN ENGINEER :

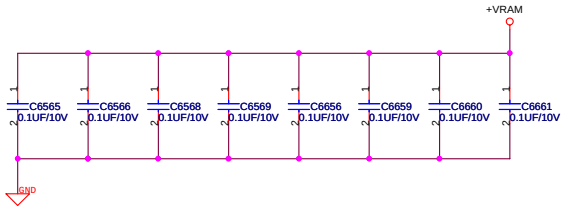


<Variant Name>

PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007	DESCRIPTION: T76S	SCHEMATIC FILE NAME :	<OrgName>
		SHEET 53 OF 70		RELEASE DATE :	DESIGN ENGINEER :

FBA CMD/ADDR Termination





<Variant Name>

ASUSTeK COMPUTER INC	Title : VGA-Terminator	
	Engineer:	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 54 of 70	

Rev	Date	Description
R1.0	2006/10/25	1. Initial release.
R1.1	2007/01/12	1. Change R6316 to 390 ohm page.21 2. Add R6662 and NET NV_OVERT# page.22 3. Del R6026 Add D6044,D6045,R6988 and R6990 page.28 4. Add R6989 page.29 5. Add R691 page.30 6. Add R6415 page.39 7. Add R6471 and Q6475 page.41 8. Add R6912 page.49 9. Change R6731,R6733 to 1.5Kohm and R6725, R6726 to 243ohm page.51 10. Add R6916 page.52 11. Add R6913 page.53
R2.0	2007/03/14	1. Add R6805 page.18 2. Change R6316 to 270 ohm page.21 3. Add R6628 page.28 4. Add R7381,Q6487 page.32 5. Change Q6483,Q6484,Q6485 to ESD protect device page.32 6. Change R6987 to 0 ohm page.35 7. Change R6859 pull high to +3VA page.36 8. Del C6595 page.49

Rev	Date	Description

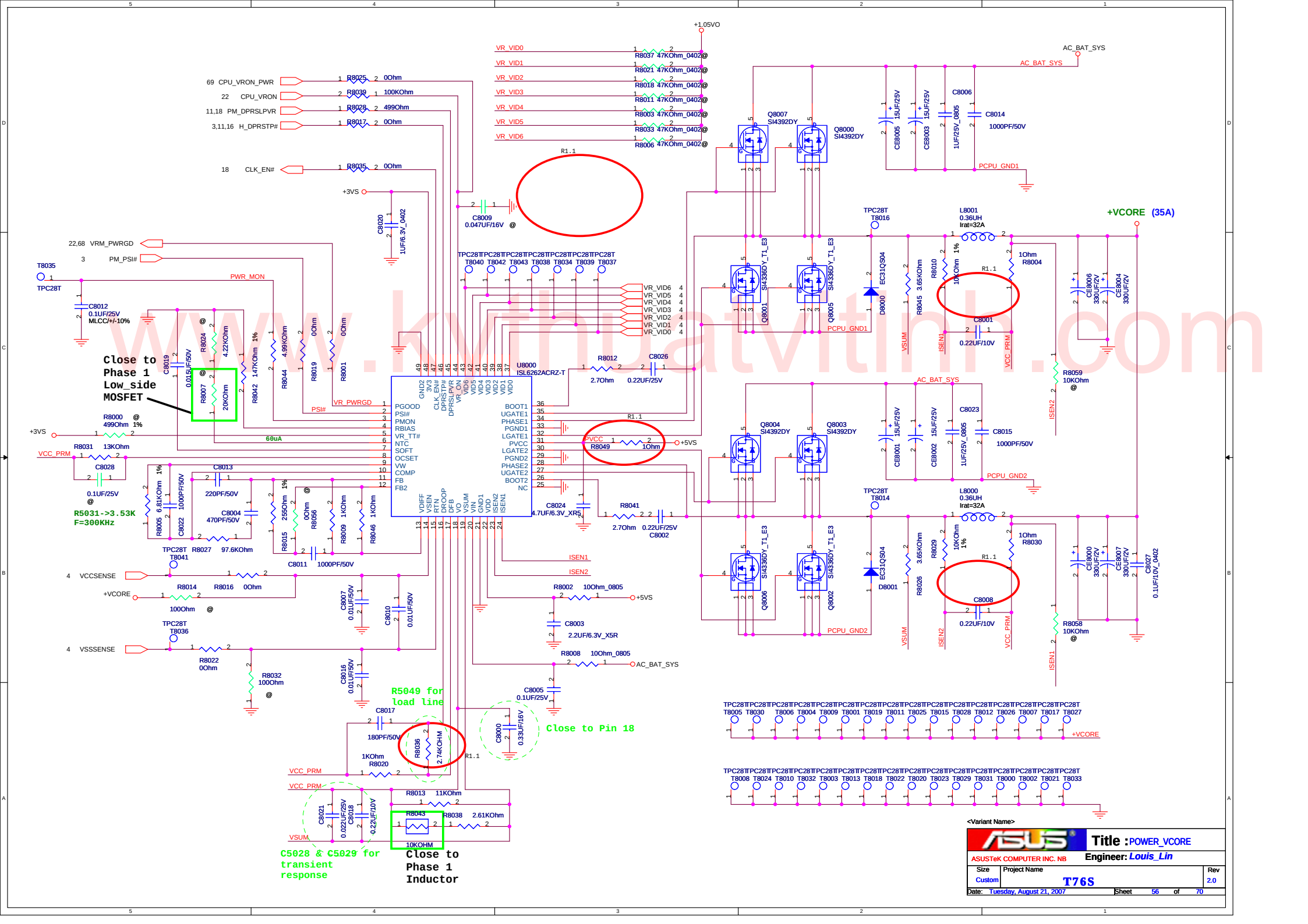
ASUSTeK COMPUTER INC

Title : History

Engineer: Lorentz_Chang

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 55 of 70


+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
R8037 47KOhm_0402@
R8021 47KOhm_0402@
R8018 47KOhm_0402@
R8011 47KOhm_0402@
R8003 47KOhm_0402@
R8033 47KOhm_0402@
R8006 47KOhm_0402@
AC_BAT_SYS
69 CPU_VRON_PWR
22 CPU_VRON
11,18 PM_DPRSLPVR
3,11,16 H_DPRSTP#
18 CLK_EN#
R8025 0Ohm
R8039 100KOhm
R8029 499Ohm
R8017 0Ohm
R8035 0Ohm
+3VS
C8020 1UF/6.3V_0402
C8009 0.047UF/16V @
R1.1
Q8007 SI4392DY
Q8000 SI4392DY
CE8005 15UF/25V
CE8003 15UF/25V
C8006 1UF/25V_0805
C8014 1000PF/50V
PCPU_GND1
+VCORE (35A)
TPC28T T8016
L8001 0.36UH Irat=32A
Q8001 SI4336DY_T1_E3
Q8005 SI4336DY_T1_E3
D8000 EC31QS04
R8045 3.65KOhm
R8010 10KOhm 1%
1Ohm R8004
C8001 0.22UF/10V
CE8006 330UF/2V
CE8004 330UF/2V
R8059 10KOhm @
22,68 VRM_PWRGD
3 PM_PSI#
T8035 TPC28T
PWR_MON
C8012 0.1UF/25V MLCC/+/-10%
Close to Phase 1 Low_side MOSFET
R8024 4.22KOhm
R8044 4.99KOhm
R8019 0Ohm
R8001 0Ohm
R8042 147KOhm 1%
R8007 20KOhm
C8019 0.015UF/50V
R8000 @ 499Ohm 1%
60uA
VR_PWRGD
PSI#
U8000 ISL6262ACRZ-T
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
R8012 2.7Ohm
C8026 0.22UF/25V
PVCC R8049 1Ohm
+5VS
C8024 4.7UF/6.3V_XR5
R8041 2.7Ohm
C8002 0.22UF/25V
R8031 13KOhm
C8028 0.1UF/25V @
R5031->3.53K F=300KHz
R8005 6.81KOhm 1%
C8022 1000PF/50V
C8013 220PF/50V
C8004 470PF/50V
R8015 255Ohm 1%
R8056 0Ohm @
R8009 1KOhm
R8046 1KOhm
C8011 1000PF/50V
TPC28T T8041
R8027 97.6KOhm
4 VCCSENSE
R8014
R8016 0Ohm
+VCORE
100Ohm @
C8007 0.01UF/50V
C8010 0.01UF/50V
TPC28T T8036
4 VSSSENSE
R8022 0Ohm
R8032 100Ohm @
C8016 0.01UF/50V
ISEN1
ISEN2
R8002 10Ohm_0805
C8003 2.2UF/6.3V_X5R
R8008 10Ohm_0805
C8005 0.1UF/25V
R5049 for load line
C8017 180PF/50V
R8036 2.74KOHM
1KOhm R8020
C8000 0.33UF/16V
Close to Pin 18
VCC_PRM
R8013 11KOhm
R8043
R8038 2.61KOhm
10KOHM
VSUM
C8021 0.022UF/25V
C8018 0.22UF/10V
C5028 & C5029 for transient response
Close to Phase 1 Inductor
TPC28T T8040 T8042 T8043 T8038 T8034 T8039 T8037
VR_VID6 4
VR_VID5 4
VR_VID4 4
VR_VID3 4
VR_VID2 4
VR_VID1 4
VR_VID0 4
Q8004 SI4392DY
Q8003 SI4392DY
CE8001 15UF/25V
CE8002 15UF/25V
C8023 1UF/25V_0805
C8015 1000PF/50V
PCPU_GND2
TPC28T T8014
L8000 0.36UH Irat=32A
Q8006 SI4336DY_T1_E3
Q8002 SI4336DY_T1_E3
D8001 EC31QS04
R8026 3.65KOhm
R8029 10KOhm 1%
1Ohm R8030
C8008 0.22UF/10V
CE8000 330UF/2V
CE8007 330UF/2V
C8027 0.1UF/10V_0402
R8058 10KOhm @
TPC28T T8005 T8030 T8006 T8004 T8009 T8001 T8019 T8011 T8025 T8015 T8028 T8012 T8026 T8007 T8017 T8027
+VCORE
TPC28T T8008 T8024 T8010 T8032 T8003 T8013 T8018 T8022 T8020 T8023 T8029 T8031 T8000 T8002 T8021 T8033
<Variant Name>
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Louis_Lin
Size Custom
Project Name T76S
Rev 2.0
Date: Tuesday, August 21, 2007
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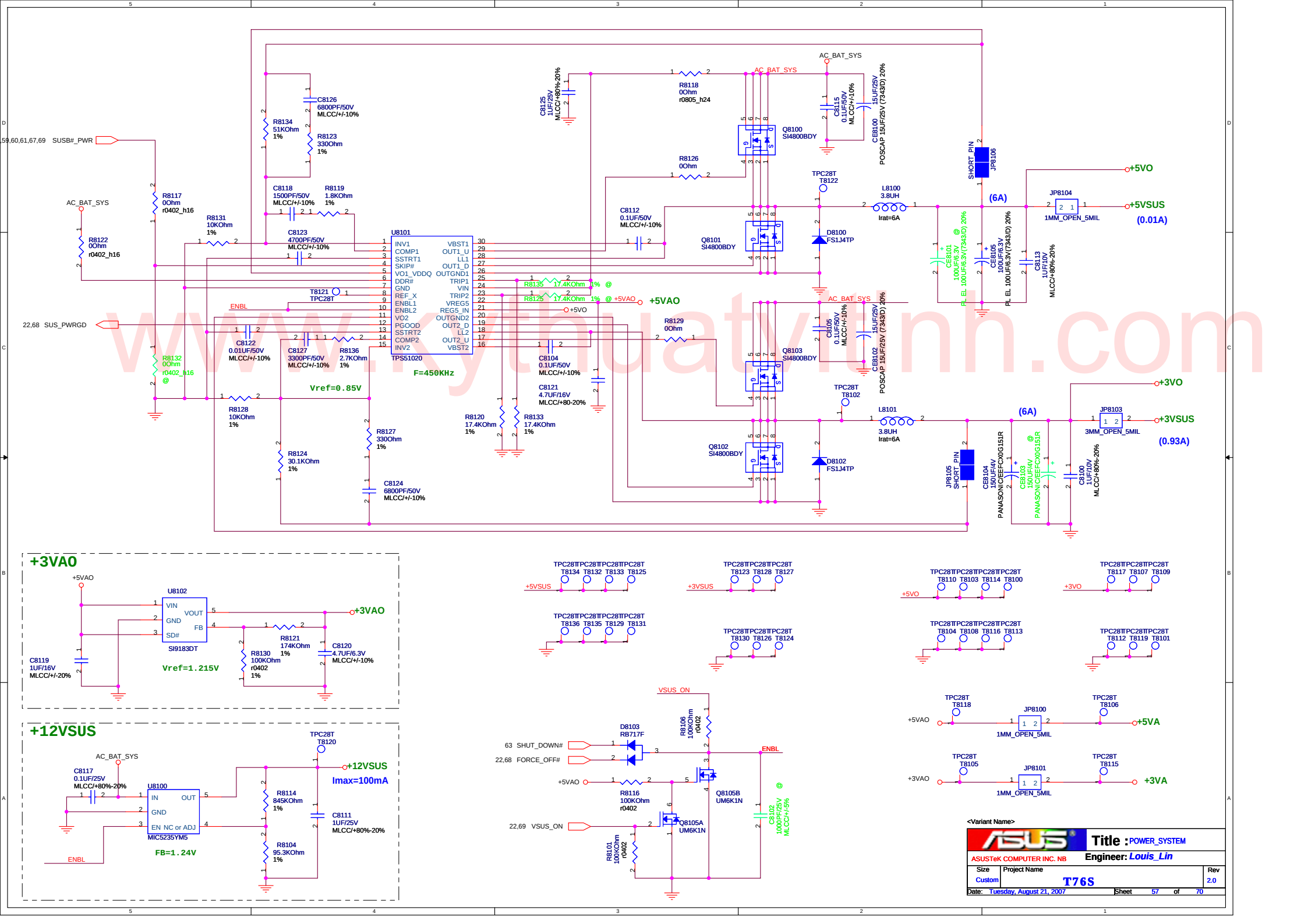
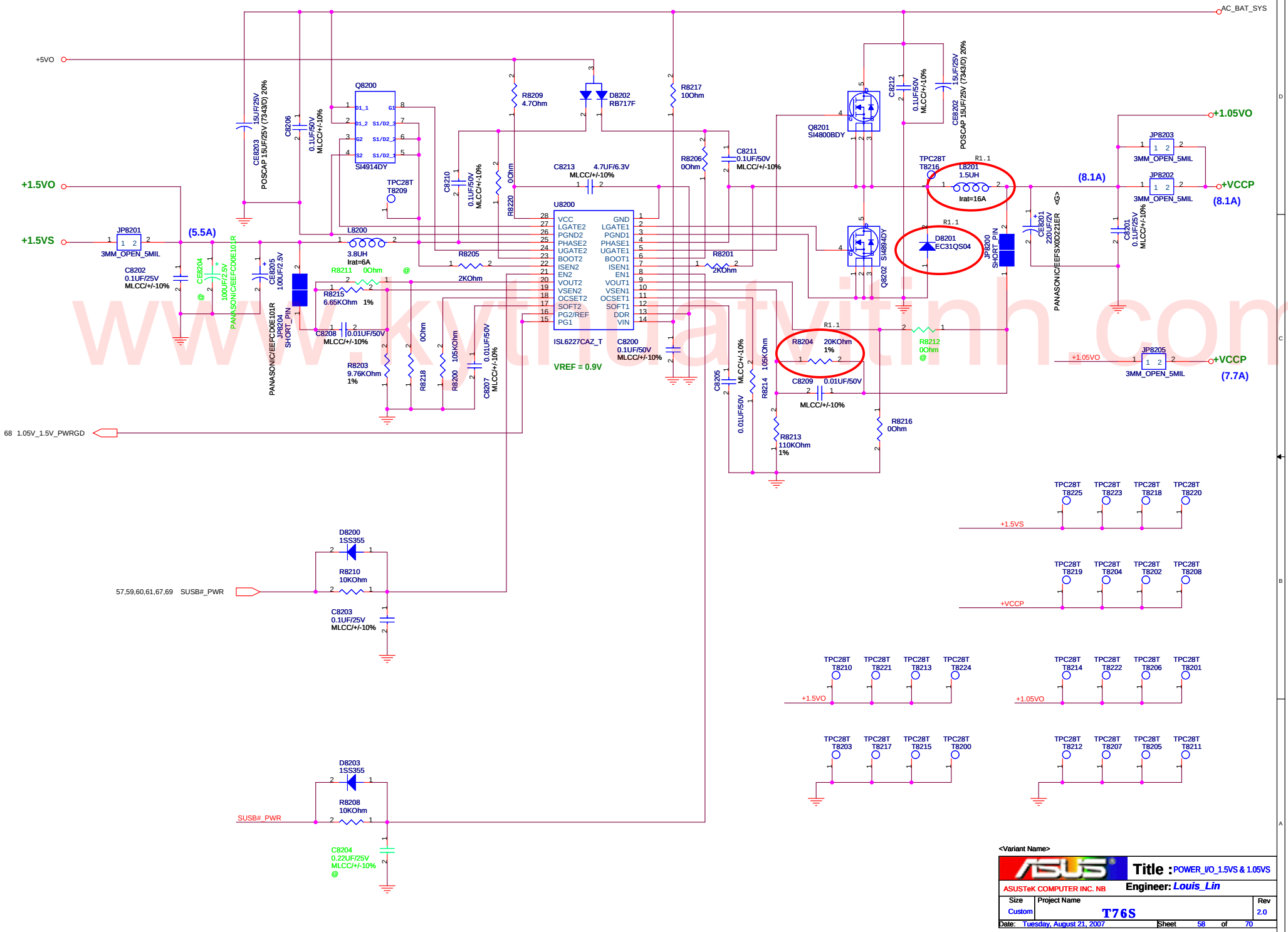
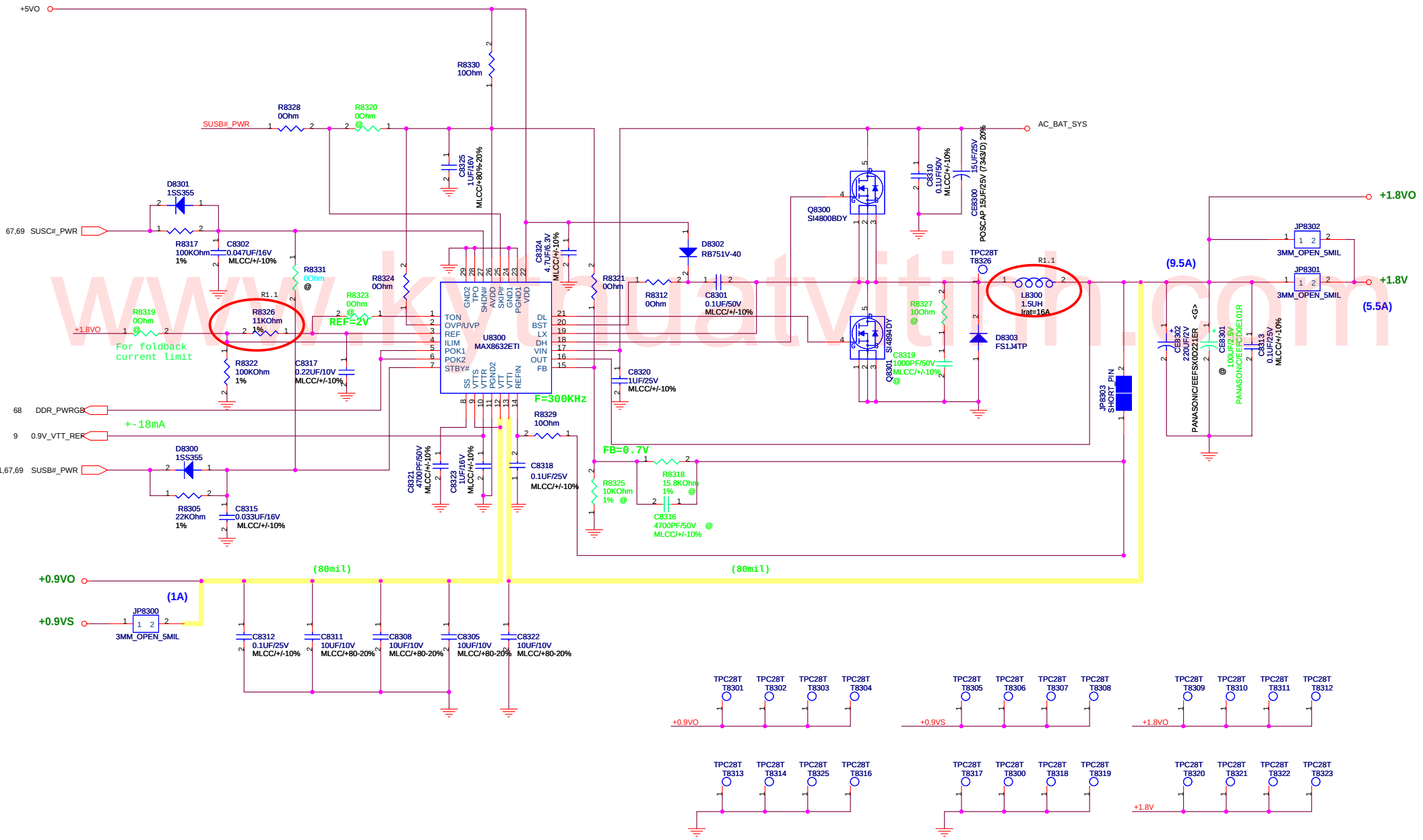






<Variant Name>

Title : POWER_I/O_DDR & VTT

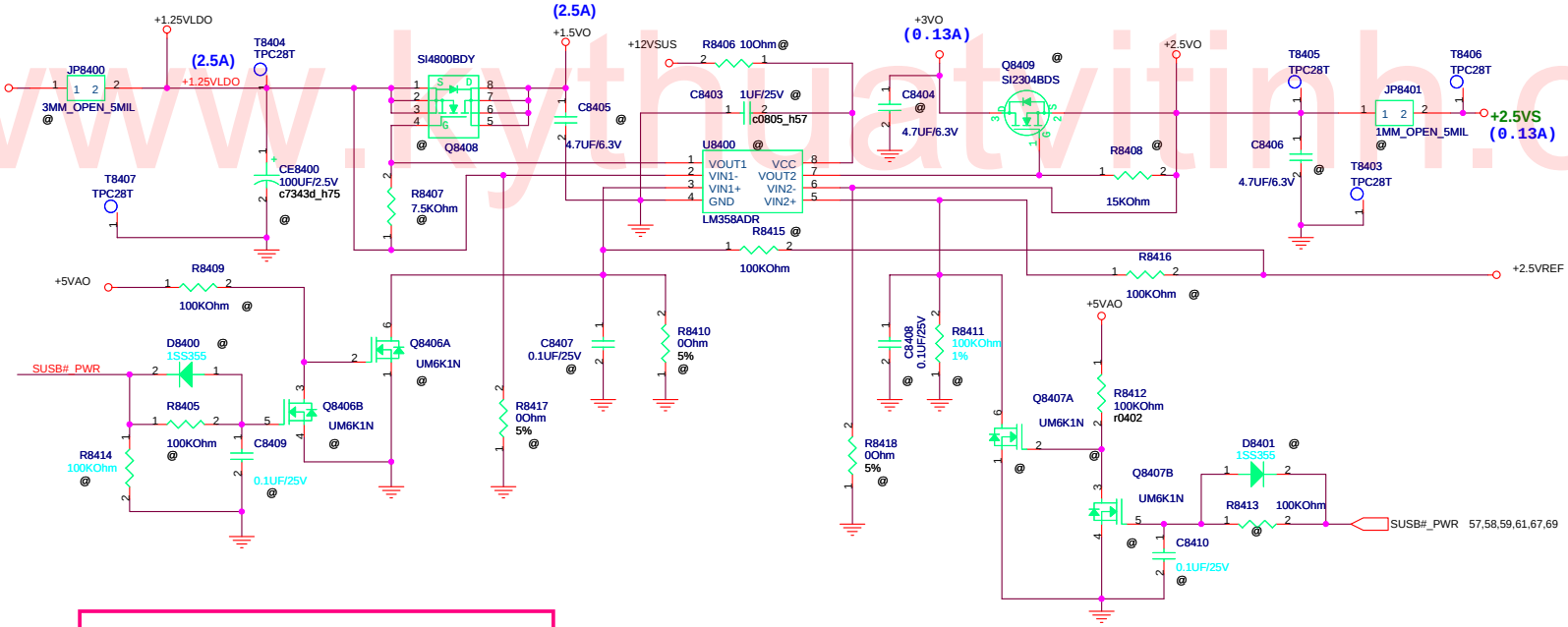
ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 59 of 70

+1.25VS & +2.5VS



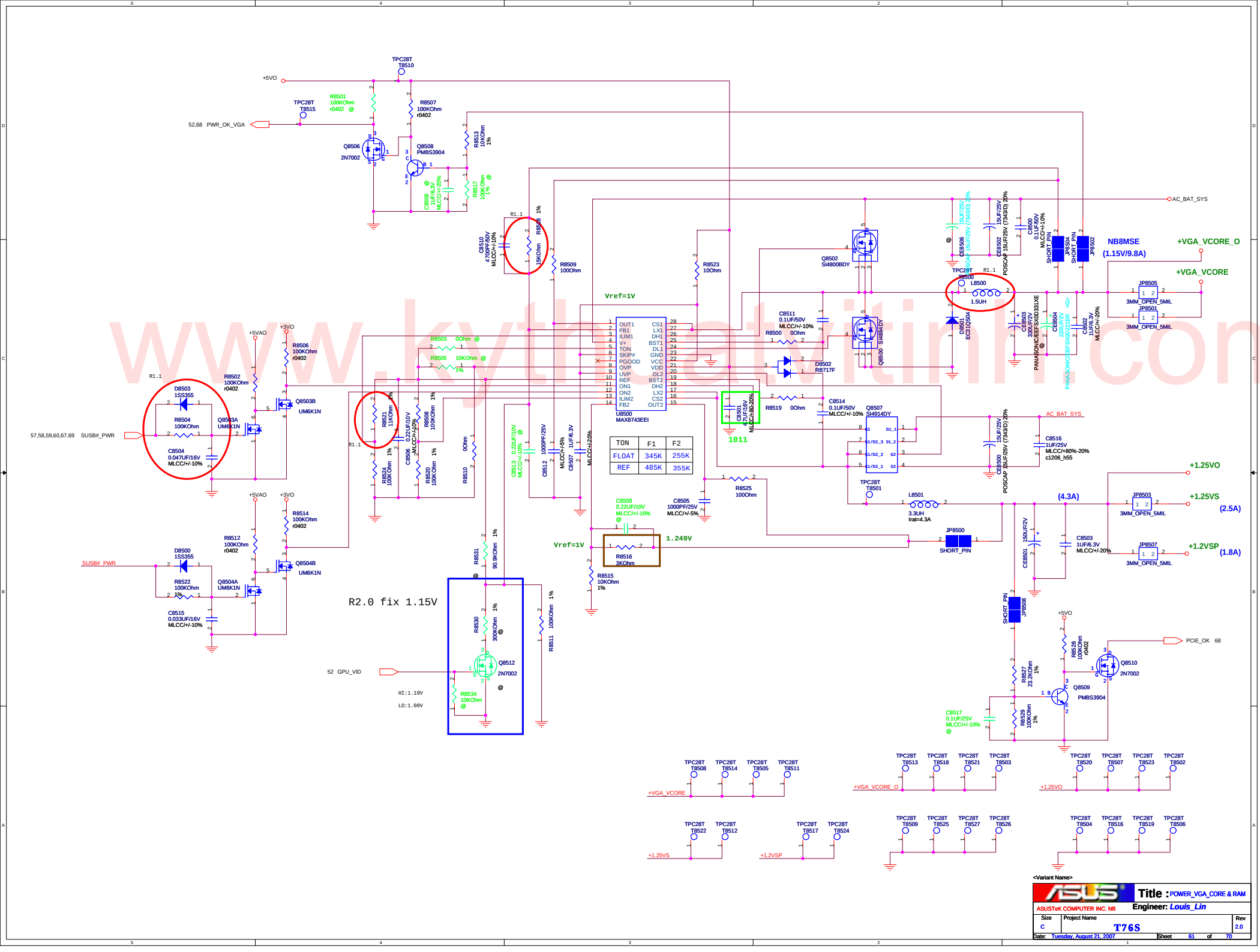
UMA Enable +1.25VS
R8417 UNMOUNT, R8410 100K 10G212100314010

Discrete VGA Disable +1.25VS
R8417 MOUNT, R8410 0 ohm 10G212000004030
And other UNMOUNT.

R8414,D8400,C8409 Always Keep UNMOUNT

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_ +1.25VS&+2.5VS	
	Engineer: Louis_Lin	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 60 of 70	


U8500
MAX8743EEI
Vref=1V
1.249V
R2.0 fix 1.15V
1011
TON F1 F2
FLOAT 345K 255K
REF 485K 355K
NB8MSE
(1.15V/9.8A)
+VGA_VCORE_O
+VGA_VCORE
+1.25VO
+1.25VS
(2.5A)
+1.2VSP
(1.8A)
(4.3A)
AC_BAT_SYS
PWR_OK_VGA
SUSB#_PWR
GPU_VID
PCIE_OK
HI:1.10V
LO:1.00V
L8500 1.5UH
L8501 3.3UH Irat=4.3A
Q8502 SI4800BDY
Q8500 SI4864DY
Q8507 SI4914DY
D8501 EC31QS04
D8502 RB717F
Q8506 2N7002
Q8508 PMBS3904
Q8512 2N7002
Q8510 2N7002
Q8509 PMBS3904
Q8503A UM6K1N
Q8503B UM6K1N
Q8504A UM6K1N
Q8504B UM6K1N
D8503 1SS355
D8500 1SS355
JP8500 SHORT_PIN
JP8502 SHORT PIN
JP8503 3MM_OPEN_5MIL
JP8505 3MM_OPEN_5MIL
JP8501 3MM_OPEN_5MIL
JP8507 3MM_OPEN_5MIL
JP8508 SHORT PIN
C8500 0.1UF/50V MLCC/+/-10%
C8502 15UF/25V POSCAP 15UF/25V (7343D) 20%
C8503 330UF/2V PANASONIC/EEFSX0D331XE
C8504 220UF/2V PANASONIC/EEFSX0D221ER
C8505 1000PF/25V MLCC/+/-5%
C8506 0.22UF/10V MLCC/+/-10%
C8507 1UF/6.3V MLCC/+/-20%
C8509 0.22UF/10V MLCC/+/-10%
C8510 4700PF/50V MLCC/+/-10%
C8511 0.1UF/50V MLCC/+/-10%
C8512 1000PF/25V MLCC/+/-5%
C8513 0.22UF/10V MLCC/+/-10%
C8514 0.1UF/50V MLCC/+/-10%
C8516 1UF/25V MLCC/+/-80%-20%
C8517 0.1UF/25V MLCC/+/-10%
C8501 470UF/16V MLCC/+/-20%
C8503 1UF/6.3V MLCC/+/-20%
R8501 100KOhm r0402 @
R8502 100KOhm r0402
R8503 0Ohm @
R8504 100KOhm
R8505 10KOhm @ 1%
R8506 100KOhm r0402
R8507 100KOhm r0402
R8508 15KOhm
R8509 100Ohm
R8510 0Ohm
R8511 100KOhm 1%
R8512 100KOhm r0402
R8513 10KOhm 1%
R8514 100KOhm r0402
R8515 10KOhm 1%
R8516 3KOhm
R8517 100KOhm 1% @
R8519 0Ohm
R8521 11KOhm
R8522 100KOhm 1%
R8523 10Ohm
R8524 100KOhm 1%
R8525 100Ohm
R8527 23.2KOhm 1%
R8528 100KOhm r0402
R8529 100KOhm 1%
R8530 300KOhm 1% @
R8531 90.9KOhm 1%
R8534 10KOhm @
C8504 0.047UF/16V MLCC/+/-10%
C8515 0.033UF/16V MLCC/+/-10%
TPC28T T8510
TPC28T T8515
TPC28T T8501
TPC28T JP8500
TPC28T T8508
TPC28T T8514
TPC28T T8505
TPC28T T8511
TPC28T T8513
TPC28T T8518
TPC28T T8521
TPC28T T8503
TPC28T T8520
TPC28T T8507
TPC28T T8523
TPC28T T8502
TPC28T T8522
TPC28T T8512
TPC28T T8517
TPC28T T8524
TPC28T T8509
TPC28T T8525
TPC28T T8527
TPC28T T8526
TPC28T T8504
TPC28T T8516
TPC28T T8519
TPC28T T8506
+5VO
+5VAO
+3VO
52,68 PWR_OK_VGA
57,58,59,60,67,69 SUSB#_PWR
52 GPU_VID
68 PCIE_OK
<Variant Name>
Title : POWER_VGA_CORE & RAM
ASUSTeK COMPUTER INC. NB
Engineer: Louis_Lin
Size C
Project Name T76S
Rev 2.0
Date: Tuesday, August 21, 2007
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<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
B	T76S	2.0

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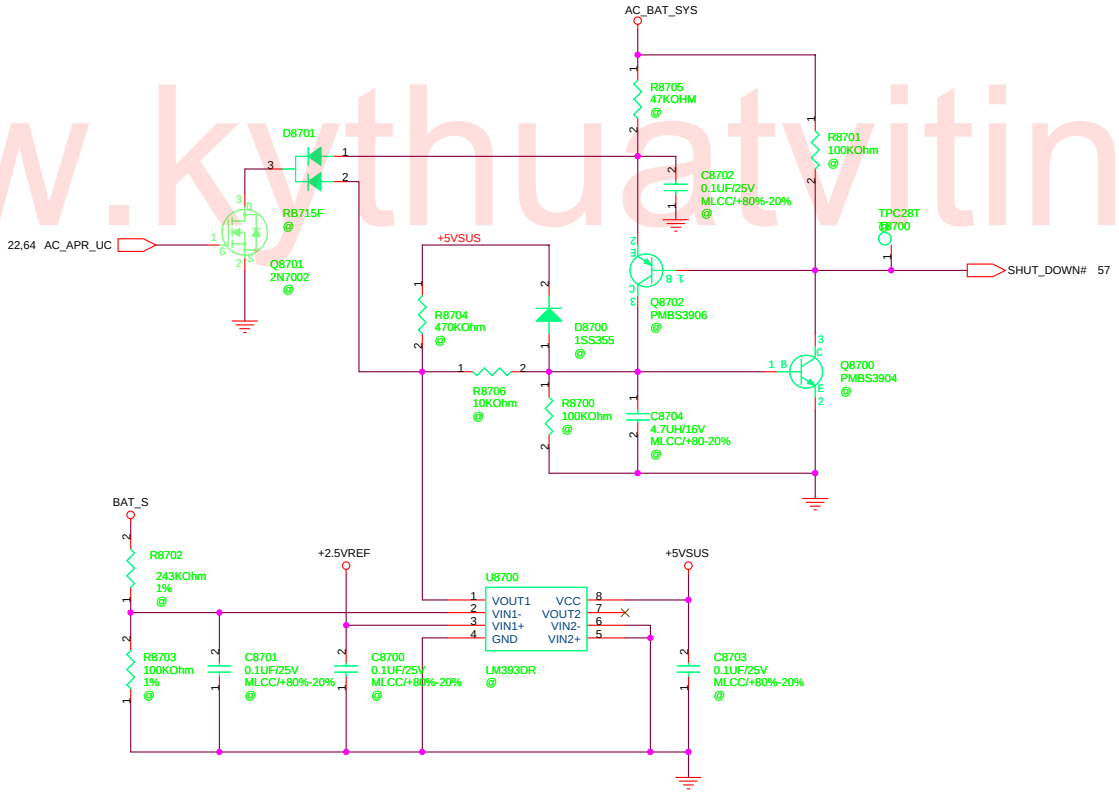
PIC only



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SHUTDOWN#

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

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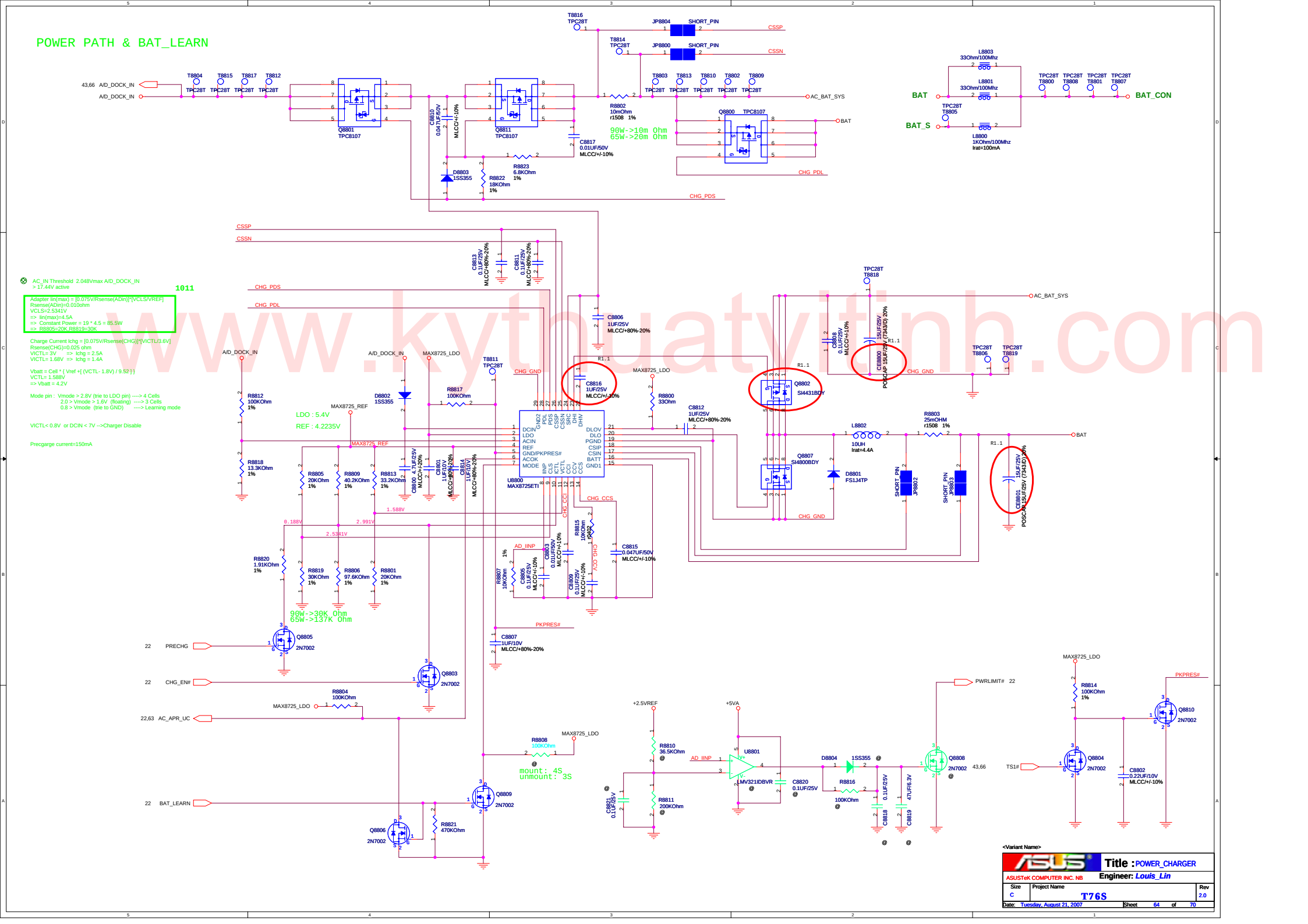
POWER PATH & BAT_LEARN



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_CHARGER

Engineer: Louis_Lin

Size	Project Name	Rev
C	T76S	2.0

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<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

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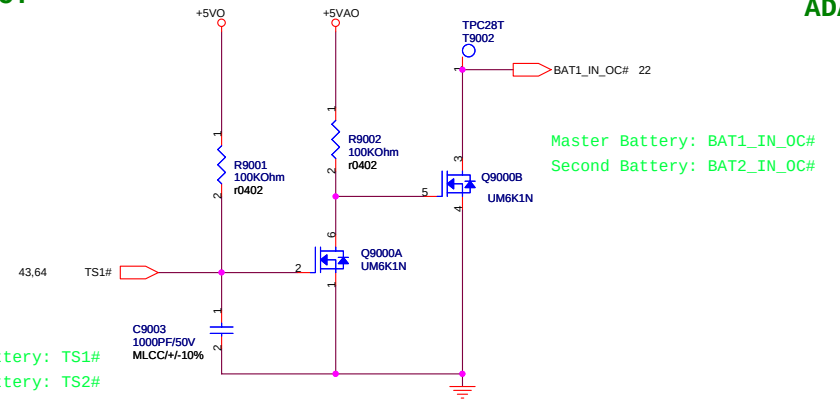
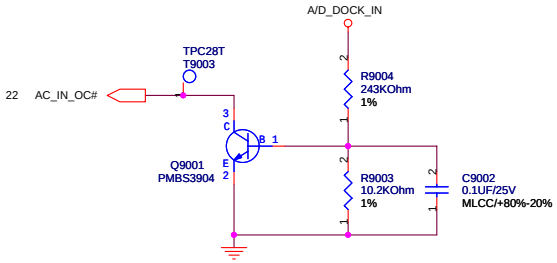
BATTERY IN DETECT



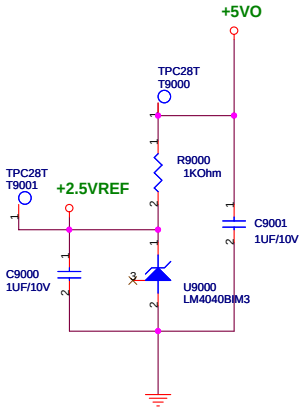
Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

Master Battery: TS1#
Second Battery: TS2#

ADAPTER IN DETECT



+2.5VREF



<Variant Name>

Title : POWER_DETECT

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

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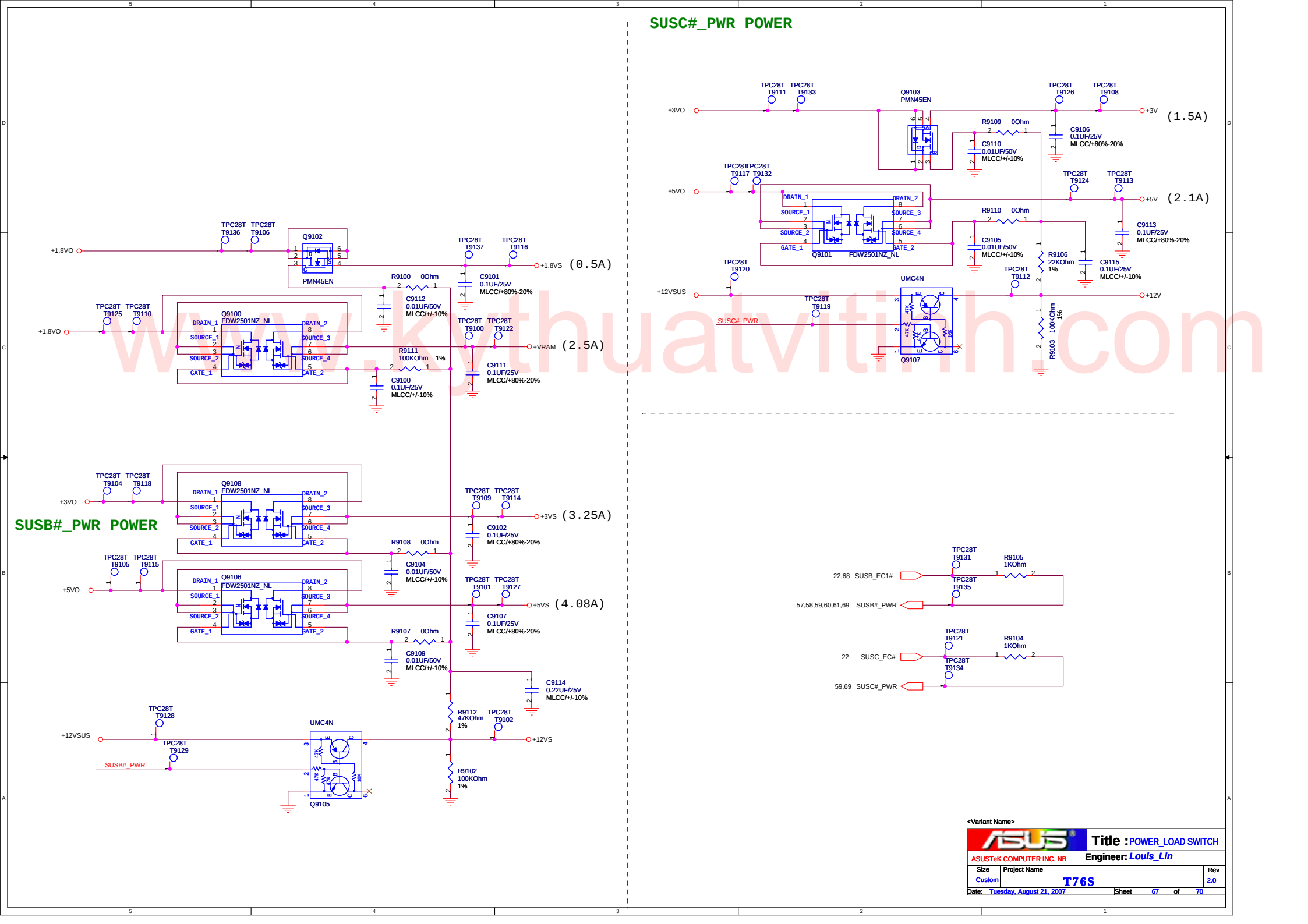
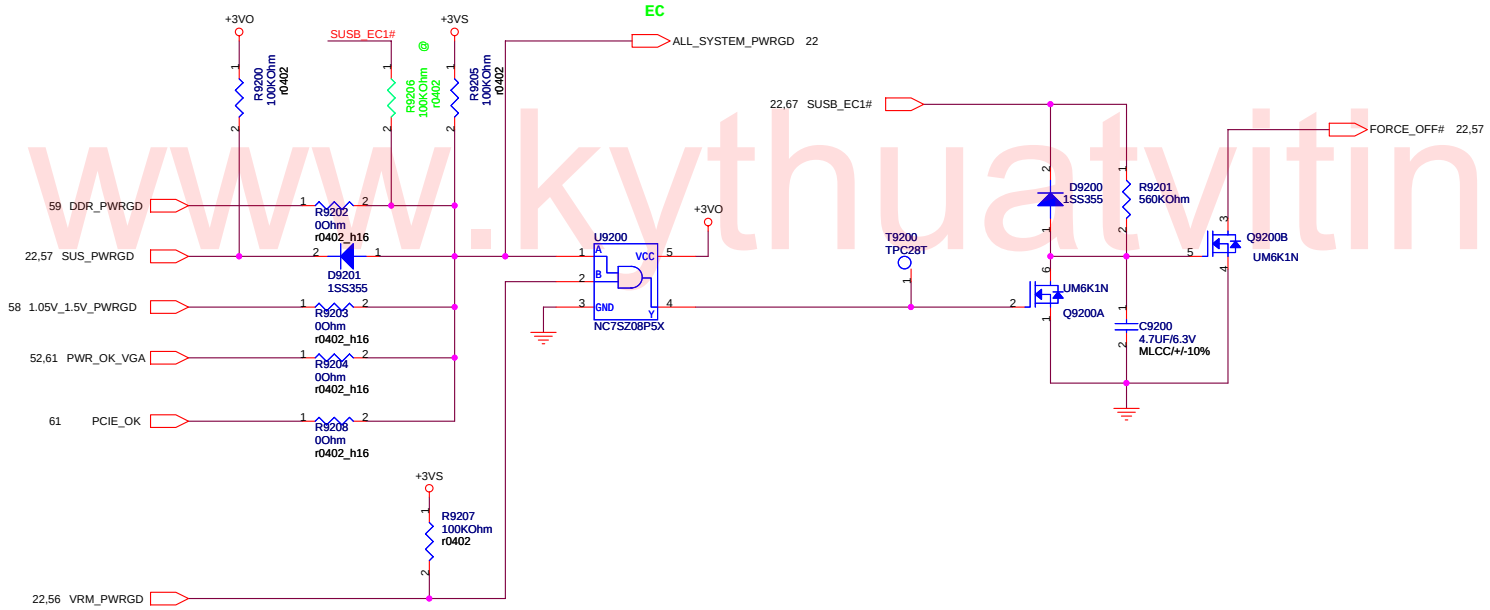


POWER GOOD DETECTER



<Variant Name>

Title : POWER_PROTECT

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 68 of 70

AC_BAT_SYS — AC_BAT_SYS 34,56,57,58,59,61,63,64

BAT — BAT 64

BAT_CON — BAT_CON 43,64

+2.5VREF — +2.5VREF 60,63,64,66

+3VA — +3VA 16,22,43,48,57

+5VAO — +5VAO 57,60,61,66

+5VO — +5VO 57,58,59,61,66,67

+5VSUS — +5VSUS 19,57,63

+5V — +5V 9,26,28,38,40,41,48,67

+5VS — +5VS 19,20,23,26,28,29,35,36,37,40,41,56,67

+3VO — +3VO 57,60,61,67,68

+3VSUS — +3VSUS 17,18,19,22,24,28,57

+3V — +3V 17,25,33,37,39,41,44,67

+3VS — +3VS 3,8,11,14,15,16,18,19,20,21,22,24,26,28,30,31,32,33,34,35,36,37,39,41,42,45,49,52,53,56,67,68

+12VSUS — +12VSUS 57,60,67

+12V — +12V 18,28,32,67

+12VS — +12VS 45,67

+1.8VO — +1.8VO 59,67

+1.8V — +1.8V 6,7,8,9,11,13,14,41,59

+1.8VS — +1.8VS 52,67

+0.9VS — +0.9VS 9,59

+0.9VO — +0.9VO 59

+1.05VO — +1.05VO 56,58

+VCCP — +VCCP 3,4,5,10,11,13,14,16,19,21,41,58

+1.5VO — +1.5VO 58,60

+1.5VS — +1.5VS 4,14,16,17,19,33,39,41,58

+2.5VO — +2.5VO 60

+2.5VS — +2.5VS 41,52,53,60

+VCORE — +VCORE 4,5,56

+VGA_VCORE — +VGA_VCORE 49,61

+VRAM — +VRAM 50,51,54,67

+1.2VSP — +1.2VSP 41,49,50,53,61

+1.25VS — +1.25VS 11,14,19,60,61

FOR POWER TEST

+3VA

JP9300 (SGL_JUMP): 1 — 1 2 — 2 — CPU_VRON_PWR 56

JP9301 (SGL_JUMP): 1 — 1 2 — 2 — SUSB#_PWR — SUSB#_PWR 57,58,59,60,61,67

JP9302 (SGL_JUMP): 1 — 1 2 — 2 — SUSC#_PWR — SUSC#_PWR 59,67

JP9303 (SGL_JUMP): 1 — 1 2 — 2 — VSUS_ON — VSUS_ON 22,57

<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

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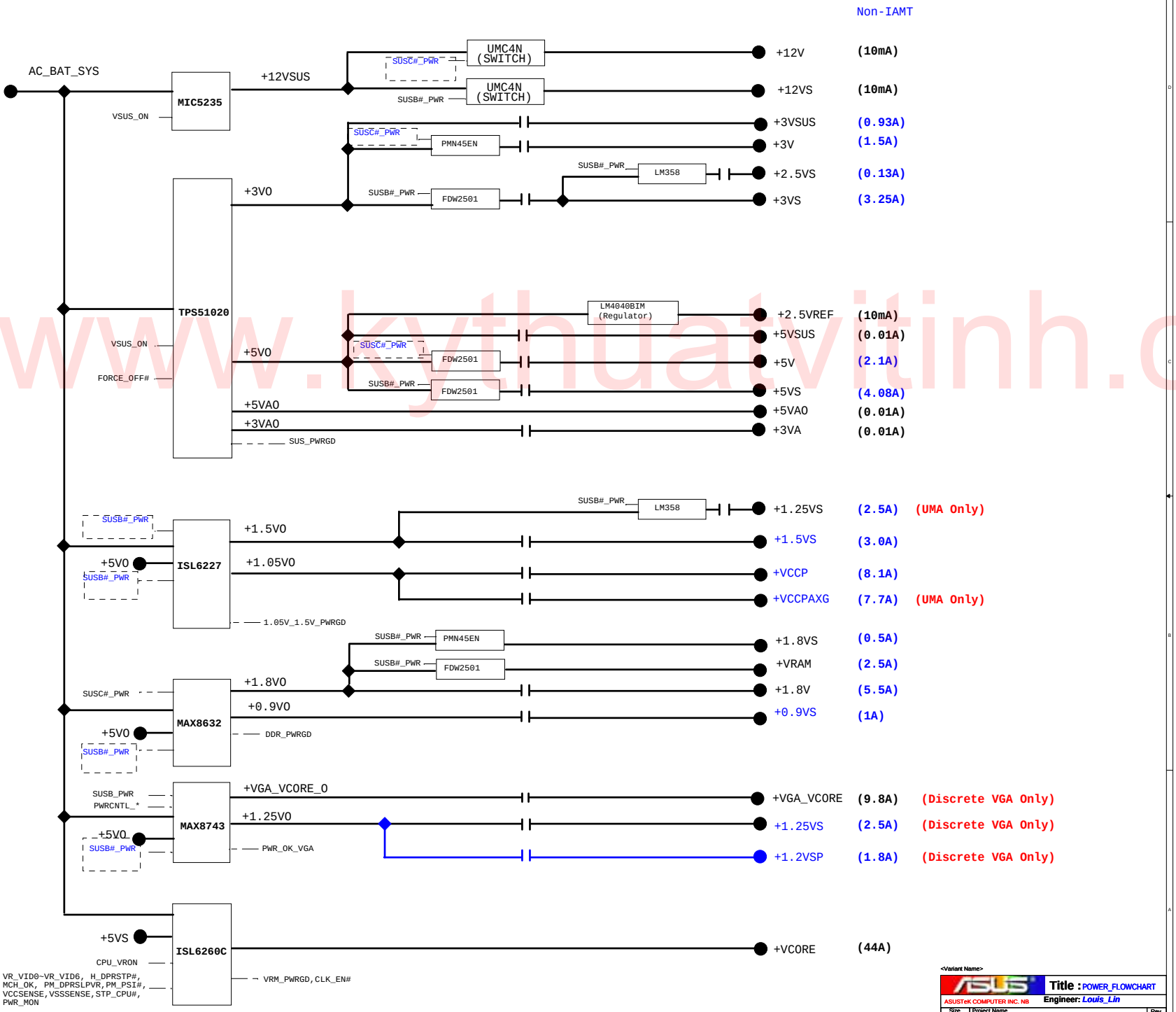

<Variant Name>

Title : POWER_FLOWCHART

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

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