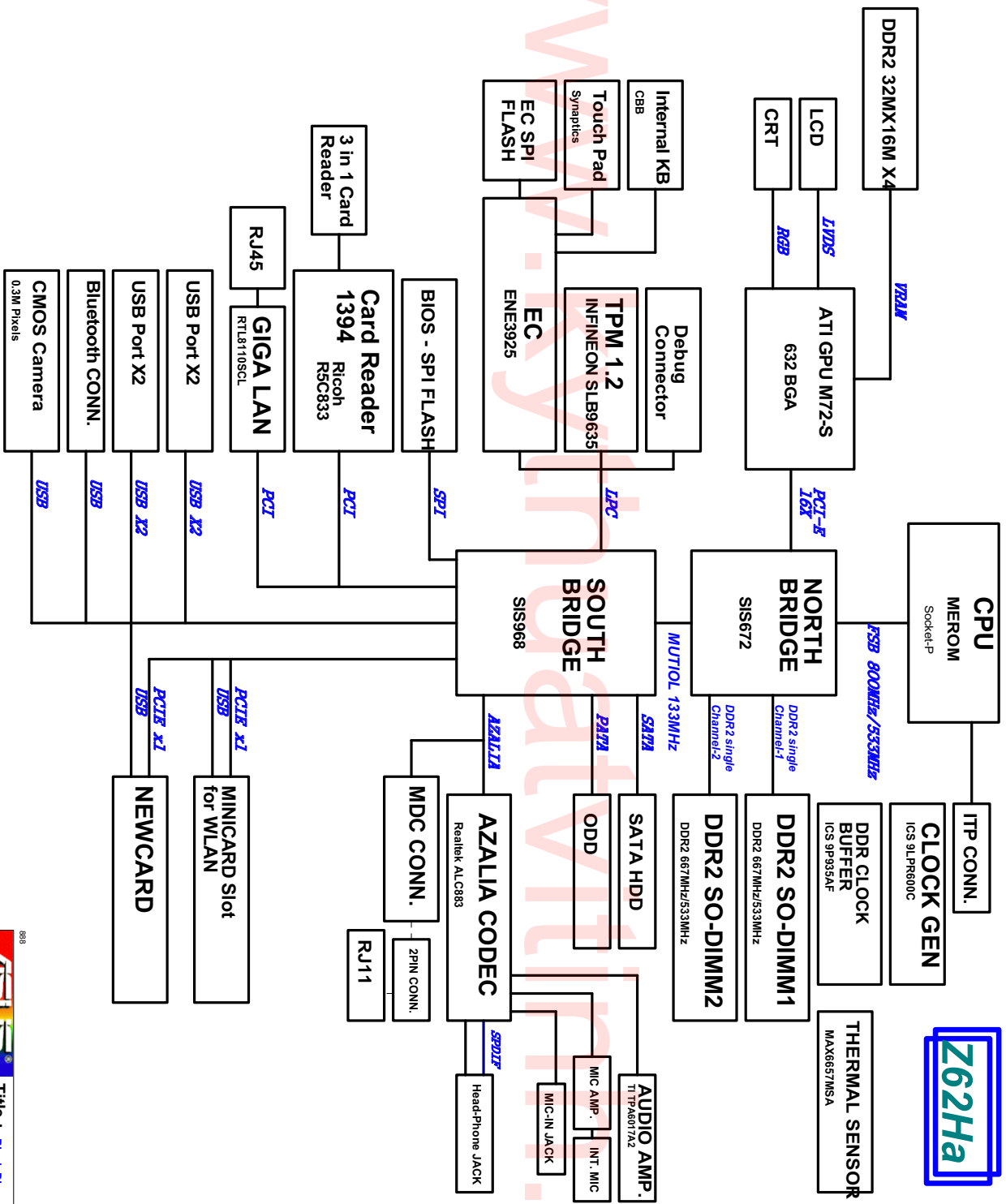


Z62Ha



ASUS
ASUSTek Computer, Inc.
Size: Custom
Title: Block Diagram
Engineer: Jack Hsu
Date: 2007.07.26

Rev	1.1
Ed	1
Bl	70

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PMW0/GPA0	BL_PWM1_DA	0
33	PMW1/GPA1	FAV_PWM1	0
36	PMW2/GPA2	CLK_PWMSAVE#	0
37	PMW3/GPA3	/	0
38	PMW4/GPA4	CHG_LED_UP#	0
39	PMW5/GPA5	PWR_LED_UP#	0
40	PMW6/GPA6	/	0
43	PMW7/GPA7	LCD_BACKOFF#	0
153	RXD/GPB0	NUM_LED	0
154	TXD/GPB1	CAP_LED	0
162	GPB2	SCRLL_LED	0
163	SMCLK0/GPB3	SMB0_CLK	0
164	SMDAT0/GPB4	SMB0_DAT	0
5	GA20/GPB5	A20GATE	0
6	KBRST#/GPB6	RC_JN#	0
165	GPB7	/	0
47	CLKOUT/GPC0	SMB1_CLK	0
169	SMCLK1/GPC1	SMB1_DAT	0
170	SMDAT1/GPC2	Mail_LED	0
171	GPC3	AC_OK#	0
172	TMR0/WUI0/GPC4	OP_SD#	0
175	GPC5	BAT_JN_OC#	0
176	TMR1/WUI1/GPC6	/	0
1	CK3CLKOUT/GC7	SUSC#	0
26	RTH/WUI0/GPD0	SUSB#	0
29	RTH/WUI1/GPD1	SUSC#	0
30	LPCRSTWUI4/GPD2	PLT_RST#	0
31	ECSCHW/GPD3	EXT_SC#	0
41	GRP4	/	0
42	GNT/GPD5	/	0
62	TACH0/GPD6	FAN0_TACH	0
63	TACH1/GPD7	/	0
87	ADCA/GPE0	EMAIL_SW#	0
88	ADCS/GPE1	INTERNET#	0
89	ADDC/GPE2	PWR4G_SW#	0
90	ADDC/GPE3	DISTP_SW#	0
2	PWRSW/GPE4	PWR_SW#	0
44	WUI5/GPE5	/	0
24	LPGRP0/WUI6/GPE6	LID_ECH	0
25	CLKRUN/WUI7/GPE7	/	0
110	PS2CLK0/GPF0	/	0
111	PS2DAT0/GPF1	/	0
114	PS2CLK1/GPF2	/	0
115	PS2DAT1/GPF3	/	0
116	PS2CLK2/GPF4	TP_CLK	0
117	PS2DAT2/GPF5	TP_DAT	0
118	PS2CLK3/GPF6	/	0
119	PS2DAT3/GPF7	/	0
113	FA16/GPG0	FA16	0
112	FA17/GPG1	FA17	0
104	FA18/GPG2	FA18	0
103	FA19/GPG3	/	0
3	FA20/GPG4	THRM_CPU#	0
4	FA21/GPG5	/	0
27	LPGR0HL/GPG6	PANTHERM#	0
28	LPGR0LL/GPG7	AC_APR_LCH	0

ICHT-M GPIO SETTING

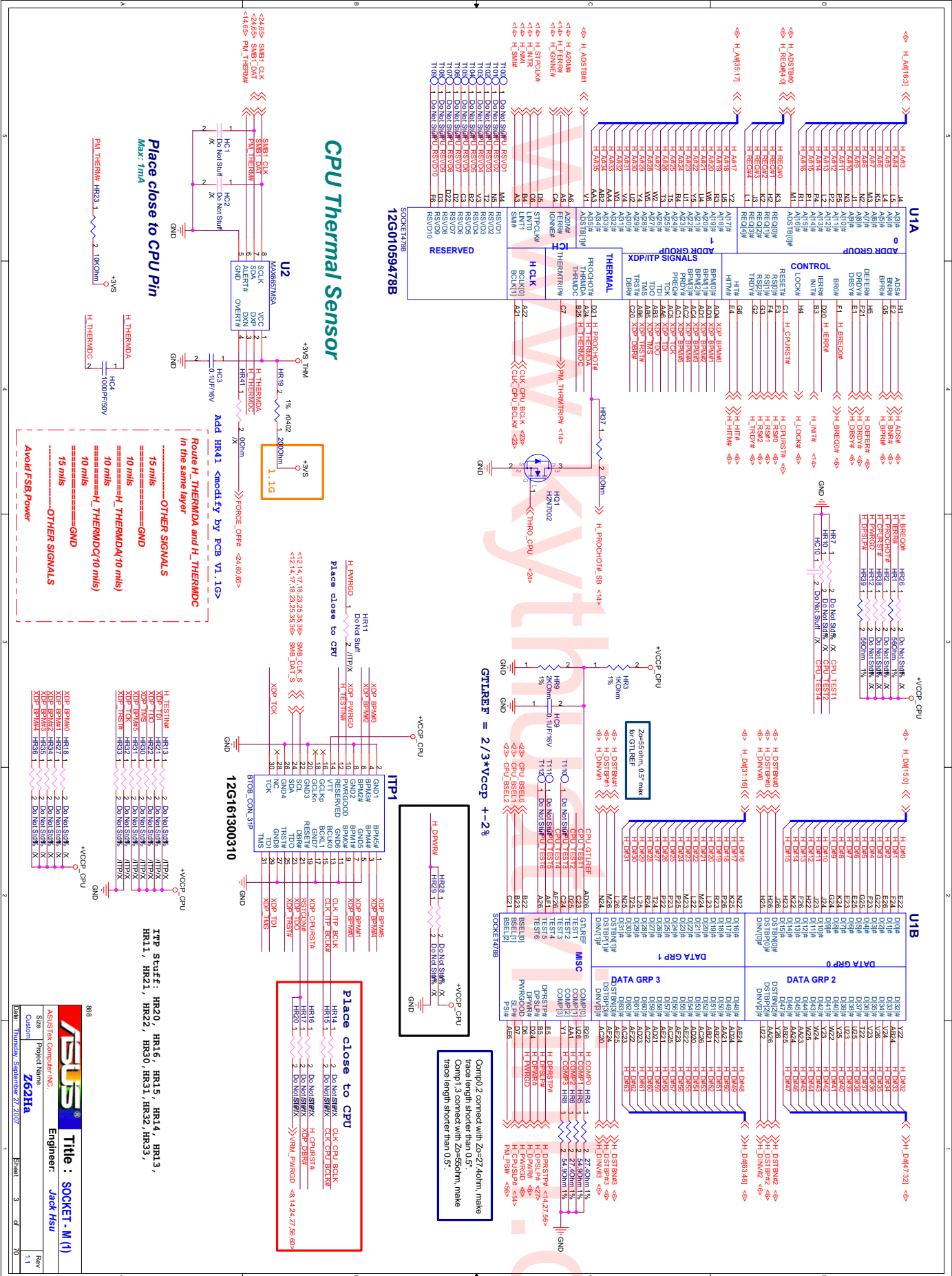
Pin	Pin Name	Signal Name	Type
48	GPH0	VUSUS_ON#	0
54	GPH1	VUSUS_GD#	0
55	GPH2	CPUPWR_GD#	0
69	GPH3	PM_PWM8BTM#	0
70	GPH4	SUSC_ON	0
75	GPH5	SUSB_ON	0
76	GPH6	CPUL_VRON	0
105	GPH7	PM_RSMRST#	0
148	GPH0	ICHT_PWMROK	0
149	GPH1	/	0
152	GPH2	MCHOK	0
155	GPH3	CHG_EN#	0
156	GPH4	PRECHG	0
168	GPH5	BAT_LL#	0
174	GPH6	BAT_LEARN	0

Pin	Pin Name	Signal Name	Type	Power Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I/O	Core(T0:3.3V)	GPI
C8	GPIO01/REQ#	PCL_REQ#	I/O	Core(T0:3.3V)	GPI
G8	GPIO02/PREQ#	PCL_INT#	I/O	Core(T0:3.3V)	GPI
F7	GPIO03/PREQ#	PCL_INT#	I/O	Core(T0:3.3V)	GPI
F8	GPIO04/PREQ#	PCL_INT#	I/O	Core(T0:3.3V)	GPI
G7	GPIO05/PREQ#	PCL_INT#	I/O	Core(T0:3.3V)	GPI
AC21	GPIO06	NC	I/O	Core(T0:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I/O	Core(T0:3.3V)	GPI
E21	GPIO08	EXTSM#	I/O	SUS(T0:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(T0:3.3V)	GPI
A20	GPIO10	WLAN_ON#	I/O	SUS(T0:3.3V)	GPI
B23	SMBALERT#/GPOT1	SMB_ALERT#	I/O	SUS(T0:3.3V)	Native
F19	GPIO12	KBC_SC#	I/O	SUS(T0:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(T0:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(T0:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(T0:3.3V)	GPI
AC22	GPIO16	PM_DRRSLPVR	I/O	Core(T0:3.3V)	Native
D8	GPIO17/GNT#	PCL_GNT#	I/O	Core(T0:3.3V)	GPO
AC20	GPIO18/STP_PCH#	STP_PCH#	0	Core(T0:3.3V)	GPO
AH18	GPIO19/SATA1G#	NC	0	Core(T0:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	0	Core(T0:3.3V)	GPO
AE19	GPIO21/SA1A0G#	NC	I/O	Core(T0:3.3V)	GPI
A13	GPIO22/REQ#	PCL_REQ#4	I/O	Core(T0:3.3V)	Native
AA5	LDRQ1#/GPRO23	TP	I/O	Core(T0:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(T0:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(T0:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(T0:3.3V)	GPO
B21	GPIO27/EL_STATED	PD_DET#	I/O	SUS(T0:3.3V)	GPO
E23	GPIO28/EL_STATED1	NC	I/O	SUS(T0:3.3V)	GPO
C3	GPIO29/OC#	USB_OC#5	I/O	SUS(T0:3.3V)	Native
A2	GPIO30/OC#	NEWCARD_OCH	I/O	SUS(T0:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(T0:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	0	Core(T0:3.3V)	GPO
AC19	GPIO33/A2_DOCK_RST#	BT_ON#	0	Core(T0:3.3V)	GPO
U2	GPIO34/A2_DOCK_RST#	NC	I/O	Core(T0:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(T0:3.3V)	GPO
AH19	GPIO36/SA1A2G#	NC	I/O	Core(T0:3.3V)	GPI
AE19	GPIO37/SA1A3G#	PCB_ID0	I/O	Core(T0:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I/O	Core(T0:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I/O	Core(T0:3.3V)	GPI
A14	GNT4#/GPIO48	PCL_GNT#4	I/O	Core(T0:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWMRGD	I/O	V_CPU_IO	Native

PIC Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD22	0	INTB-->INTB
LAN	AD24	REQ#2/GNT#2	INTA-->INTA INTA-->INTC

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

ASUSTek Computer, Inc.
ASUS
 Title : System Setting
 Engineer: Jack Hsu
 Size: 11x11
 Date: 2007.07.20



CPU Thermal Sensor

Place close to CPU Pin
Max. 7mA

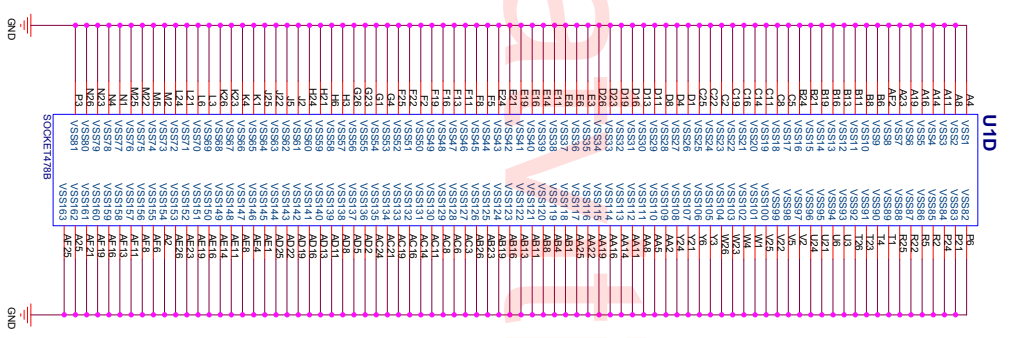
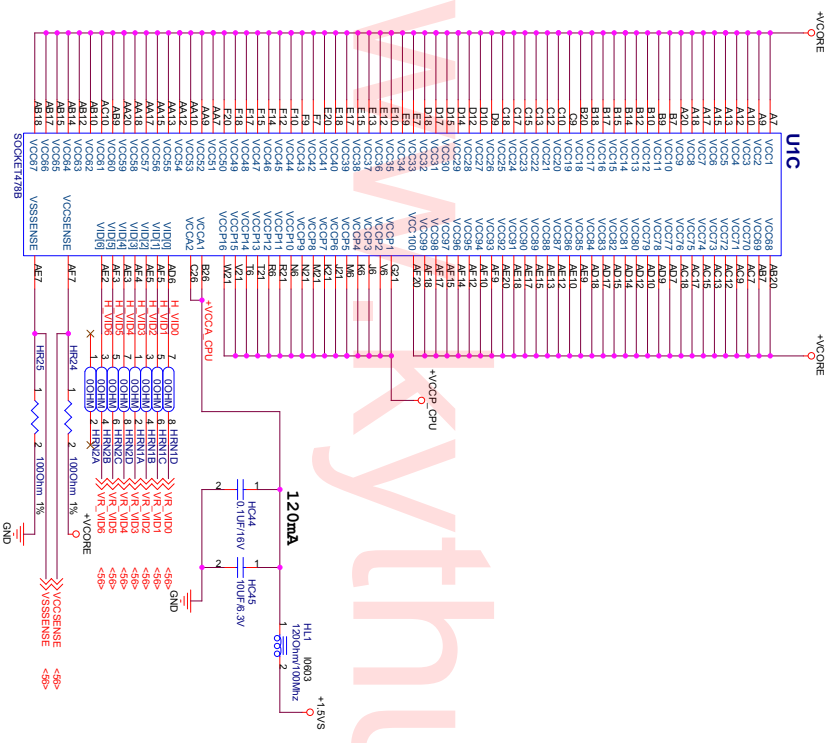
Add HR14 <modify by PCB V1.1G>
Route H_THERM0A and H_THERM1C
in the same layer

- OTHER SIGNALS
- 15 mils
- 10 mils
- 10 mils
- 10 mils
- 10 mils
- 15 mils
- OTHER SIGNALS
- Avoid FSb Power

Place close to CPU

Comp'd 2 connect with Zo=27.4ohm, make trace length shorter than 0.5"
Comp 1,3 connect with Zo=55ohm, make trace length shorter than 0.5"

ASUS		Title : SOCKET_M (1)	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62Ha	1.1	
Date: Thursday, September 27, 2007	Sheet	3	70



898

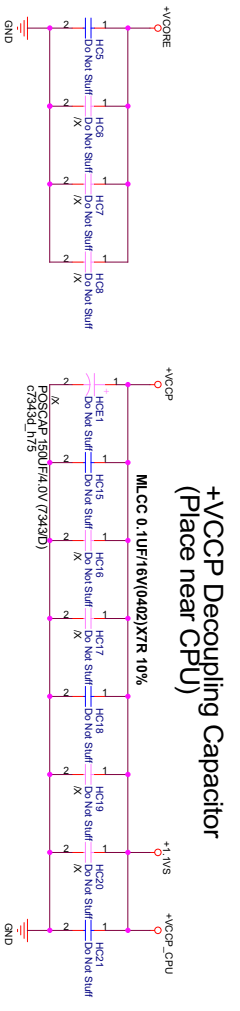
Title : SOCKET - M(2)

ASUSTek Computer INC. **Engineer: Jack Hsu**

Size: Project Name: **Custom Z62Ha**

Rev: 1.1

DATE: Thursday, September 27, 2007 Sheet: 4 of 70



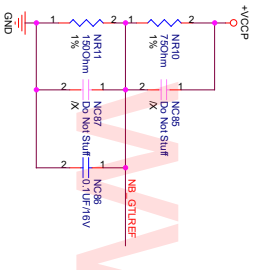
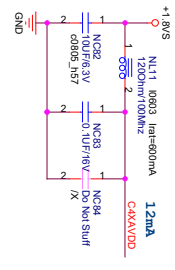
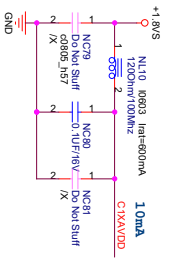
**Decoupling guide from INTEL
44A for Merom**

VCCORE 22uF/10V * 32pcs, 330uF/2V * 6pcs
 VCCP 0.1uF * 6pcs, 150uF * 1pcs

**+VCCP Decoupling Capacitor
(Place near CPU)**

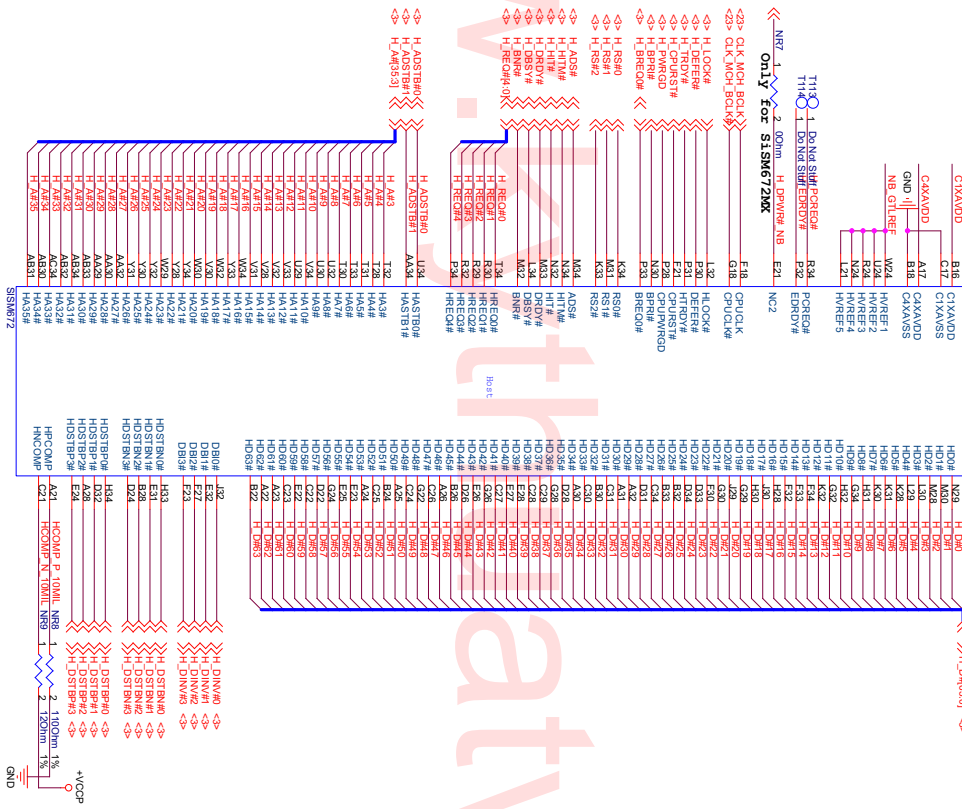
888

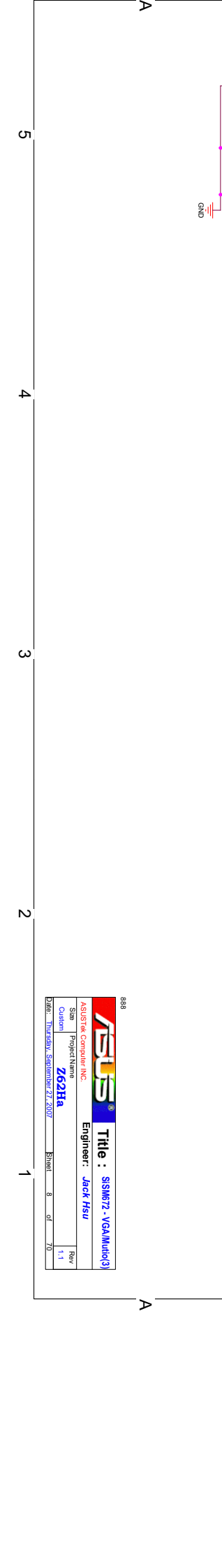
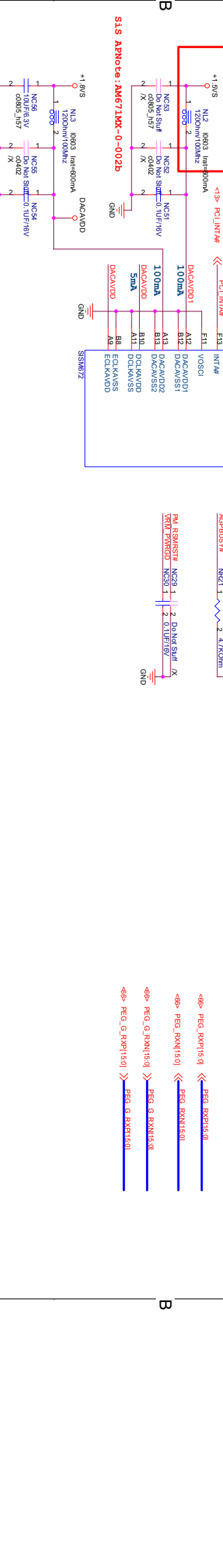
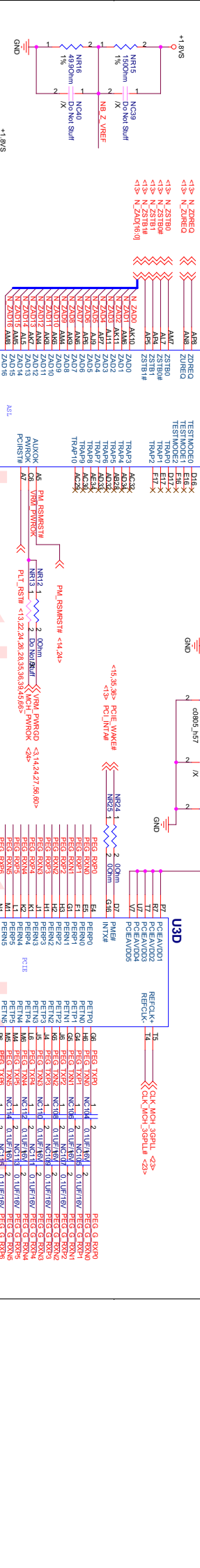
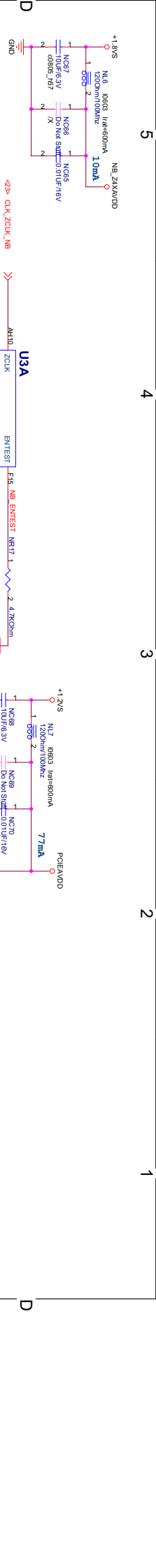
		Title : CPU CAP	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62HA		1.1
Date: Thursday, September 27, 2007	Sheet	5	of 70



Place 0.1uF under M672 solder side,
less 100mls from M672 pin

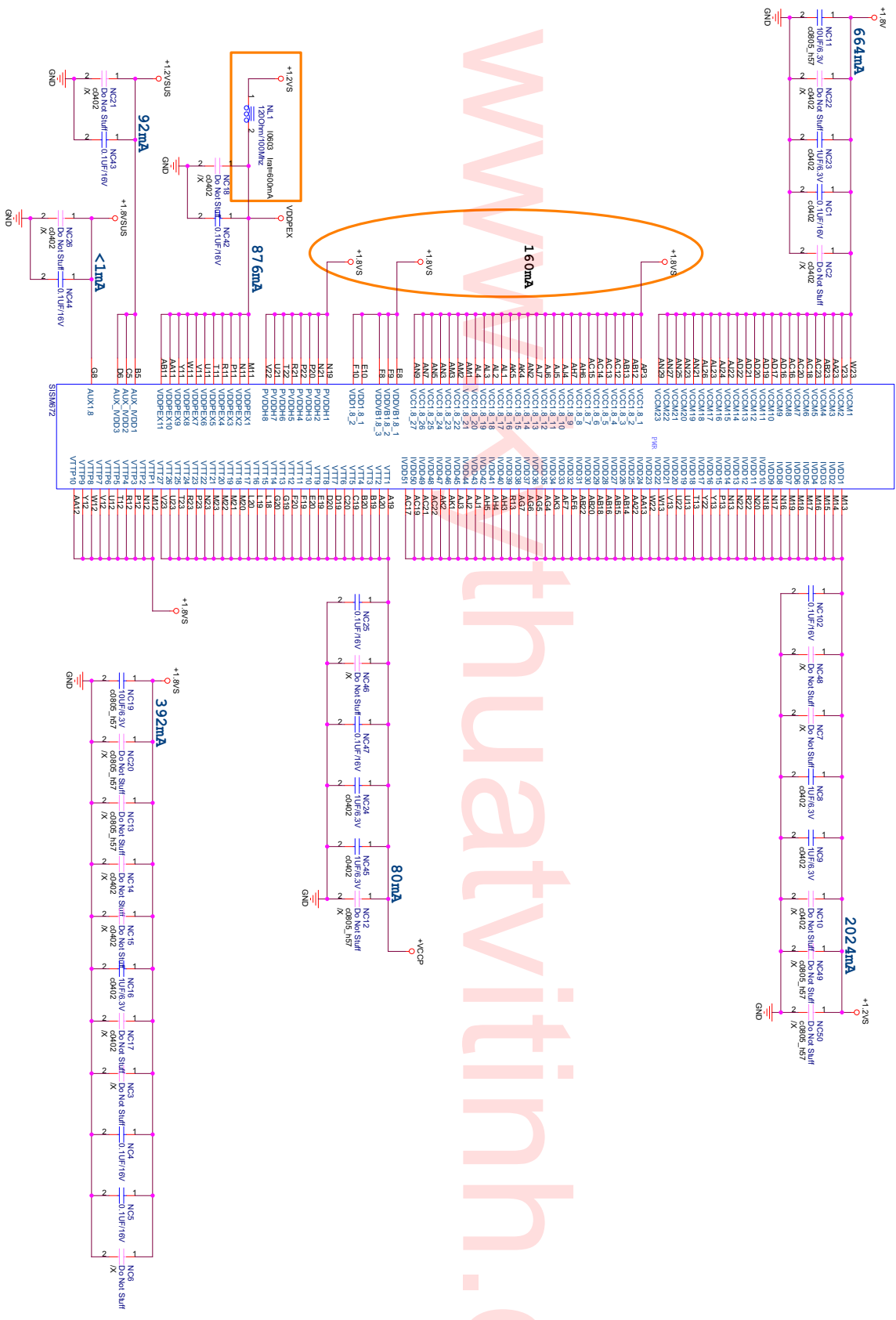
U3C





5 4 3 2 1

888
ASUSTek Computer Inc.
 Title : SISM672_VGAM(udc3)
 Project Name :
 Engineer : Jack Hsu
 Date : Thursday, September 27, 2007
 Sheet : 8 of 70



ASUS®

ASUSTek Computer INC.

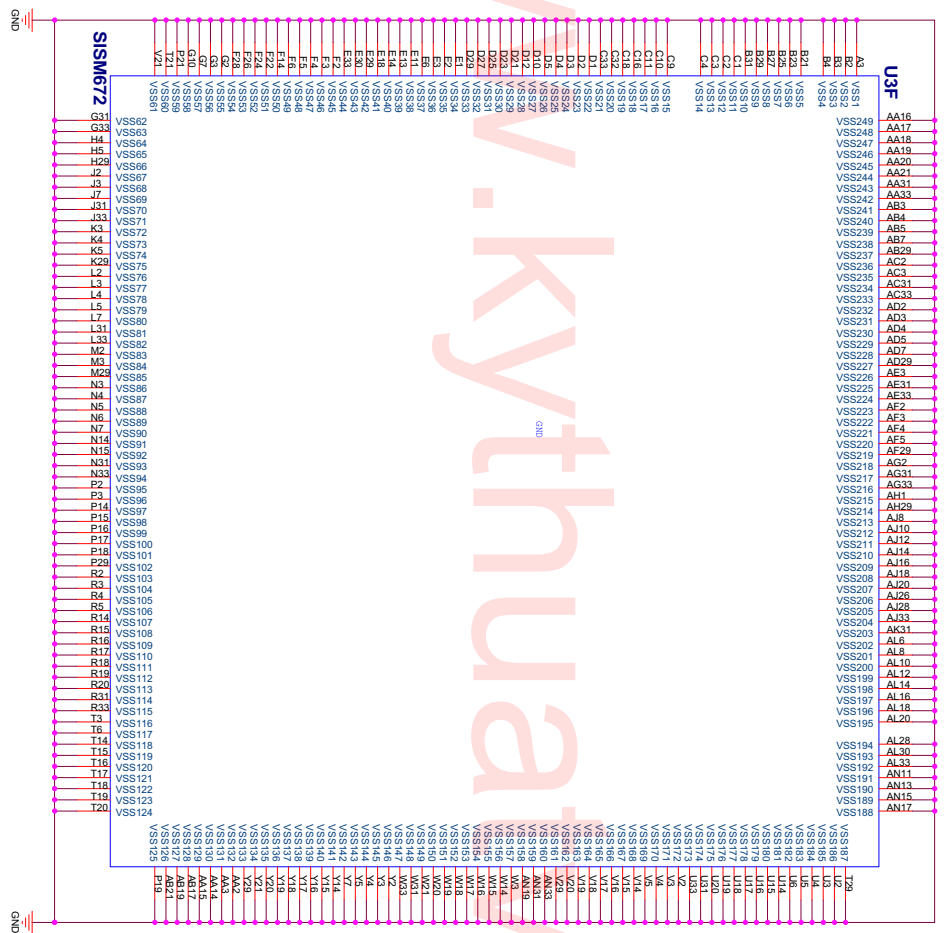
Project Name: Z62HA

Title: SISW672 - POWER(4)

Engineer: Jack Hsu

Rev: 1.1

Date: Thursday, September 27, 2007




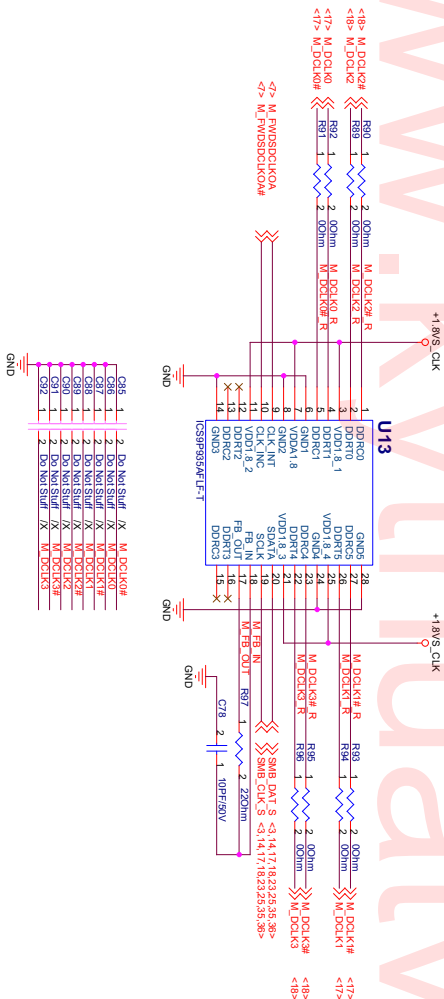
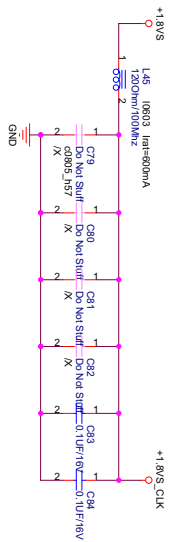
888

ASUS		Title : SISM672 - GND(6)	
ASUSTek Computer INC.		Project Name	
Custom		Z62Ha	
Date : Thursday, September 27, 2007		Sheet 10 of 70	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size		Rev	
Custom		1.1	

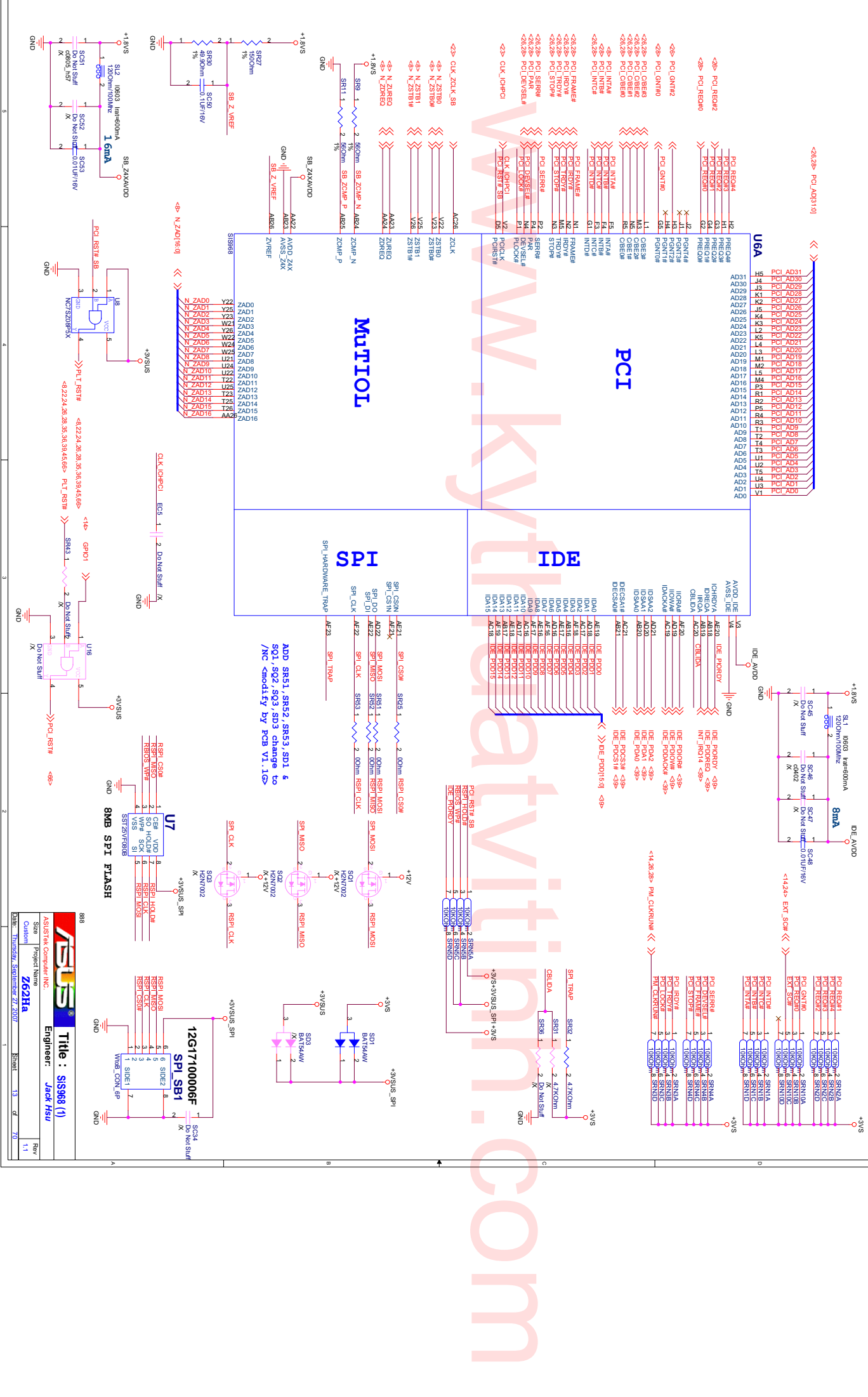
www.kythuatvitinh.com

888

		Title : BLANK	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62Ha		1.1
Date: Thursday, September 27, 2007	Sheet	11	of 20



WWW.KYU-KEY.COM



ASUS Logo

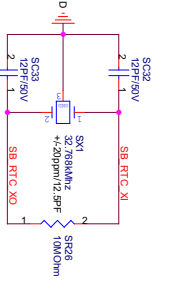
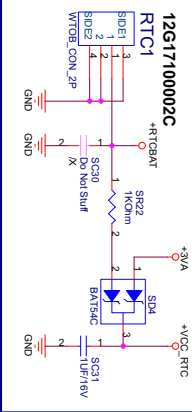
Title : SIS968 (1)

ASUSTek Computer INC. Engineer: Jack Hsu

Size: Project Name: Custom Z62Ha

Date: Thursday, September 27, 2007 Sheet: 13 of 70

RTC BATTERY



Place on the Door Area



U6B

CPU_S

APIC

LPC

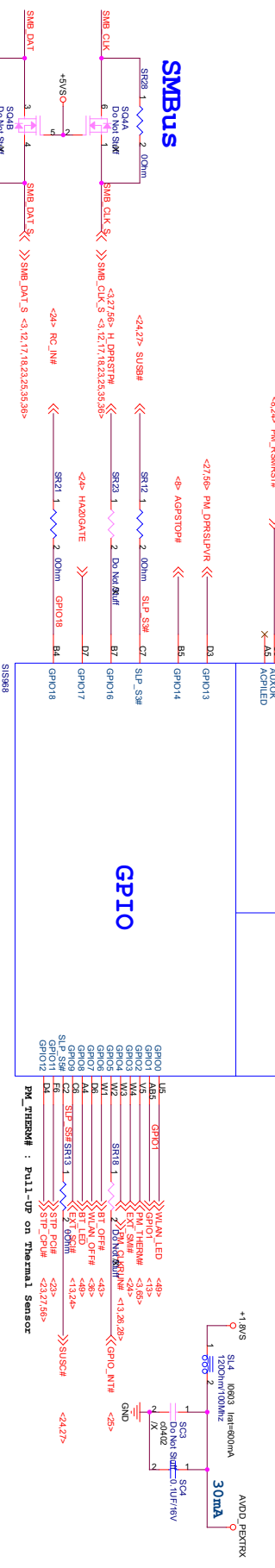
RTC

SMBUS

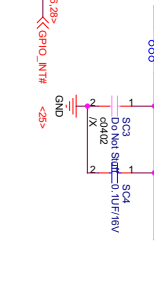
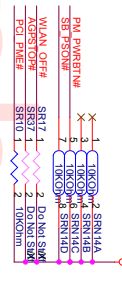
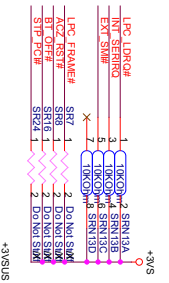
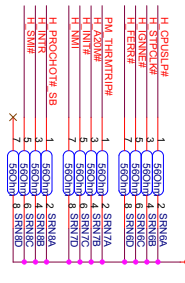
HD Audio

ACPI/Others

GPIO

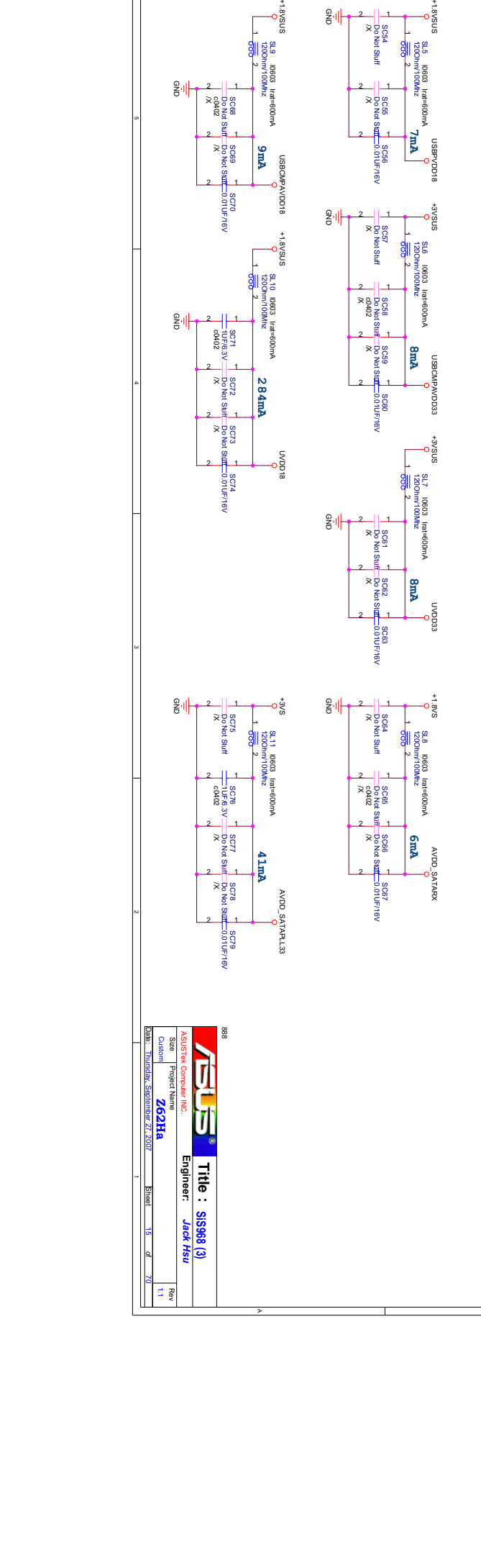
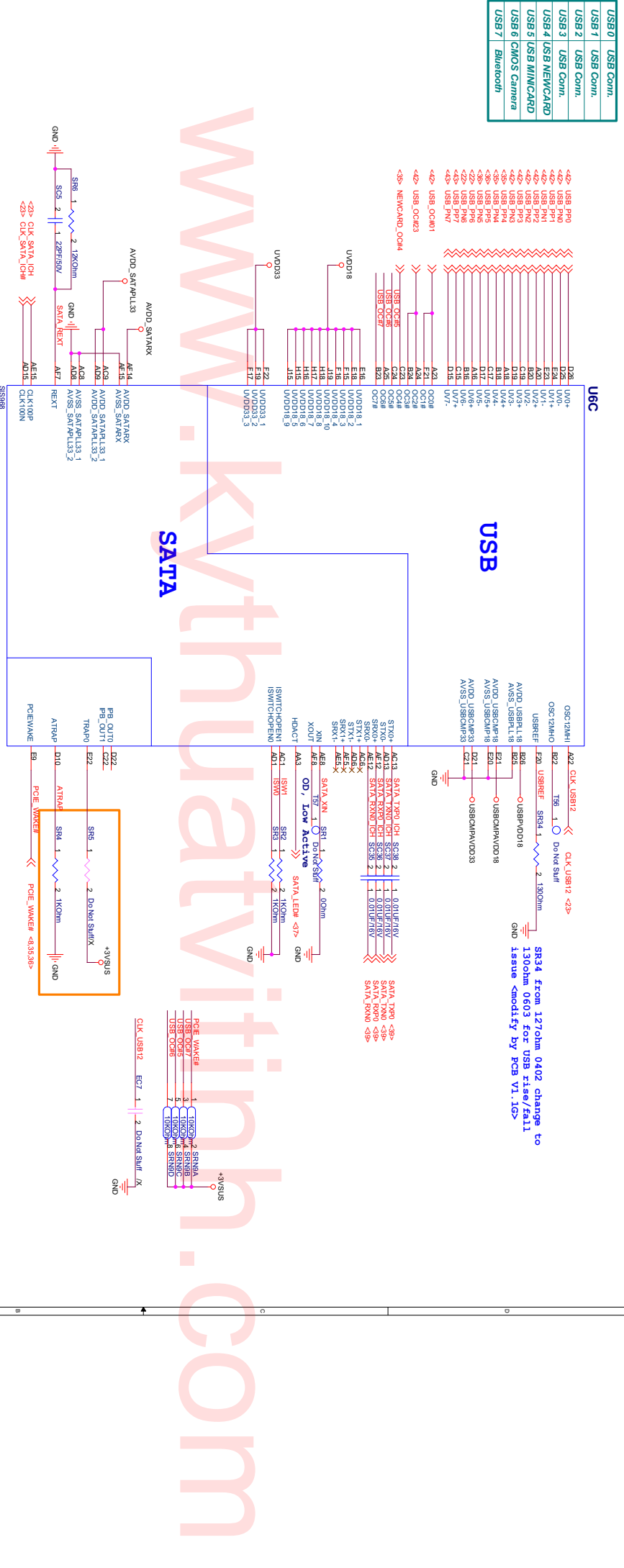


1.8V5US



ASUS		Title : SIS968 (1)	
ASUSTek Computer INC.	Project Name	Engineer: Jack Hsu	Rev
Custom	Z62Ha		1.1
Date: Thursday, September 27, 2007	Sheet	14	70

USB 0	USB Comm.
USB 1	USB Comm.
USB 2	USB Comm.
USB 3	USB Comm.
USB 4	USB NEWCARD
USB 5	USB MINICARD
USB 6	CMOS Camera
USB 7	Bluetooth



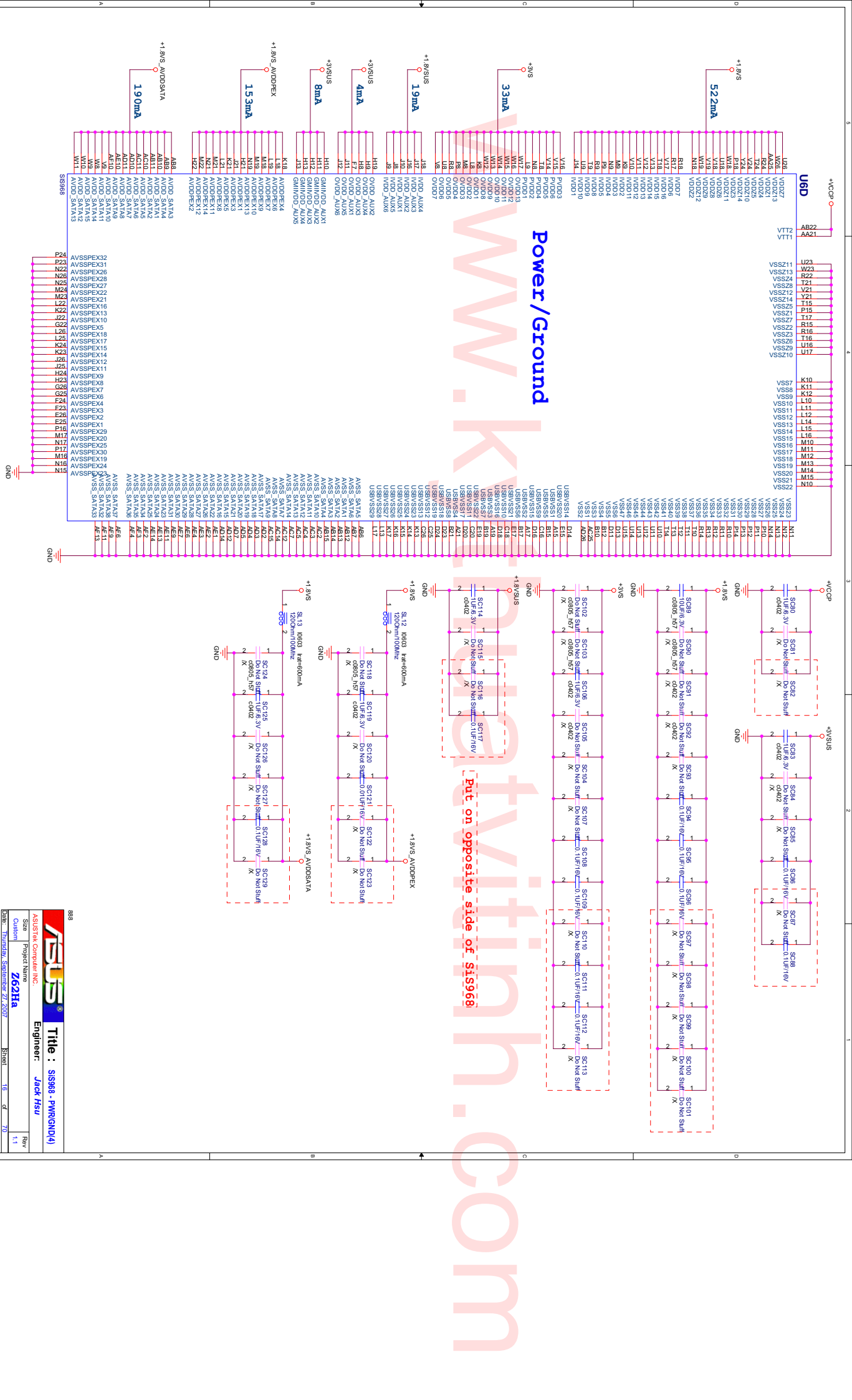
888

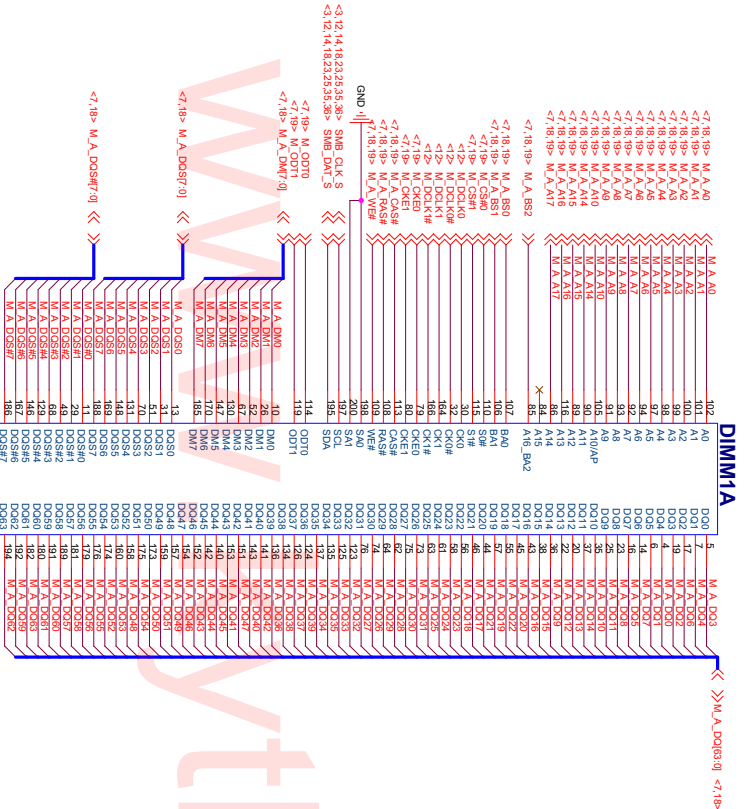
Title : SIS988 (3)

ASUSTek Computer INC. **Engineer: Jack Hsu**

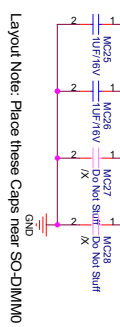
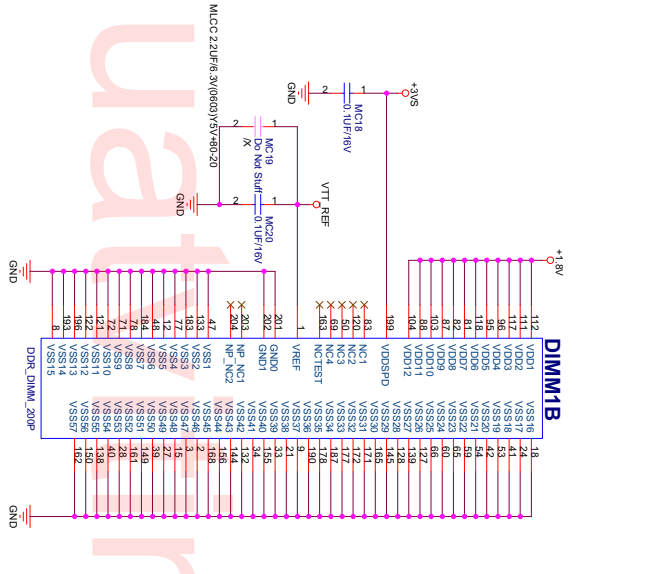
Size: Project Name: Custom **Z62Ha**

Date: Thursday, September 27, 2007 Sheet: 15 of 70





H=9.2mm Standard Type, 12G025C22000
Channel A, DIMM 0



Layout Note: Place these Caps near SO-DIMM0

888

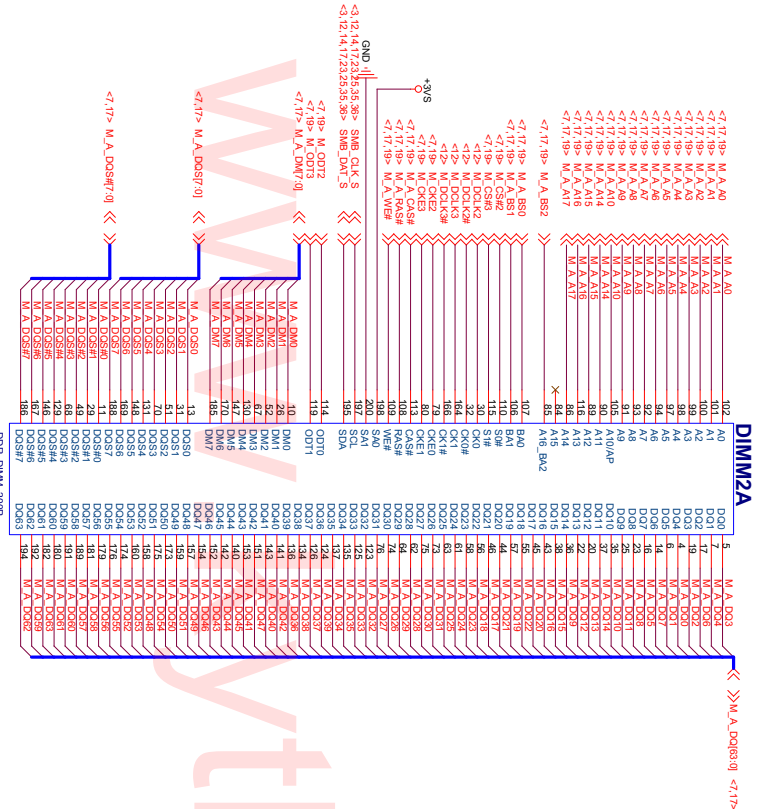
Title : DDR SO-DIMM0

ASUSTek Computer INC. **Engineer: Jack Hsu**

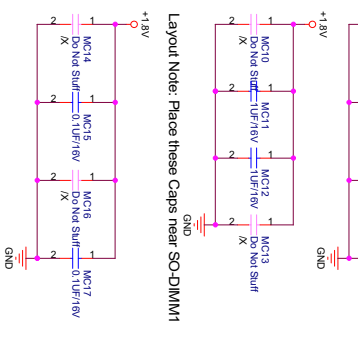
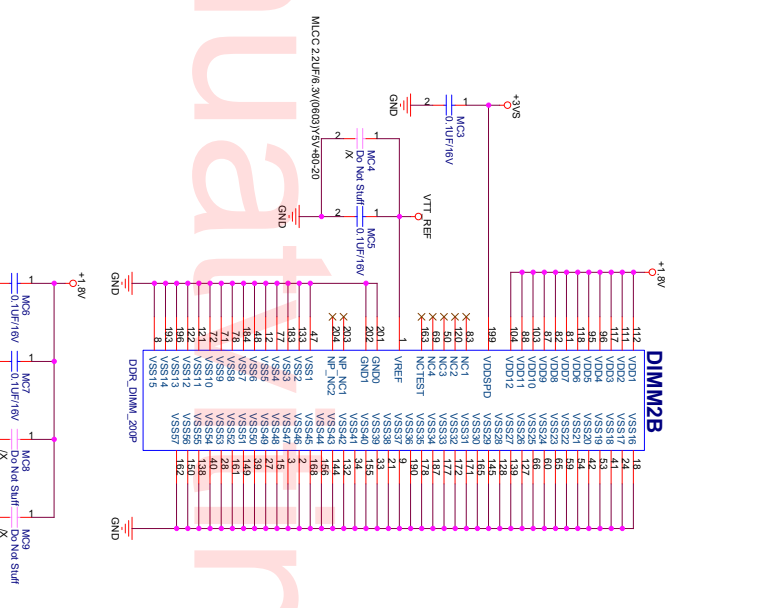
Size: Project Name: **Z62Ha**

Custom: 1.1

Date: Thursday, September 27, 2007 Sheet: 17 of 70



H=5.2mm Standard Type, 12G025122007
Channel A, DIMM 1



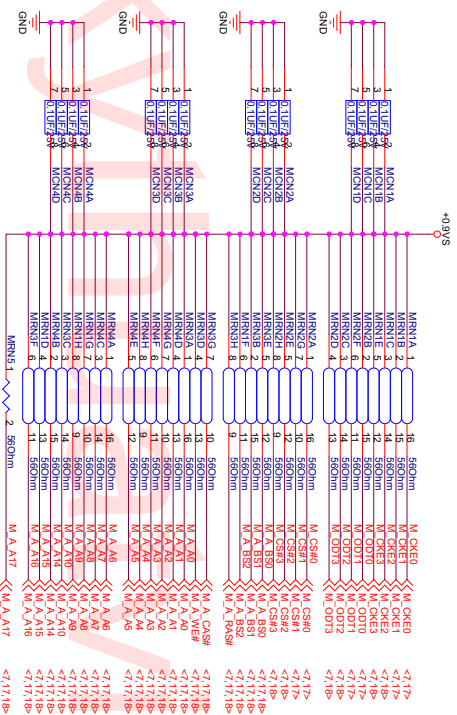
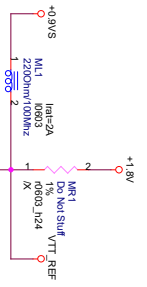
Layout Note: Place these High-Freq decoupling Caps near the GMCH

ASUSTeK Computer INC. **Title : DDR SO-DIMM1**

Project Name: **Z62Ha** Engineer: **Jack Hsu**

Size: Custom Rev: 1.1

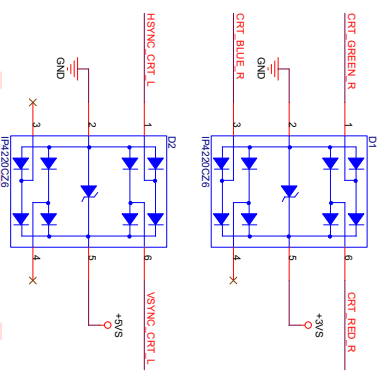
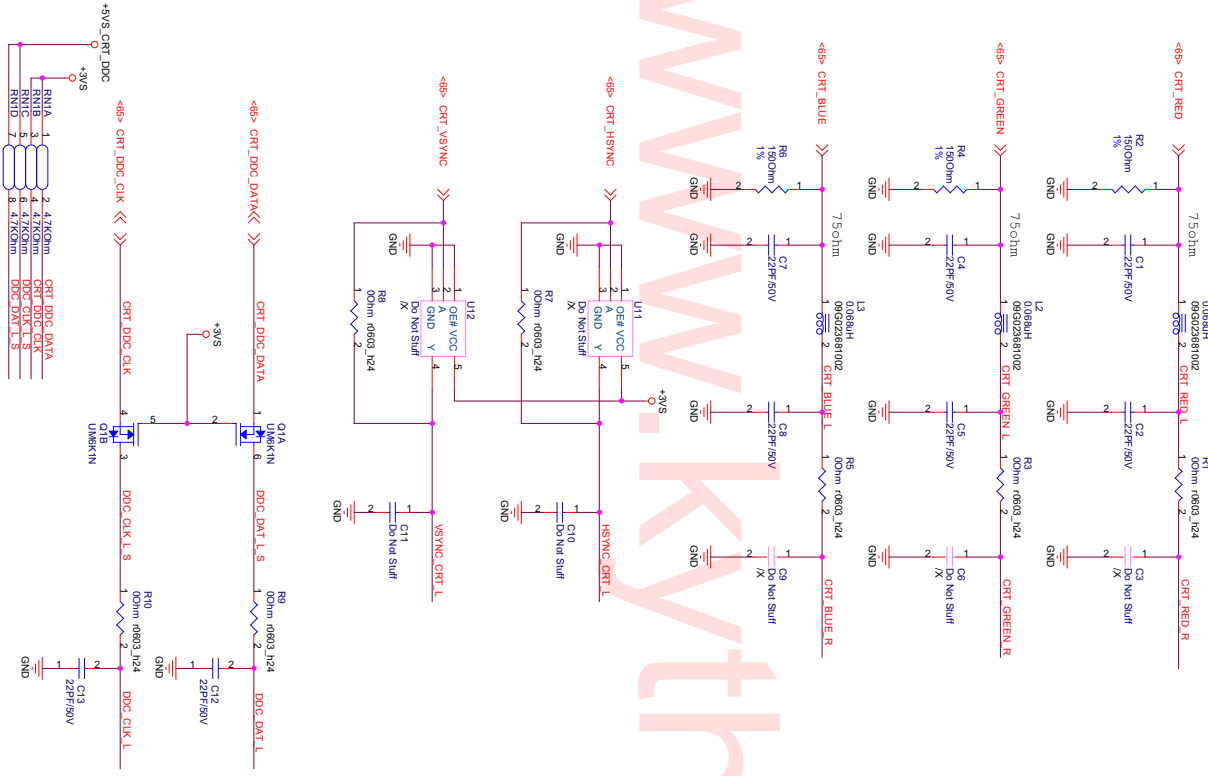
Date: Thursday, September 27, 2007 Sheet: 18 of 70



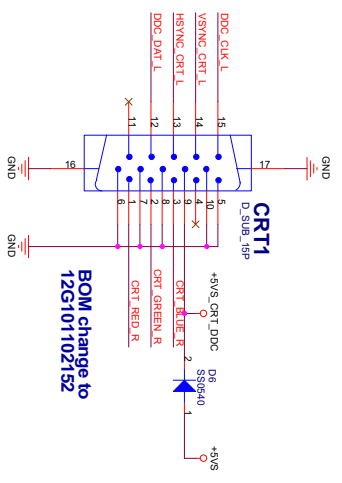
DDR2 : Command, Control signal need termination

Layout note: Place one cap close to every 2 pull-up resistors terminated to +0.9V

I1 I2 I3 from 27nH change to 0.068uH for VGA
measure <modify by PCB VI.1G>



Place ESD Diodes near CRT Connector

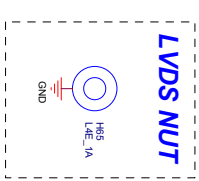
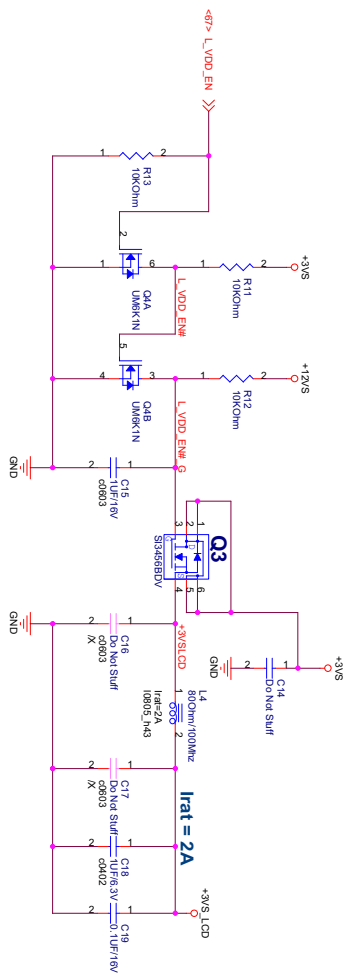


BOM change to 12G101102152

CRT Connector

888	
ASUS	
Title : CRT Connector	
ASUSTek Computer INC. Engineer: Jack Hsu	
Size	Project Name
Custom	Z62Ha
Date: Thursday, September 27, 2007	Sheet 20 of 70

LCD Power Switch

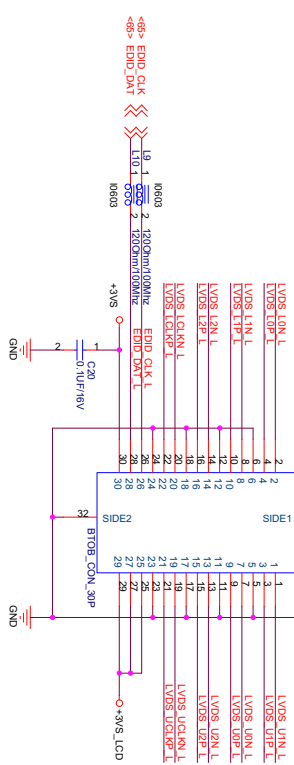


C14, C20 for EXT. solution
 modify by PCB VI.1G

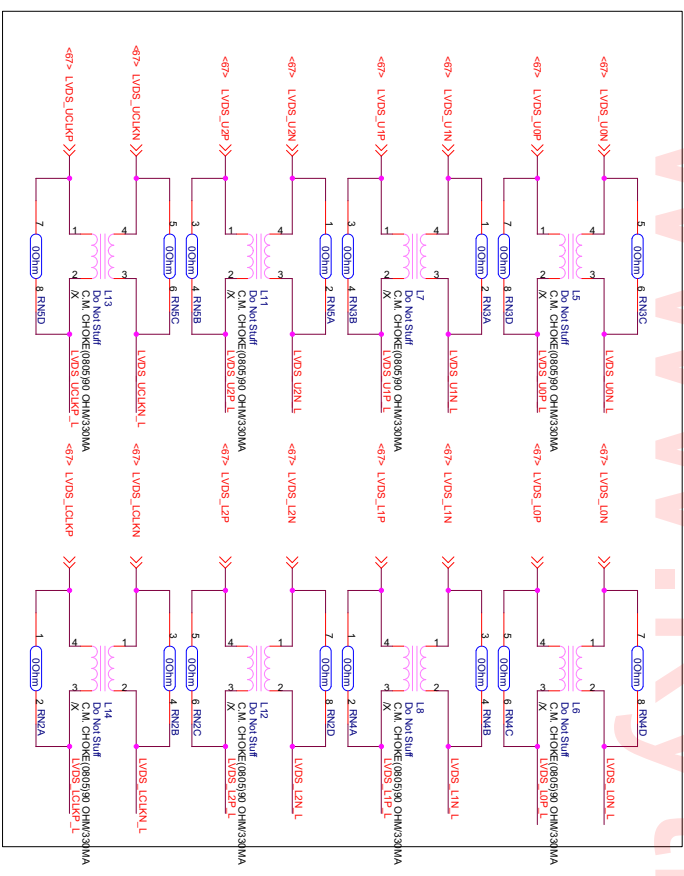
LVDS Connector

12G17001030B

LVDS1



Cable Requirement:
 Impedance: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"



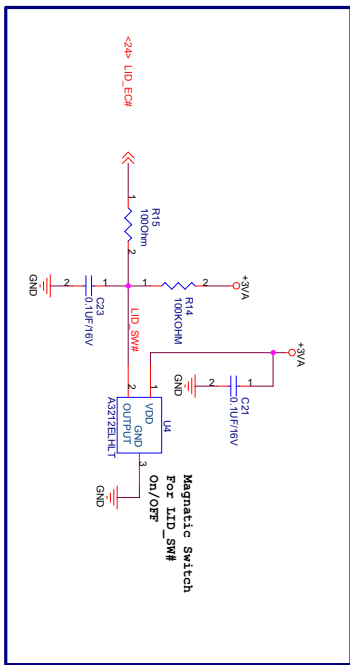
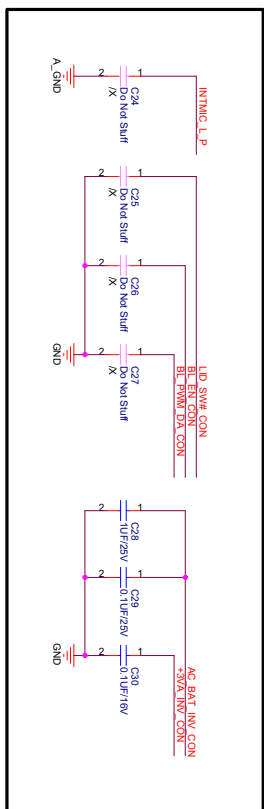
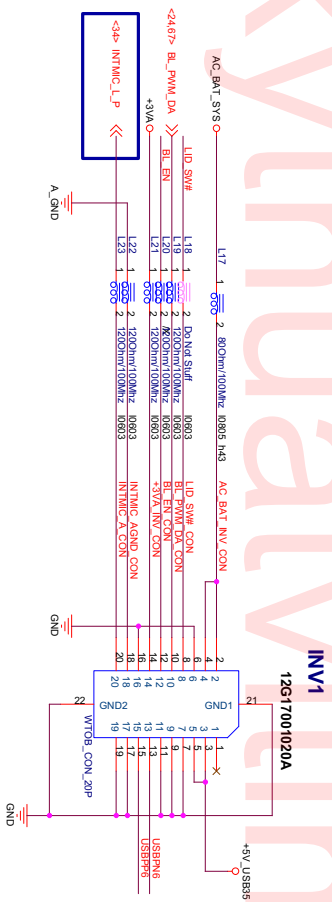
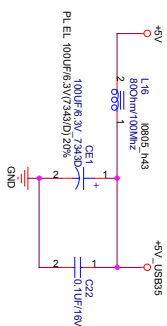
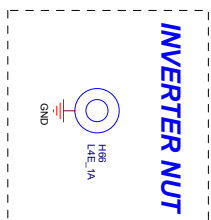
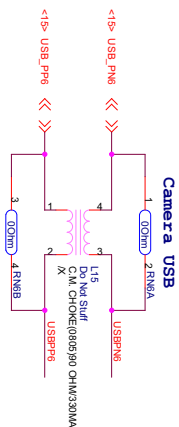
ASUSTek Computer INC.
ASUS
 Project Name: **Z62Ha**
 Engineer: **Jack Hsu**
 Title: **LVDS Connector**
 Size: Custom
 Date: Thursday, September 27, 2007
 Sheet: 21 of 70

INVERTER Interface

BIOS ICD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS BACK_ADJ: KBC output PWM signal (adjust pulse width) to adjust Back Light.

Inverter Board built in 14.1W LCD Panel

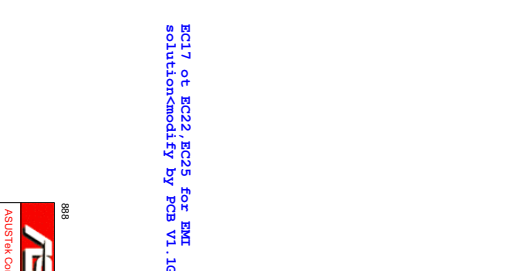
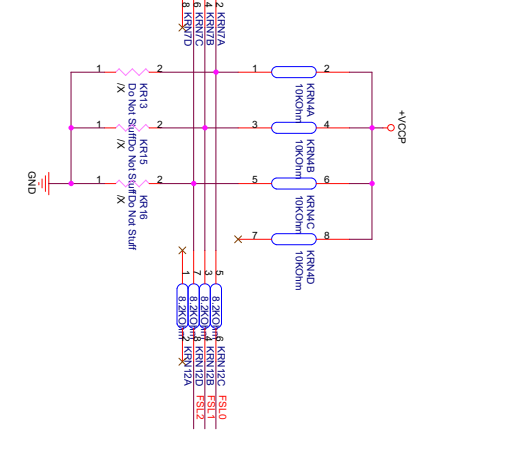
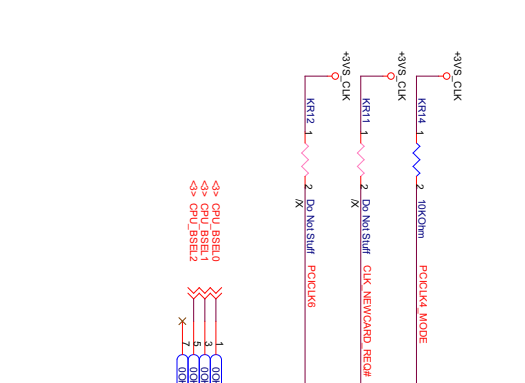
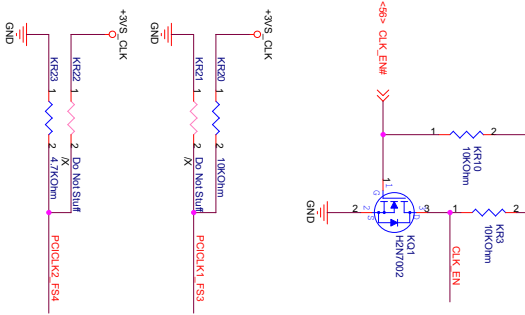
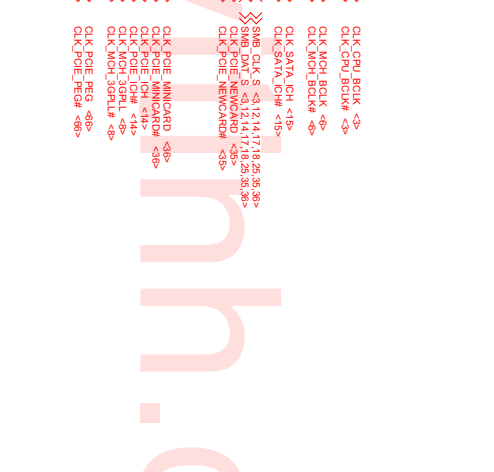
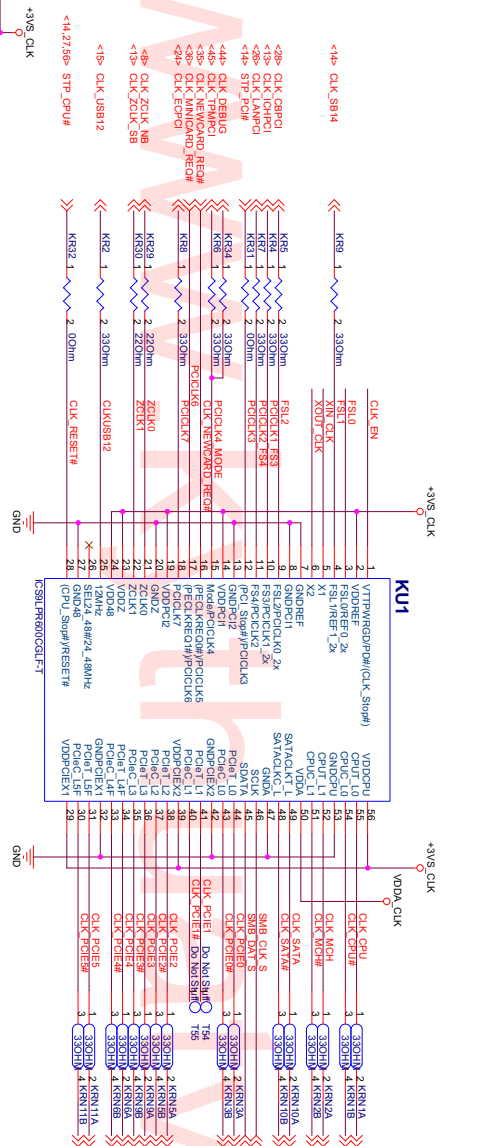
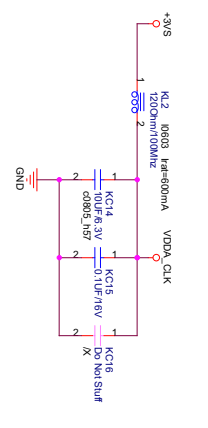
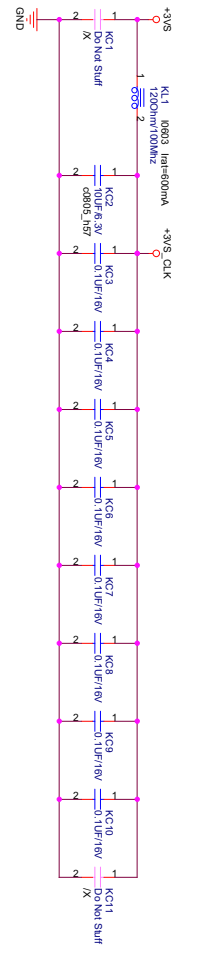
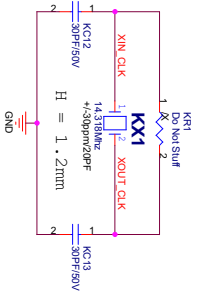


888

Title : Inverter

ASUSTek Computer INC.
 Project Name: **Z62Ha**
 Engineer: **Jack Hsu**

Size: Custom
 Date: Thursday, September 27, 2007
 Sheet: 22 of 70



CLK trapped by CPU's BSEL

BSEL#	BSEL1	BSEL0	CLK#
0	0	1	CLK_CPU
0	1	0	CLK_MOCH
0	1	1	CLK_PCIE
1	0	0	CLK_CPU
1	0	1	CLK_MOCH
1	1	0	CLK_PCIE

EC17	EC22	EC25	CLK#
0	0	0	CLK_CPU
0	0	1	CLK_MOCH
0	1	0	CLK_PCIE
1	0	0	CLK_CPU
1	0	1	CLK_MOCH
1	1	0	CLK_PCIE

EC17 at EC22, EC25 for EN1 solution<modify by PCB V1.1G>

888

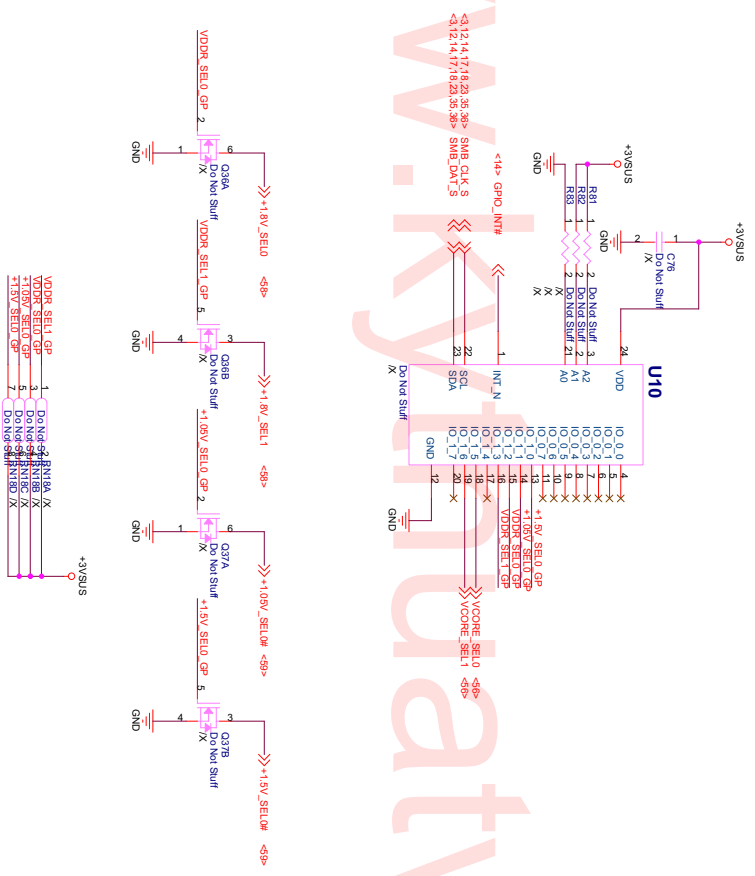
Title : ICS9LPR600

ASUSTek Computer INC. **Engineer: Jack Hsu**

Size Project Name **Custom Z62HA**

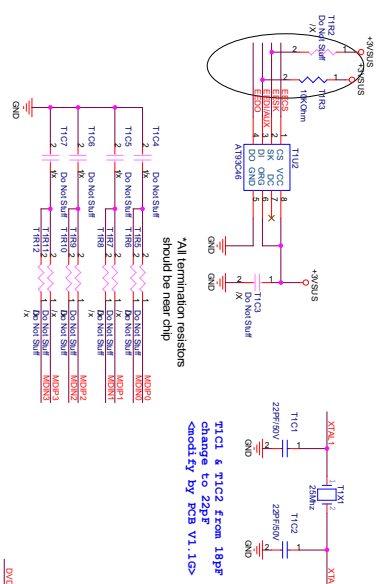
Date: Thursday, September 27, 2007 Sheet 23 of 70 Rev 1.1

www.kyauatvitinh.com



888

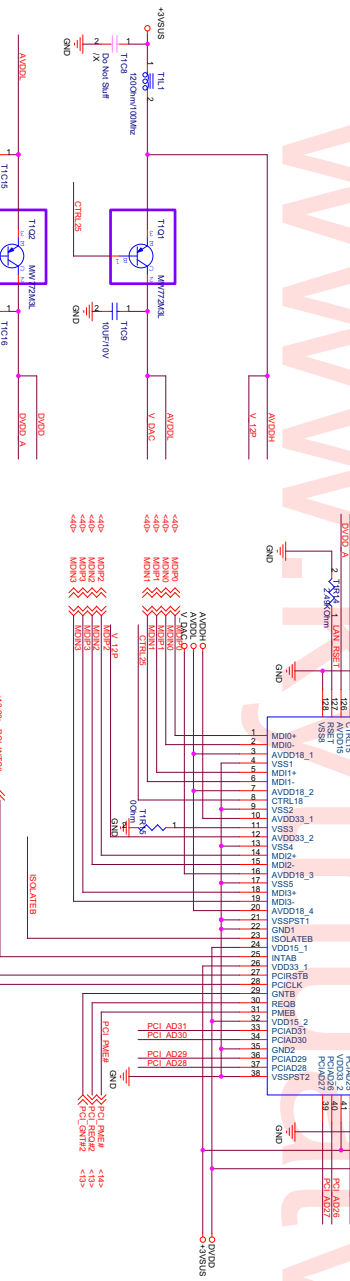
ASUS		Title : GPIO EXP.
ASUSTEK COMPUTER INC.		Engineer: Jack Hsu
Size: Custom	Project Name: Z62HA	Rev: 1.1
Date: Thursday, September 27, 2017	Sheet: 25	of 70



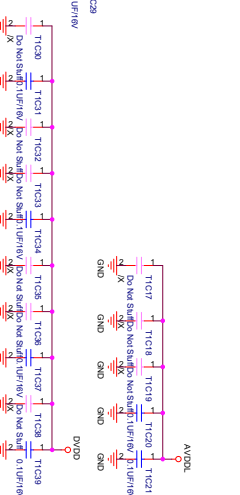
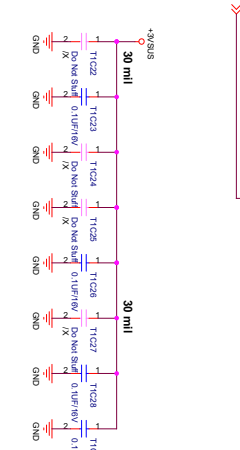
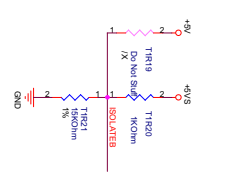
All termination resistors should be near chip

TI C1 & TI C2 from 18pf change to 22pf for RCB V1.10 >

10/100 => 5.6K, 1% resistor
QLAN => 249K, 1% resistor



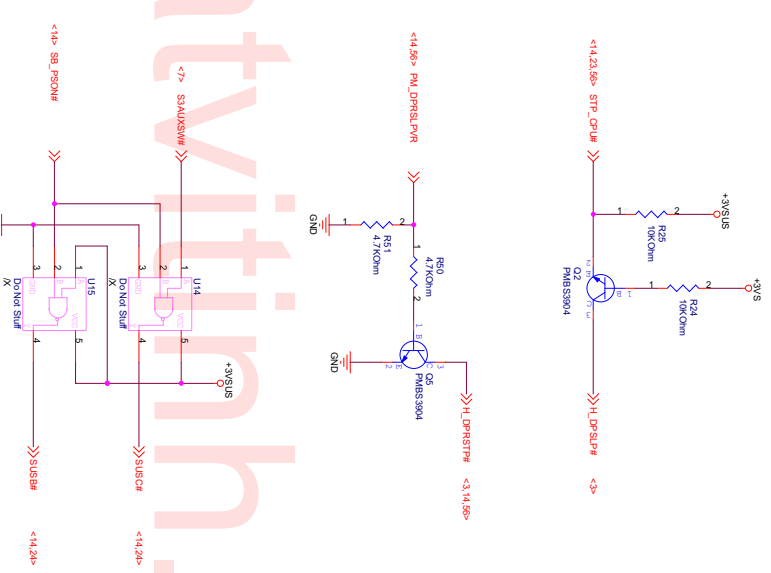
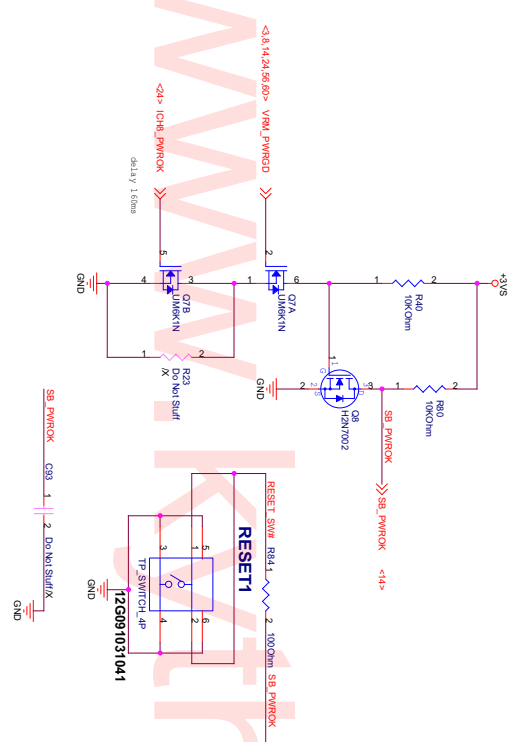
HSBC Quality Issues, change part.



AVDDH	2.5AVDD	2.5AVDD	2.5AVDD	2.5AVDD
V12P	3.3AVDD	3.3AVDD	3.3AVDD	3.3AVDD
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	2.5AVDD
V_DAC	2.5VDD	1.8VDD	1.2VDD	2.5AVDD
DVDD	2.5VDD	1.8VDD	1.2VDD	2.5AVDD
DVDD_A	N/A	1.8AVDD	1.2AVDD	2.5AVDD

PIN 24/32/5/54/64 / 7/8/9/11/10/11/6
PIN 126

ASUS
ASUSTek Computer Inc.
Project Name: Z62HA
Engineer: Jack Hsu
Title: LAN Marvell 88E8066
Rev: 1.1
Date: 2011.02.23



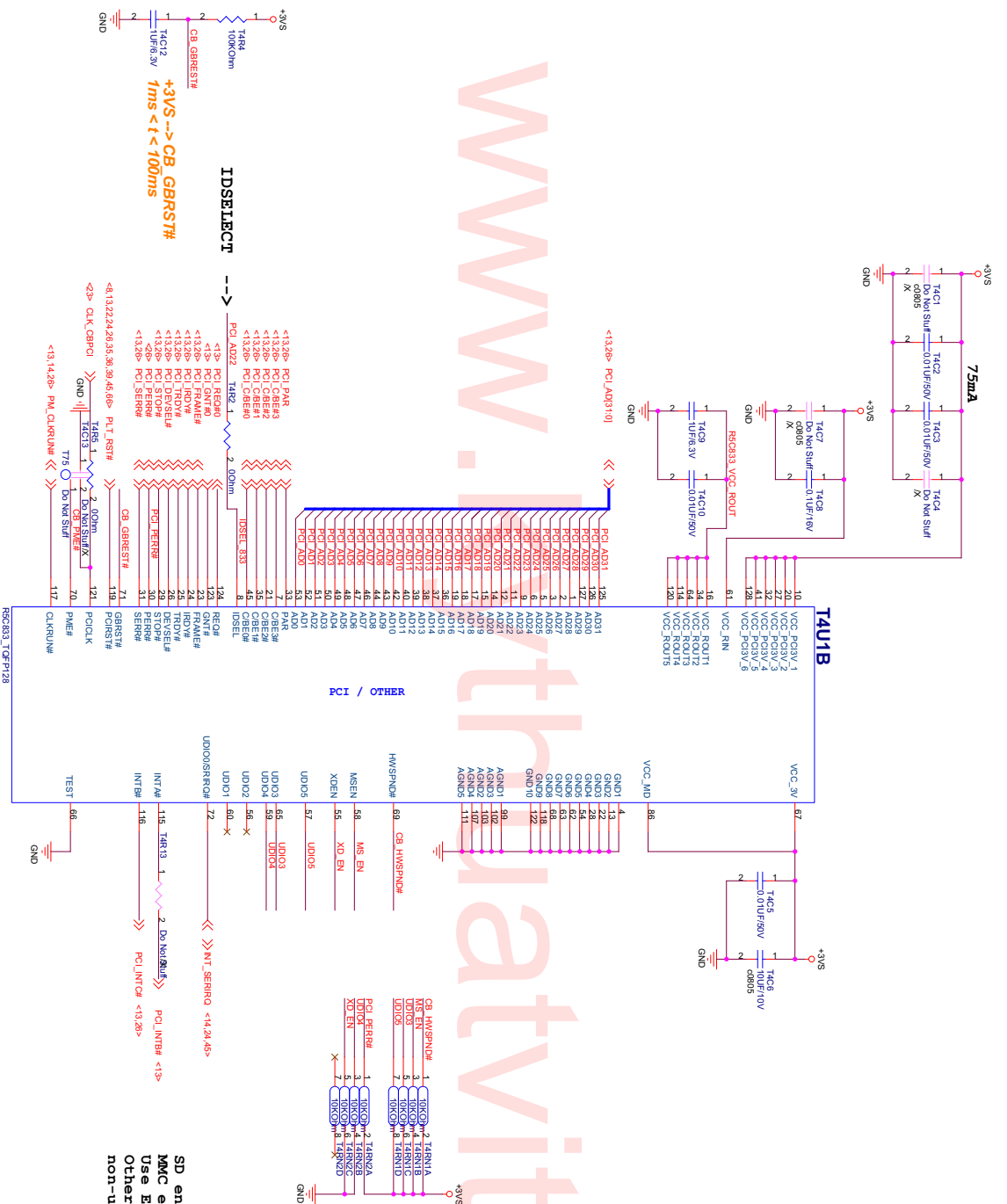
Sleep & Wake up

	S0	S3	S4	S0
S3AUXSW#	1	0	0	1
SB_PSON#	0	0	1	0
SUSC# (S4)	1	1	1	1
SUSB# (S3)	1	0	1	1
Power Status	Main	Main	System, S4	Main

Power ON & OFF:

	S5	S0	S5
S3AUXSW#	1	1	1
SB_PSON#	1	0	1
SUSC# (S4)	0	1	0
SUSB# (S3)	0	1	0
Power Status	System	Main	System

ASUS
ASUSTek Computer Inc.
Project Name: 262Ha
Engineer: Jack Hsu
Title: Other
Date: 2007/07/27

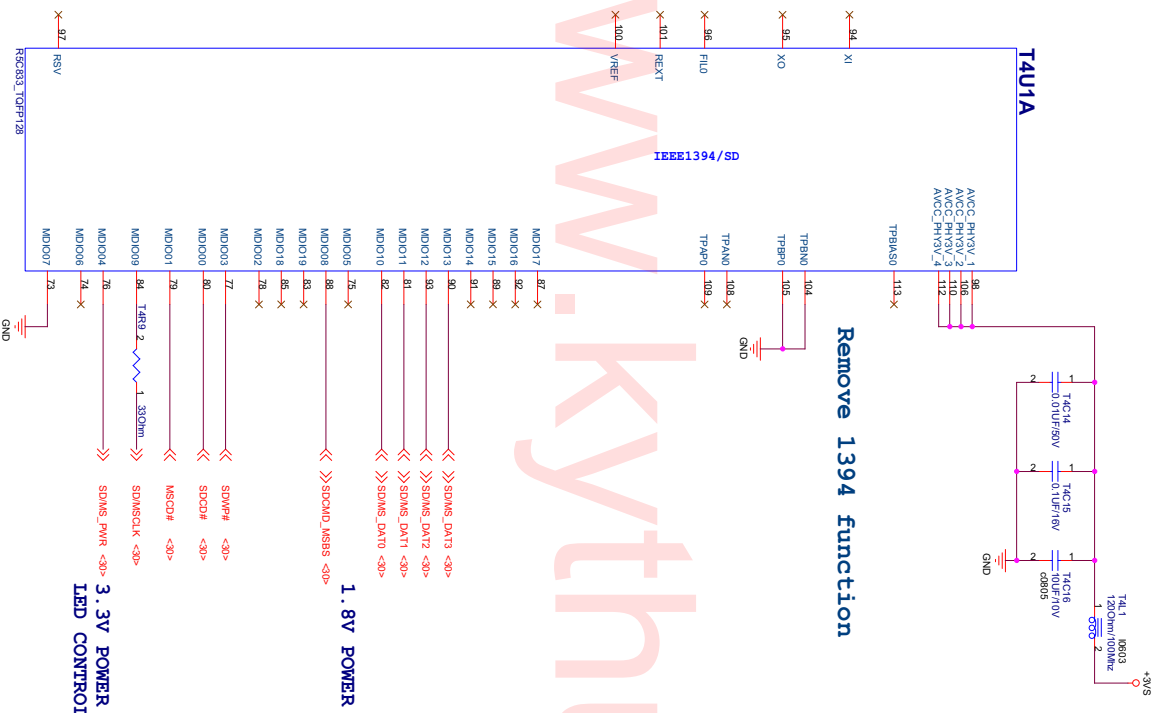


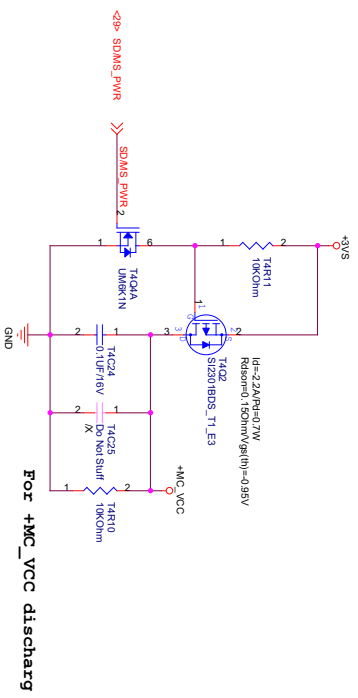
SD enable : UDIO3 pull-up
 MMC enable : UDIO4 pull-up
 Use EEPROM : UDIO5 pull-down
 Otherwise : disable or non-use

888

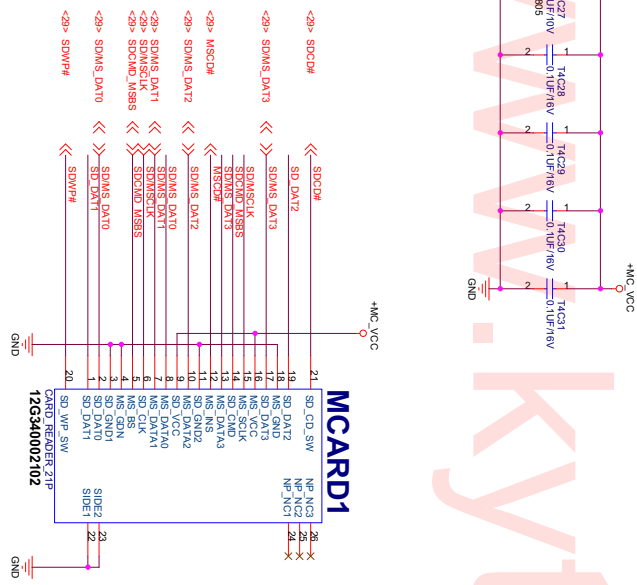
		Title : RSG383_PCI	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62Ha	1.1	

DATE: Thursday, September 27, 2007 28 of 70

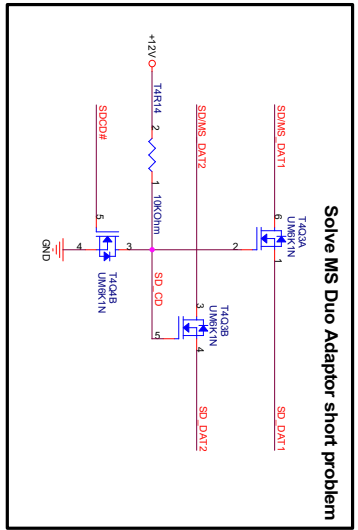
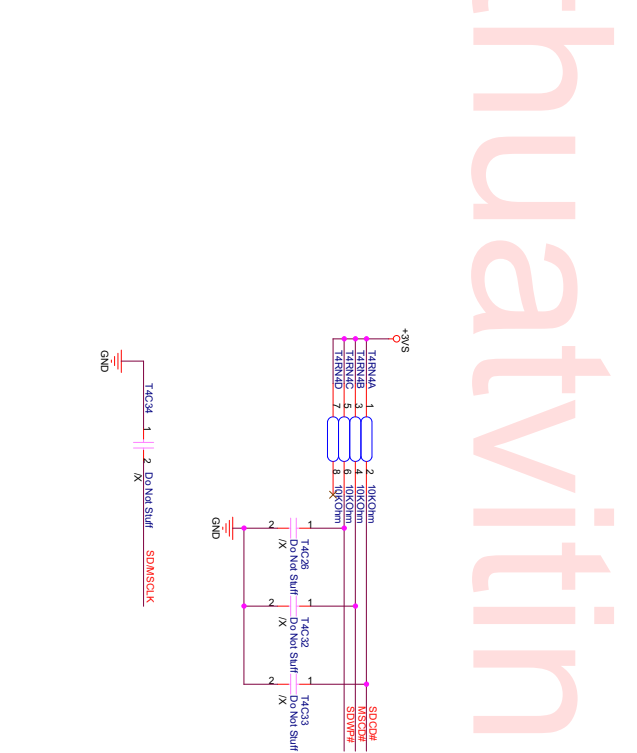




Card Reader Power Switcher



3 in 1 Card Reader



WWW.kythuatvitinh.com

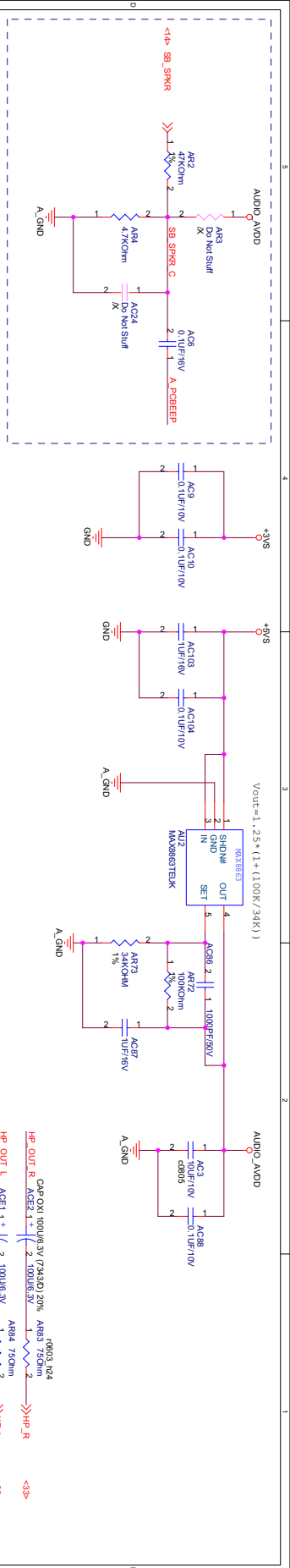
888

Title 3 in 1 Card Reader

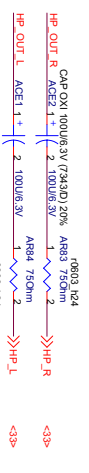
ASUSTek Computer INC. **Engineer: Jack Hsu**

Size: Custom **Z62Ha** Raw: 1/1

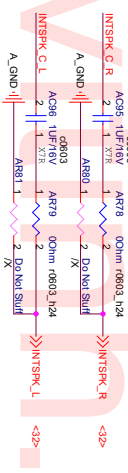
Date: Thursday, September 27, 2007 Sheet: 30 of 70



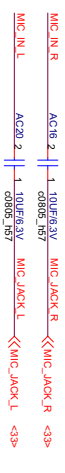
Headphone Output



Internal MIC Input



Internal Speaker



MIC Input



02G611002200 C.S ALC883-GR LOFP-48 REALTEK
 AUDIO CODEC:HP ALC883

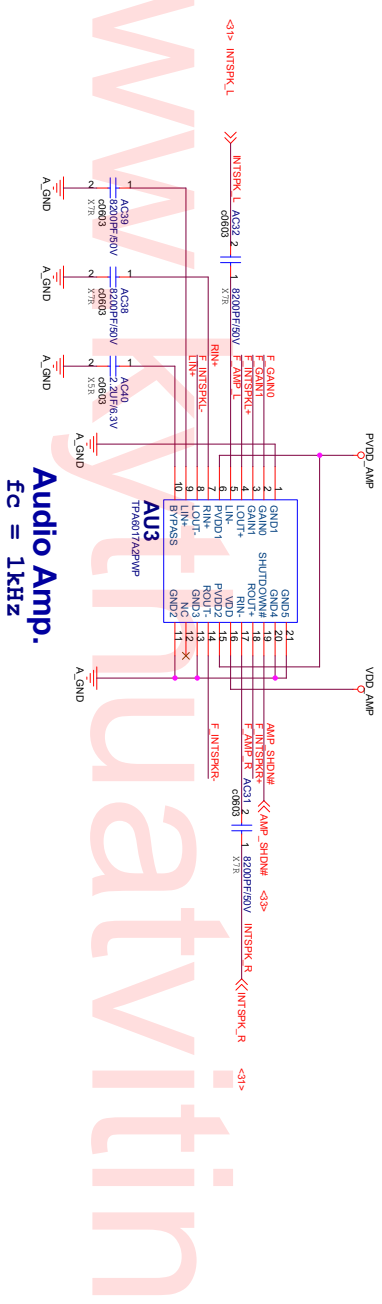
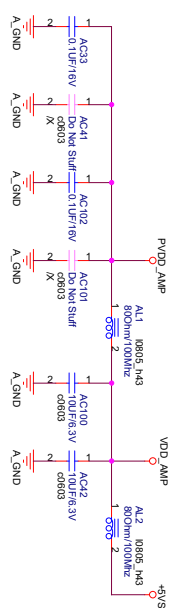
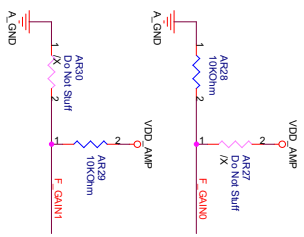
02G611001310 C.S ALC882 Rev'B1 LQFP-48
 REALTEK AUDIO CODEC ALC882

02G611002910 C.S ALC888-GR A1 LQFP-48
 REALTEK AUDIO CODEC ALC888 GR

		Title : Audio ALC882H	
		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62Ha	1.1	
Date: Thursday, September 27, 2007	Sheet	31	d
			70

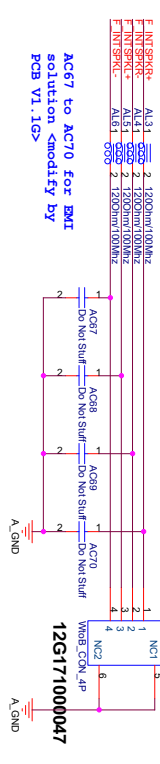
GAIN Control

GAIN0	GAIN1	
0	0	6dB
0	1	0dB
1	0	15.6dB
1	1	21.6dB



Audio Amp.
fc = 1KHz

12G171000047
Internal Speaker Connector



988

Title : Audio Amp. & Conn.

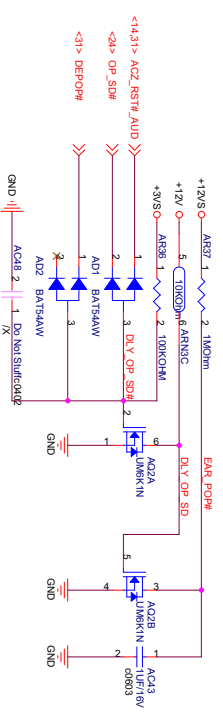
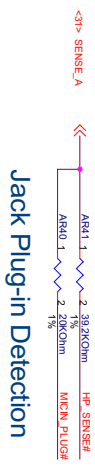
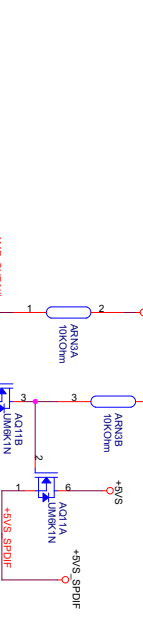
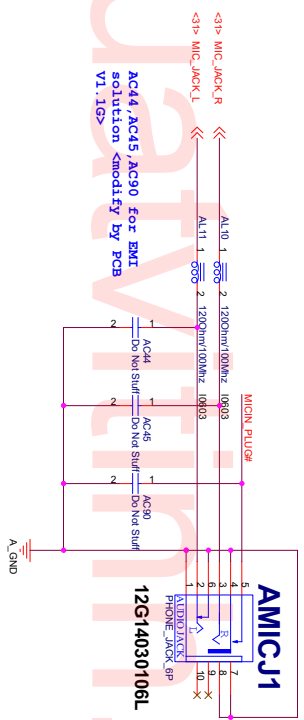
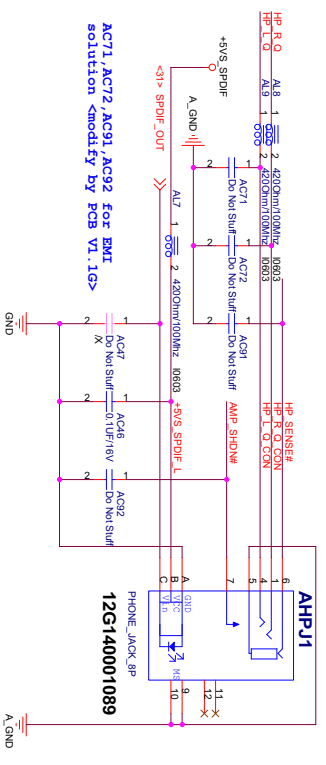
ASUSTek Computer INC. **Engineer:** Jack Hsu

Size: **Project Name**

Custom: **262Ha**

Date: Thursday, September 27, 2007 **Sheet** 20 of 70 **Rev** 1.1

Headphone & S/PDIF Jack

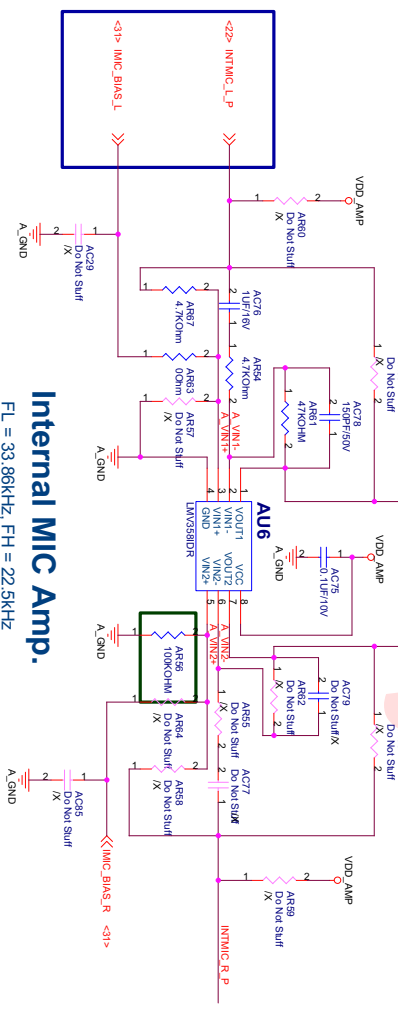


888

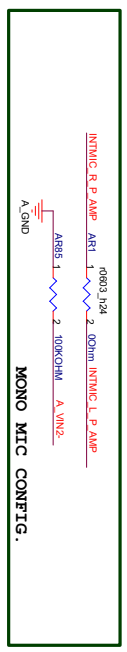
ASUSTeK Computer INC.		Title : Audio JACK	
Size	Project Name	Engineer	Jack Hsu
Custom	262HA		
Drawn	Tuesday, September 27, 2007	Sheet	33 of 70
		Rev	1.1

WWW.KYTHUAT.COM

5 4 3 2 1



Internal MIC Amp.
 FL = 33.86KHz, FH = 22.5KHz

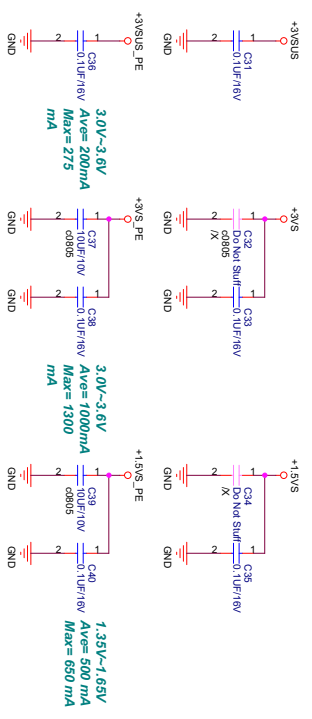
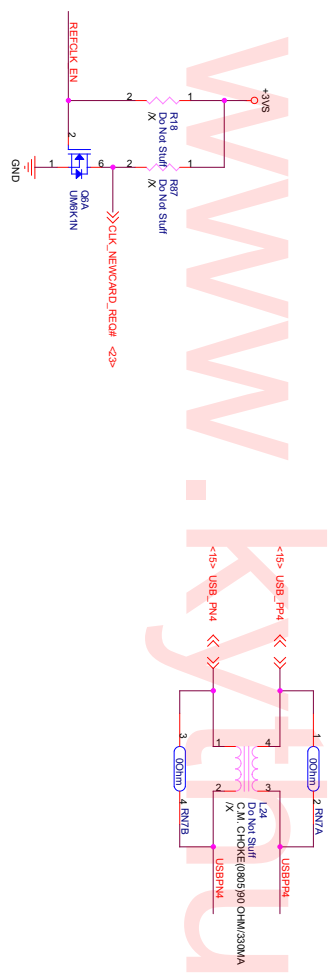
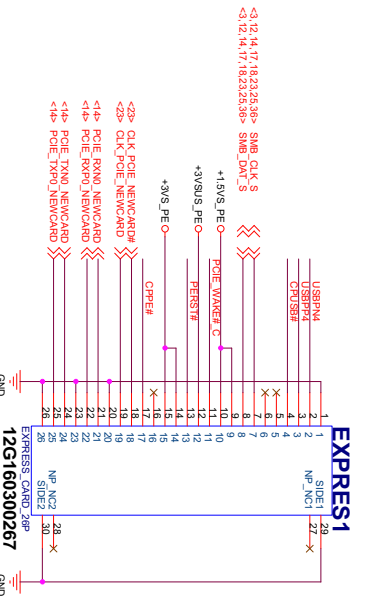
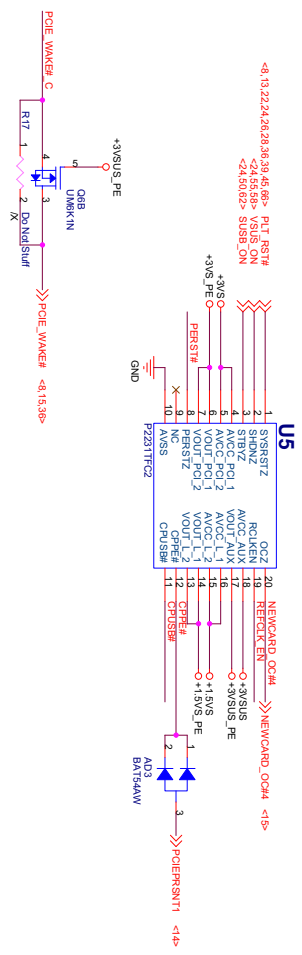


5 4 3 2 1

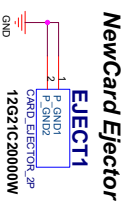
888

		Title : MIC Preamp.
Size	Project Name	Engineer: Jack Hsu
Custom	262HA	Rev
Date: Thursday, September 27, 2007	Sheet	34 of 70

NewCard Header



ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

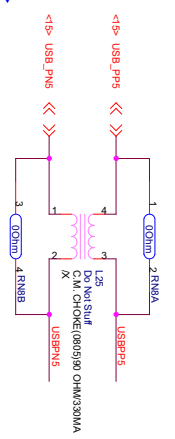
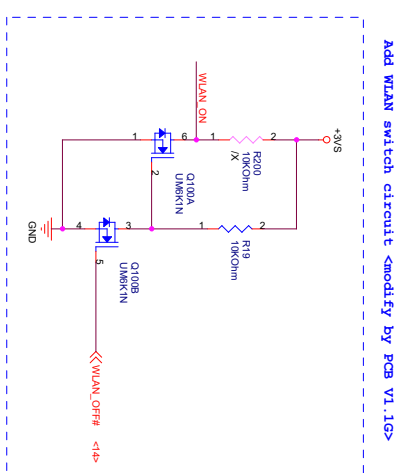
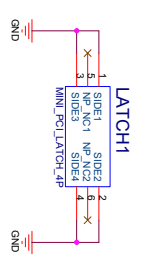
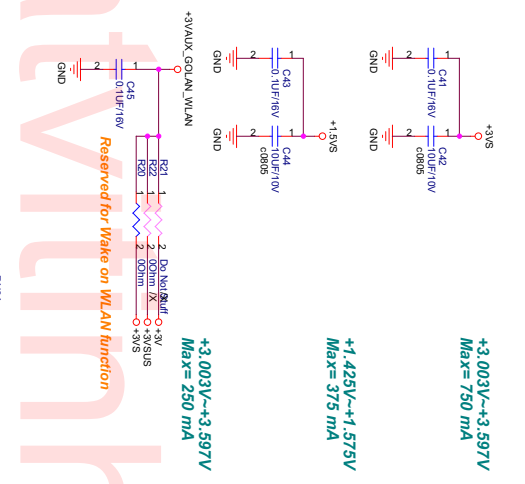
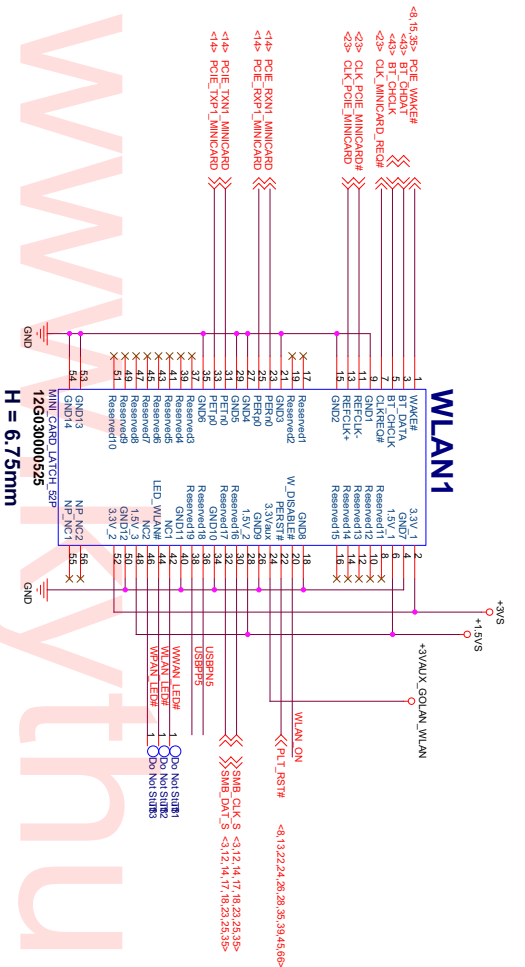


888

Title : NEWCARD
 ASUSTek Computer INC.
 Project Name: **Z62Ha**
 Engineer: **Jack Hsu**

Size	Project Name	Rev
Custom	Z62Ha	1.1

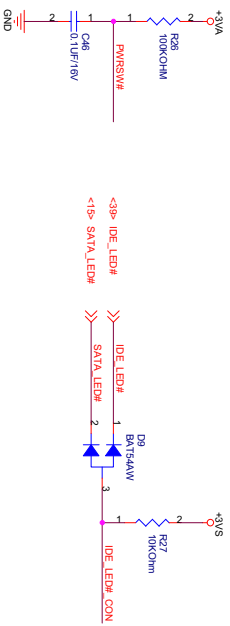
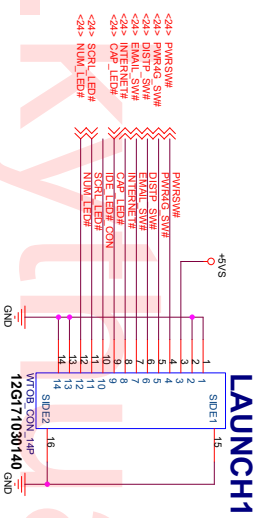
DATE: Thursday, September 27, 2007 Sheet 35 of 70



888

ASUSTek Computer INC.		ASUS	
Size	Project Name	Title : MINICARD - WLAN	
Custom	Z62Ha	Engineer :	Jack Hsu
Date : Thursday, September 27, 2007	Sheet	38	of
			70
			Rev
			1.1

LAUNCH BOARD Connector



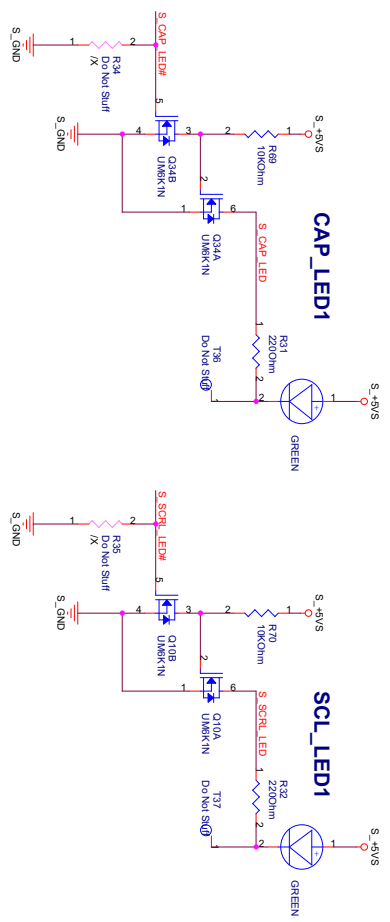
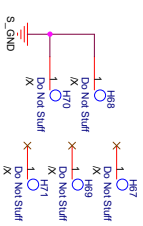
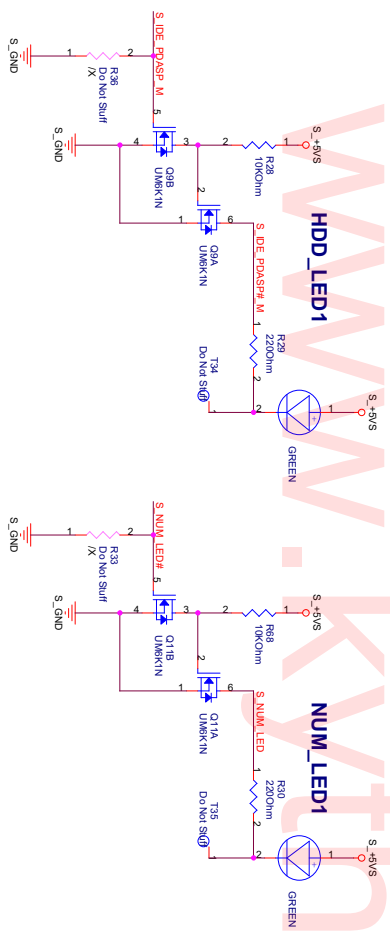
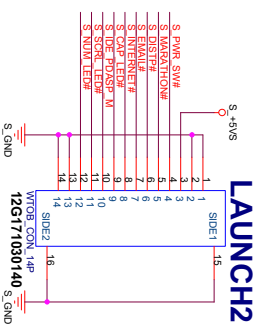
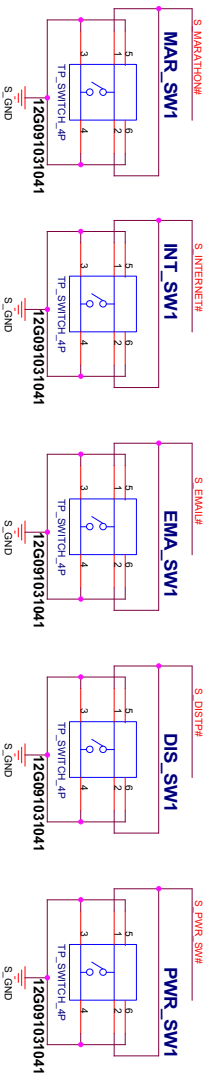
EC568_1	2	DO NOT SOLDER	PWR/SW#
EC567_1	2	DO NOT SOLDER	PWR/CLK SW#
EC566_1	2	DO NOT SOLDER	DISK SW#
EC565_1	2	DO NOT SOLDER	INTERNAL SW#
EC564_1	2	DO NOT SOLDER	INTENET SW#
EC563_1	2	DO NOT SOLDER	IDE_LED#
EC562_1	2	DO NOT SOLDER	IDE_LED#_CON
EC561_1	2	DO NOT SOLDER	SCRL_LED#
EC560_1	2	DO NOT SOLDER	NUM_LED#

EC57 to EC64 for BMT solution
<modify by PCB VI.1G>

888

FSUS		Title : LAUNCH B Conn.	
ASUS Risk Computer INC.		Engineer: Jack Hsu	
Site	Project Name	Rev	
Calson	Z62HA	1.1	
Date: Thursday, September 27, 2007	Sheet: 37	of	70

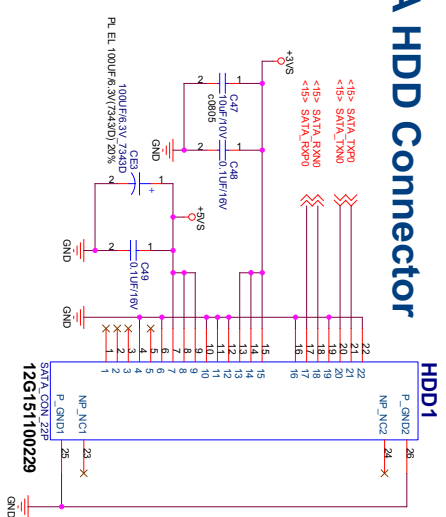
www.kyattivityinh.com



5 4 3 2 1

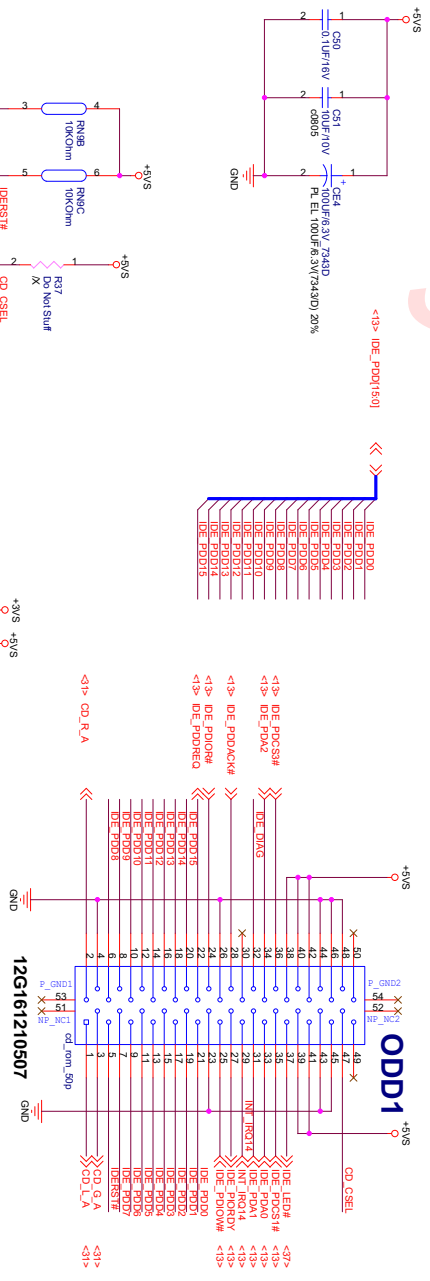
888	ASUS	Title : LAUNCH BOARD
ASUSTek Computer INC.	Project Name	Jack Hsu
Custom	262HA	Engineer
Drawn: Thursday, September 27, 2007	Sheet	38 of 70
	Rev	1.1

SATA HDD Connector



www.kytruatvitiuh.com

ODD Connector

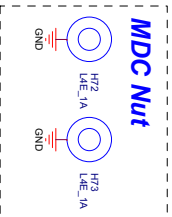
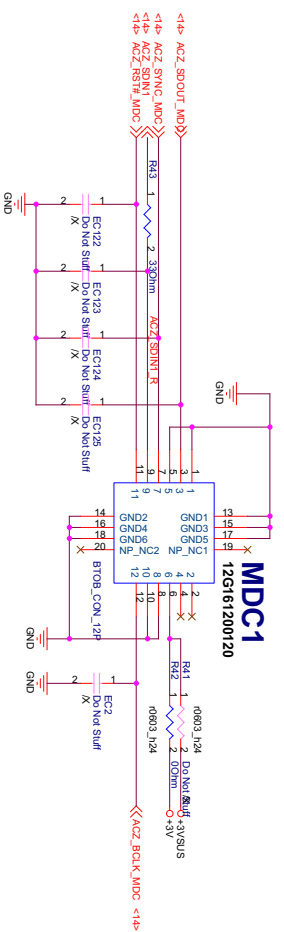


<13> DE_P001[50]

ODD_CSEL# : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master

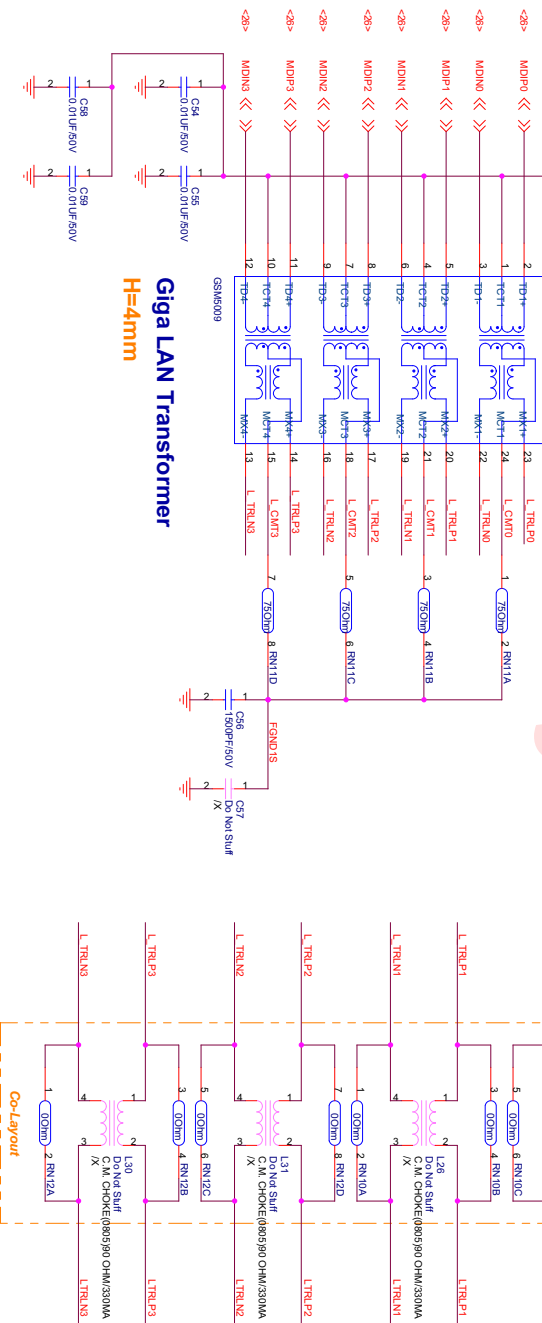
ASUS®
ASUSTek Computer INC.
Project Name: Z62Ha
Title: HDD & ODD
Engineer: Jack Hsu
Date: Thursday, September 27, 2007
Sheet: 38 of 70

MDC Connector



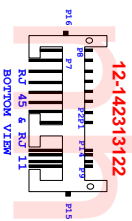
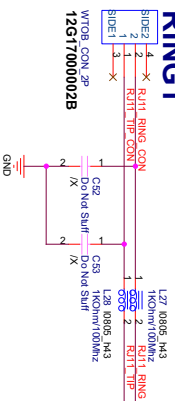
www.kytlh.com

TRANS1

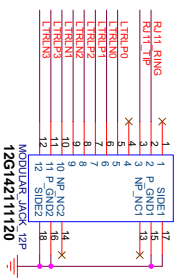


Giga LAN Transformer
H=4mm

RING1

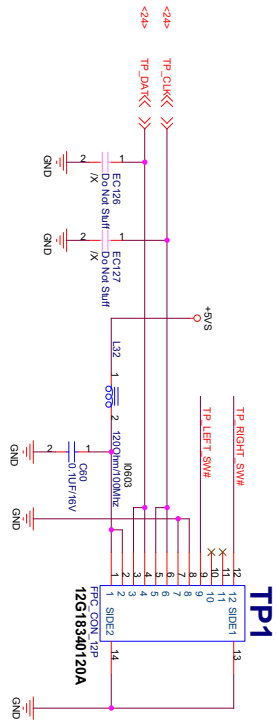


RJ45_11



ASUSTek Computer Inc.	Title : MDC RJ45 RJ11		
Project Name	Z62Ha		
Engineer	Jack Hsu		
Size	A4		
Custom	1:1		
Date	Thursday, September 27, 2007	Sheet	40 of 70

TouchPad Connector

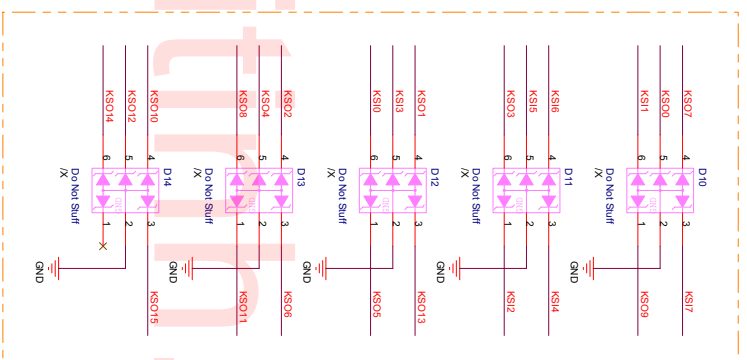
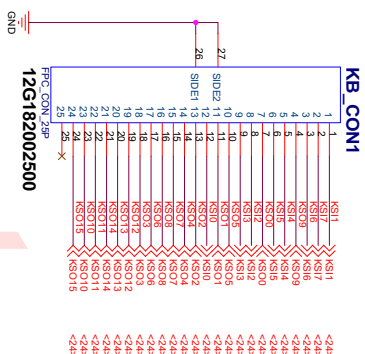


Touch pad Definition

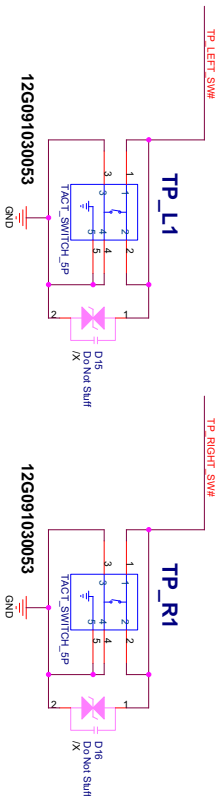
1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	x	1	GND	GND	CLK	CLK	CLK	DAT	DAT

z62f: pin1 reversal

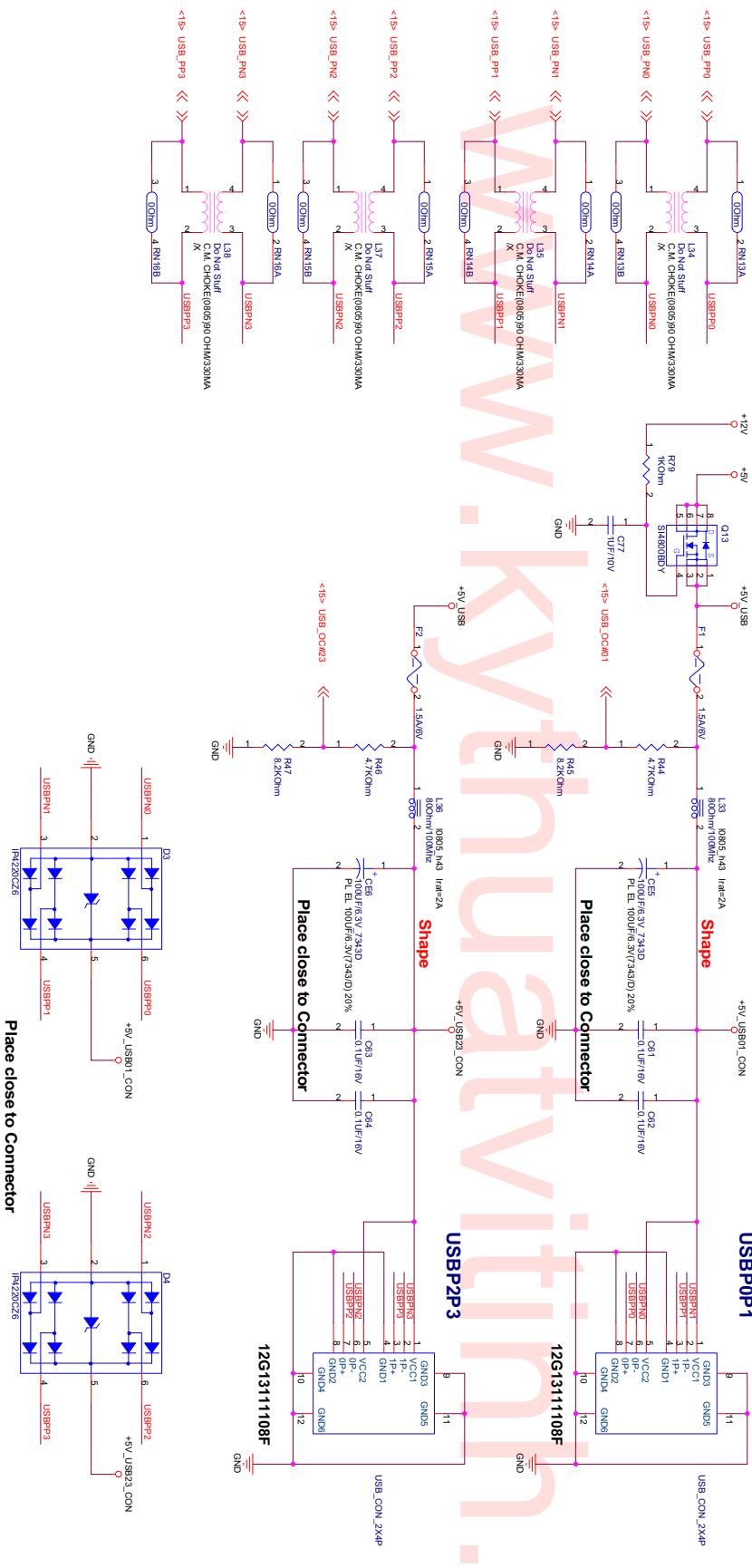
Keyboard Connector



TOUCH PAD SWITCH



USB Power & OC Alert



888

Title : USB Connector

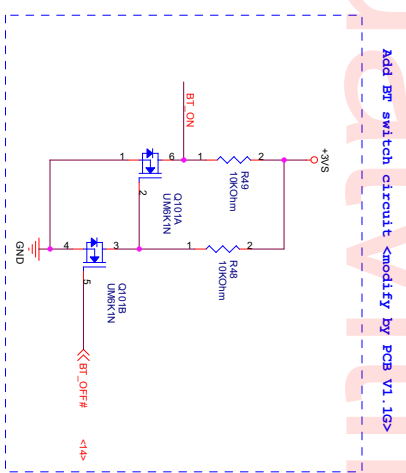
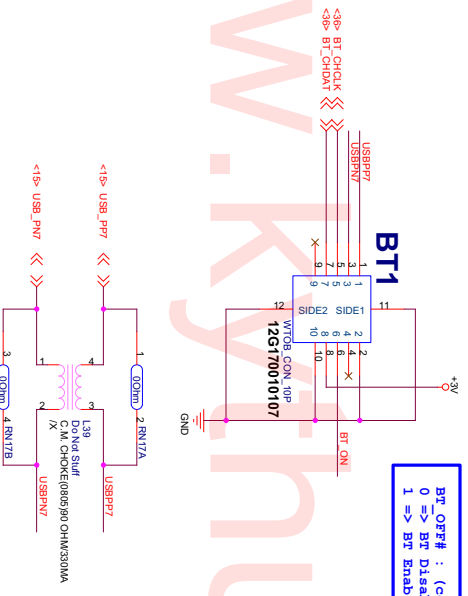
ASUSTek Computer INC. **Engineer: Jack Hsu**

Size: Custom **Revision: 1.1**

Date: Thursday, September 27, 2007 Sheet: 42 of 70

Bluetooth Connector

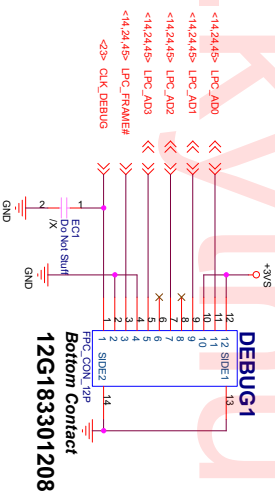
BT_OFF# : (connect to GPO, push-pull, default High)
 0 => BT Disabled
 1 => BT Enabled



888

		Title : Bluetooth Conn.	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62HA		1.1
Date: Thursday, September 27, 2007	Sheet	43	of 70

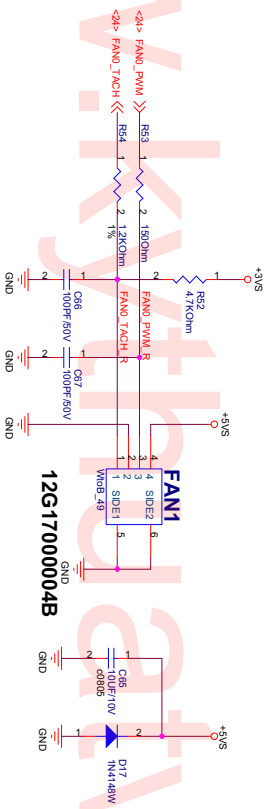
Debug Connector



Bottom Contact
12G183301208

898

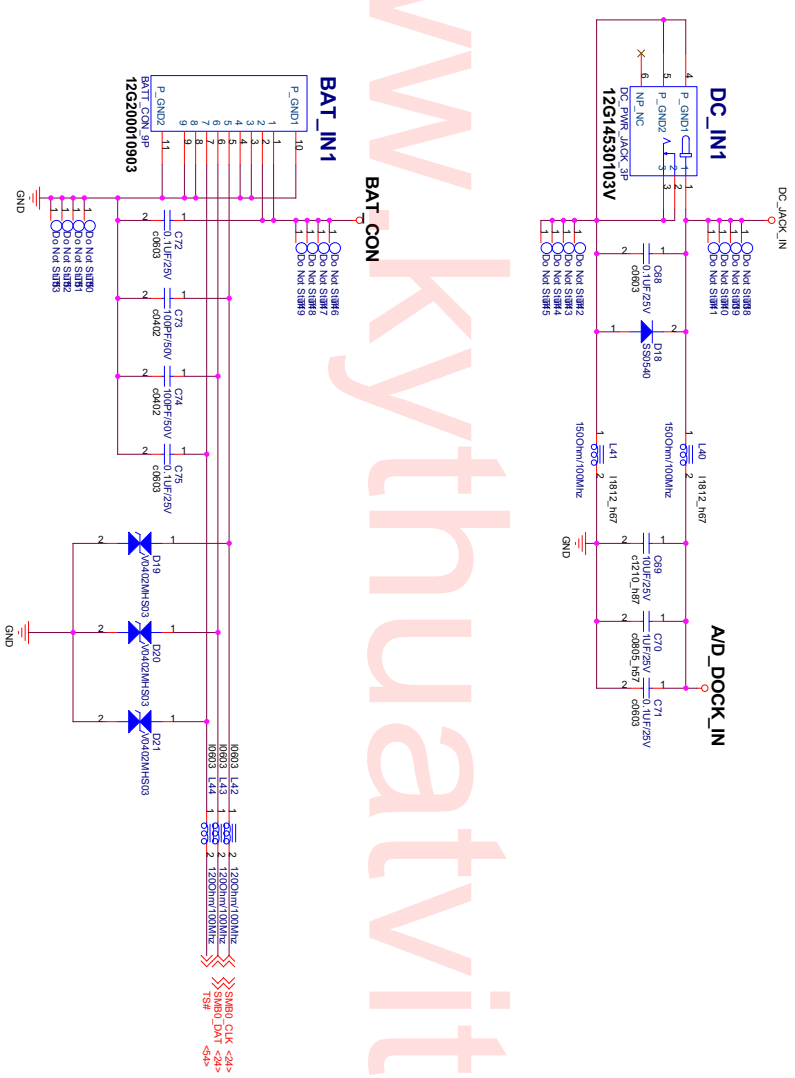
		Title : Debug Port	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62HA		1.1
Date: Thursday, September 27, 2007	Sheet	44	of 70



SYSTEM Fan Connector

 Title : Fan Connector	
ASUSTek Computer INC. Engineer: Jack Hsu	
Size	Project Name
Custom	Z62Ha
Date	Thursday, September 27, 2007
Sheet	48 of 70
Rev	1.1

www.kythuatvithinh.com



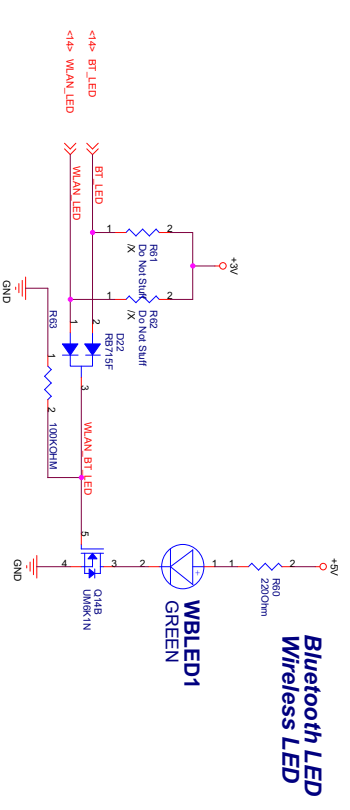
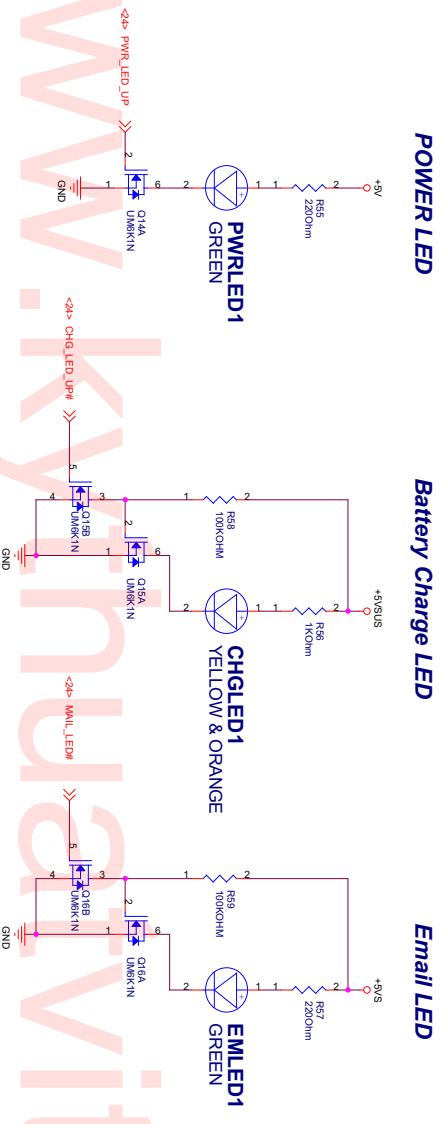
888

		Title : DC-IN & BAT-IN	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62Ha		1.1
Date: Thursday, September 27, 2007	Sheet	47	70

www.kythuatvitinh.com

888

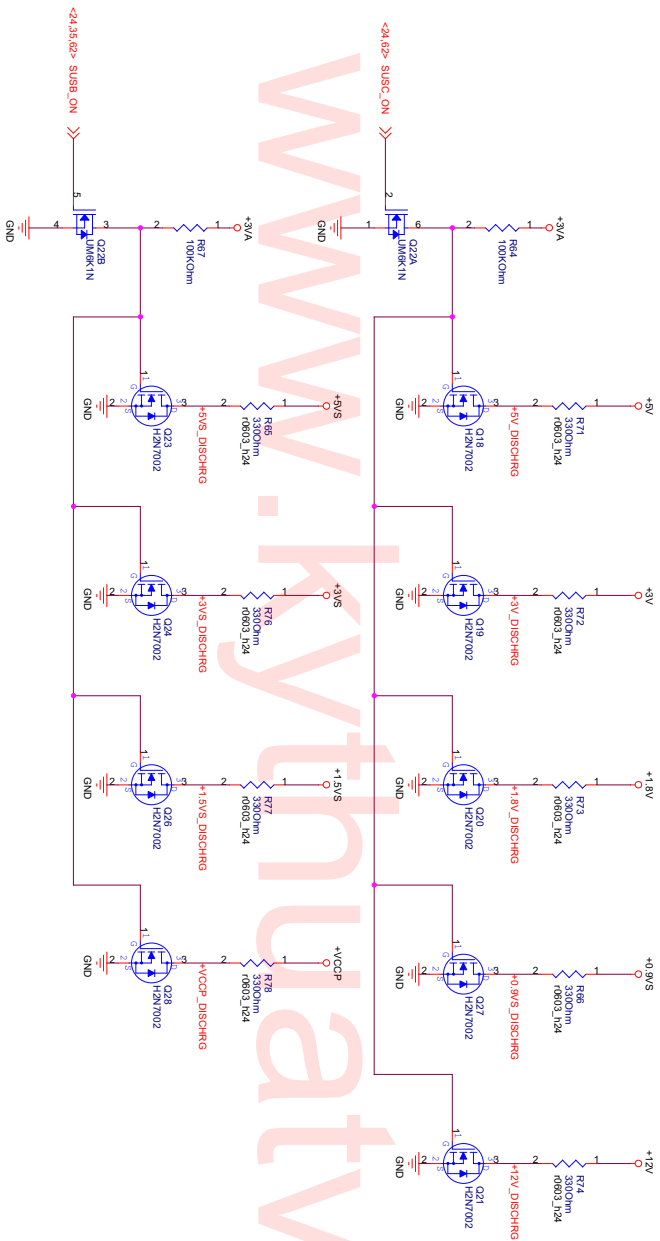
		Title : BLANK	
ASUSTEK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Sheet	Rev
Custom	262HA	48	1.1
Date: Thursday, September 27, 2012			



www.kynvithinh.com

888

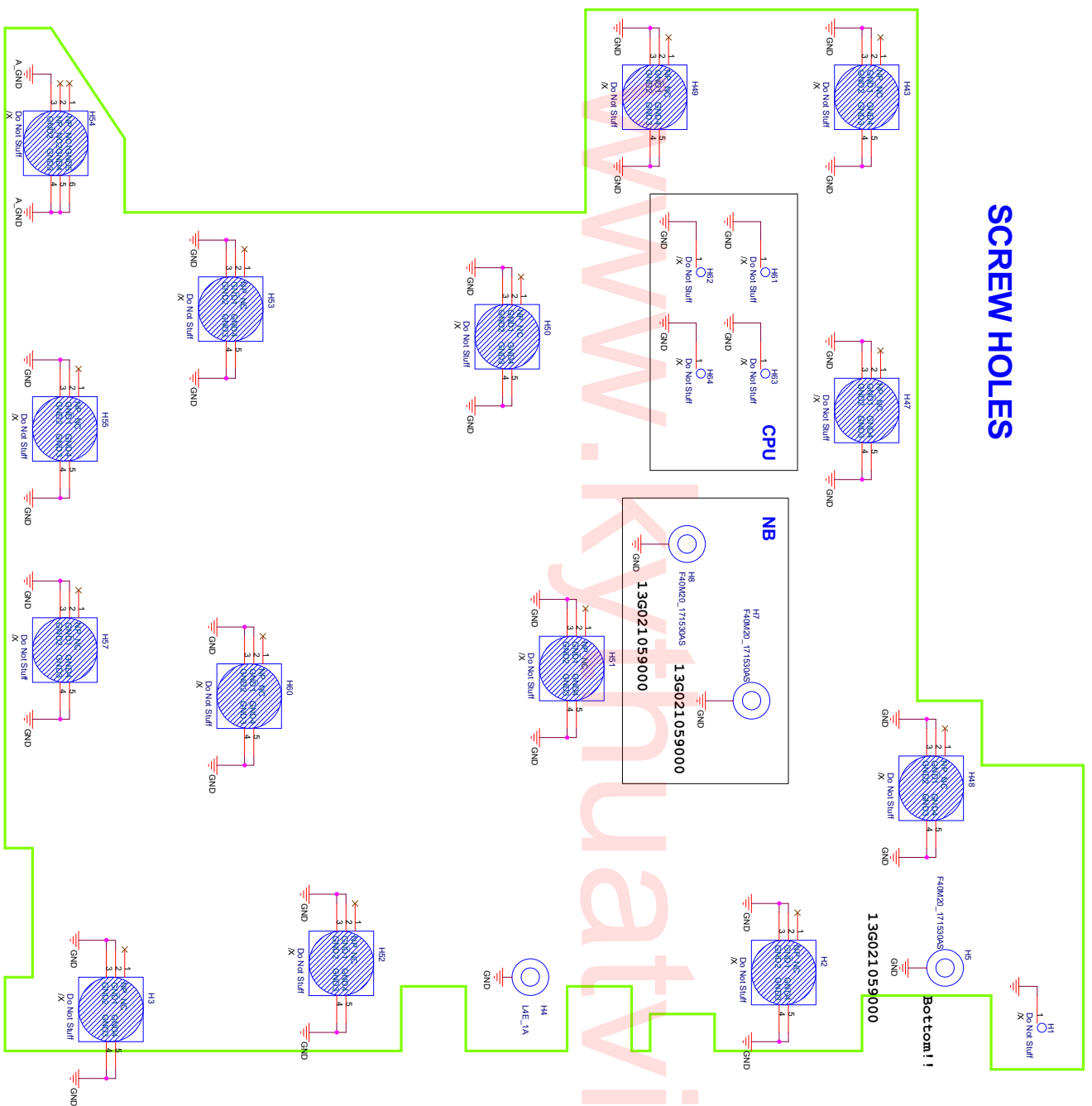
		Title : LED
ASUSTek Computer INC.		Engineer: Jack Hsu
Size	Project Name	Rev
Custom	Z62Ha	1.1
Date	Thursday, September 27, 2007	Sheet
		48 of 70



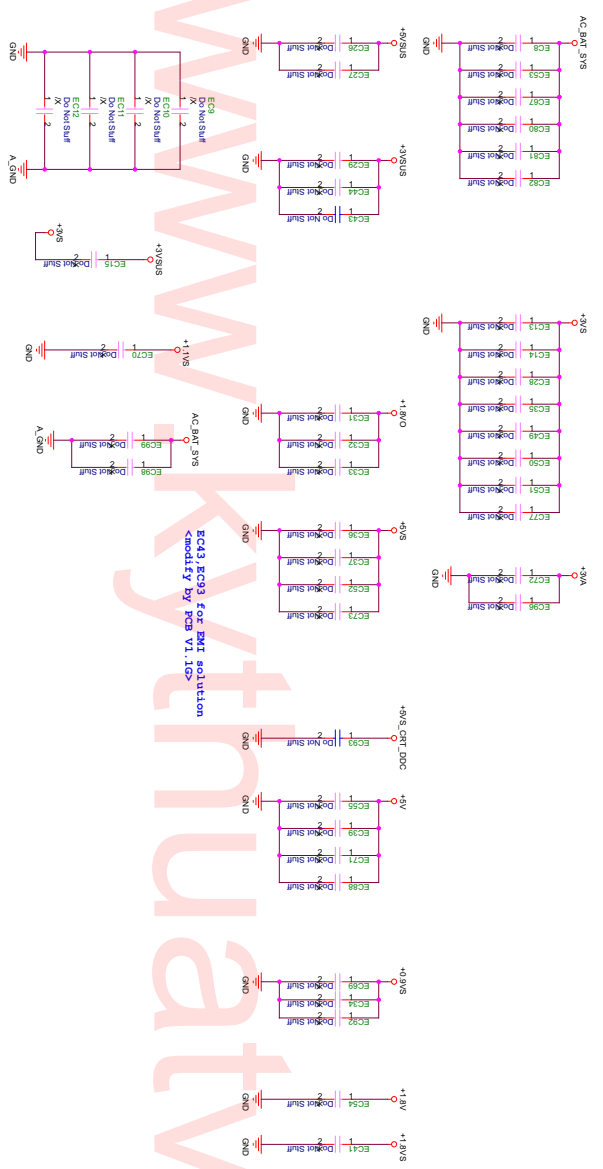
888

		Title : Discharge	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Sheet	d
Custom	Z62Ha	50	70
Date: Thursday, September 27, 2007			

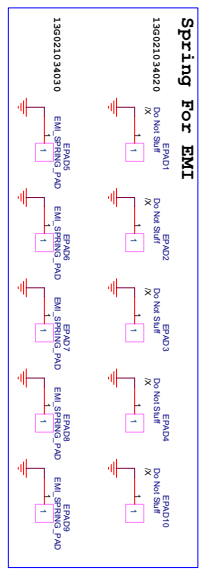
SCREW HOLES



888		ASUS		Title : Screw Hole	
ASUSTek Computer INC.		Project Name		Engineer: Jack Hsu	
Custom		Z62Ha		Rev: 1.1	
Date: Thursday, September 27, 2007		Sheet: 51		of: 70	



EC03 EC03 for EMI solution
<modify by PCB V1.1.0>



898

FEBS Title: **EMICAP**

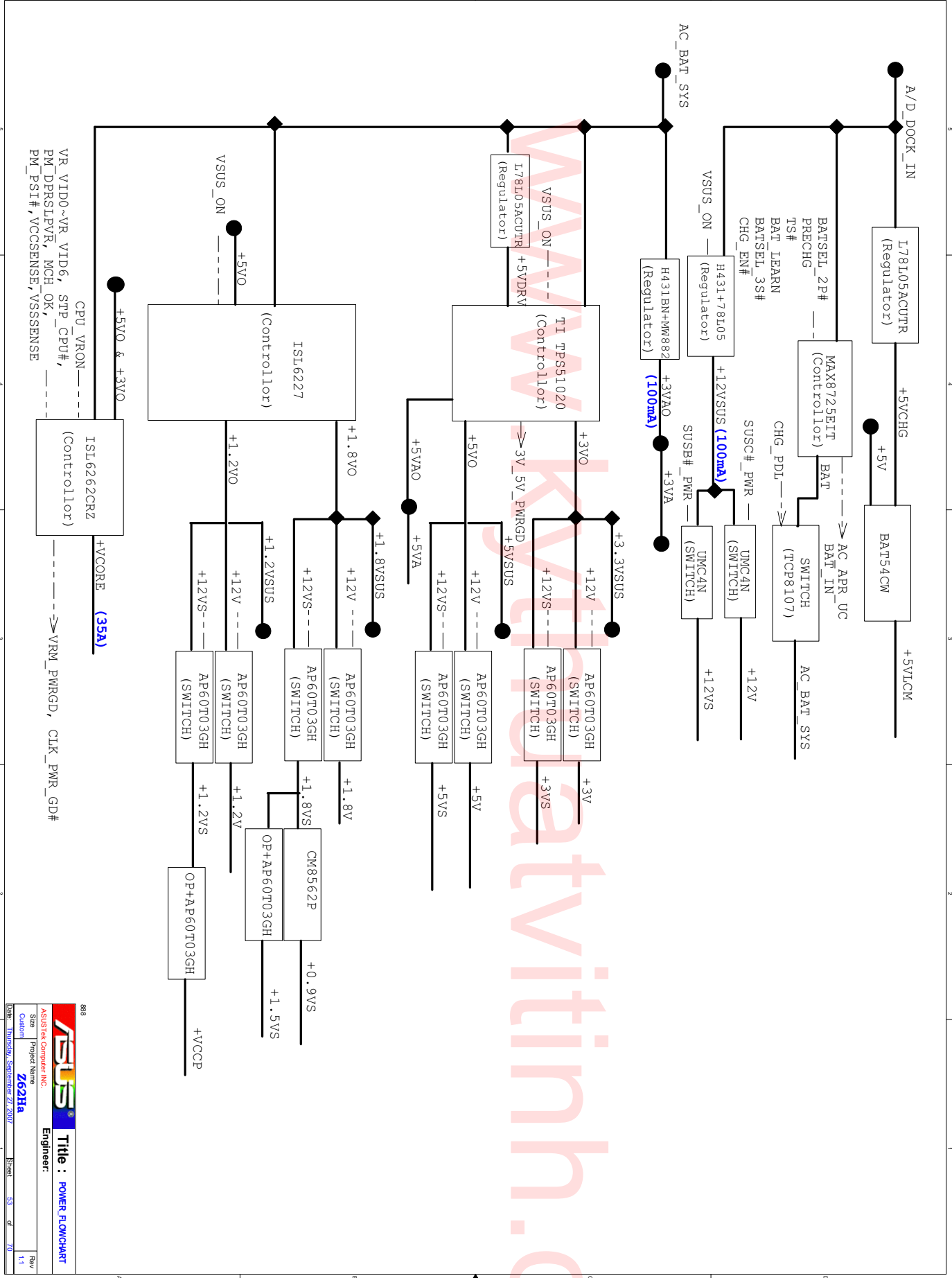
ASISTEK COMPUTER INC.

Size Project Number: **26211a** Engineer: **Jack Hsu**

Rev: 1.1

DATE: Thursday, September 22, 2011 11:20 AM

5 4 3 2 1



VR_VIDD~VR_VID6, STP_Cpu#, CPU_VRON
PM_DPSL1PVR, MCH_OK, ISL6262CRZ (Controller)
PM_PSI#, VCCSENSE, VSSSENSE +VCCORE (35A)
VIM_PMRGD, CLK_PMR_GD#

AC_IN Threshold: 2.048Vmax AD_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter In(max) = (0.075V/RsenseADIN)*VCC5VREF
VCC5V = 2.885V
PR6708=20K PR6714 = 178K limit = 4.5A, 81W
PR6708=21K PR6714 = 47K limit = 3.175A, 50W

Setting the Charge Voltage

Vcell = Cell * Vref * (VCTL - 1.8V) / 9.5211
VCTL = 1.588V => Vbat = 4.2V

Setting the Charge Current

Charge Current Ichg = (0.075V/RsenseCHG)*VCTL3.6V
RsenseCHG = 15mOhm

Pre-Charging Mode

Precharging current = Ichg - I52mA
Vctf = 0.107V - 0.109V

Battery Cell Selection

BATSEL_2PH = 1, 3 Cells; Vctf = 2.084V
=> Icharge = 1.6933A
BATSEL_2PH = 0, 6 or 9 Cells; Vctf = 2.111V
=> Icharge = 2.9329A
PR5708 = 120K PR5715 = 120K; Icharge = 2.9329A

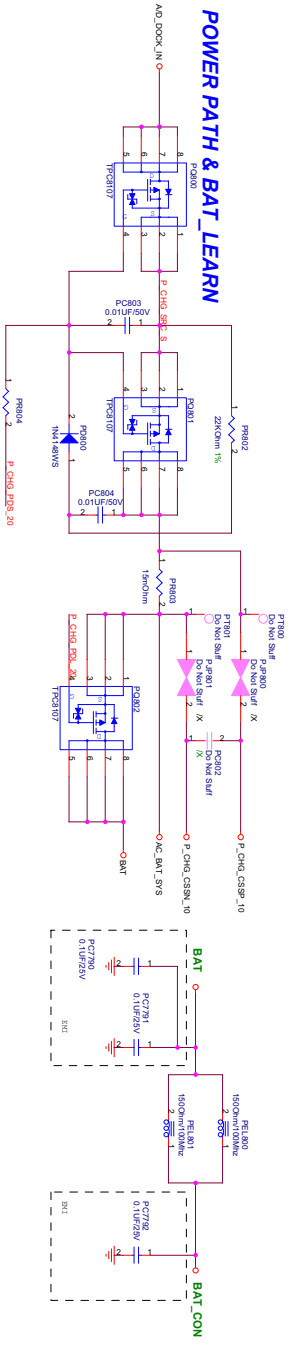
Mode pin

Mode pin : Vmode > 2.8V (the B_LDO pin) -> 4 Cells
2.0 > Vmode > 1.6V (floating) -> 3 Cells
0.5 > Vmode (tied to GND) -> Learning mode
VCTL < 0.8V * FCDIN < 7V -> Charge Disable

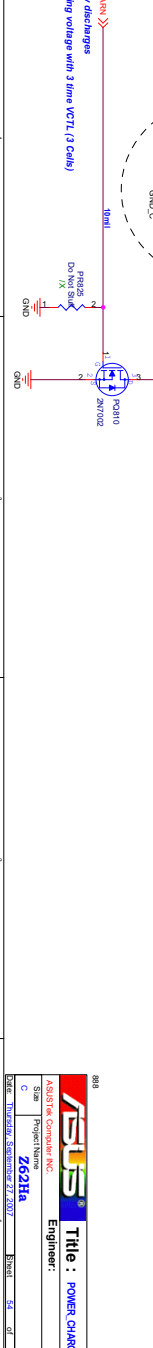
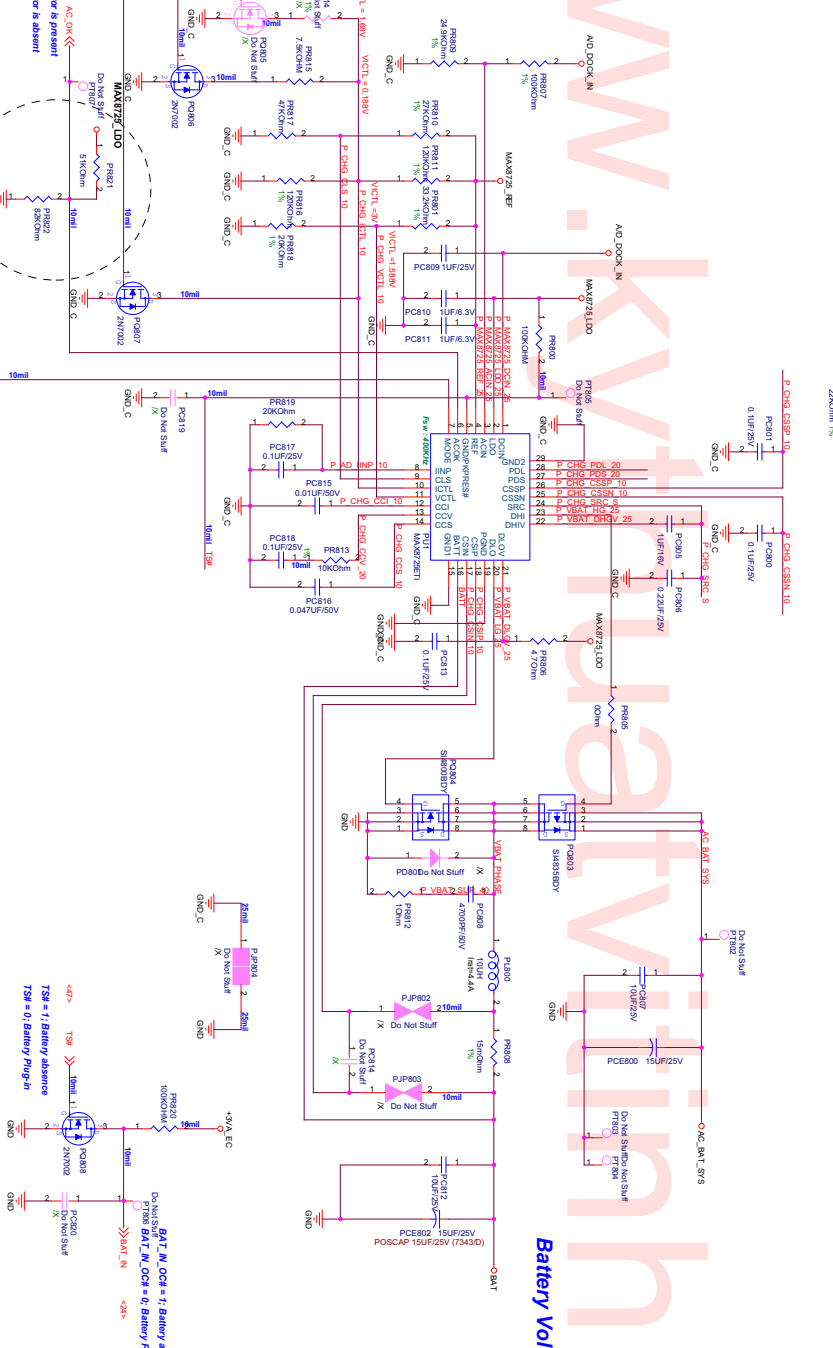
MAX8725 REF: 4.2235V

MAX8725_LDO: 5.4V

POWER PATH & BAT_LEARN

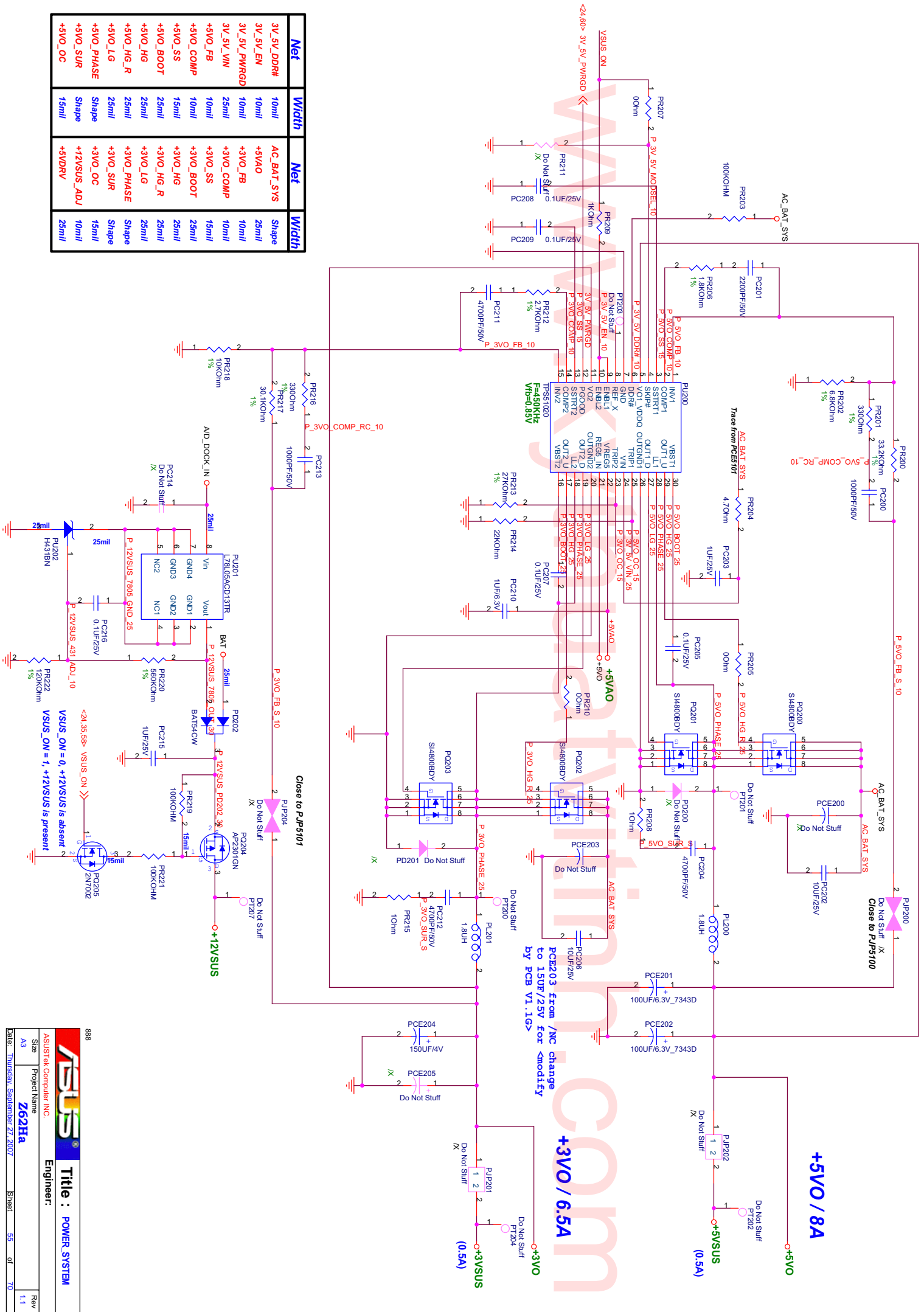


Battery Voltage



ASUS ROG Z621HA
Title: POWER CHARGER
Engineer:
Rev: 1.1

Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3V0_FB	10mil
3V_5V_VIN	25mil	+3V0_COMP	10mil
+3V0_BOOT	10mil	+3V0_SS	25mil
+3V0_COMP	10mil	+3V0_BOOT	25mil
+3V0_SS	15mil	+3V0_HG	25mil
+3V0_BOOT	25mil	+3V0_HG_R	25mil
+3V0_HG	25mil	+3V0_LG	25mil
+3V0_HG_R	25mil	+3V0_PHASE	Shape
+3V0_LG	25mil	+3V0_SUR	Shape
+3V0_PHASE	Shape	+12VSUS_ADJ	15mil
+3V0_SUR	Shape	+5VDDR	10mil
+5V0_OC	15mil		25mil



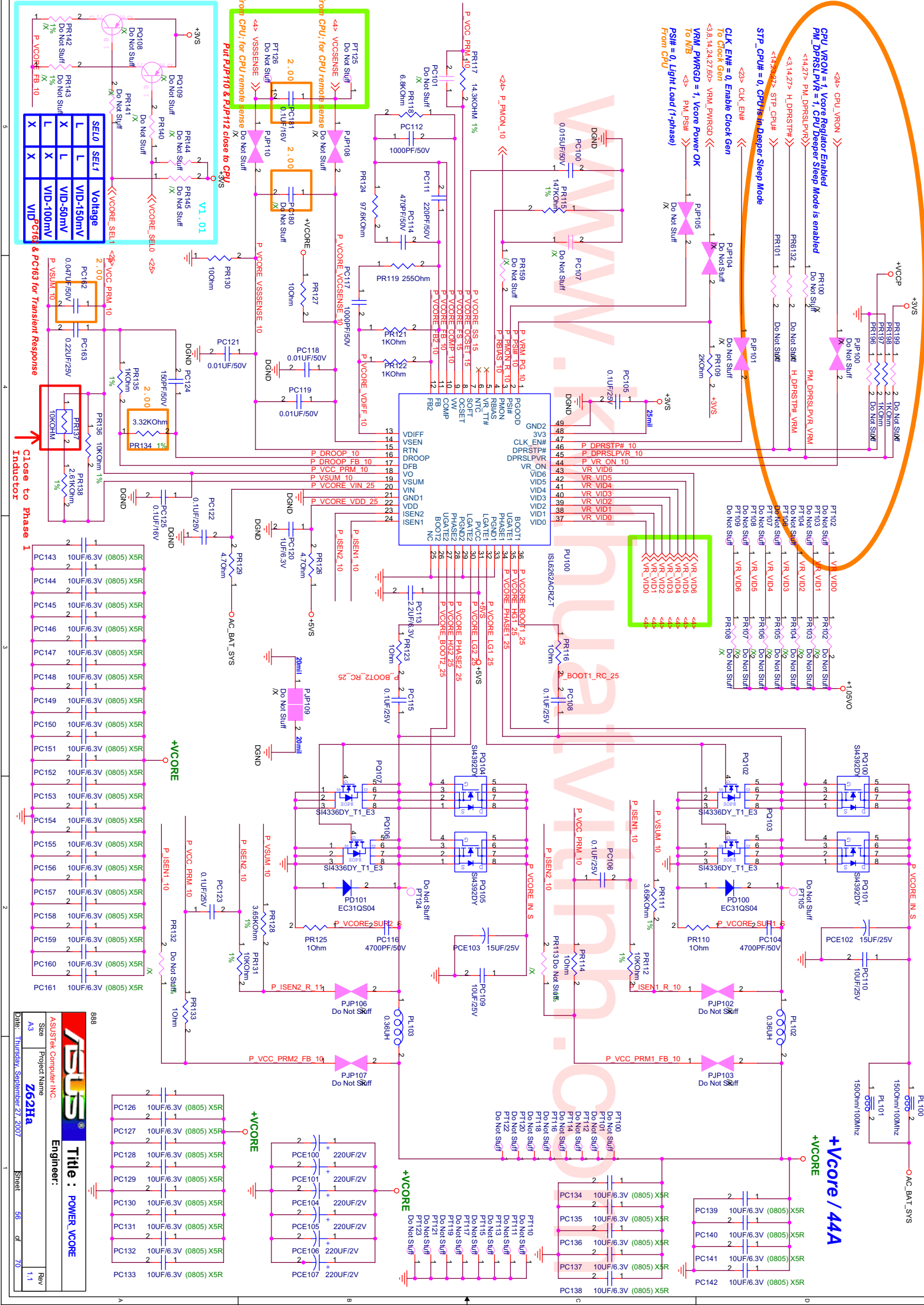
PCE203 from /NC change to 150UF/25V for V_{SUS_ON} by PCB V1.1G>

+3V0 / 6.5A

+5V0 / 8A

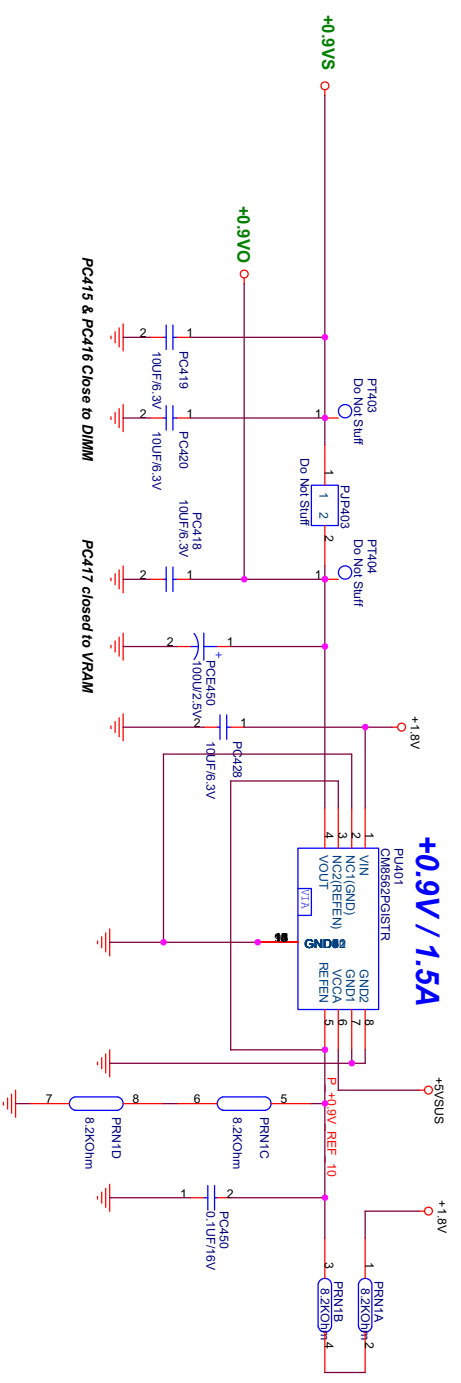
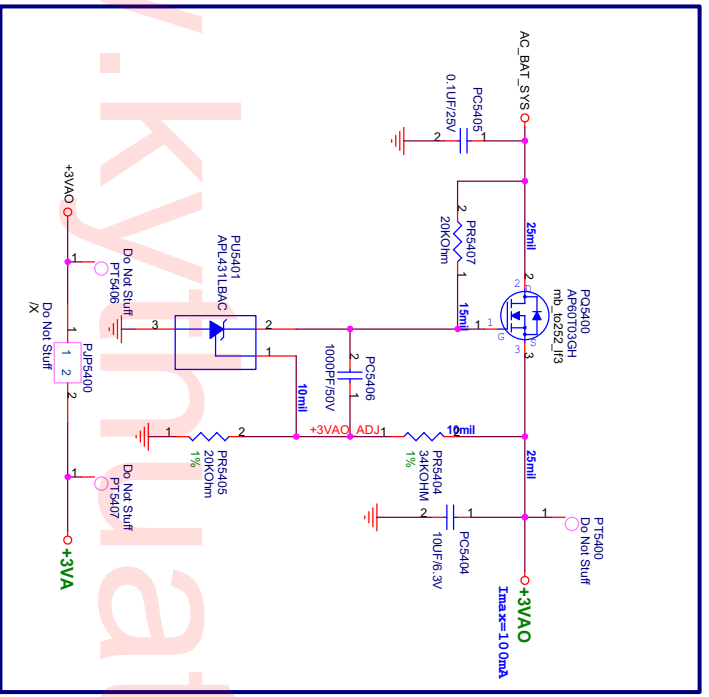
+3VSUS (0.5A)

+5VSUS (0.5A)



888
ASUSTek Computer, INC.
Project Name: 7622Ha
Title: POWER VCore
Engineer:
Date: Thursday, September 27, 2007
Sheet: 96 of 70
Rev: 1.1

PC100	150Ohm/100mHz
PL101	150Ohm/100mHz
P100	150Ohm/100mHz

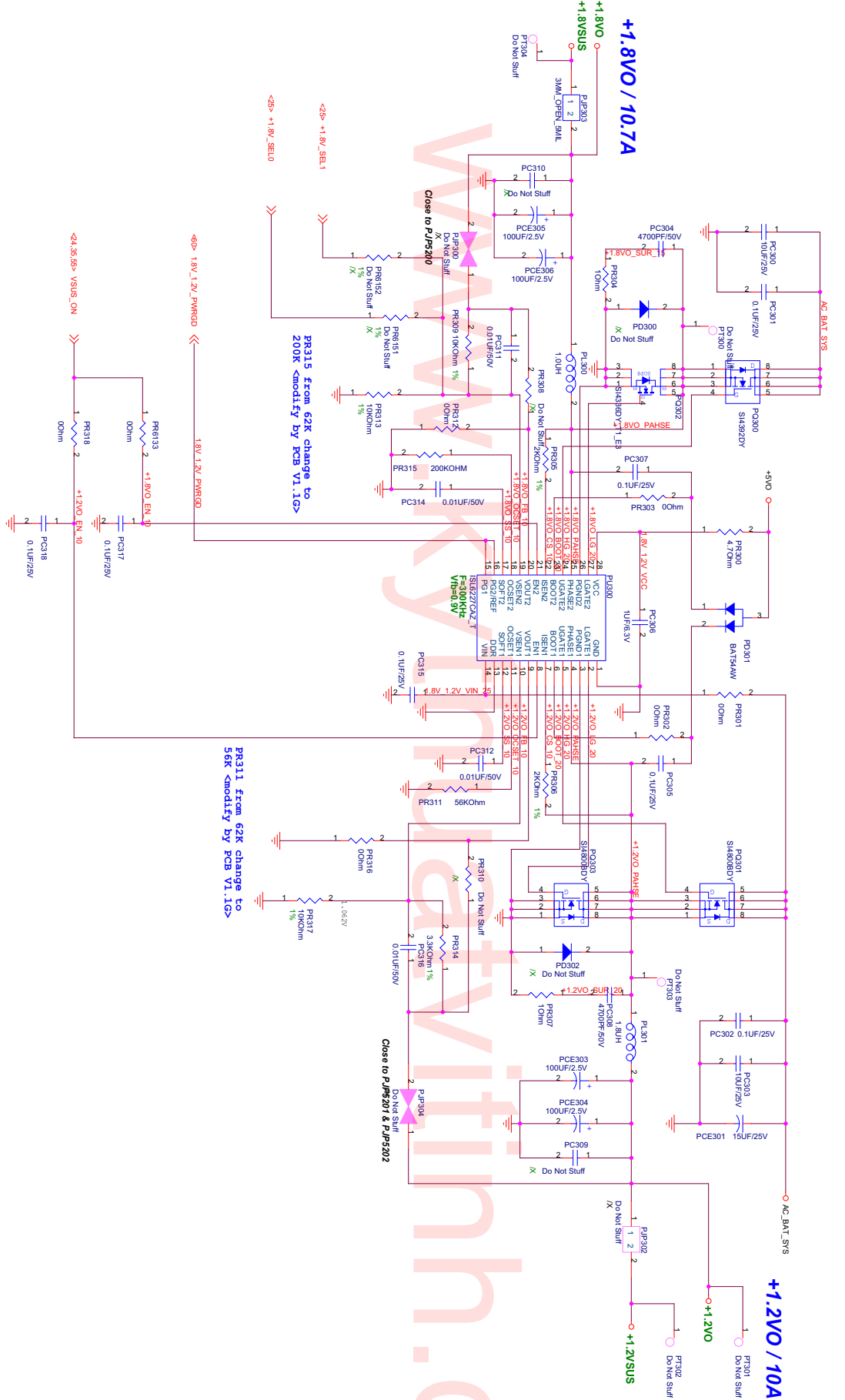


DDR Power Rev:1.00

888

		Title :	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Sheet	of
A3	Thursday, September 27, 2007	57	70
Date	Rev		
	1.1		

www.kylinatv.itinh.com



PR315 from 62k change to 200k <modify by PCB V1.1G>

PR311 from 62k change to 56k <modify by PCB V1.1G>

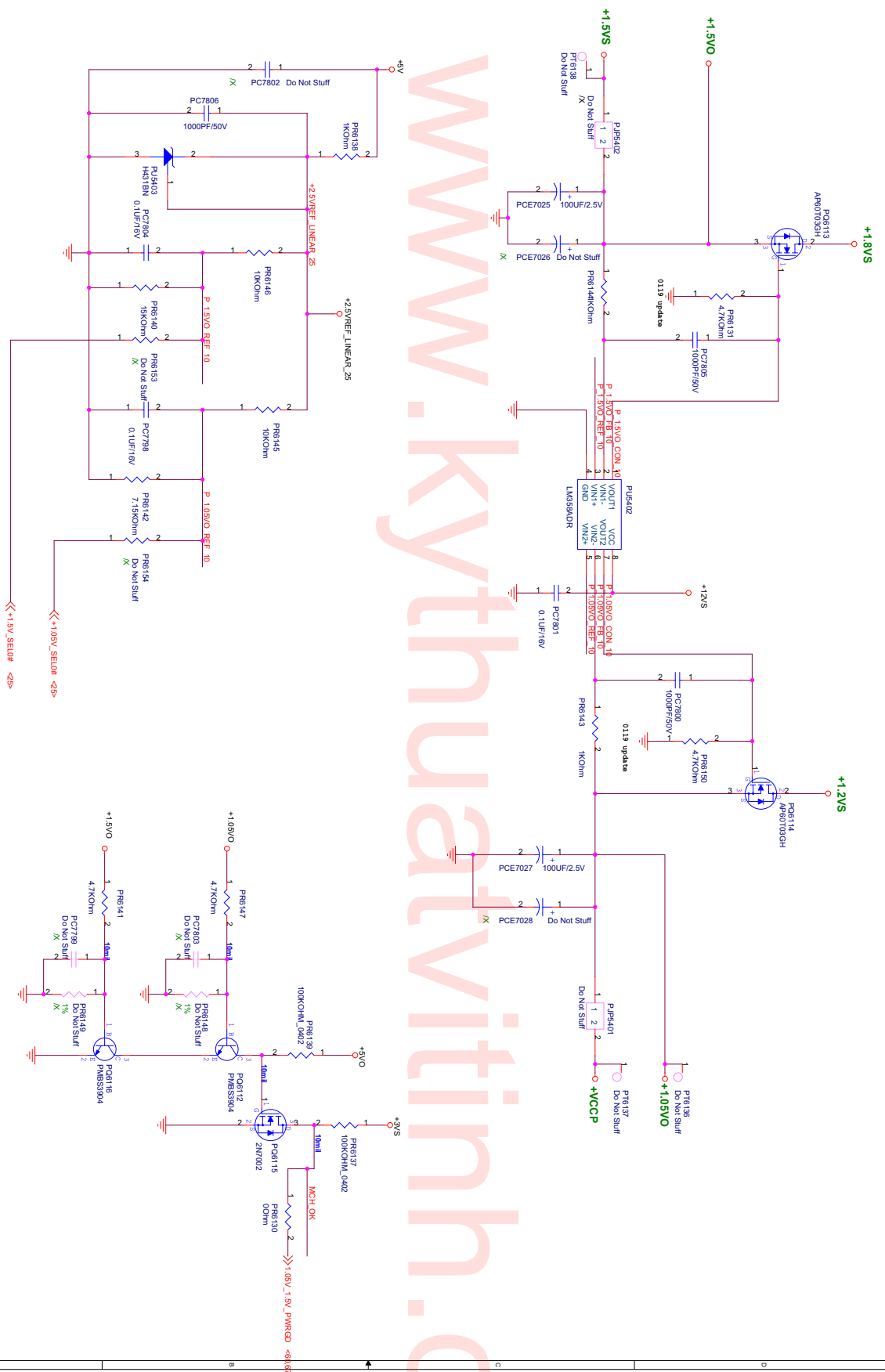
898

ASUS Title POWER IO_13V8 & 1.8V8

ASUSTek Computer, INC. Project Name: Z62Ha

Engineer: 1.1

Date: Thursday, September 27, 2007 Sheet: 58 of 70

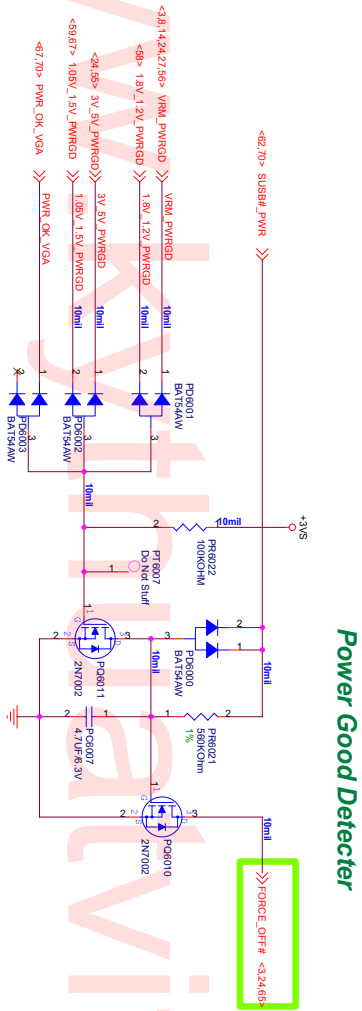


www.kytluati.com

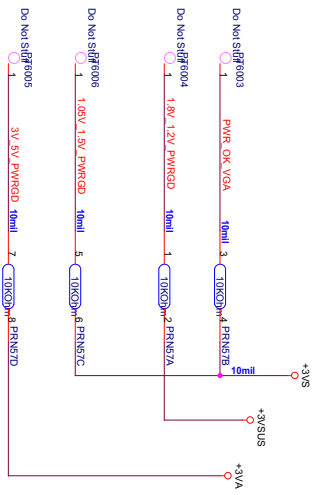
898

Title : POWER_I/O_+3VA & +2.5V

ASUSTeK Computer, Inc.
 Size: Project Name:
 Custom: 262Ha
 Engineer:
 Date: Thursday, September 27, 2007
 Sheet: 59 of 70
 Rev: 1.1




Power Good Detector

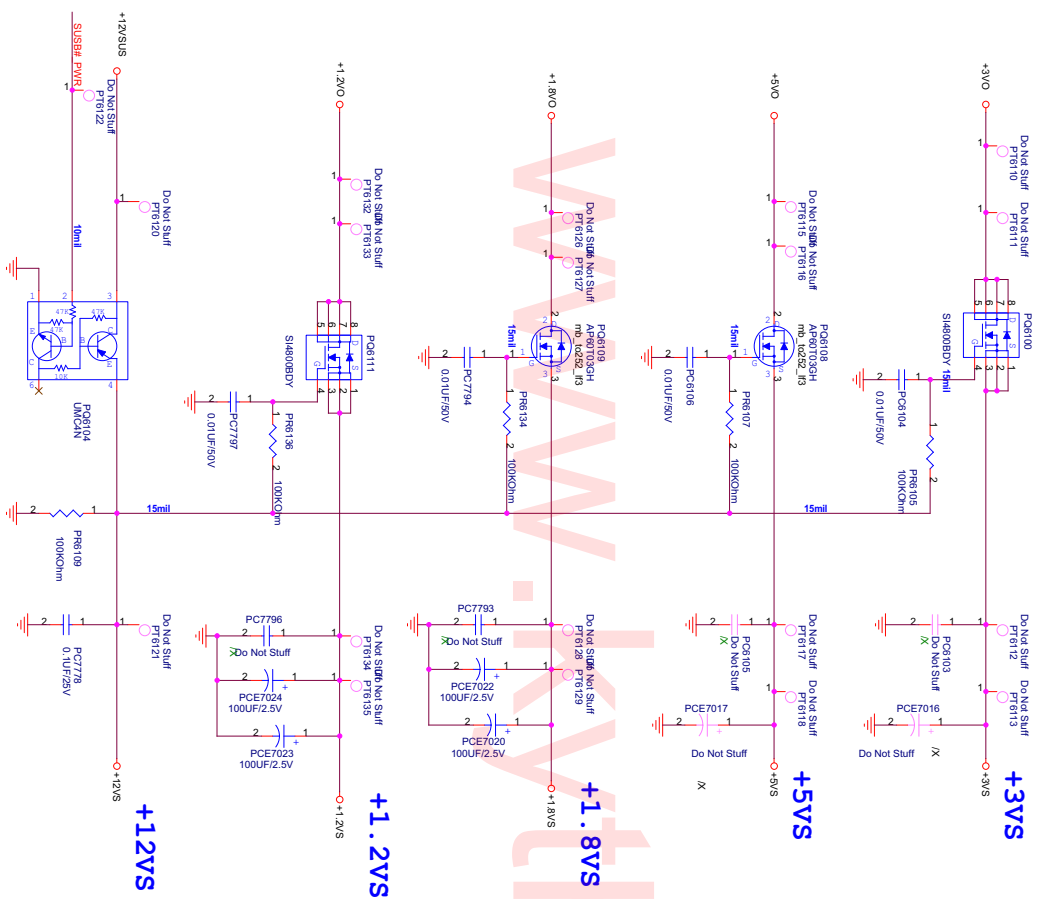


www.kythuatvitinh.com

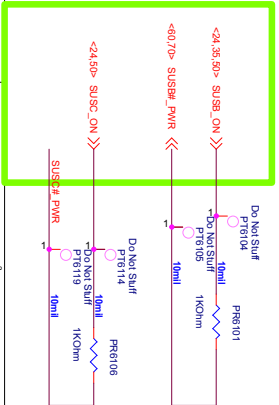
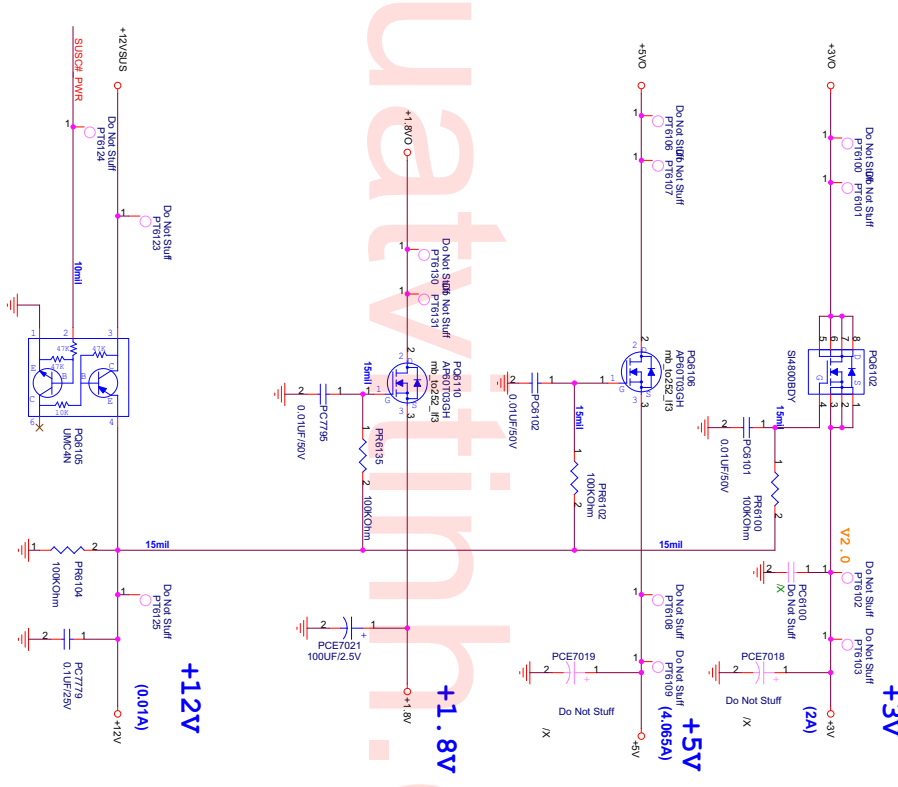
888

		Title : POWER BLANK	
Engineer:			
ASUSTek Computer INC.	Project Name		Rev
Size	Revision	262Ha	1.1
Date	Thursday, September 27, 2012	Sheet	41 of 70

SUSB#_PWR POWER



SUSC#_PWR POWER



888

ASUSTek Computer, Inc.
 Title : POWER_LOAD SWITCH
 Engineer:
 Z62Ha
 Date: Thursday, September 27, 2007 Sheet: 62 of 70 Rev: 1.1

www.kytnuatvitiinh.com

Rev	Date	Description
1.0	2007/02/14	1. Initial release.
1.1	2007/05/29	1. Change to SISM67.2, SIS968, SIS307

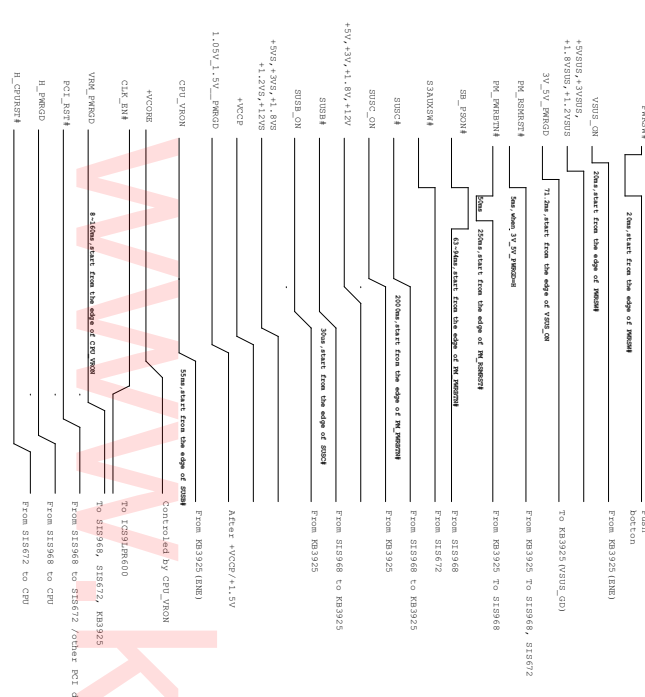
Rev	Date	Description
-----	------	-------------

388

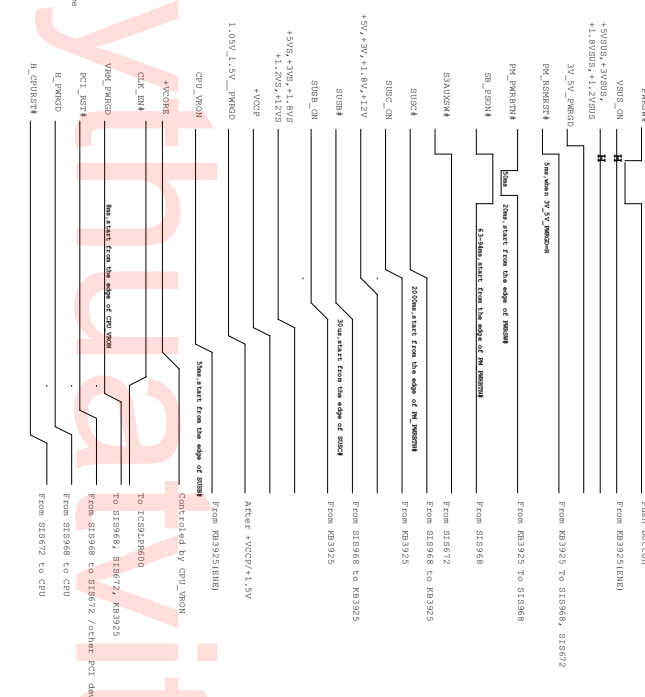


Title : History
ASUSTek Computer INC. **Engineer: Chihwan**
Size | Project Name
Custom | **Z62HA** | Rev
Date : Thursday, September 27, 2007 | Sheet 63 of 70

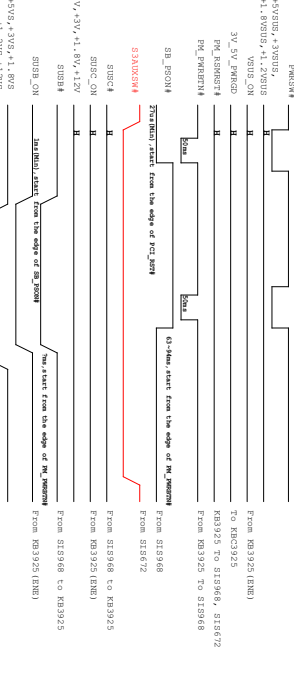
BATTERY ONLY POWER ON TIMING



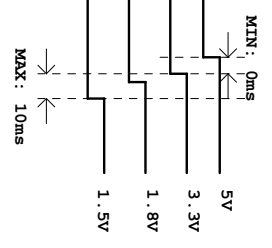
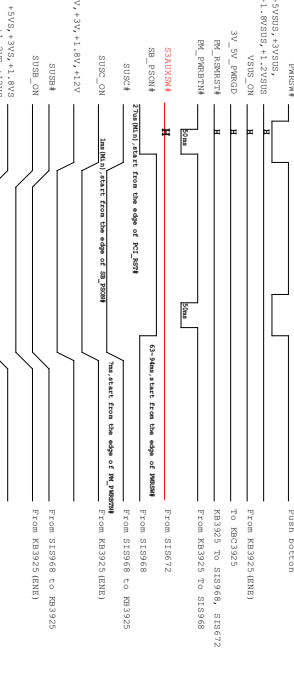
First Time DCIN power on sequence (Adaptor)



2628 S3 SUSPEND AND RESUME TIMING



2628 S4 SUSPEND AND RESUME TIMING



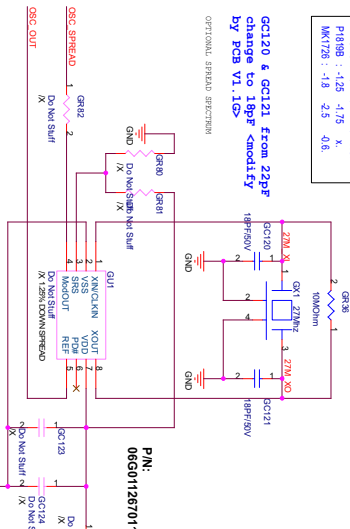
888

REV	A
DATE	2007-06-20
DOC	000001629
FILE	11-2007-06-20

1

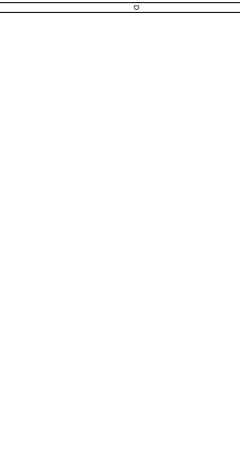
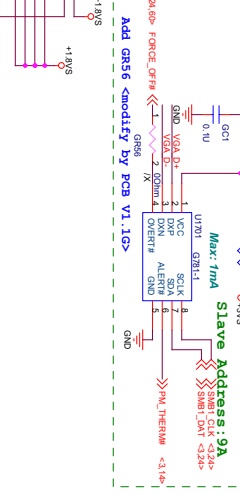
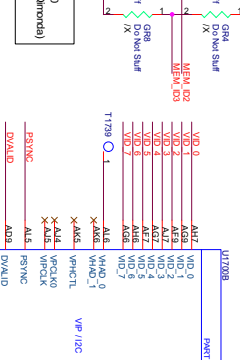
—SIS: 0 / 1 / KC
 P1818B: -1.25 -1.75 X
 M1725: -1.8 2.5 0.6

ADD GR26 100kOhm for
 27MHz On-Oscillator
 Smoother By PCB VI.1G>



PN: 066011267011

MEM_ID1 MEM_ID0
 0 0 -> RNF(NONONOhmna)
 0 1 -> Hynix



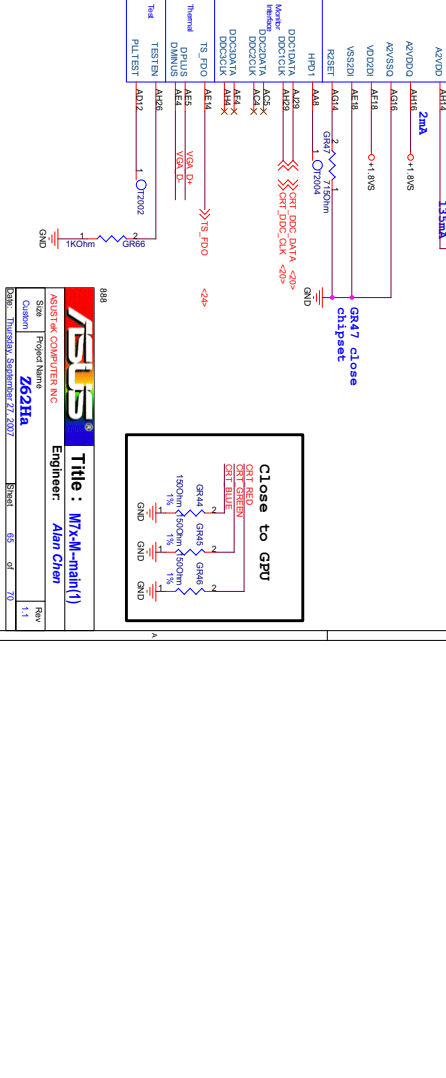
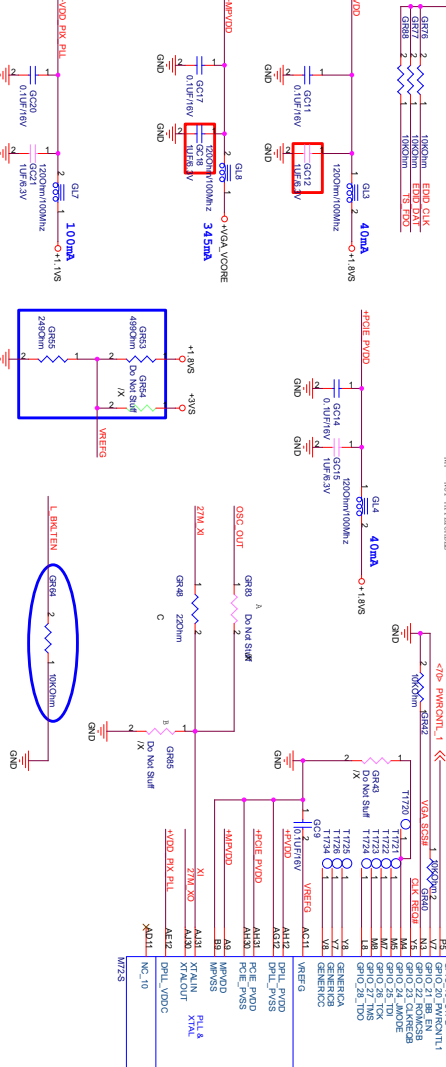
GR10(0): Tx Power Savings Enable
 0: GR10 Tx power savings enable
 1: full tx output swing (recommended) 1: Tx de-emphasis enable (default 0, internal pull-down)

GR10(1): Tx De-emphasis Enable
 0: GR10 Tx de-emphasis enable
 1: Tx de-emphasis enable (default 0, internal pull-down)

Pin	Demultiplexion	Hex	ATM	ATM	ATM
PT0	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT1	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT2	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT3	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT4	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT5	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT6	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT7	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT8	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT9	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT10	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT11	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT12	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT13	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT14	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT15	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT16	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT17	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT18	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT19	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT20	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT21	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT22	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT23	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT24	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT25	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT26	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT27	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT28	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT29	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT30	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT31	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT32	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT33	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT34	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT35	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT36	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT37	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT38	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT39	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT40	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT41	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT42	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT43	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT44	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT45	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT46	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT47	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT48	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT49	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT50	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT51	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT52	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT53	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT54	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT55	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT56	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT57	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT58	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT59	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT60	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT61	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT62	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT63	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT64	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT65	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT66	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT67	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT68	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT69	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT70	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT71	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT72	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT73	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT74	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT75	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT76	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT77	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT78	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT79	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT80	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT81	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT82	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT83	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT84	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT85	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT86	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT87	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT88	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT89	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT90	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT91	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT92	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT93	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT94	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT95	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT96	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT97	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT98	RESERVED STATE TRANSITION ENABLE	0	0	0	0
PT99	RESERVED STATE TRANSITION ENABLE	0	0	0	0

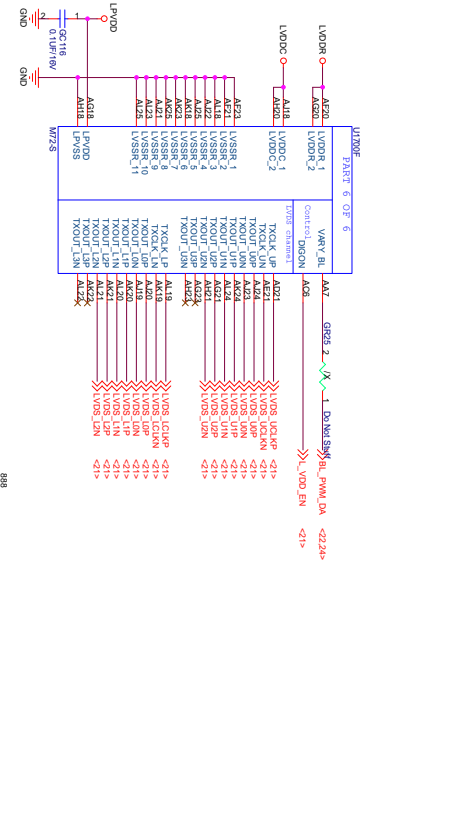
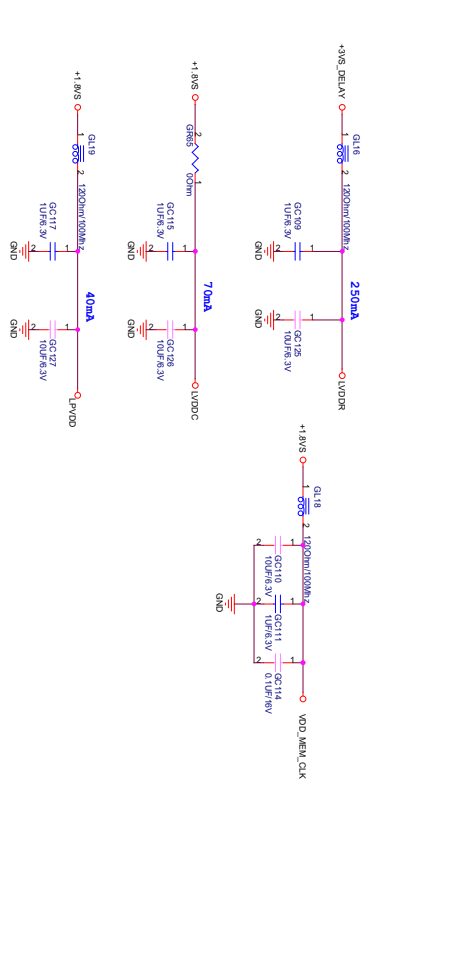
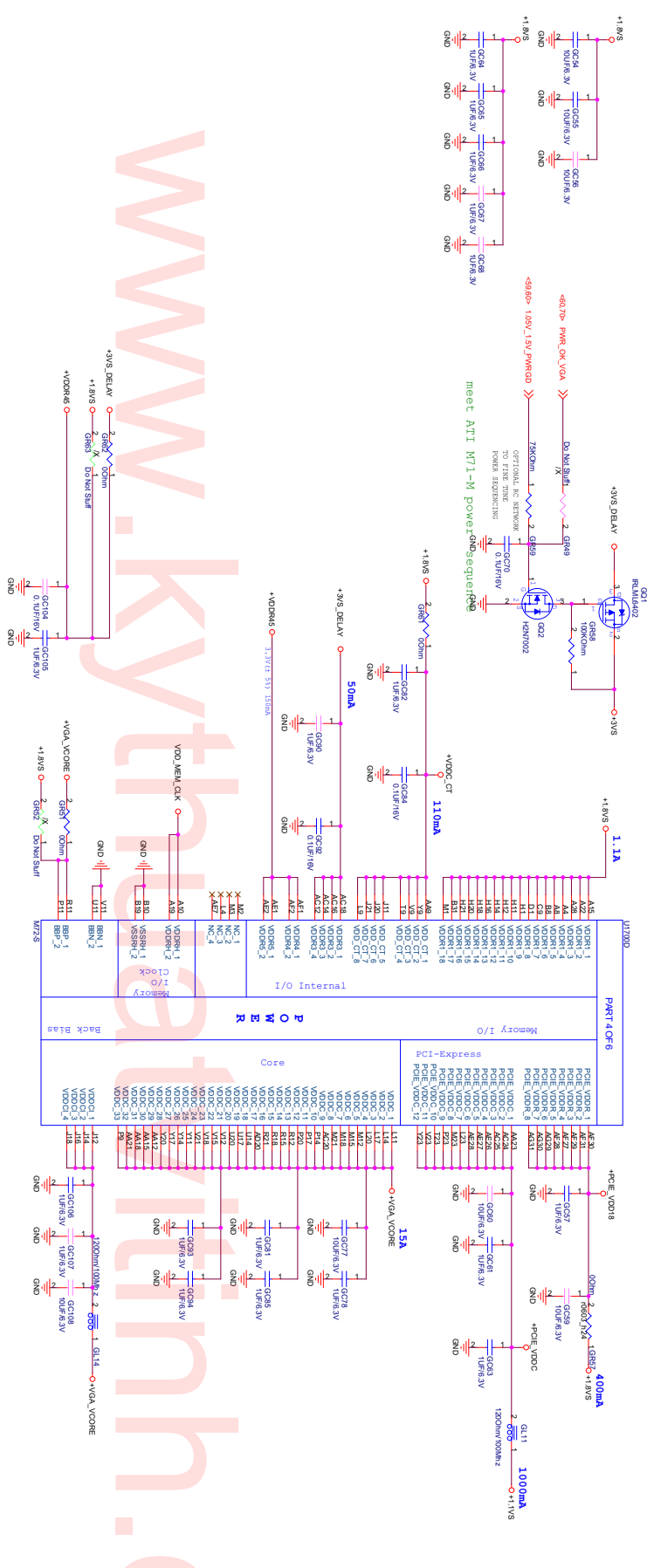
R1.1 Item 35

RECOMMENDED SETTINGS
 0 = DO NOT INSTALL RESISTOR
 1 = INSTALL 18K RESISTOR
 X = NOT RECOMMENDED
 N/A = NOT APPLICABLE



ASUS
 ASSISTANT COMPUTER INC
 Project Name: Z62Ha
 Engineer: Alan Chen
 Title: M7X-M-main(1)

Close to GPU
 GR1 RED
 GR2 BLUE
 GR3 BLUE
 GR4 BLUE
 GR5 BLUE
 GR6 BLUE
 GR7 BLUE
 GR8 BLUE
 GR9 BLUE
 GR10 BLUE
 GR11 BLUE
 GR12 BLUE
 GR13 BLUE
 GR14 BLUE
 GR15 BLUE
 GR16 BLUE
 GR17 BLUE
 GR18 BLUE
 GR19 BLUE
 GR20 BLUE
 GR21 BLUE
 GR22 BLUE
 GR23 BLUE
 GR24 BLUE
 GR25 BLUE
 GR26 BLUE
 GR27 BLUE
 GR28 BLUE
 GR29 BLUE
 GR30 BLUE
 GR31 BLUE
 GR32 BLUE
 GR33 BLUE
 GR34 BLUE
 GR35 BLUE
 GR36 BLUE
 GR37 BLUE
 GR38 BLUE
 GR39 BLUE
 GR40 BLUE
 GR41 BLUE
 GR42 BLUE
 GR43 BLUE
 GR44 BLUE
 GR45 BLUE
 GR46 BLUE
 GR47 BLUE
 GR48 BLUE
 GR49 BLUE
 GR50 BLUE
 GR51 BLUE
 GR52 BLUE
 GR53 BLUE
 GR54 BLUE
 GR55 BLUE
 GR56 BLUE
 GR57 BLUE
 GR58 BLUE
 GR59 BLUE
 GR60 BLUE
 GR61 BLUE
 GR62 BLUE
 GR63 BLUE
 GR64 BLUE
 GR65 BLUE
 GR66 BLUE
 GR67 BLUE
 GR68 BLUE
 GR69 BLUE
 GR70 BLUE
 GR71 BLUE
 GR72 BLUE
 GR73 BLUE
 GR74 BLUE
 GR75 BLUE
 GR76 BLUE
 GR77 BLUE
 GR78 BLUE
 GR79 BLUE
 GR80 BLUE
 GR81 BLUE
 GR82 BLUE
 GR83 BLUE
 GR84 BLUE
 GR85 BLUE
 GR86 BLUE
 GR87 BLUE
 GR88 BLUE
 GR89 BLUE
 GR90 BLUE
 GR91 BLUE
 GR92 BLUE
 GR93 BLUE
 GR94 BLUE
 GR95 BLUE
 GR96 BLUE
 GR97 BLUE
 GR98 BLUE
 GR99 BLUE
 GR100 BLUE



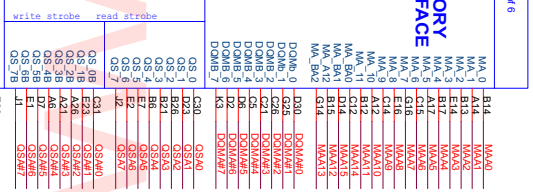
Pin	Signal	Value	Pin	Signal	Value
AV1	VDD0_1	1.8V	AV18	VDD0_18	1.8V
AV2	VDD0_2	1.8V	AV19	VDD0_19	1.8V
AV3	VDD0_3	1.8V	AV20	VDD0_20	1.8V
AV4	VDD0_4	1.8V	AV21	VDD0_21	1.8V
AV5	VDD0_5	1.8V	AV22	VDD0_22	1.8V
AV6	VDD0_6	1.8V	AV23	VDD0_23	1.8V
AV7	VDD0_7	1.8V	AV24	VDD0_24	1.8V
AV8	VDD0_8	1.8V	AV25	VDD0_25	1.8V
AV9	VDD0_9	1.8V	AV26	VDD0_26	1.8V
AV10	VDD0_10	1.8V	AV27	VDD0_27	1.8V
AV11	VDD0_11	1.8V	AV28	VDD0_28	1.8V
AV12	VDD0_12	1.8V	AV29	VDD0_29	1.8V
AV13	VDD0_13	1.8V	AV30	VDD0_30	1.8V
AV14	VDD0_14	1.8V	AV31	VDD0_31	1.8V
AV15	VDD0_15	1.8V	AV32	VDD0_32	1.8V
AV16	VDD0_16	1.8V	AV33	VDD0_33	1.8V
AV17	VDD0_17	1.8V	AV34	VDD0_34	1.8V

ASUSTek COMPUTER INC.
ASUS
 Title : MTX-M-POWER(3)
 Engineer: Alan Chen
 Project Name: 26218
 Date: Thursday, September 27, 2007
 Sheet: 07 of 71

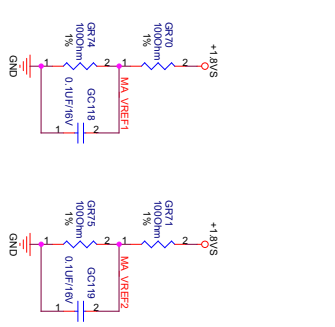
MDA03.01 <->

<-> MAA15.01 <-89-
 <-> DDMW7.01 <-89-
 <-> OSMW7.01 <-89-
 <-> OSMW7.01 <-89-

UT200C
 Part 3 of 6



MA_VREF1	E20	MA_0	B14	MAA0	<-89-
MA_VREF2	E21	MA_1	B15	MAA0	<-89-
		MA_2	E14	MAA0	<-89-
		MA_3	E14	MAA3	<-89-
		MA_4	B17	MAA4	<-89-
		MA_5	C15	MAA5	<-89-
		MA_6	C16	MAA6	<-89-
		MA_7	E16	MAA7	<-89-
		MA_8	C14	MAA8	<-89-
		MA_9	C14	MAA9	<-89-
		MA_10	A12	MAA10	<-89-
		MA_11	C12	MAA11	<-89-
		MA_12	C12	MAA12	<-89-
		MA_13	E21	MAA13	<-89-
		MA_14	B16	MAA14	<-89-
		MA_15	E18	MAA15	<-89-
		MA_BM2	B18	MAA17	<-89-
				MCA11	<-89-
				MCA12	<-89-
				MCA13	<-89-
				MCA14	<-89-
				MCA15	<-89-
				MCA16	<-89-
				MCA17	<-89-
				MCA18	<-89-
				MCA19	<-89-
				MCA20	<-89-
				MCA21	<-89-
				MCA22	<-89-
				MCA23	<-89-
				MCA24	<-89-
				MCA25	<-89-
				MCA26	<-89-
				MCA27	<-89-
				MCA28	<-89-
				MCA29	<-89-
				MCA30	<-89-
				MCA31	<-89-
				MCA32	<-89-
				MCA33	<-89-
				MCA34	<-89-
				MCA35	<-89-
				MCA36	<-89-
				MCA37	<-89-
				MCA38	<-89-
				MCA39	<-89-
				MCA40	<-89-
				MCA41	<-89-
				MCA42	<-89-
				MCA43	<-89-
				MCA44	<-89-
				MCA45	<-89-
				MCA46	<-89-
				MCA47	<-89-
				MCA48	<-89-
				MCA49	<-89-
				MCA50	<-89-
				MCA51	<-89-
				MCA52	<-89-
				MCA53	<-89-
				MCA54	<-89-
				MCA55	<-89-
				MCA56	<-89-
				MCA57	<-89-
				MCA58	<-89-
				MCA59	<-89-
				MCA60	<-89-
				MCA61	<-89-
				MCA62	<-89-
				MCA63	<-89-
				MCA64	<-89-
				MCA65	<-89-
				MCA66	<-89-
				MCA67	<-89-
				MCA68	<-89-
				MCA69	<-89-
				MCA70	<-89-
				MCA71	<-89-
				MCA72	<-89-
				MCA73	<-89-
				MCA74	<-89-
				MCA75	<-89-
				MCA76	<-89-
				MCA77	<-89-
				MCA78	<-89-
				MCA79	<-89-
				MCA80	<-89-
				MCA81	<-89-
				MCA82	<-89-
				MCA83	<-89-
				MCA84	<-89-
				MCA85	<-89-
				MCA86	<-89-
				MCA87	<-89-
				MCA88	<-89-
				MCA89	<-89-
				MCA90	<-89-
				MCA91	<-89-
				MCA92	<-89-
				MCA93	<-89-
				MCA94	<-89-
				MCA95	<-89-
				MCA96	<-89-
				MCA97	<-89-
				MCA98	<-89-
				MCA99	<-89-
				MCA100	<-89-



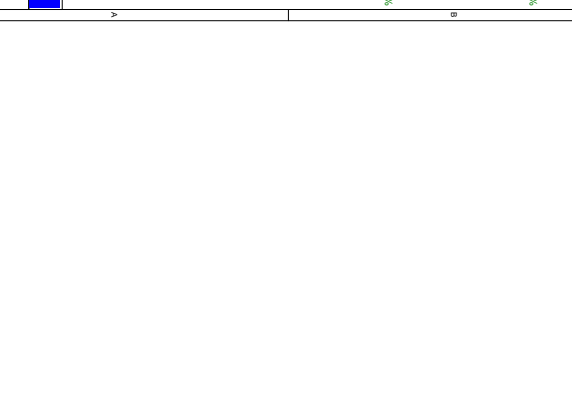
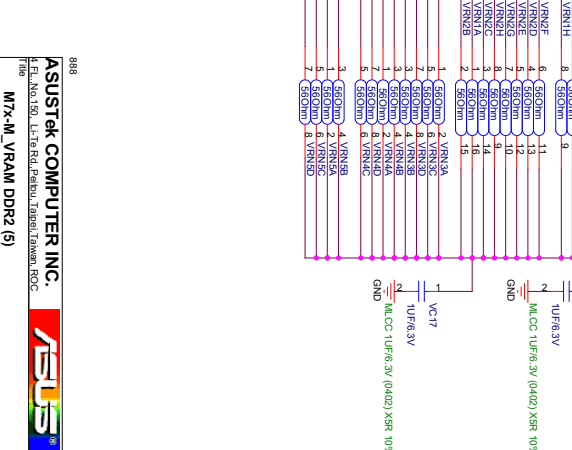
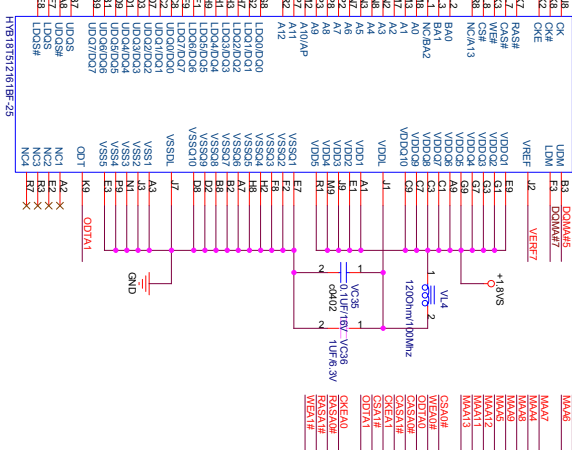
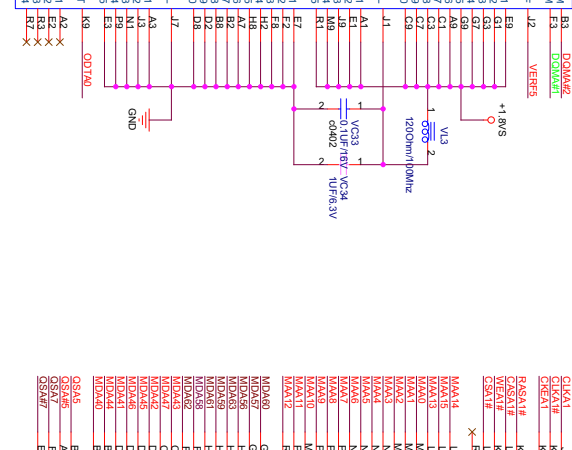
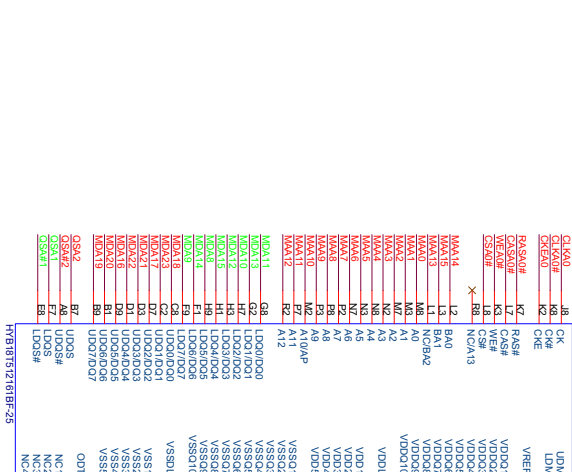
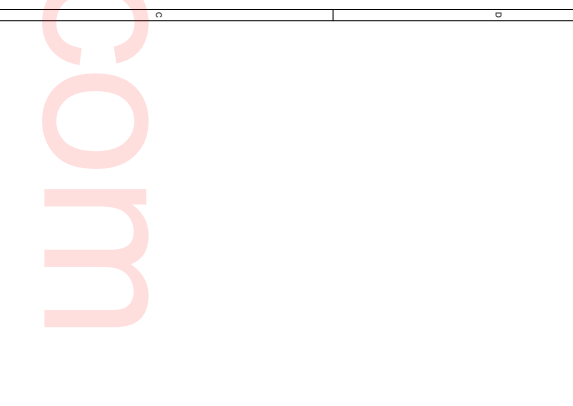
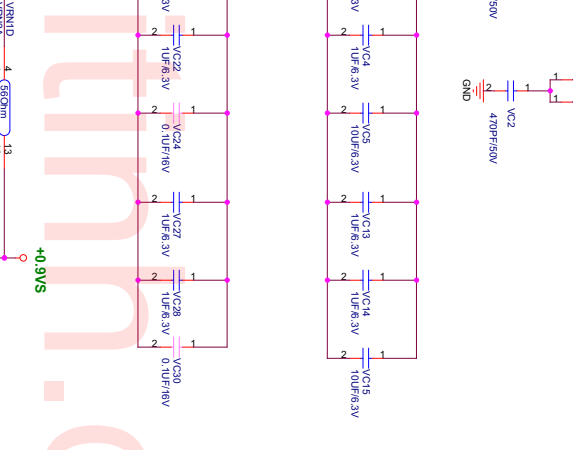
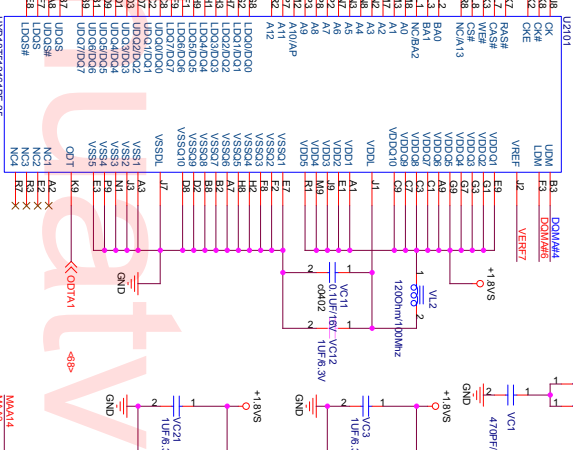
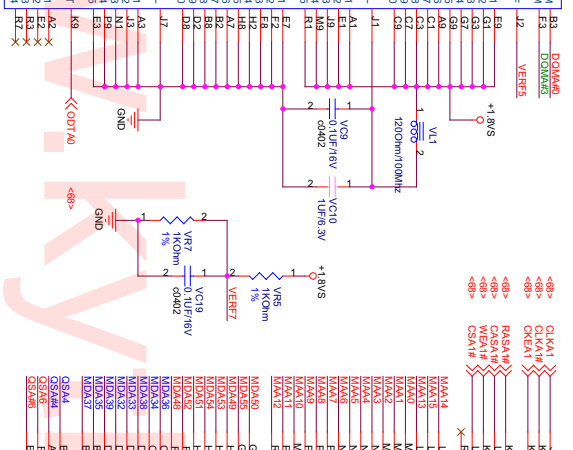
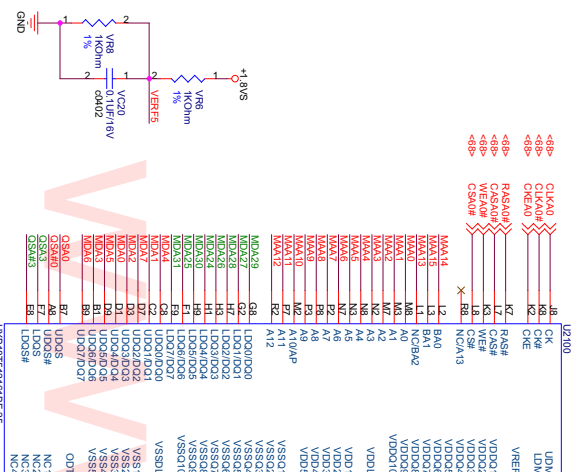
WREFD-S_L/VB

R ->+1.8VS	R ->GND
GDDR2 100	100
GDDR3 40.2	100

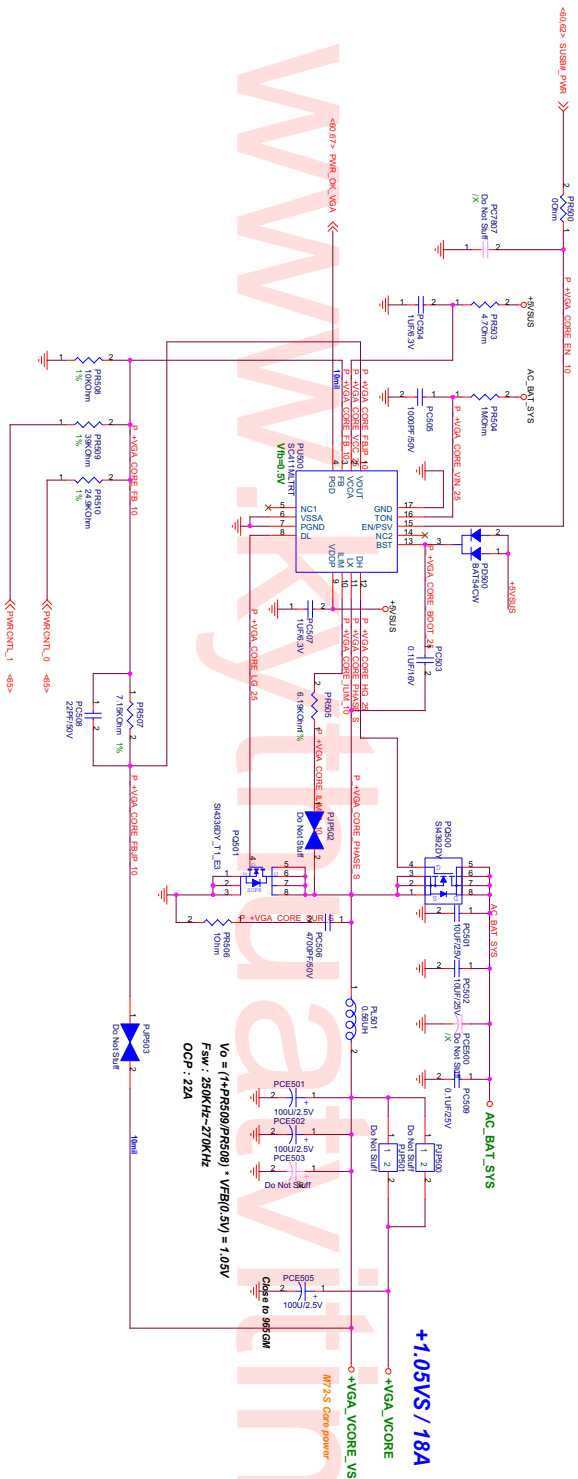
898

Title : MR-HL VRAM A(4)
 ASUSTeK COMPUTER INC
 Project Name : **Z62Ha**
 Engineer : **Alan Chen**

Size :
 Custom :
 Date : Thursday, September 27, 2007
 Sheet : 68 of 70
 Rev : 1.1



Enable Signal :
 Implement Intel 965GM -> PR902
 Implement M72-S Chipset -> PR900



$V_o = (1 + \frac{P9809}{P9808}) \cdot \frac{V_{FB}(0.5V)}{1.05V}$
 $F_{sw} : 250KHz - 270KHz$
 $OCP : 22A$

+1.05VS

VOMCH_SELO	VOMCH_SEL1	Voltage
L	L	1.093V
X	L	1.001V
L	X	0.949V
X	X	0.857V