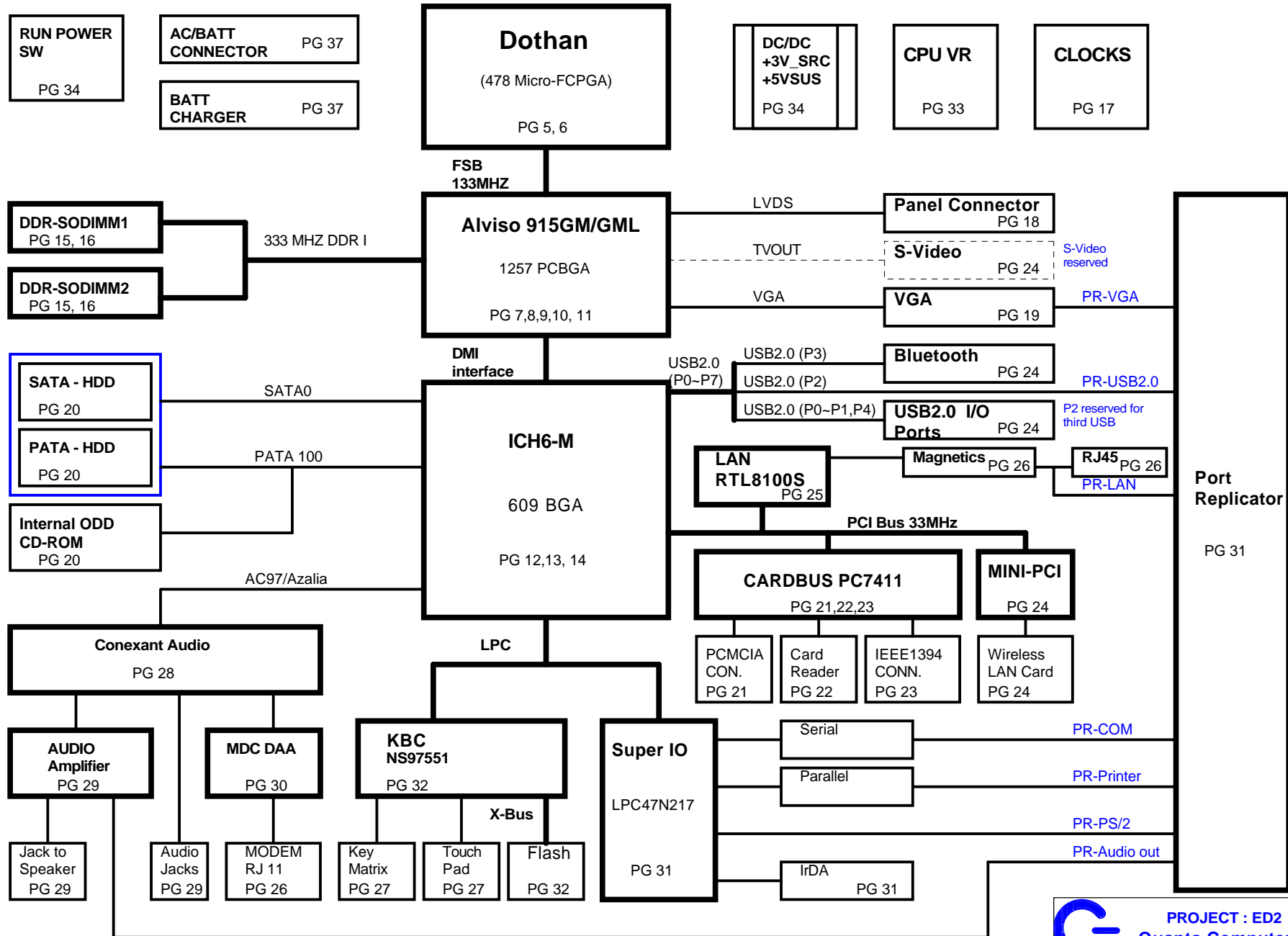


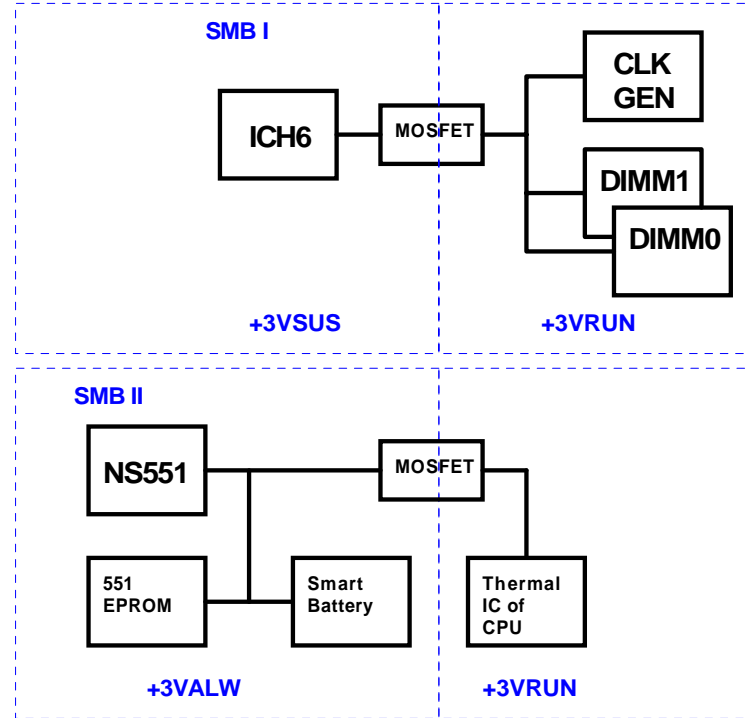
ED2-UMA DESIGN

VER : 1C



PROJECT : ED2
Quanta Computer Inc.

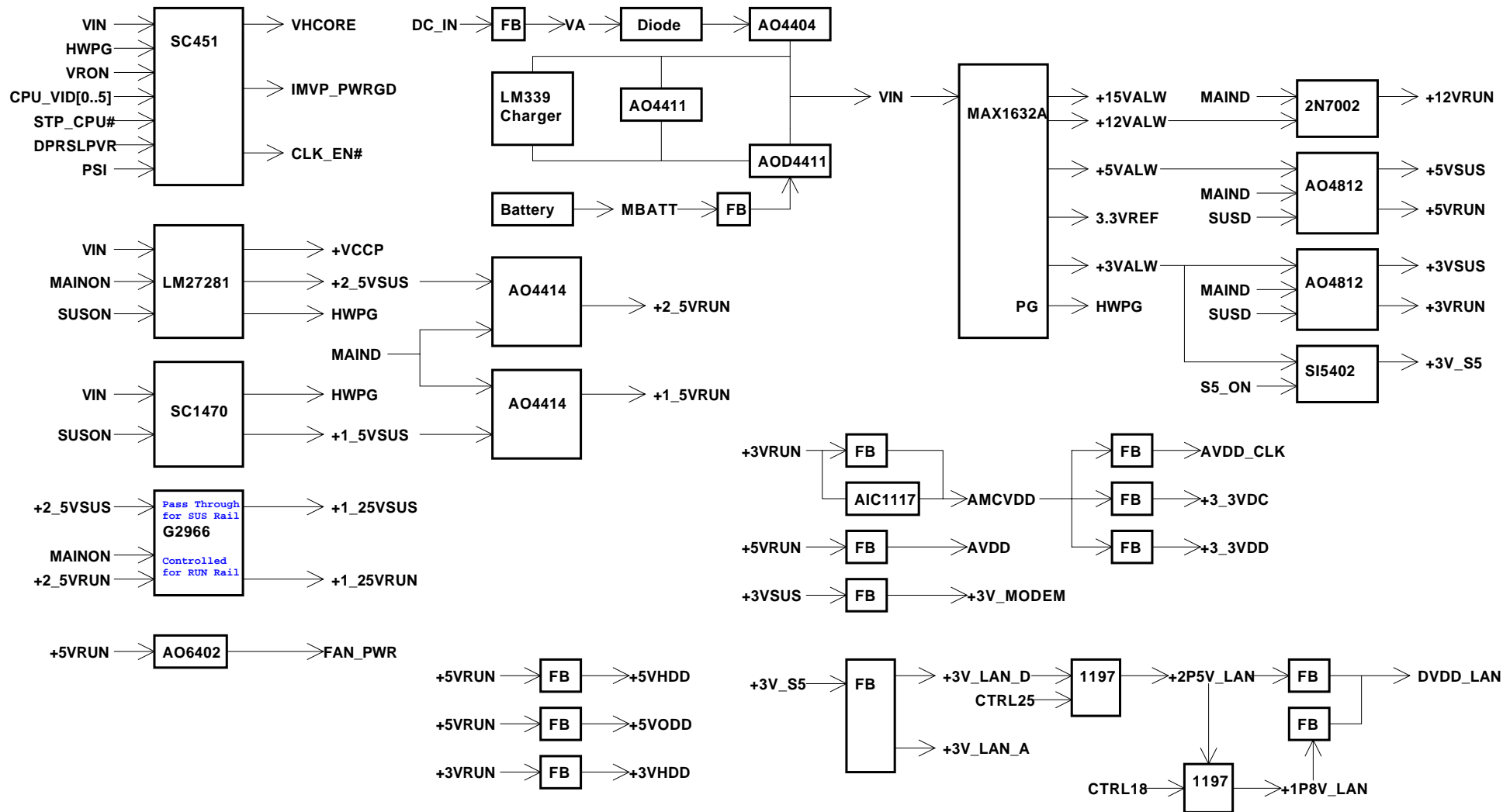
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD24	PIRQA#	RTL8110S
REQ2# / GNT2#	AD19	PIRQB# , PIRQD#	MINI-PCI
REQ1# / GNT1#	AD17	PIRQC#,PIRQD#,PIRQA#	TI 7411



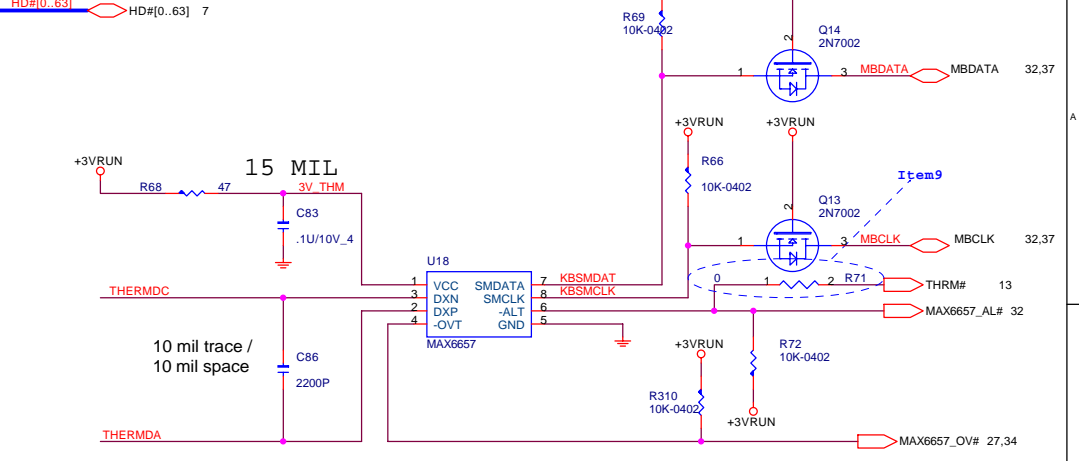
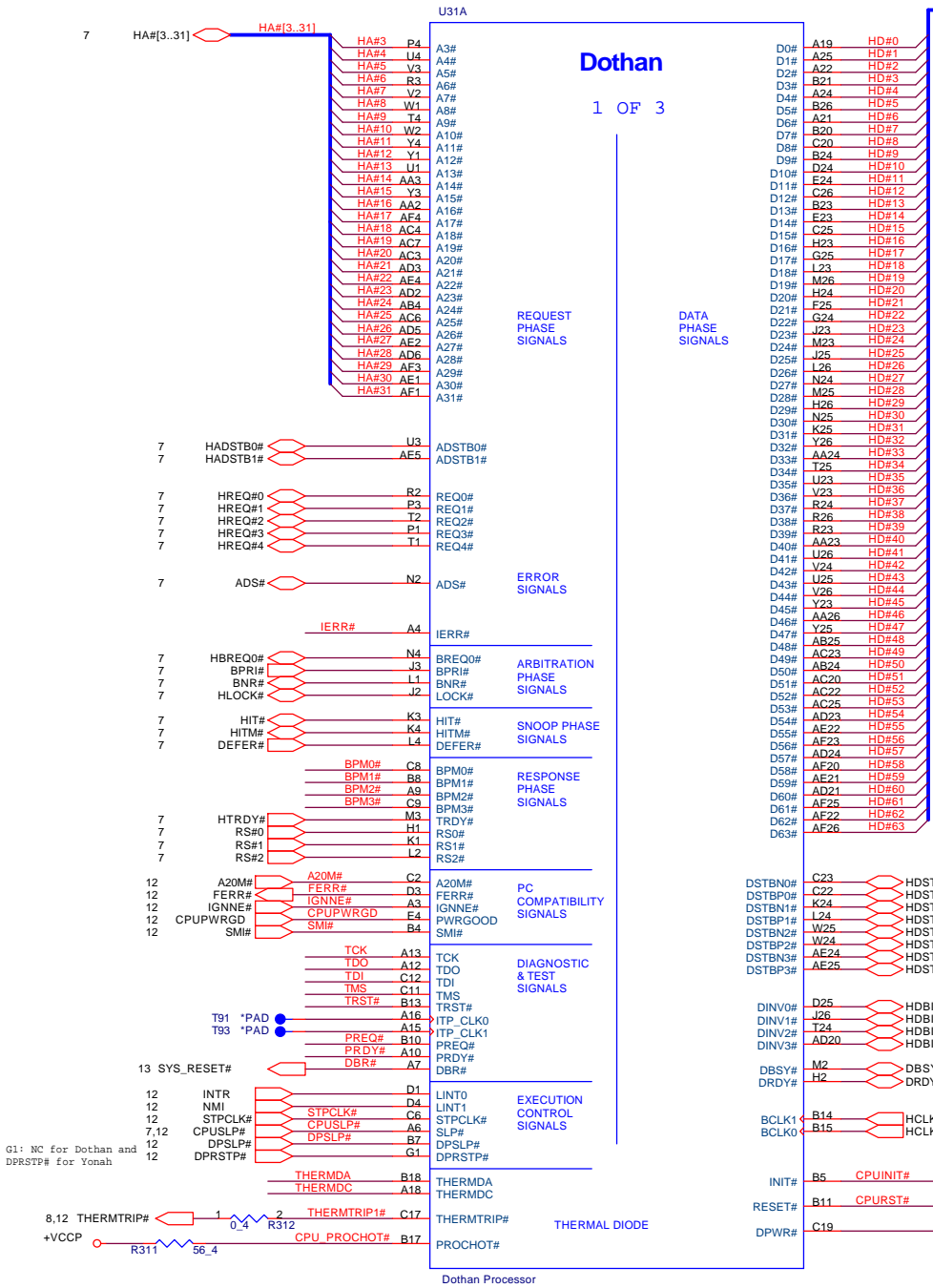
PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram 2	C2A
Date:	Friday, October 22, 2004	Sheet 2 of 38

Power Rail Flow

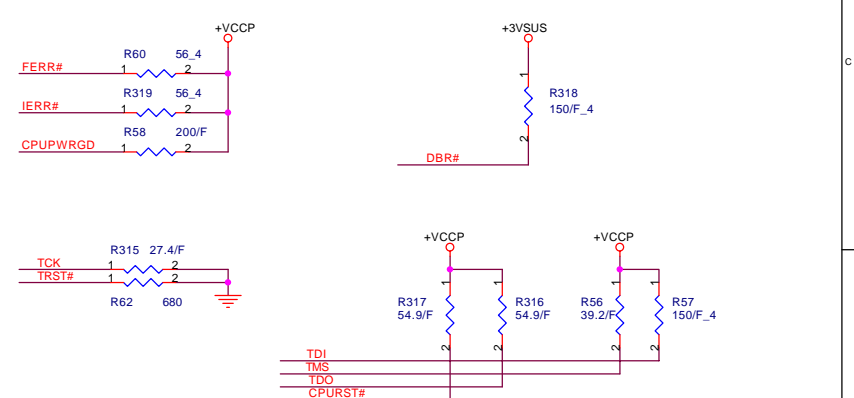


CT_0505: Change footprint to BGA479M-SOCKET from L100505 from MPGA479M



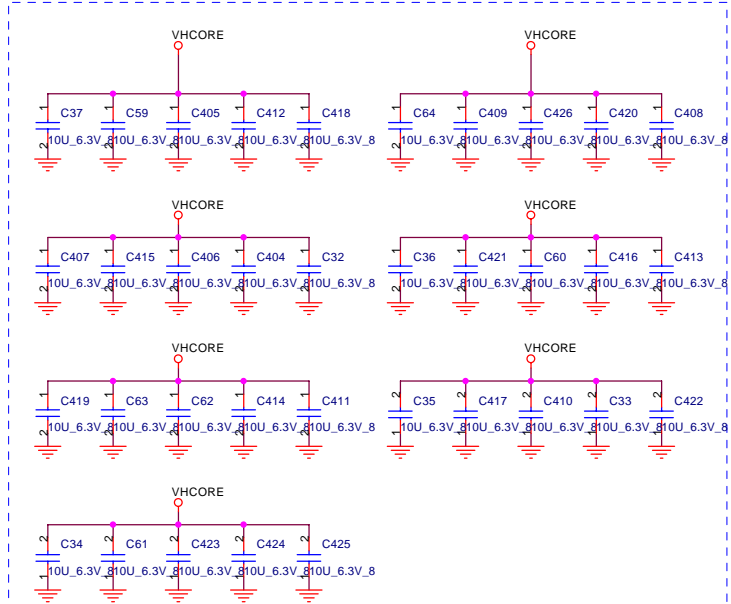
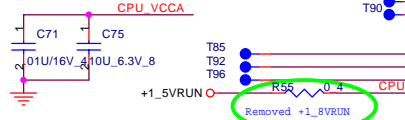
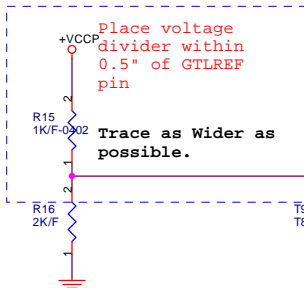
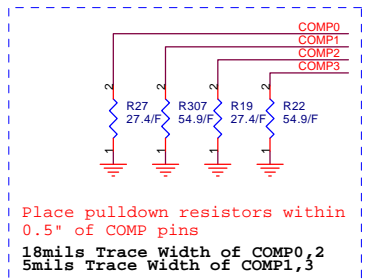
ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU

Note: Populate R58, R62 when ITP connector is populated.

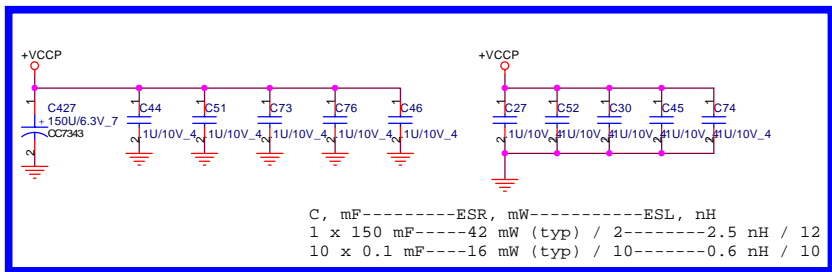


PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	Dothan (HOST)	C2A
Date:	Friday, October 22, 2004	Sheet 5 of 38



VHCORE
 Total caps = 1670 uF > 1430 uF (Intel Recommendation)
 ESR = 9m ohm/4 // 5m ohm/35 ---> = 0.1343m ohm



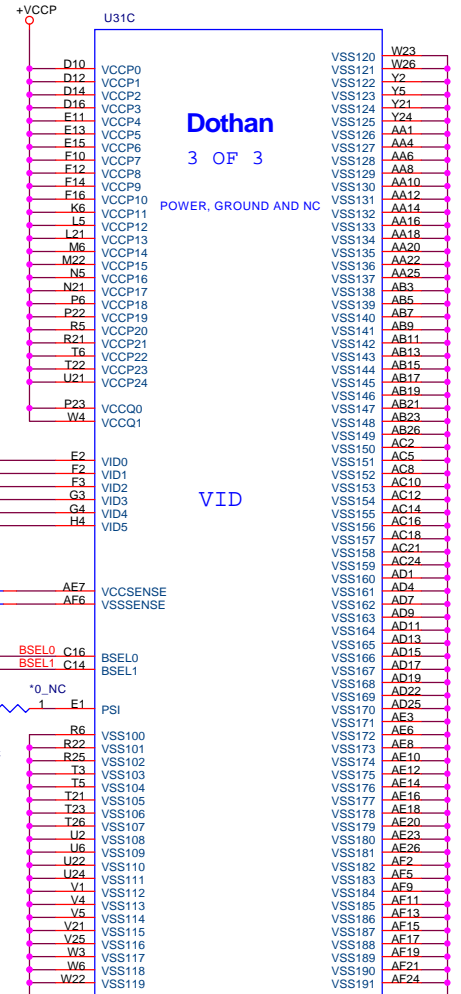
C, mF	ESR, mW	ESL, nH
1 x 150 mF	42 mW (typ)	2.5 nH / 12
10 x 0.1 mF	16 mW (typ)	0.6 nH / 10

U31B	U31C
COMP0 P25	VSS00 A2
COMP1 P26	VSS01 A5
COMP2 AB2	VSS02 A8
COMP3 AB1	VSS03 A11
	VSS04 A14
	VSS05 A17
	VSS06 A20
	VSS07 A23
	VSS08 A26
	VSS09 B3
	VSS10 B6
	VSS11 B9
	VSS12 B12
	VSS13 B16
	VSS14 B19
	VSS15 B22
	VSS16 B25
	VSS17 C1
	VSS18 C4
	VSS19 C7
	VSS20 C10
	VSS21 C13
	VSS22 C15
	VSS23 C18
	VSS24 C21
	VSS25 C24
	VSS26 D2
	VSS27 D5
	VSS28 D7
	VSS29 D9
	VSS30 D11
	VSS31 D13
	VSS32 D15
	VSS33 D17
	VSS34 D19
	VSS35 D21
	VSS36 D23
	VSS37 D26
	VSS38 E3
	VSS39 E6
	VSS40 E8
	VSS41 E10
	VSS42 E12
	VSS43 E14
	VSS44 E16
	VSS45 E20
	VSS46 E22
	VSS47 E25
	VSS48 F1
	VSS49 F4
	VSS50 F5
	VSS51 F7
	VSS52 F9
	VSS53 F11
	VSS54 F13
	VSS55 F15
	VSS56 F17
	VSS57 F19
	VSS58 F21
	VSS59 F24
	VSS60 G2
	VSS61 G6
	VSS62 G22
	VSS63 G23
	VSS64 G26
	VSS65 H3
	VSS66 H5
	VSS67 H21
	VSS68 H25
	VSS69 J1
	VSS70 J4
	VSS71 J6
	VSS72 J22
	VSS73 J24
	VSS74 K2
	VSS75 K5
	VSS76 K21
	VSS77 K23
	VSS78 K26
	VSS79 L3
	VSS80 L25
	VSS81 L6
	VSS82 L22
	VSS83 M1
	VSS84 M4
	VSS85 M5
	VSS86 M21
	VSS87 M24
	VSS88 N3
	VSS89 N6
	VSS90 N22
	VSS91 N23
	VSS92 N26
	VSS93 P2
	VSS94 P5
	VSS95 P21
	VSS96 P24
	VSS97 R1
	VSS98 R4
	VSS99

Dothan
 2 OF 3

POWER, GROUND, RESERVED SIGNALS

Dothan Processor

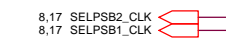
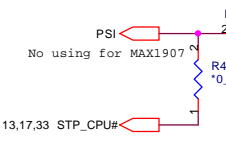
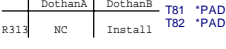
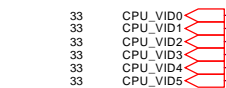


Dothan
 3 OF 3

POWER, GROUND AND NC

VID

Dothan Processor

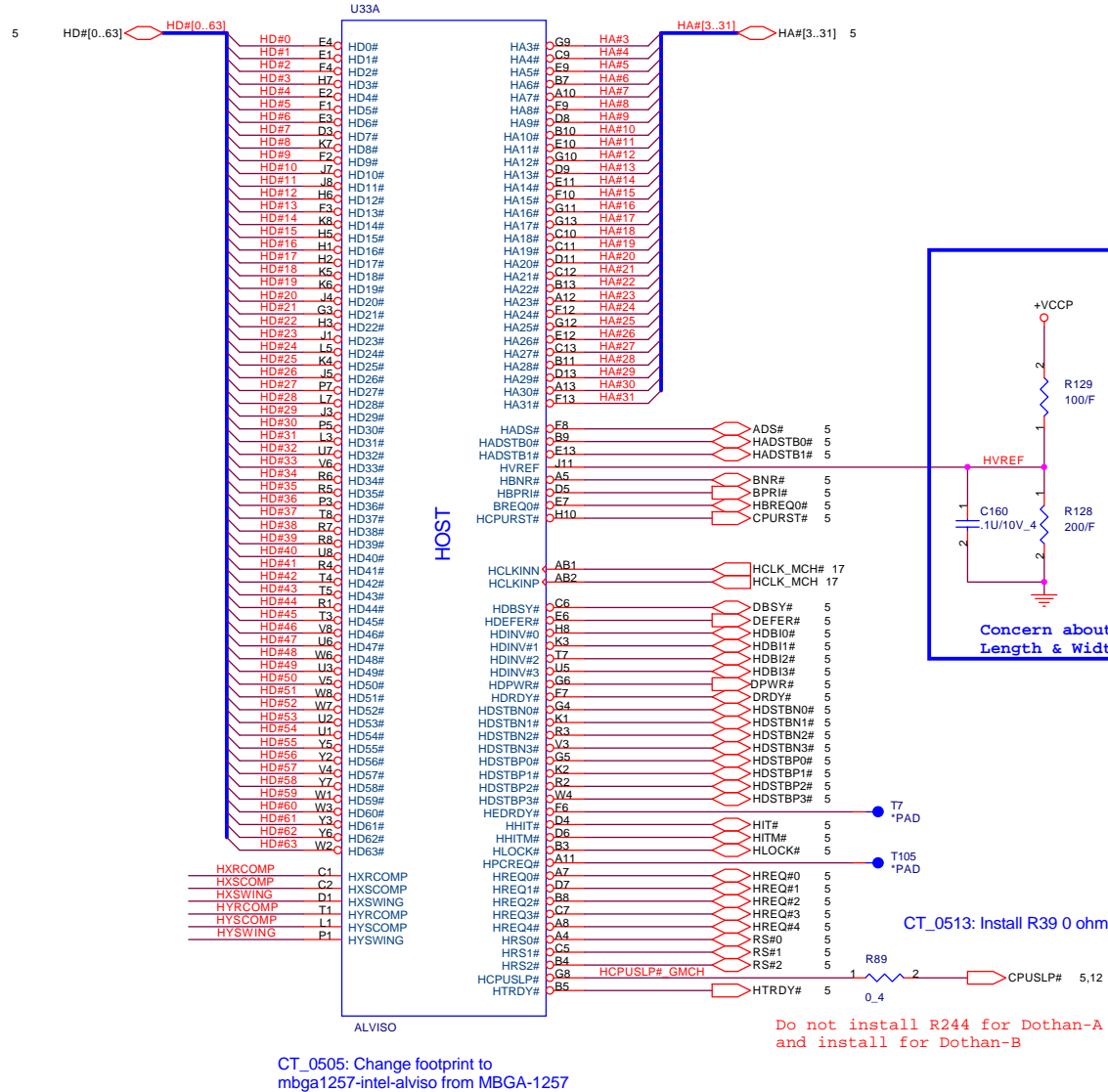
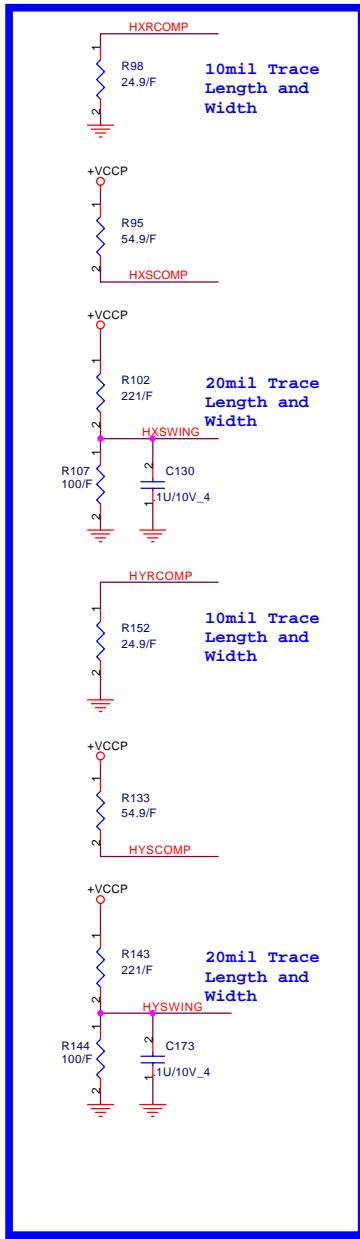


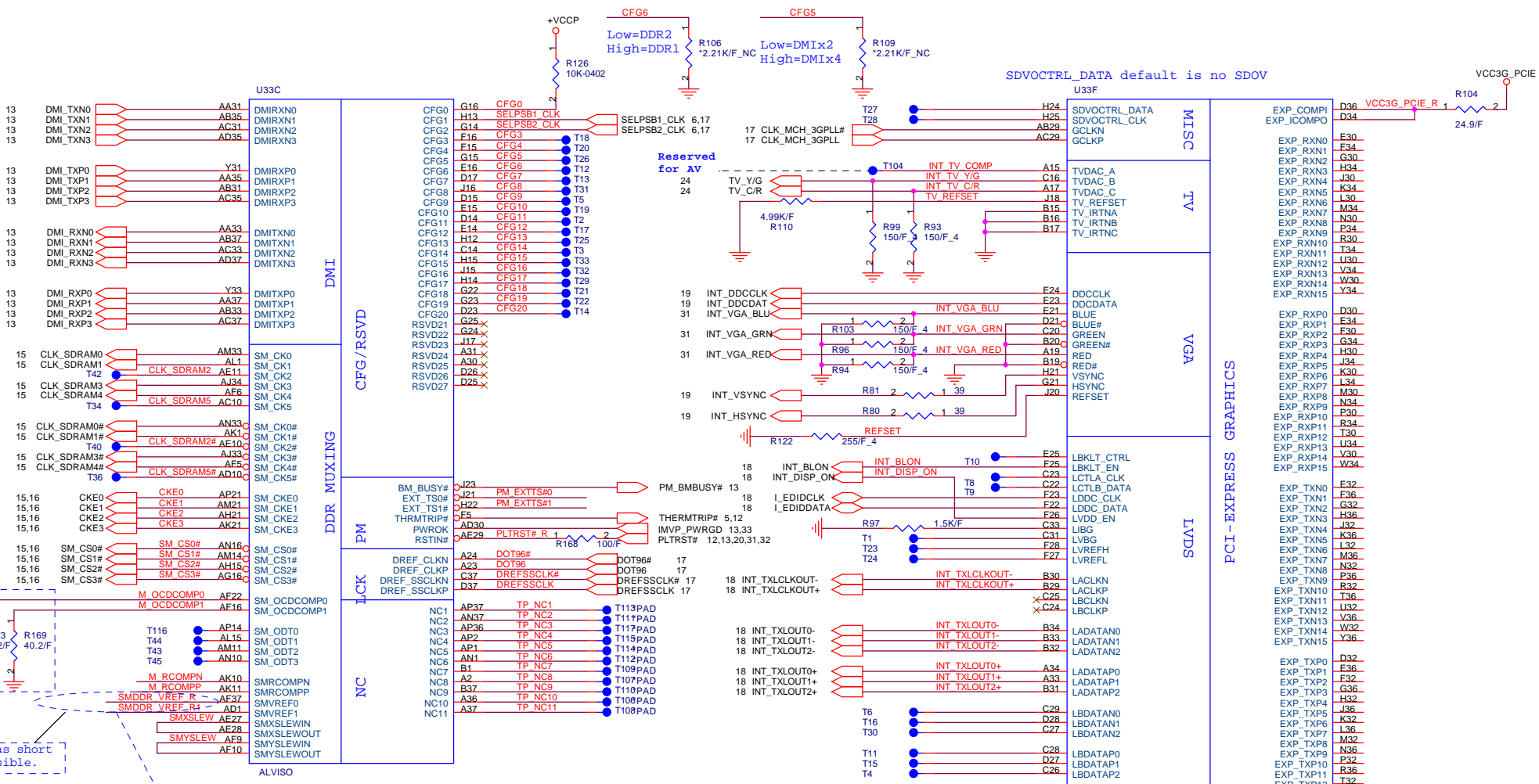
13,17,33 STP_CPU#



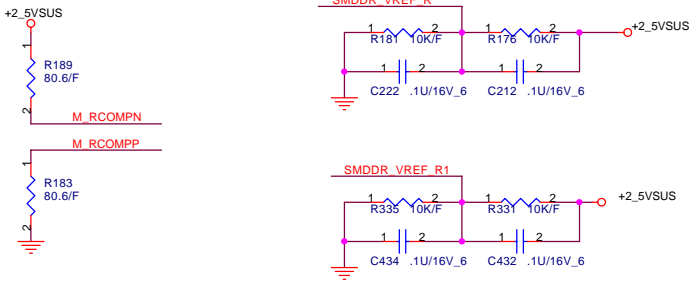
PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	Dothan (Power)	C2A
Date:	Friday, October 22, 2004	Sheet 6 of 38






It's point to point, 55ohm trace, keep as short as possible. close Alviso.



System memory throttling using

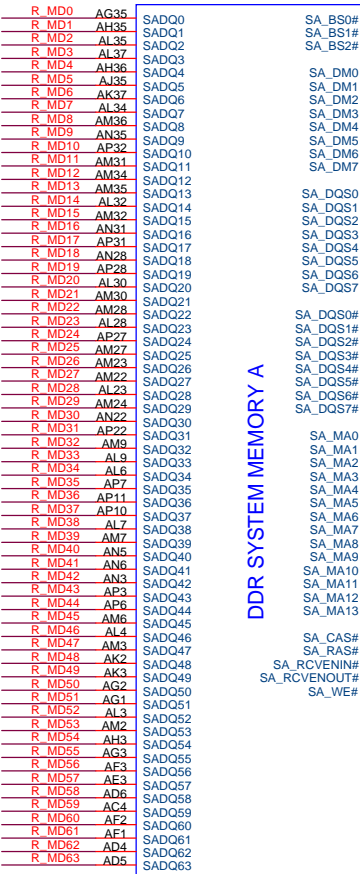
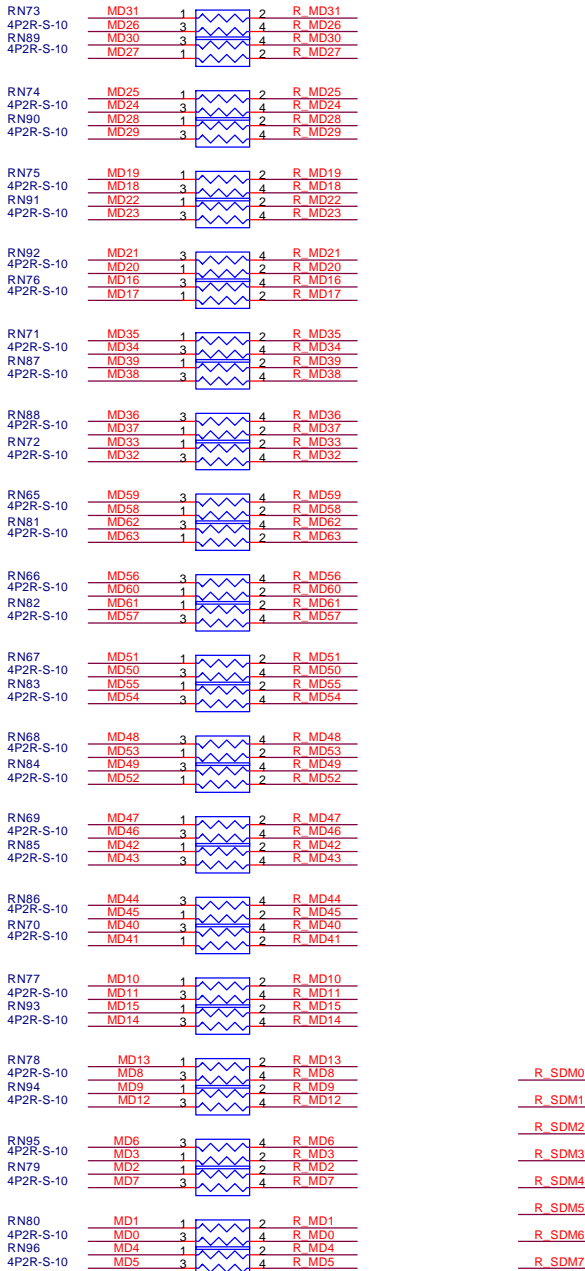


PROJECT : ED2
Quanta Computer Inc.

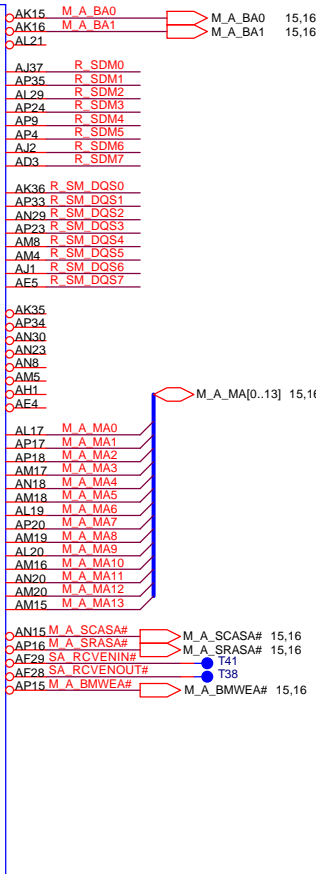
Size	Document Number	Rev
	Alviso (VGA, DMI)	C2A
Date:	Friday, October 22, 2004	Sheet 8 of 38

MD[0..63] 15,16
 SM_DQS[0..7] 15,16
 SDM[0..7] 15,16

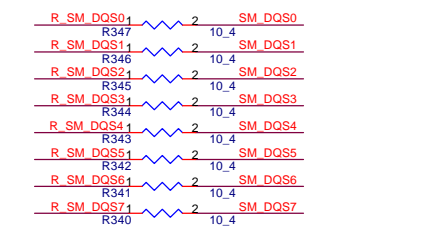
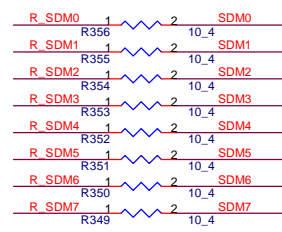
U33B



DDR SYSTEM MEMORY A



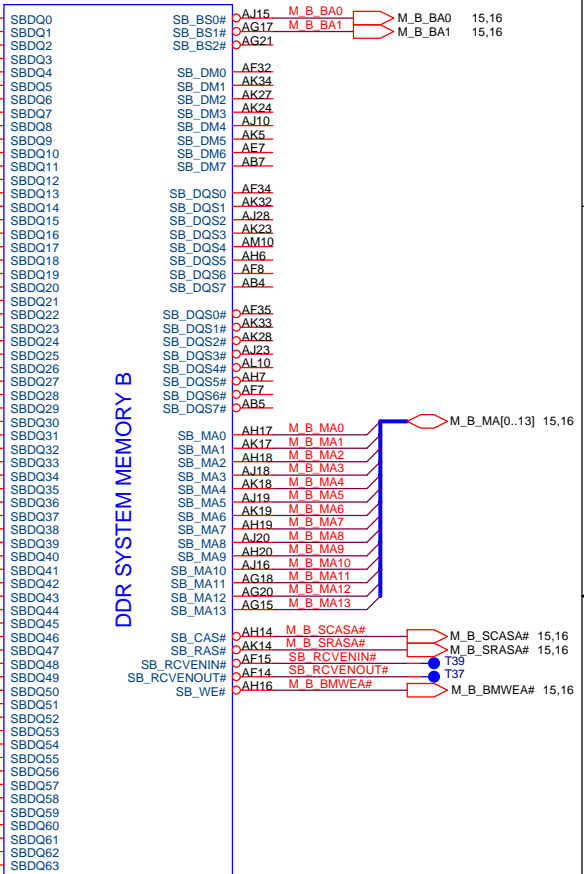
ALVISO



U33G

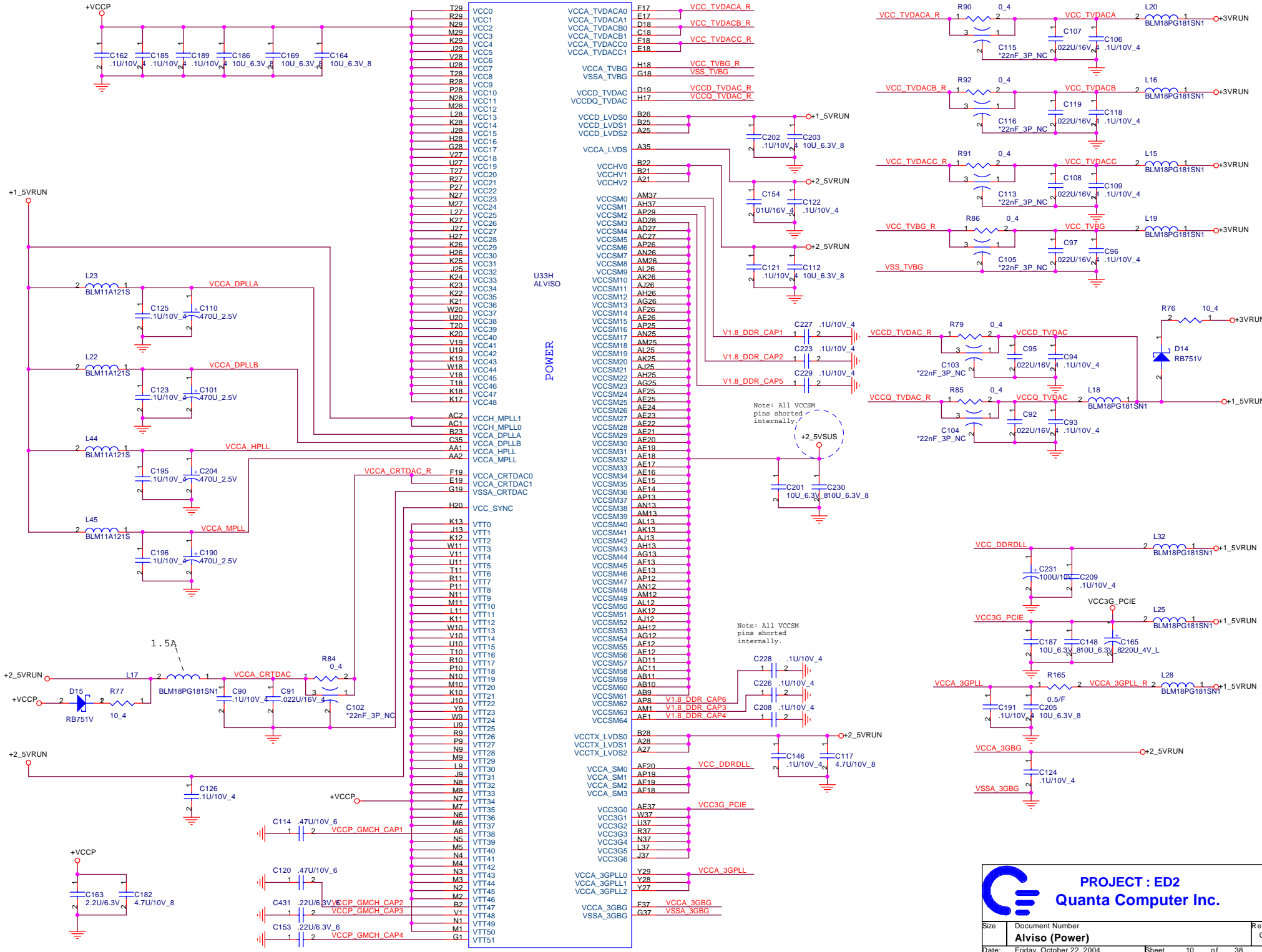



DDR SYSTEM MEMORY B

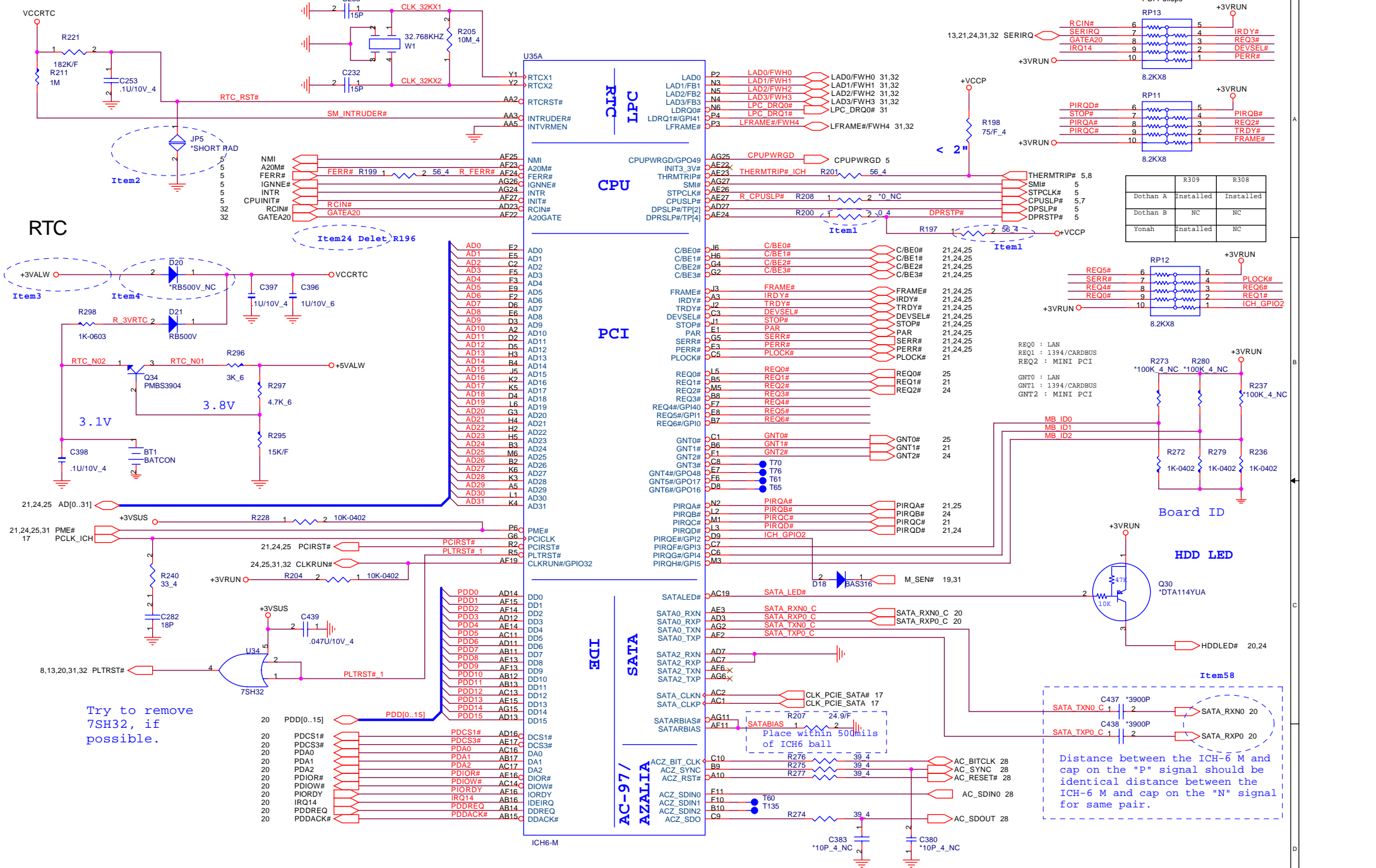


ALVISO





 PROJECT : ED2 Quanta Computer Inc.		
Date: Friday, October 22, 2004		Sheet 10 of 38



RTC

RTC

CPU

PCI

IDE

SATA

AC-97 / AZALIA



PROJECT : ED2
Quanta Computer Inc.

Try to remove 7SH32, if possible.

Distance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

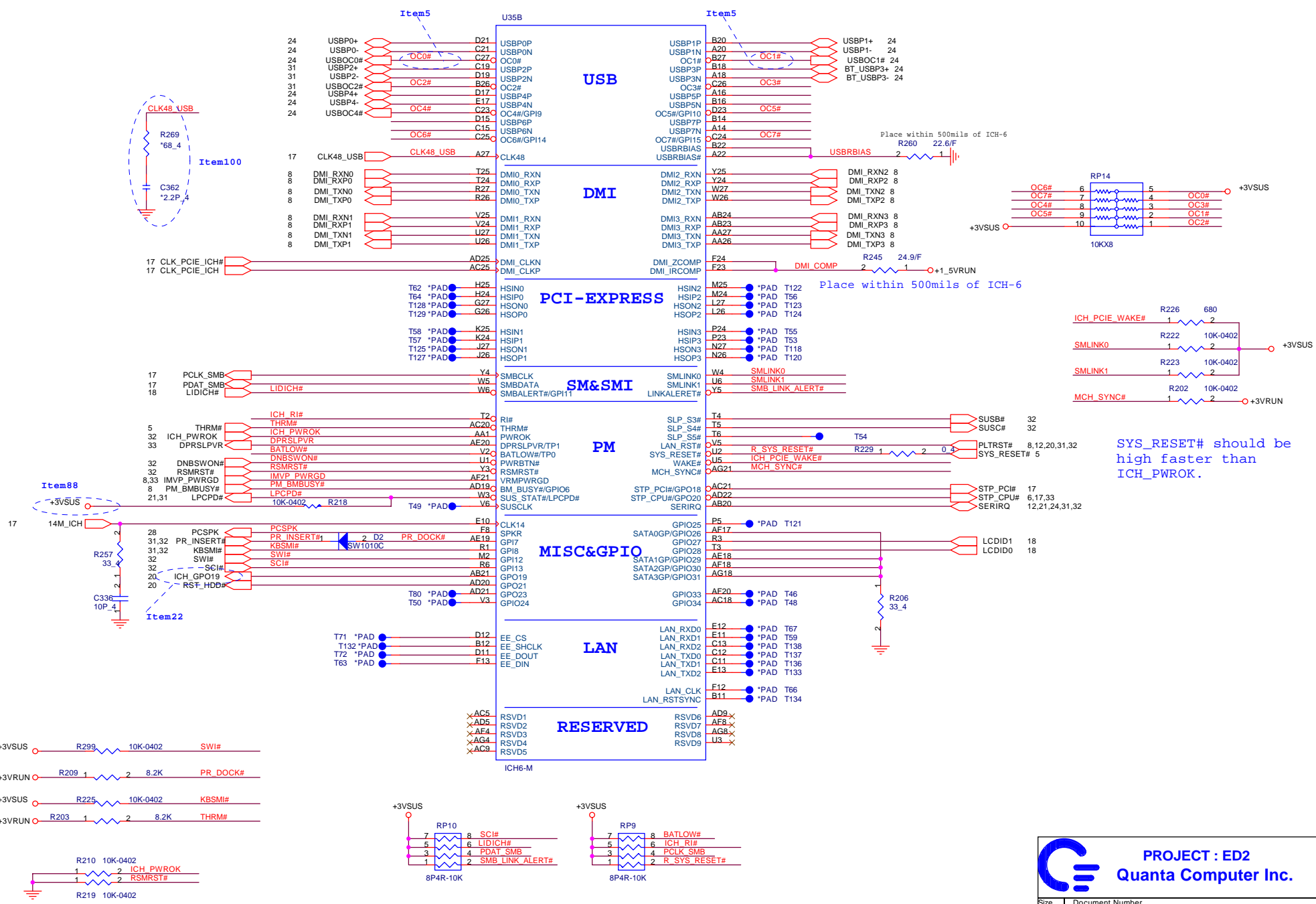
	R309	R308
Dothan A	Installed	Installed
Dothan B	NC	NC
Yonah	Installed	NC

REQ0 : LAN
 REQ1 : 1394/CARDBUS
 REQ2 : MINI PCI
 GNT0 : LAN
 GNT1 : 1394/CARDBUS
 GNT2 : MINI PCI

Board ID

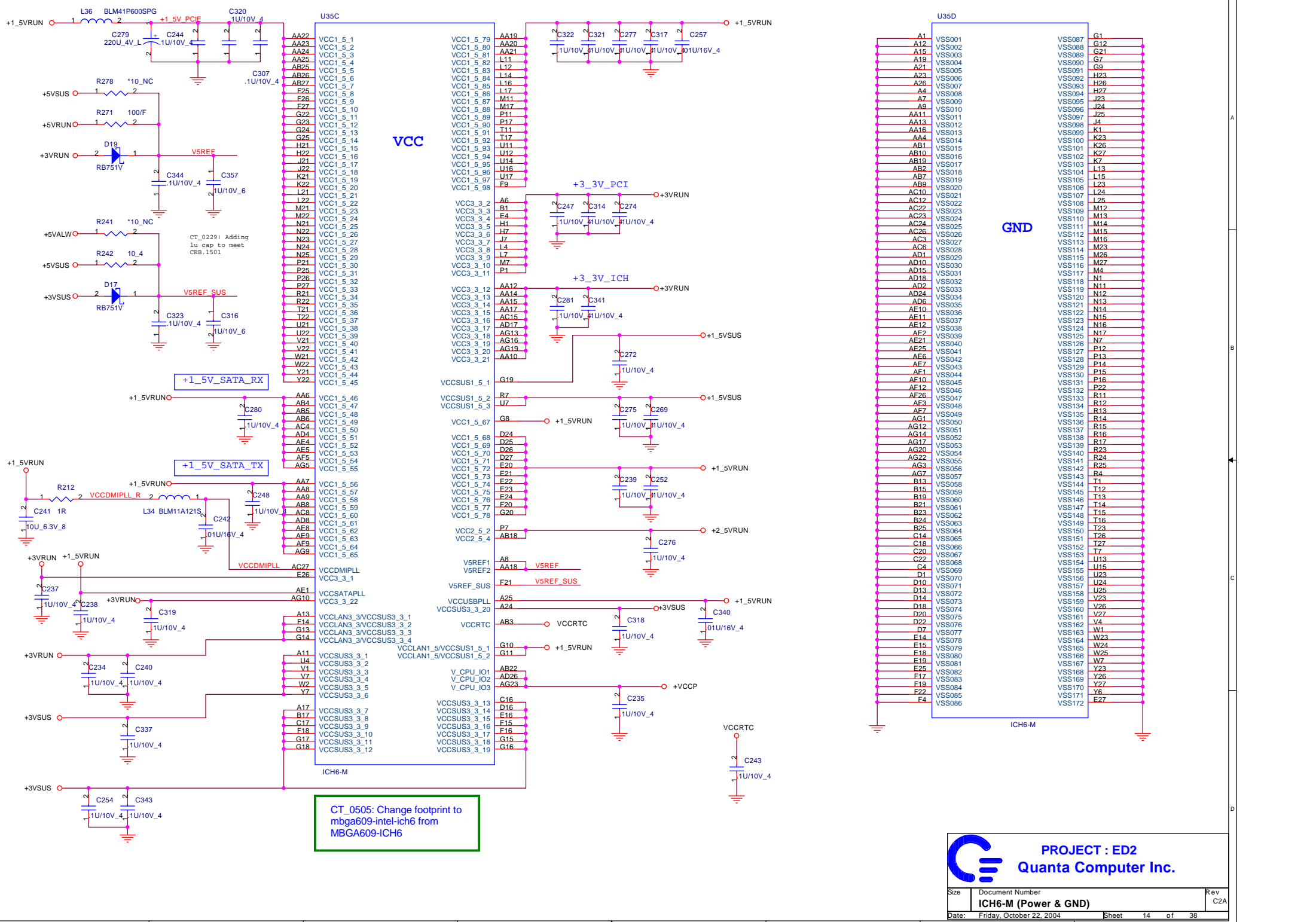
HDD LED

Place within 500mils of ICH6 ball

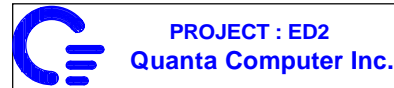


PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	ICH6-M (USB, DMI, LPC)	C2A
Date:	Friday, October 22, 2004	Sheet 13 of 38

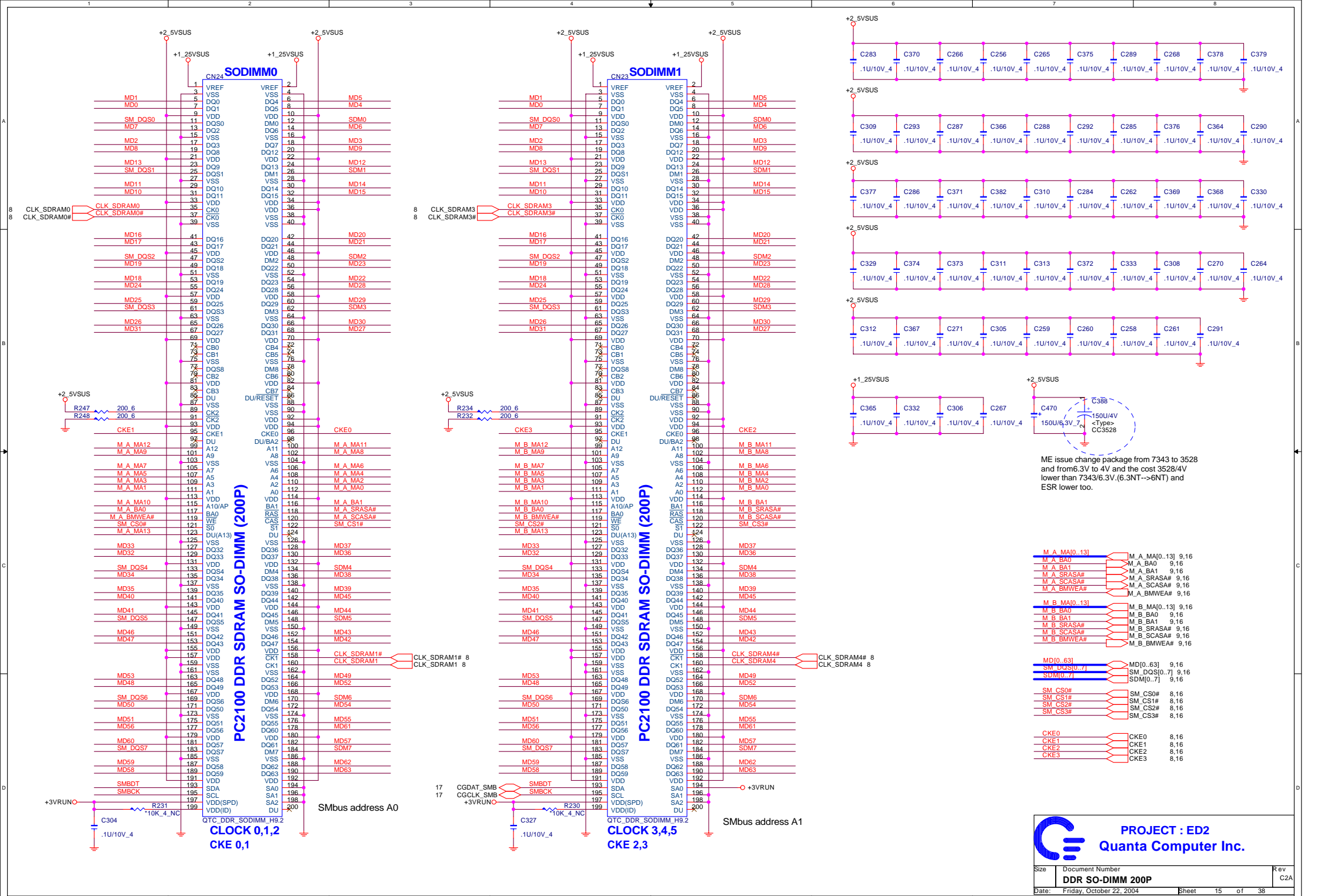


CT_0505: Change footprint to mbga609-intel-ich6 from MBGA609-ICH6



PROJECT : ED2
Quanta Computer Inc.

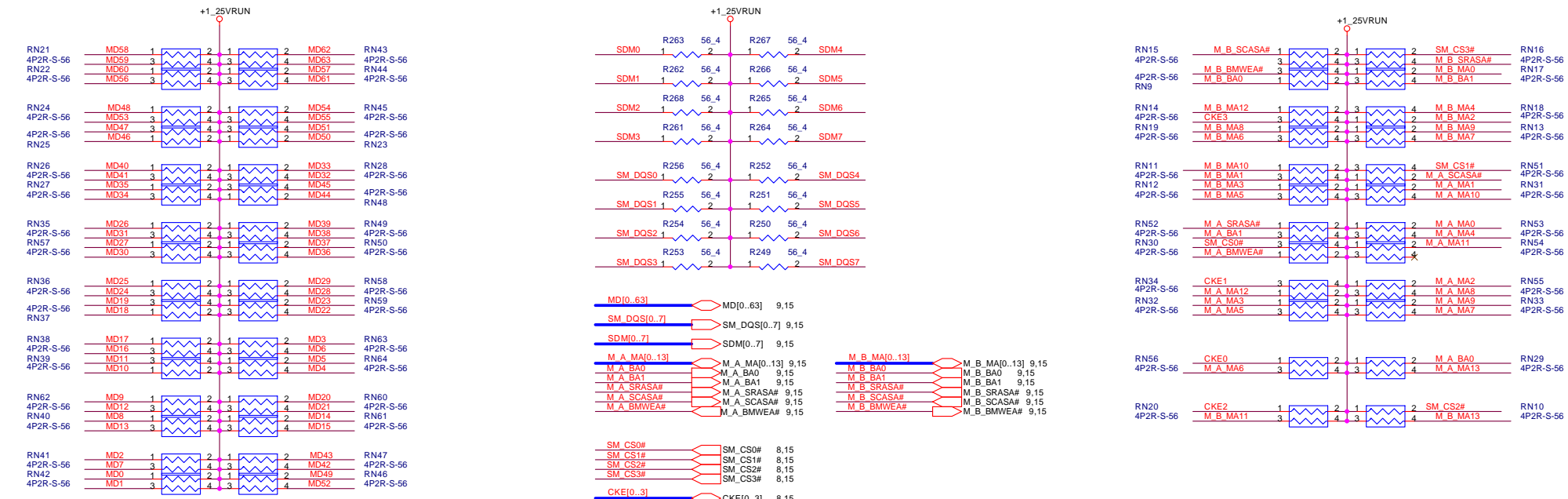
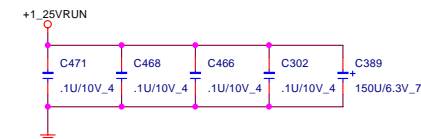
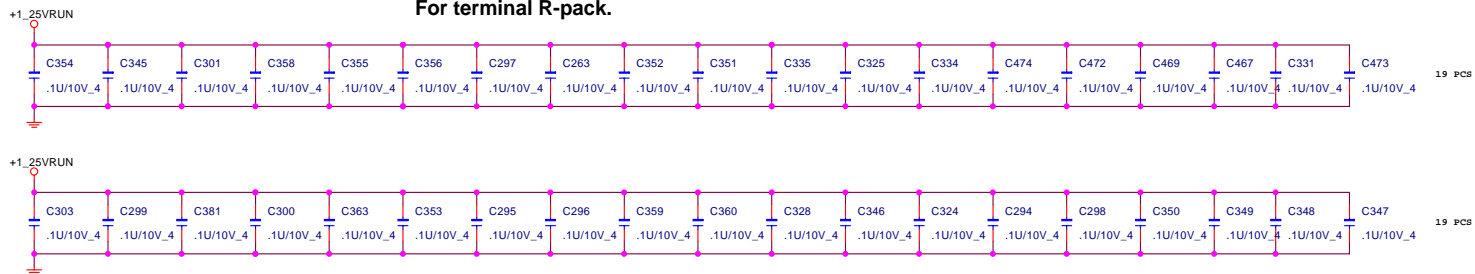
Size	Document Number	Rev
	ICH6-M (Power & GND)	C2A
Date:	Friday, October 22, 2004	Sheet 14 of 38



ME issue change package from 7343 to 3528 and from 6.3V to 4V and the cost 3528/4V lower than 7343/6.3V. (6.3NT-->6NT) and ESR lower too.

- M_A MA[0..13] M_A MA[0..13] 9,16
- M_B BA0 M_B BA0 9,16
- M_A SRASA# M_A BA1 9,16
- M_A SRASA# M_A SRASA# 9,16
- M_A SCASA# M_A SCASA# 9,16
- M_B BMWEA# M_A BMWEA# 9,16
- M_B MA[0..13] M_B MA[0..13] 9,16
- M_B BA0 M_B BA0 9,16
- M_B BA1 M_B BA1 9,16
- M_B SRASA# M_B SRASA# 9,16
- M_B SCASA# M_B SCASA# 9,16
- M_B BMWEA# M_B BMWEA# 9,16
- MD[0..63] MD[0..63] 9,16
- SM_DQS[0..7] SM_DQS[0..7] 8,16
- SM[0..7] SDM[0..7] 8,16
- SM_CS# SM_CS# 8,16
- SM_CS1# SM_CS1# 8,16
- SM_CS2# SM_CS2# 8,16
- SM_CS3# SM_CS3# 8,16
- CKE0 CKE0 8,16
- CKE1 CKE1 8,16
- CKE2 CKE2 8,16
- CKE3 CKE3 8,16

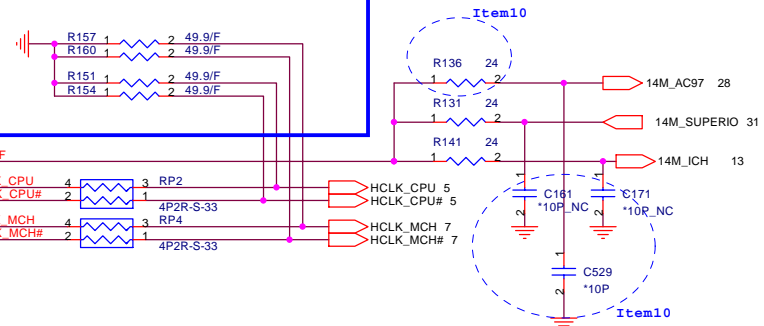
For terminal R-pack.



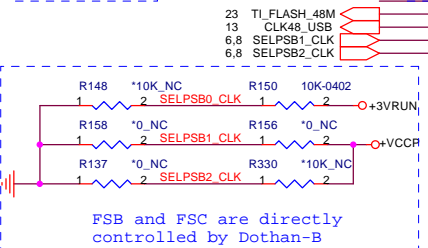
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

	DothanA	DothanB
R137	Install	NC
R330	NC	NC

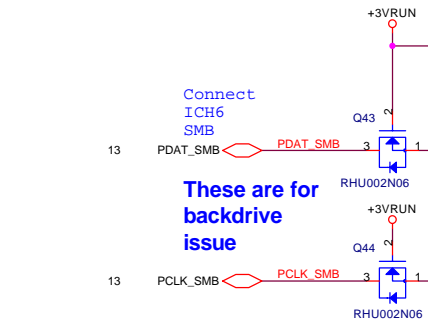
Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.



SMBus address D2

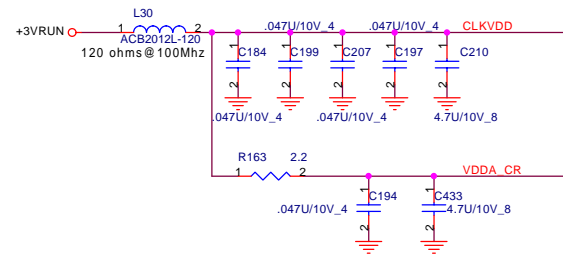


FSB and FSC are directly controlled by Dothan-B



These are for backdrive issue

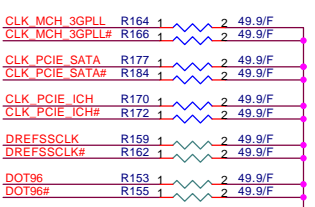
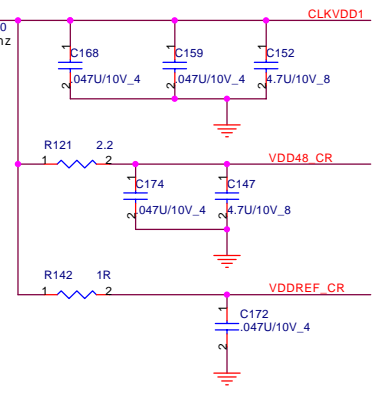
CT_0229: Change MOS to RHU002N06 due to layout concern.



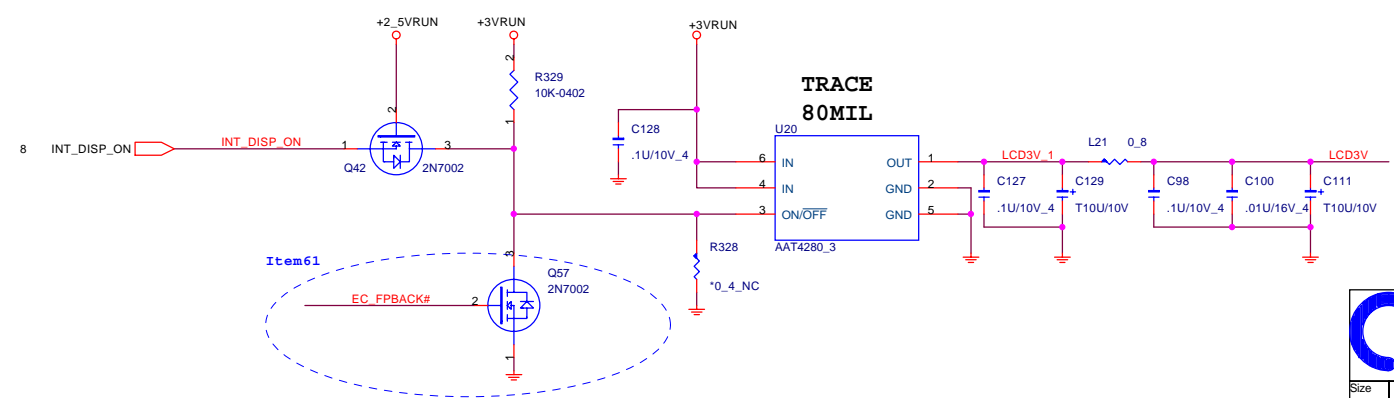
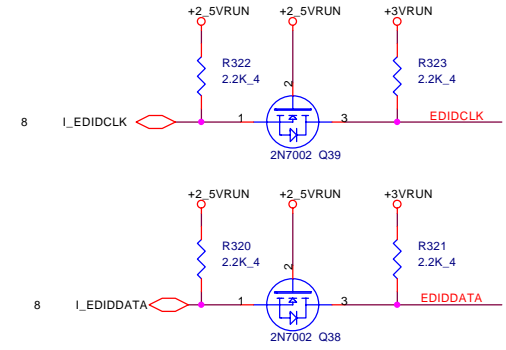
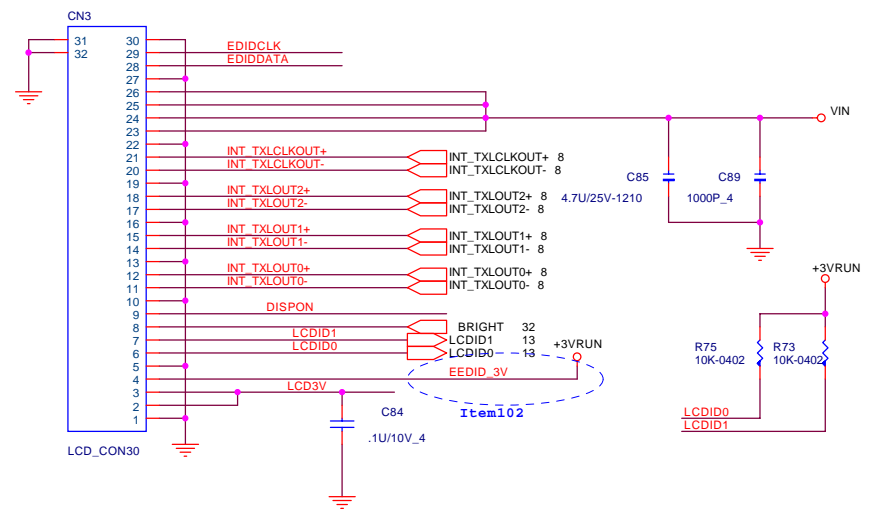
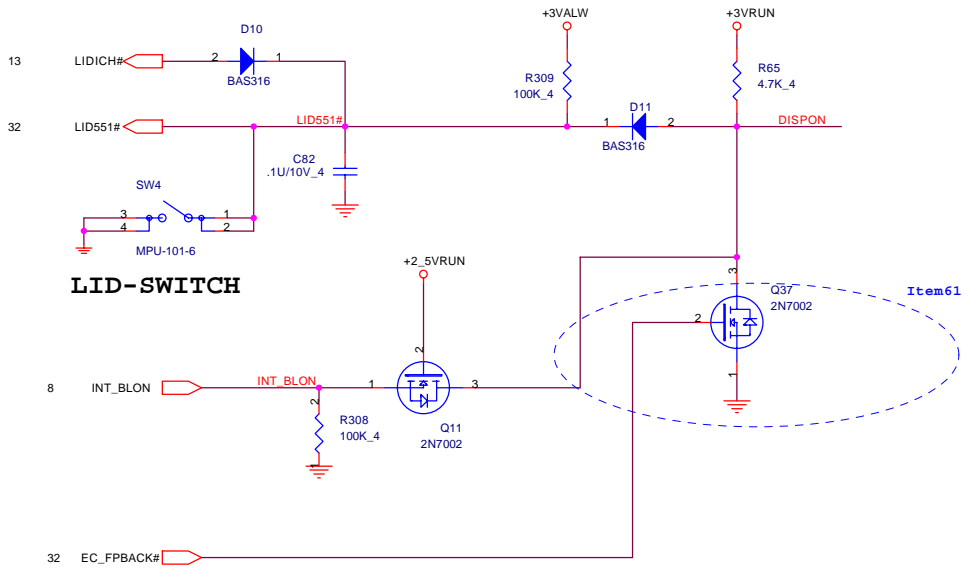
Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

Tie to VCC (Logic 1) is for ITP using. Tie to GND (Logic 0) is for PCIE using.

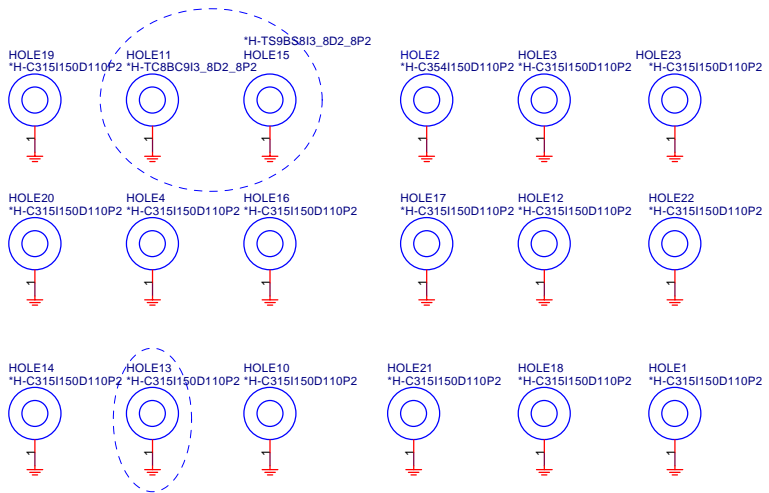
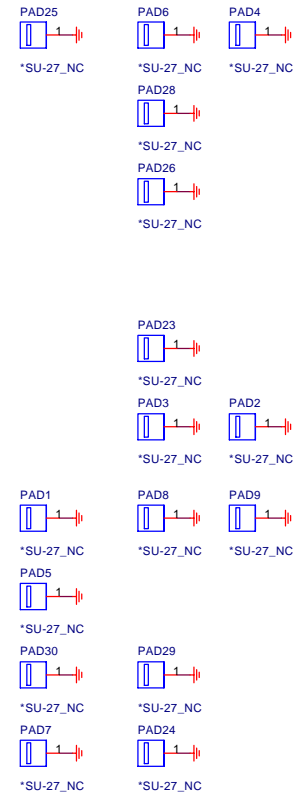
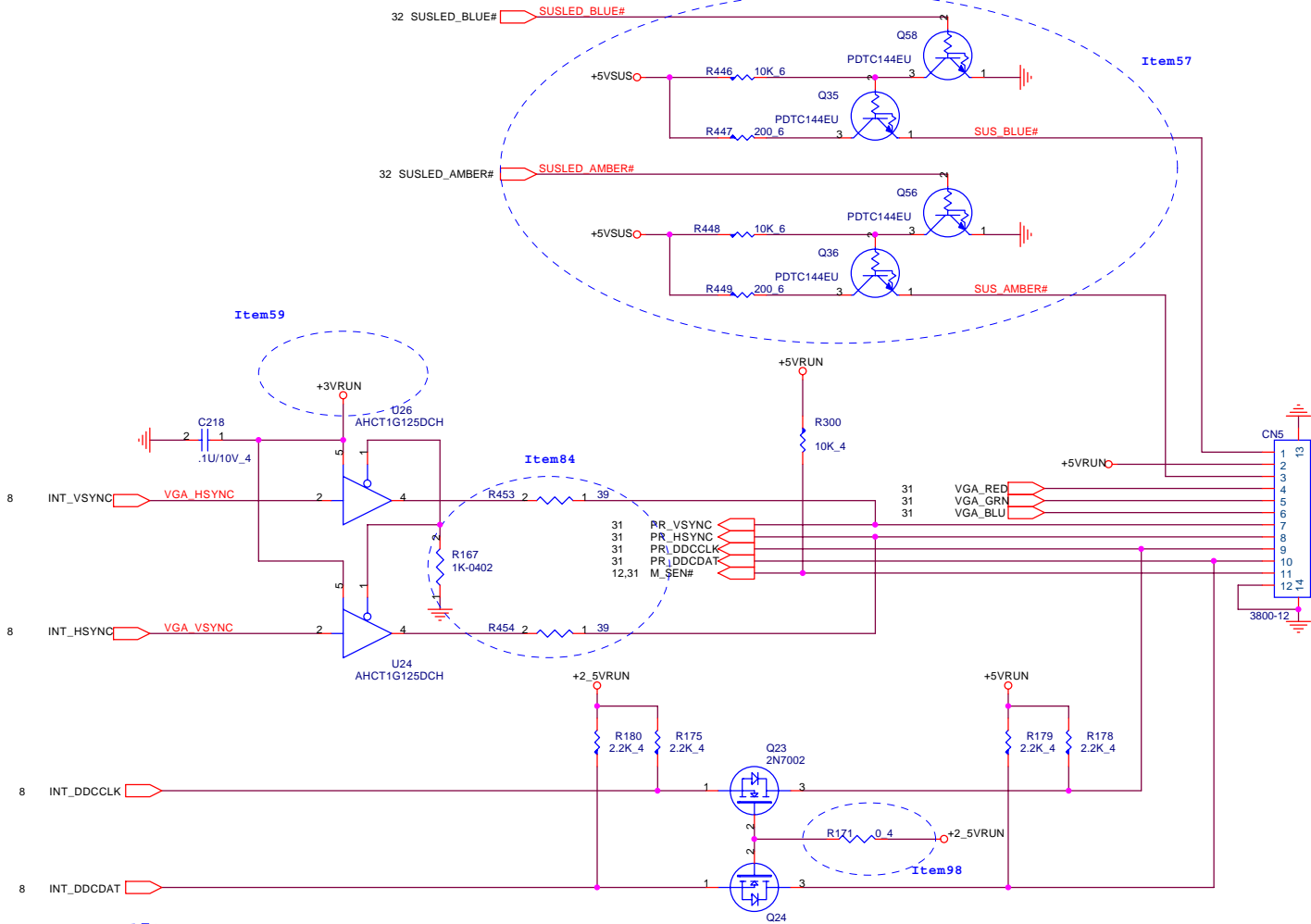


Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

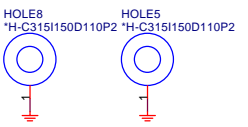


PROJECT : ED2
Quanta Computer Inc.

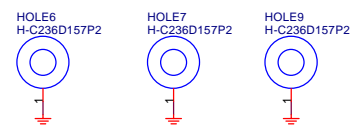
Size	Document Number	Rev
	LCD Connector	C2A
Date:	Friday, October 22, 2004	Sheet 18 of 38



TV-Board fixing Nut



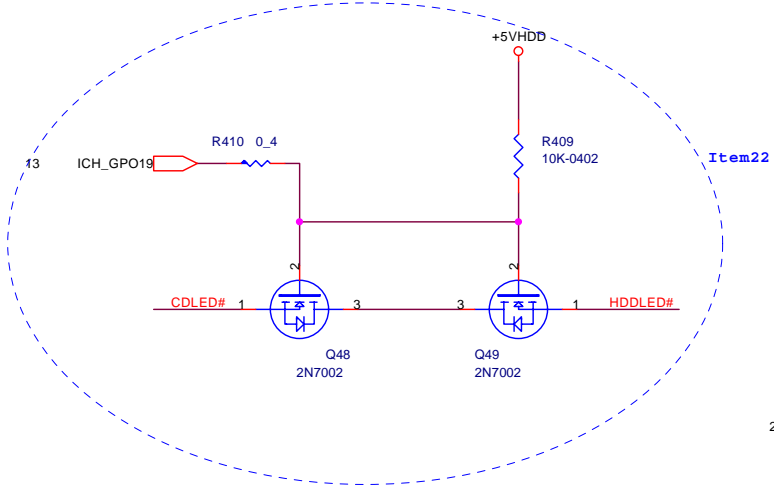
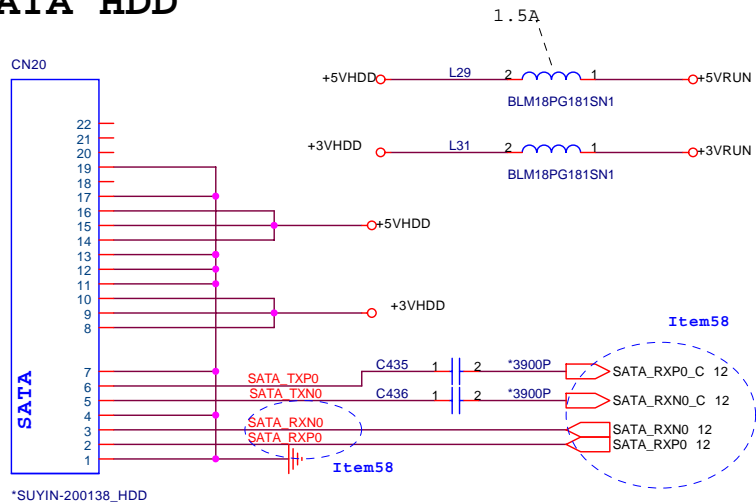
CPU SOCKET



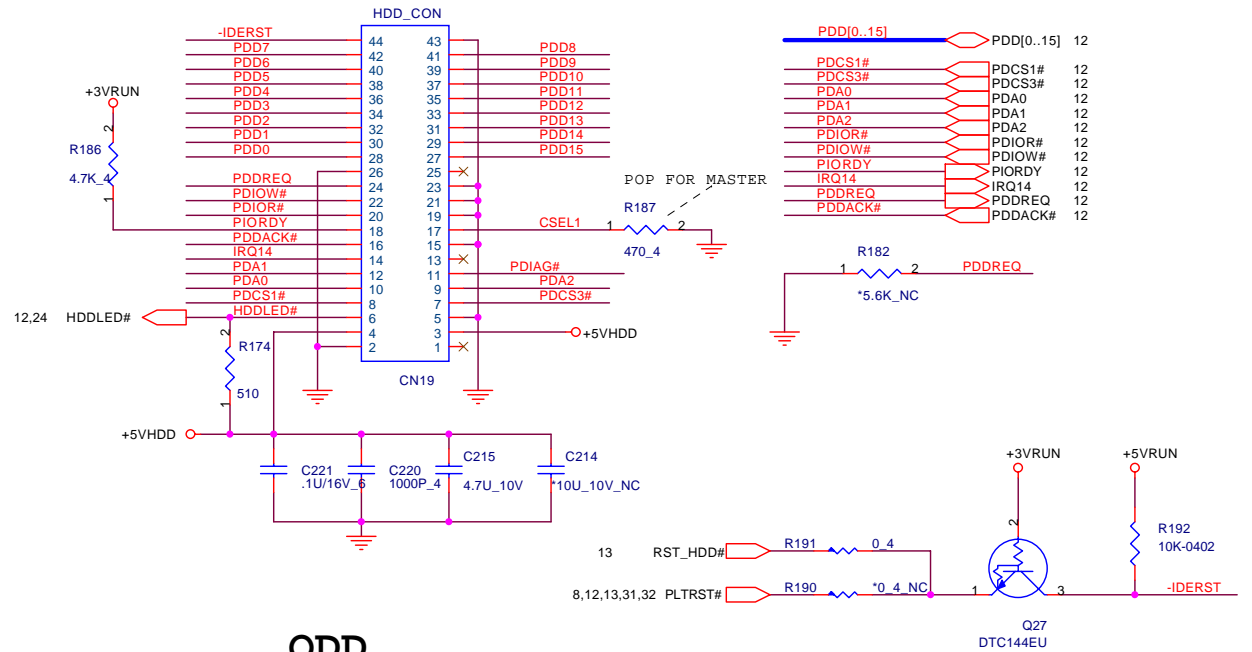
PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	CRT & TV Connector	C2A
Date:	Friday, October 22, 2004	Sheet 19 of 38

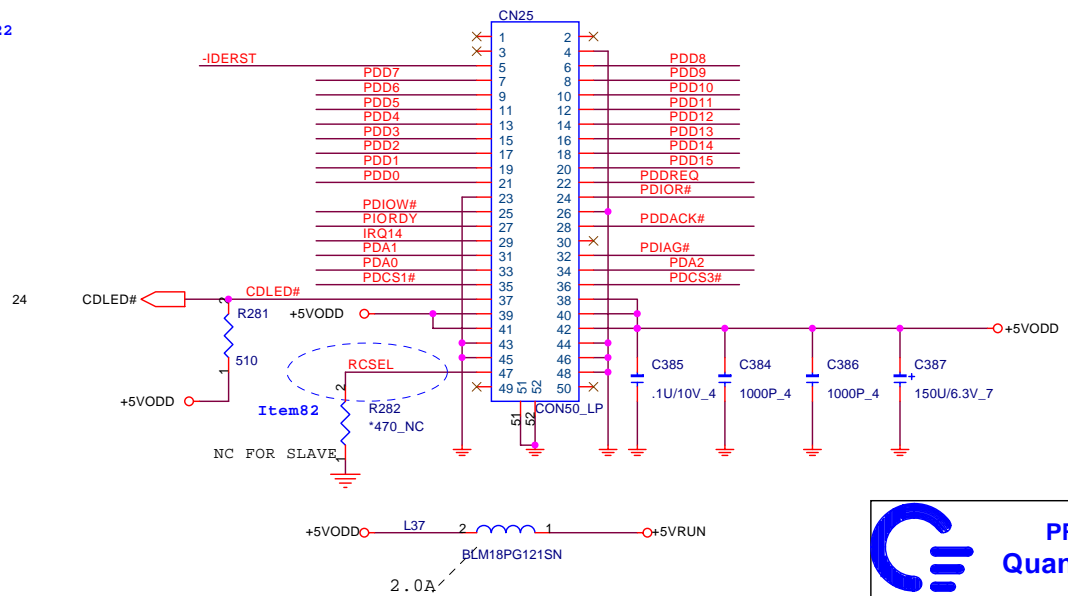
SATA HDD



PATA HDD

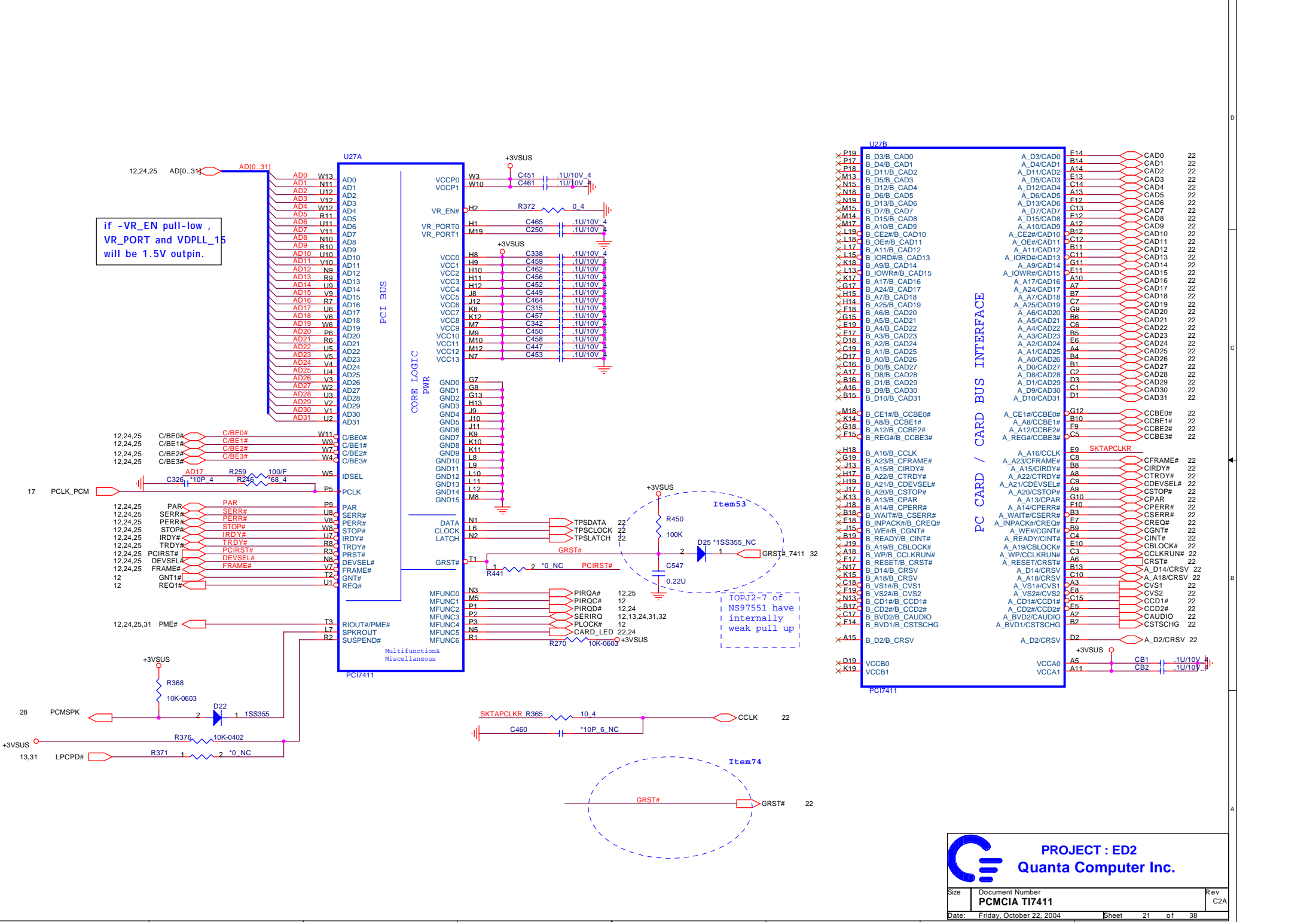


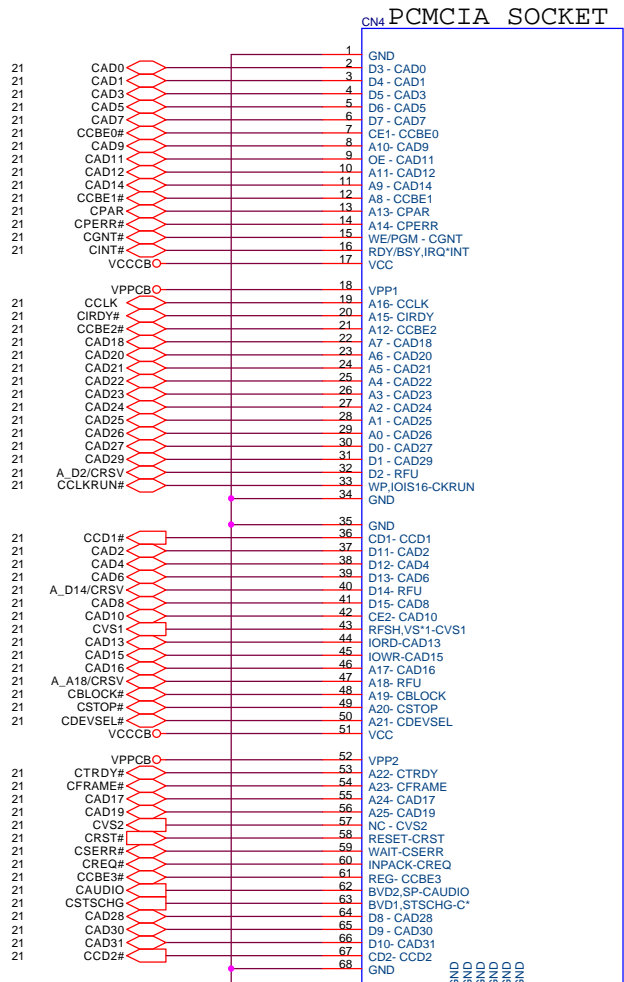
ODD



PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM Connector	C2A
Date:	Friday, October 22, 2004	Sheet 20 of 38

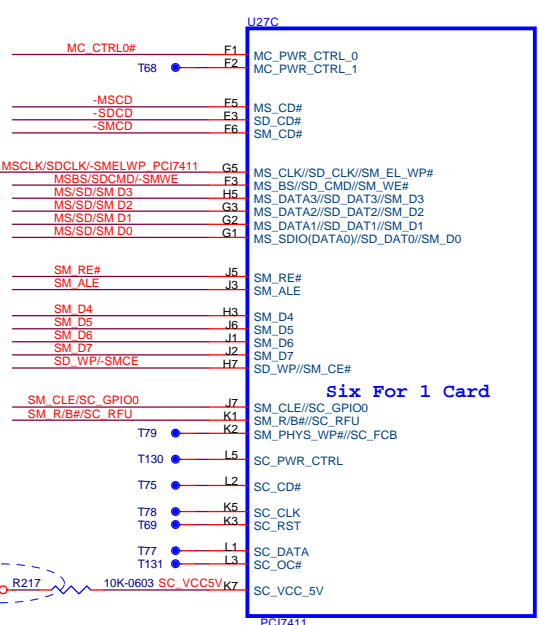
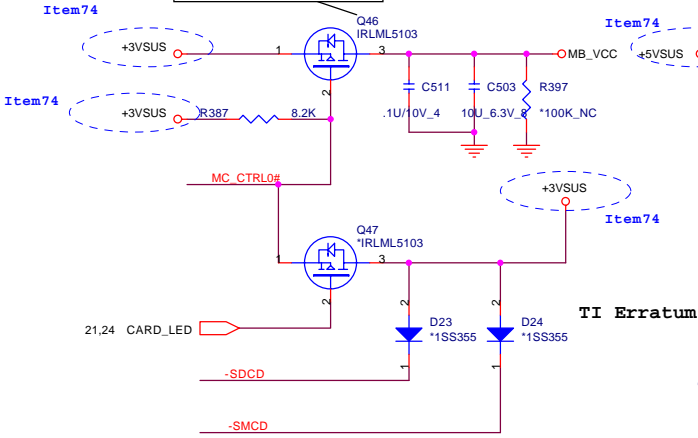




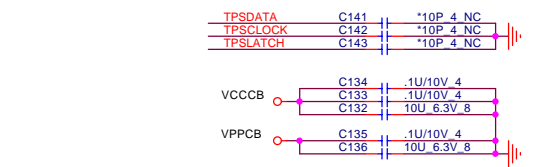
MC_PWR_CTRL low active(default), or change register to high active

Flash Media Layout Guidelines:
 1. Signal traces should be 60 Ohm +/- 10%.
 2. All signal traces should be routed with equal propagation delay, and with trace lengths as short as practical.
 3. A 56 Ohm damping resistor for MS_CLK and SD_CLK should be placed near the PCI7411 source.

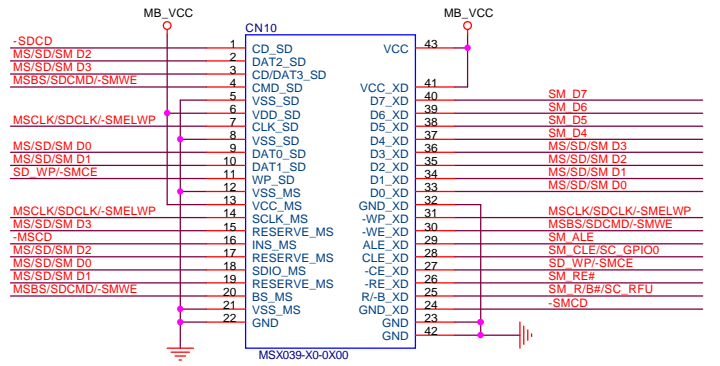
IRLML5103
 Rds(on) = 0.6



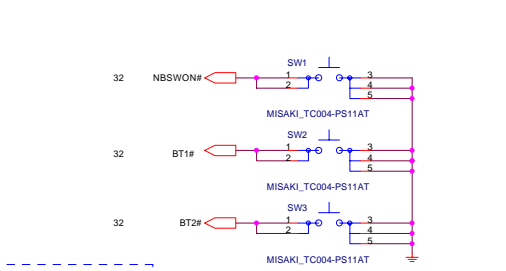
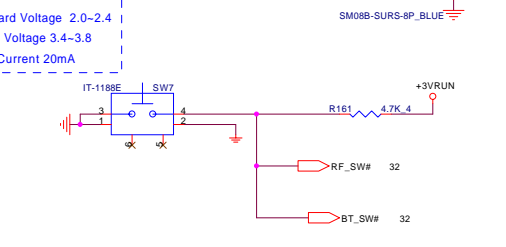
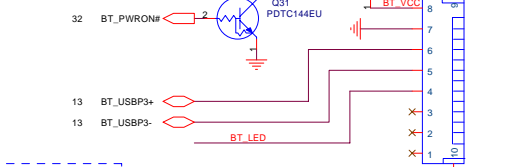
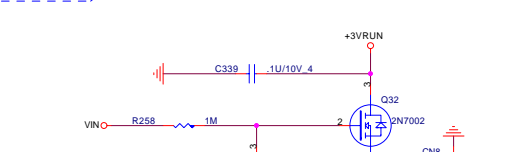
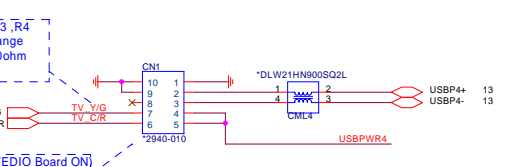
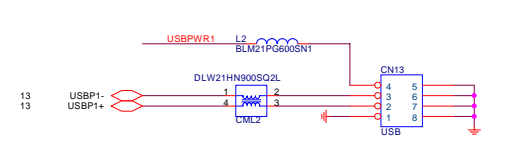
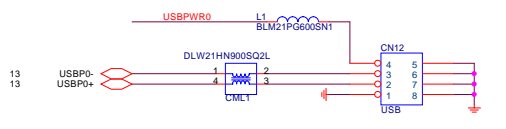
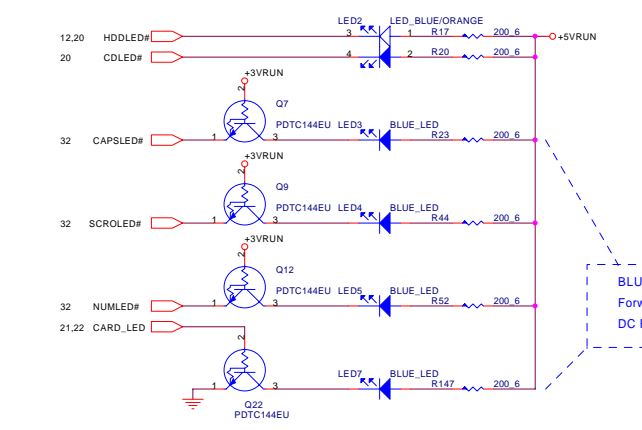
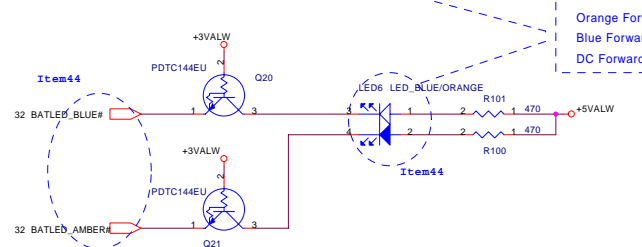
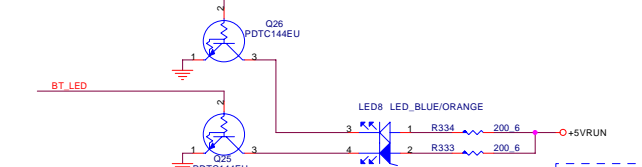
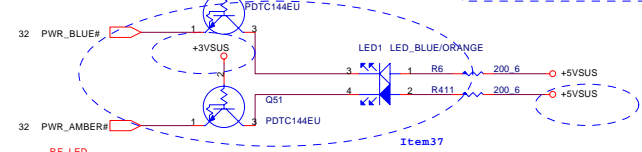
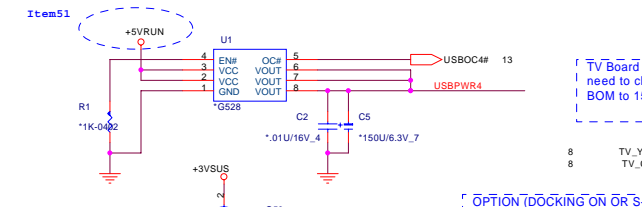
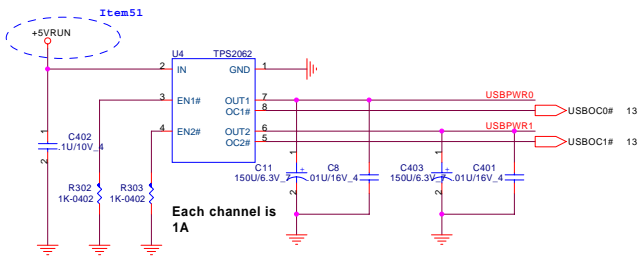
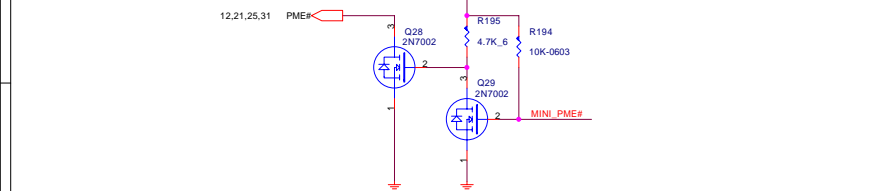
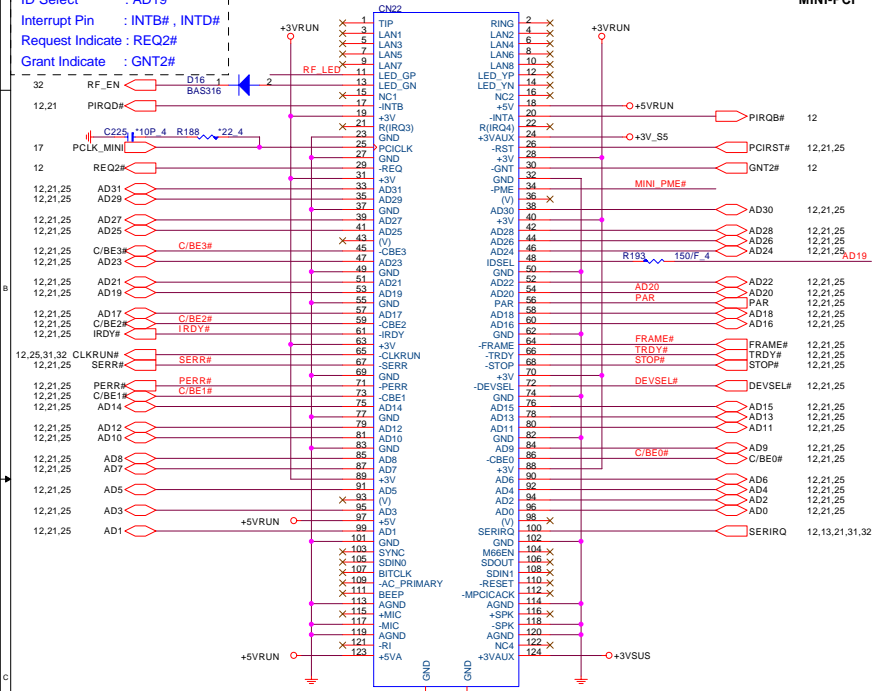
Six For 1 Card



4 IN1 CARD READER (XD, MMC/SD, MS)

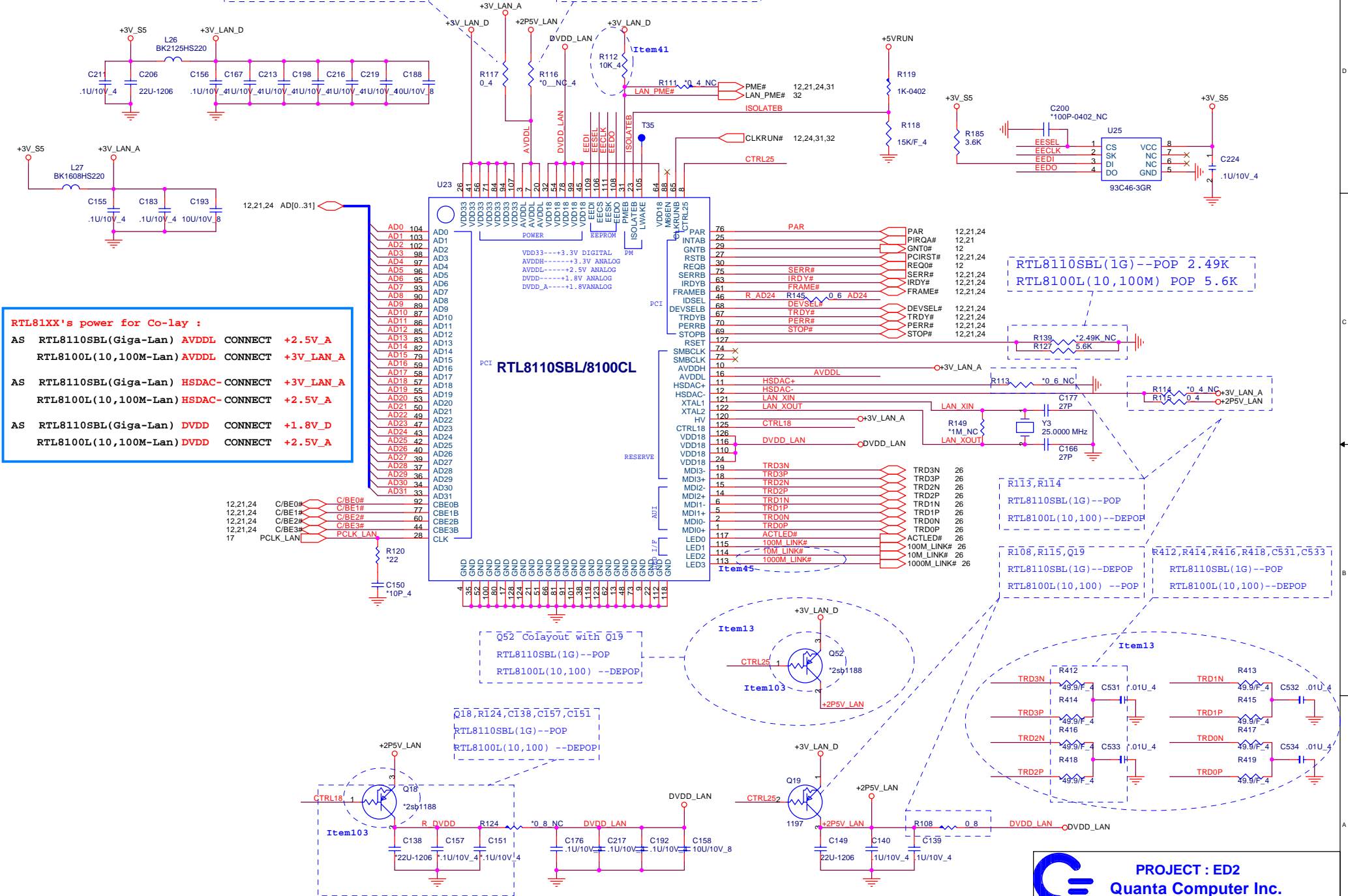


ID Select : AD19
 Interrupt Pin : INTB#, INTD#
 Request Indicate : REQ2#
 Grant Indicate : GNT2#



R117
RTL8110SBL(1G)--DEPOP
RTL8100L(10,100)--POP

R116
RTL8110SBL(1G)--POP
RTL8100L(10,100)--DEPOP

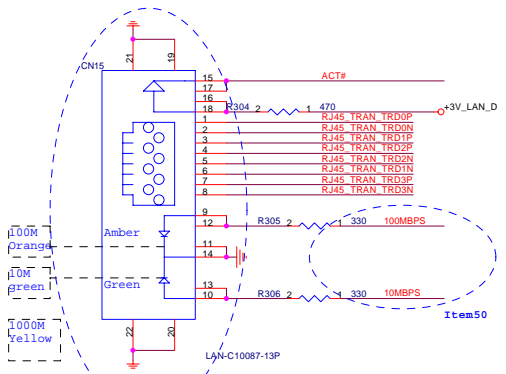


RTL81XX's power for Co-layer :

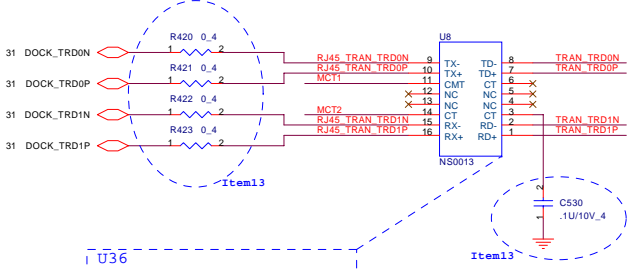
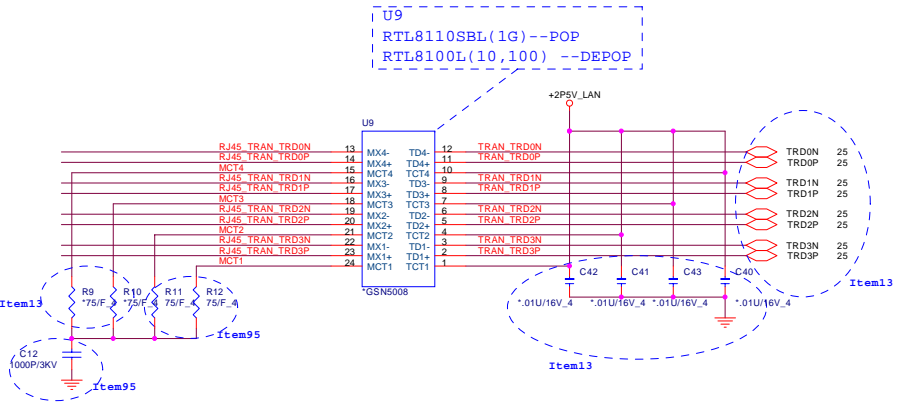
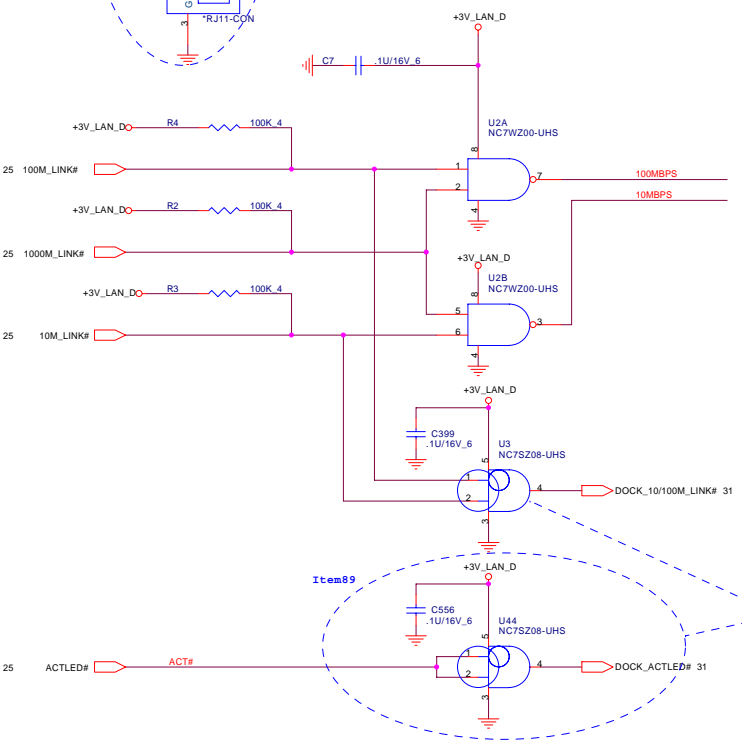
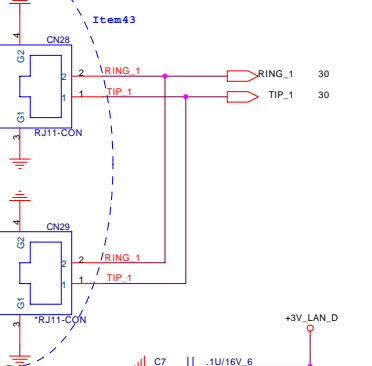
AS	RTL8110SBL(Giga-Lan)	AVDDL	CONNECT	+2.5V_A
	RTL8100L(10,100M-Lan)	AVDDL	CONNECT	+3V_LAN_A
AS	RTL8110SBL(Giga-Lan)	HSDAC-CONNECT	CONNECT	+3V_LAN_A
	RTL8100L(10,100M-Lan)	HSDAC-CONNECT	CONNECT	+2.5V_A
AS	RTL8110SBL(Giga-Lan)	DVDDL	CONNECT	+1.8V_D
	RTL8100L(10,100M-Lan)	DVDDL	CONNECT	+2.5V_A

RTL8110SBL/8100CL

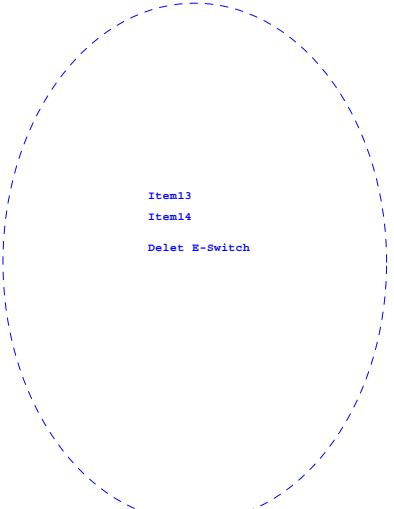
AD0	104	AD0	104
AD1	103	AD1	103
AD2	102	AD2	102
AD3	98	AD3	98
AD4	97	AD4	97
AD5	96	AD5	96
AD6	95	AD6	95
AD7	93	AD7	93
AD8	90	AD8	90
AD9	87	AD9	87
AD10	86	AD10	86
AD11	85	AD11	85
AD12	83	AD12	83
AD13	82	AD13	82
AD14	81	AD14	81
AD15	79	AD15	79
AD16	78	AD16	78
AD17	69	AD17	69
AD18	58	AD18	58
AD19	57	AD19	57
AD20	55	AD20	55
AD21	53	AD21	53
AD22	49	AD22	49
AD23	47	AD23	47
AD24	43	AD24	43
AD25	42	AD25	42
AD26	40	AD26	40
AD27	39	AD27	39
AD28	37	AD28	37
AD29	36	AD29	36
AD30	34	AD30	34
AD31	33	AD31	33
	32		32
	77		77
	60		60
	44		44
	28		28



For ME issue colayout



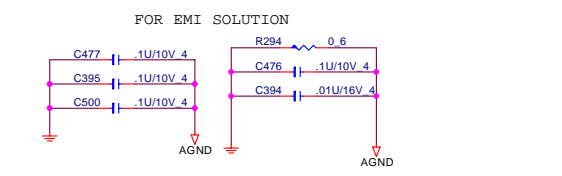
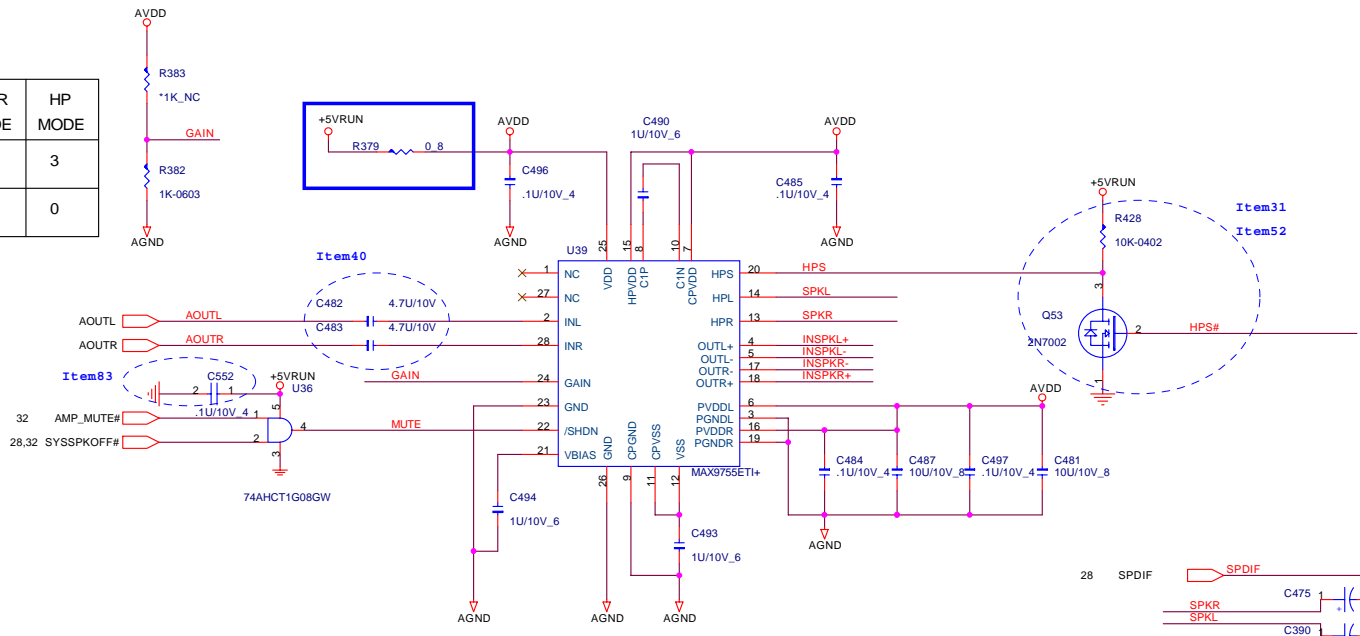
U36
RTL8110SBL(1G)--DEPOP
RTL8100L(10,100) --POP



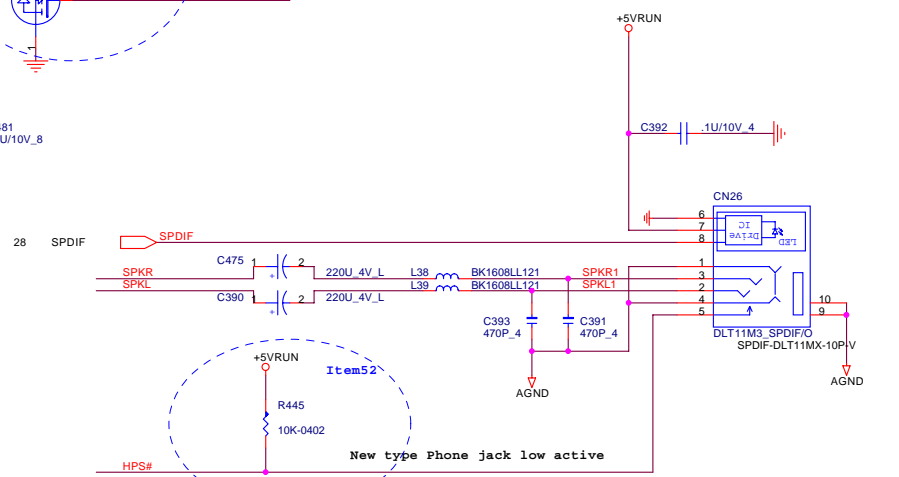
	For RTL8100C	For RTL8110SB
R116	UN-POP	POP
R117	POP	UN-POP
R139	UN-POP	POP
R127	POP	UN-POP
R113	UN-POP	POP
R114	UN-POP	POP
R115	POP	UN-POP
R108	POP	UN-POP
R124	UN-POP	POP
C151	UN-POP	POP
C138	UN-POP	POP
C157	UN-POP	POP
Q52	UN-POP	POP
Q18	UN-POP	POP
Q19	POP	UN-POP
R412	UN-POP	POP
R414	UN-POP	POP
R416	UN-POP	POP
R418	UN-POP	POP
C531	UN-POP	POP
C533	UN-POP	POP
C40	UN-POP	POP
C41	UN-POP	POP
C42	UN-POP	POP
C43	UN-POP	POP
R9	UN-POP	POP
R10	UN-POP	POP
R420	POP	UN-POP
R421	POP	UN-POP
R422	POP	UN-POP
R423	POP	UN-POP
C530	POP	UN-POP
U8	POP	UN-POP
U9	UN-POP	POP
U44	POP	UN-POP
C556	POP	UN-POP
U3	POP	UN-POP
C399	POP	UN-POP

U44, U3, C399, C556
RTL8110SBL(1G)--DEPOP
RTL8100L(10,100) --POP

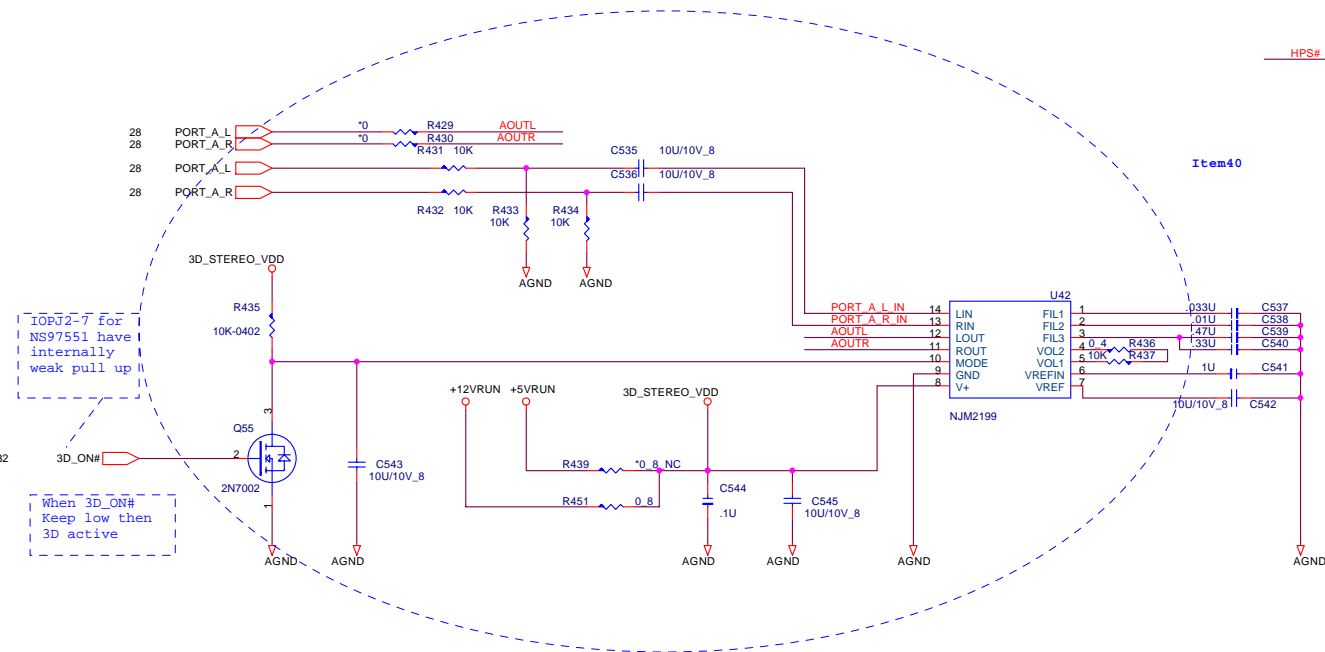
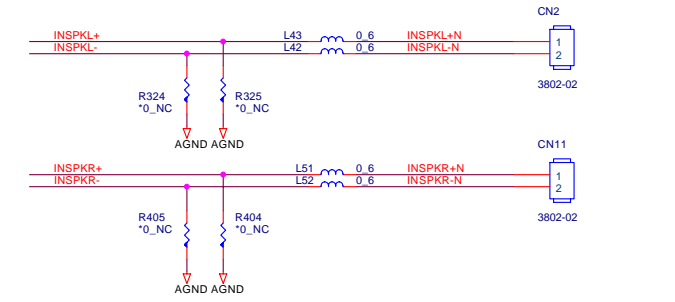
GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0



Headphone out / SPDIF OUT



SPEAKER CON.



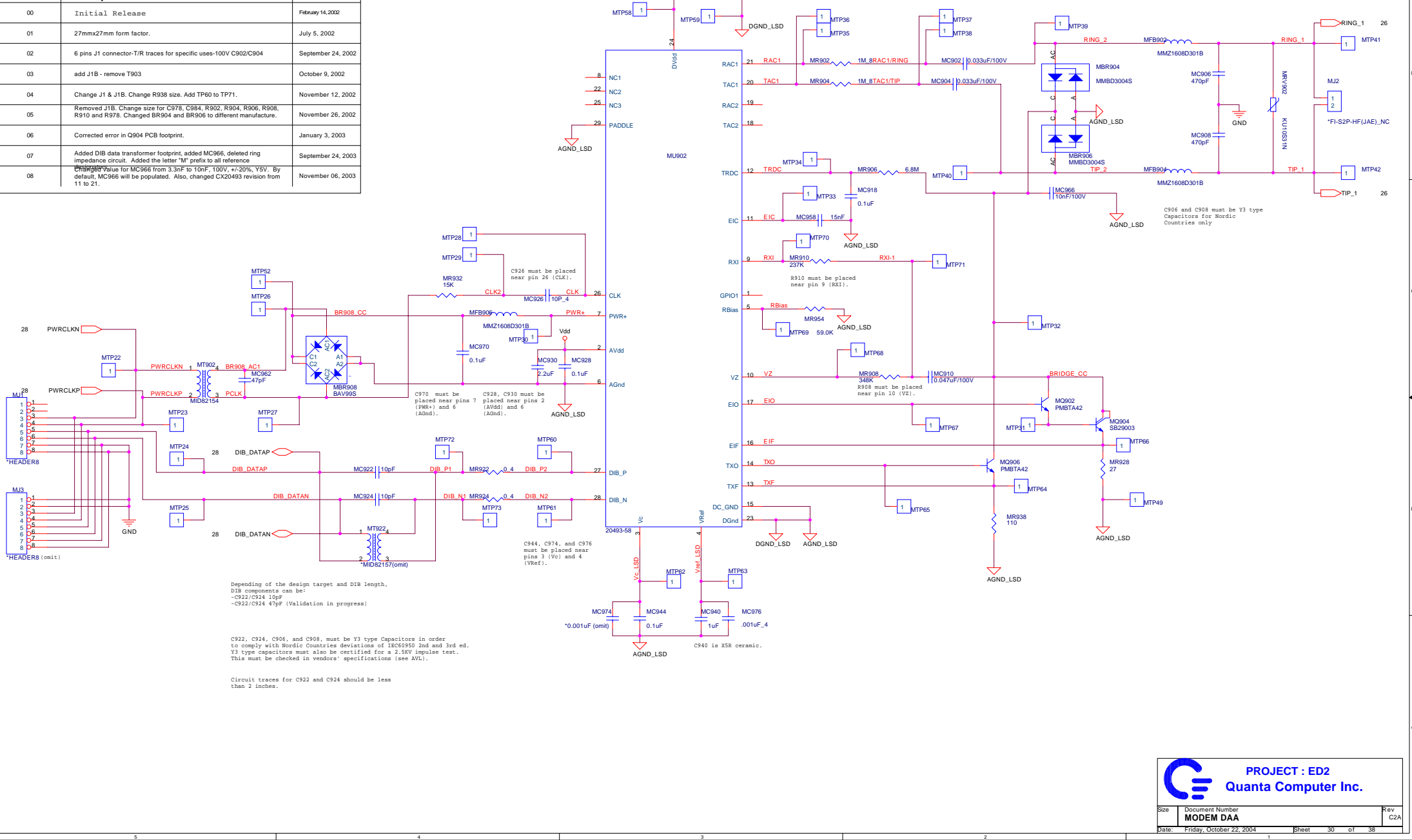
IOP32-7 for NS97551 have internally weak pull up

When 3D_ON# Keep low then 3D active

Revision History

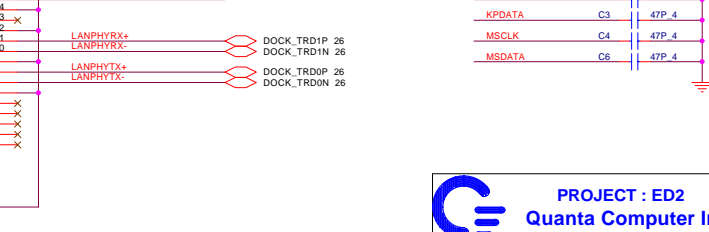
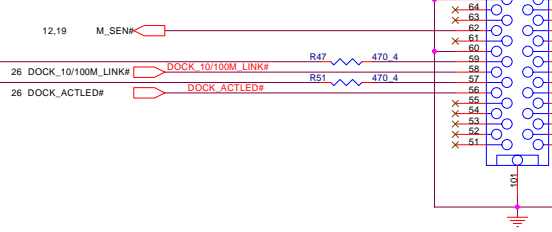
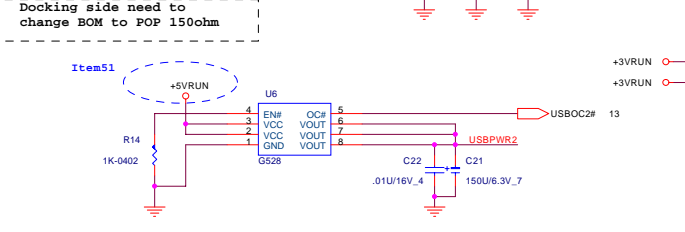
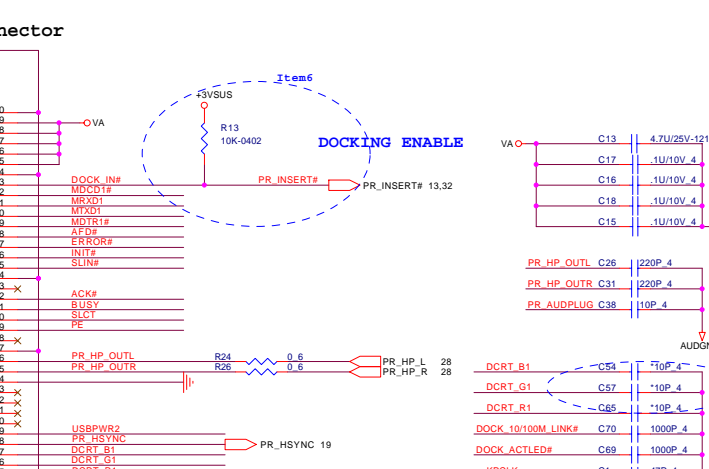
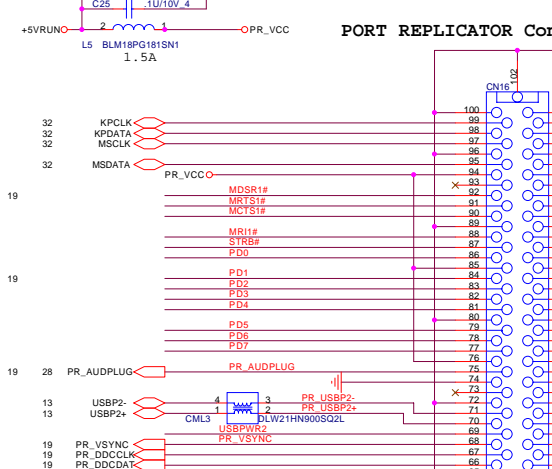
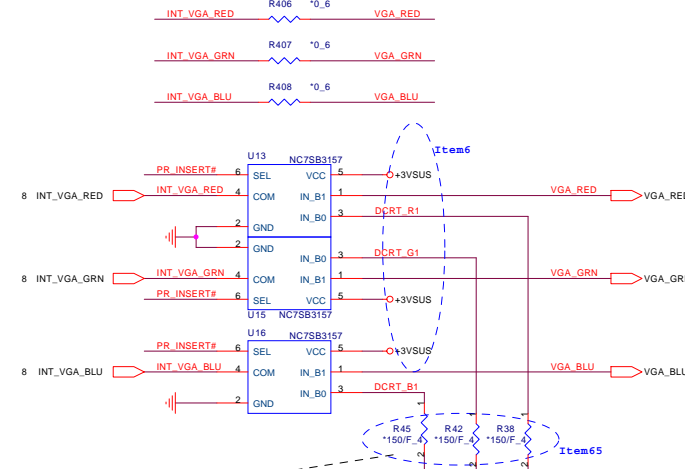
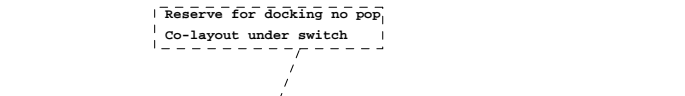
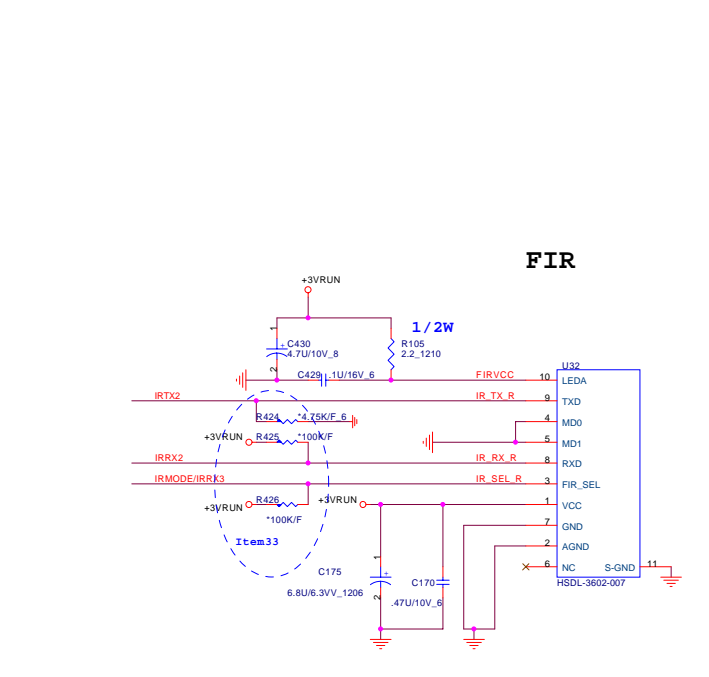
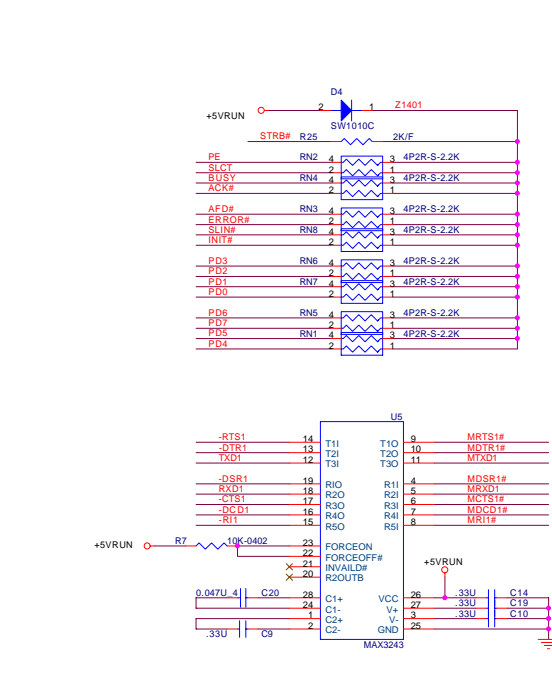
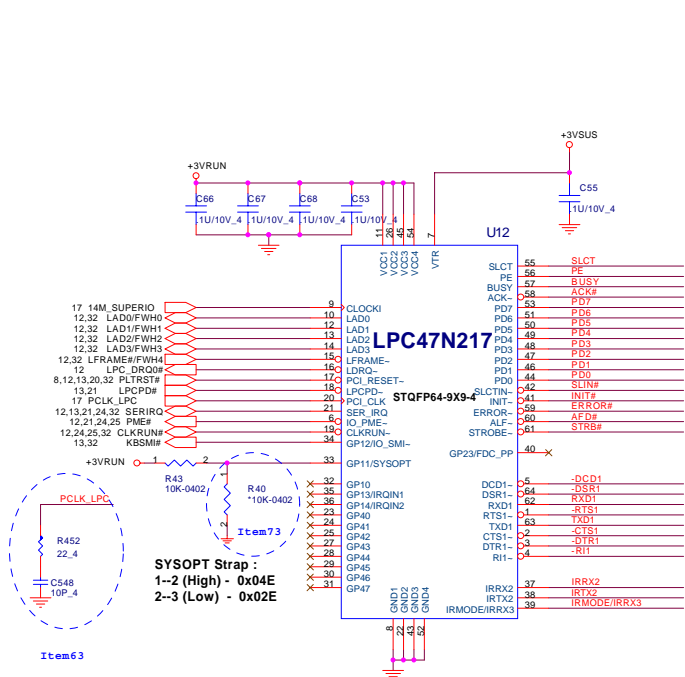
REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	September 24, 2003
08		November 06, 2003

REV:B MODIFY FOR USE NEW MODEM MODULE



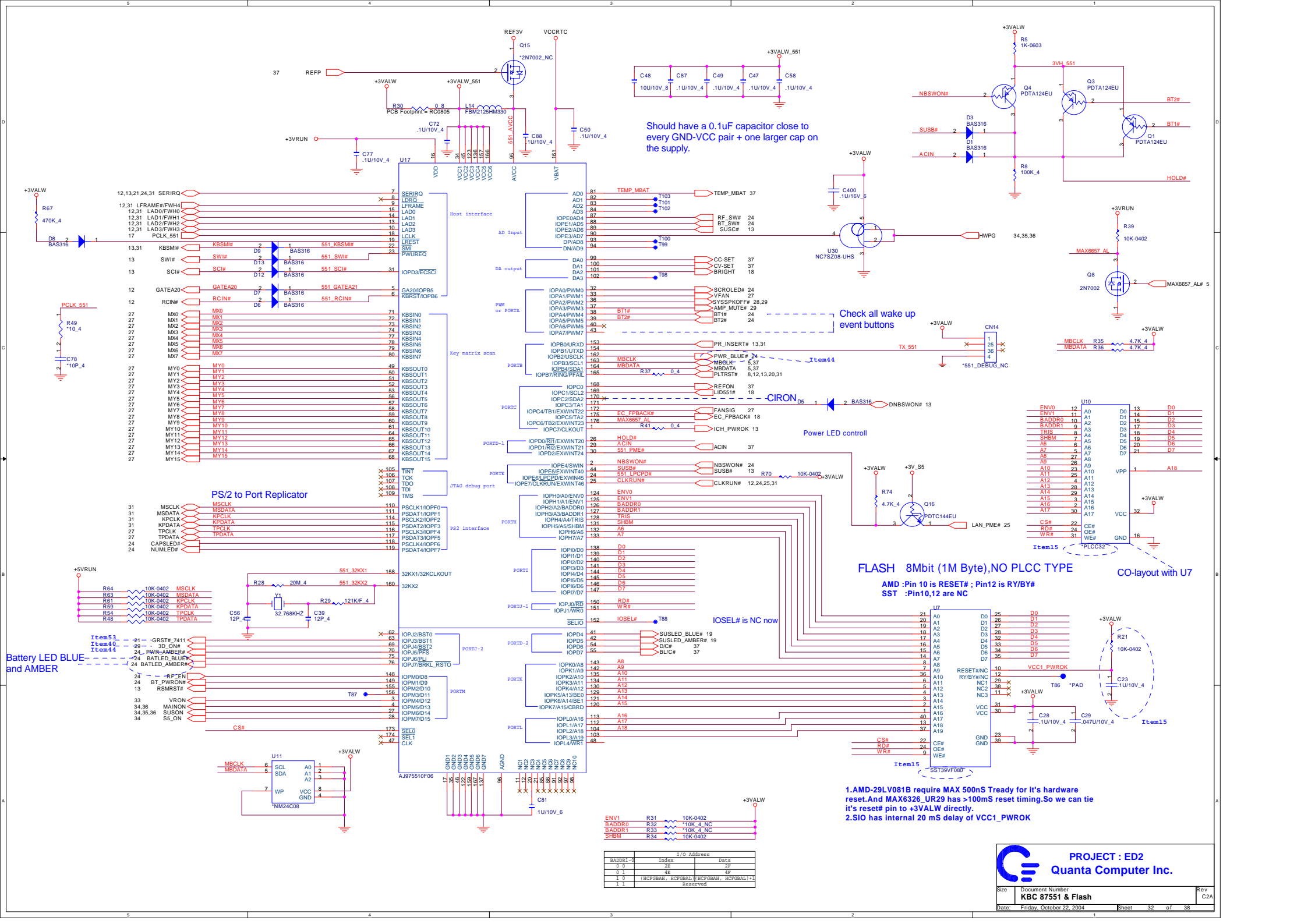
PROJECT : ED2
MODEM DAA

Size	Document Number	Rev
	MODEM DAA	C2A
Date:	Friday, October 22, 2004	Sheet 30 of 38



Docking side need to change BOM to POP 150ohm

Reserve for docking no pop
Co-layout under switch



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

Check all wake up event buttons

Power LED control

FLASH 8Mbit (1M Byte), NO PLCC TYPE

AMD : Pin 10 is RESET# ; Pin12 is RY/B#

SST : Pin10,12 are NC

IOSEL# is NC now

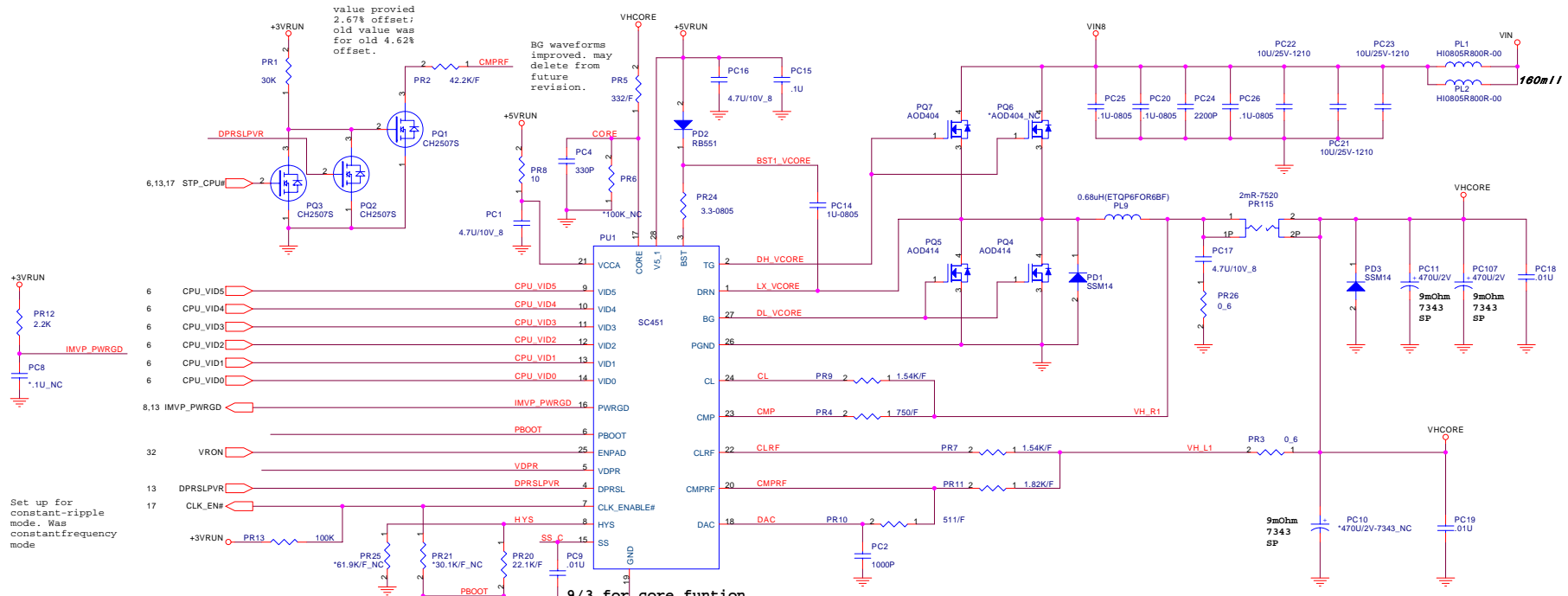
- 1.AMD-29LV081B require MAX 500ns Tready for it's hardware reset.And MAX6326 UR29 has >100ms reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

I/O Address		
Index	Address	Data
0	0	2F
0	4E	4F
I/O	(MCP0BAH, MCP0BAL, MCP0BAN, MCP0BAL+1)	Reserved
1	1	

PROJECT : ED2
Quanta Computer Inc.

Size: Document Number
KBC 87551 & Flash

Date: Friday, October 22, 2004 Sheet 32 of 38



V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	

