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33	Audio (HP,EXT MIC)	A00					
34	Audio (SPKR)	A00					
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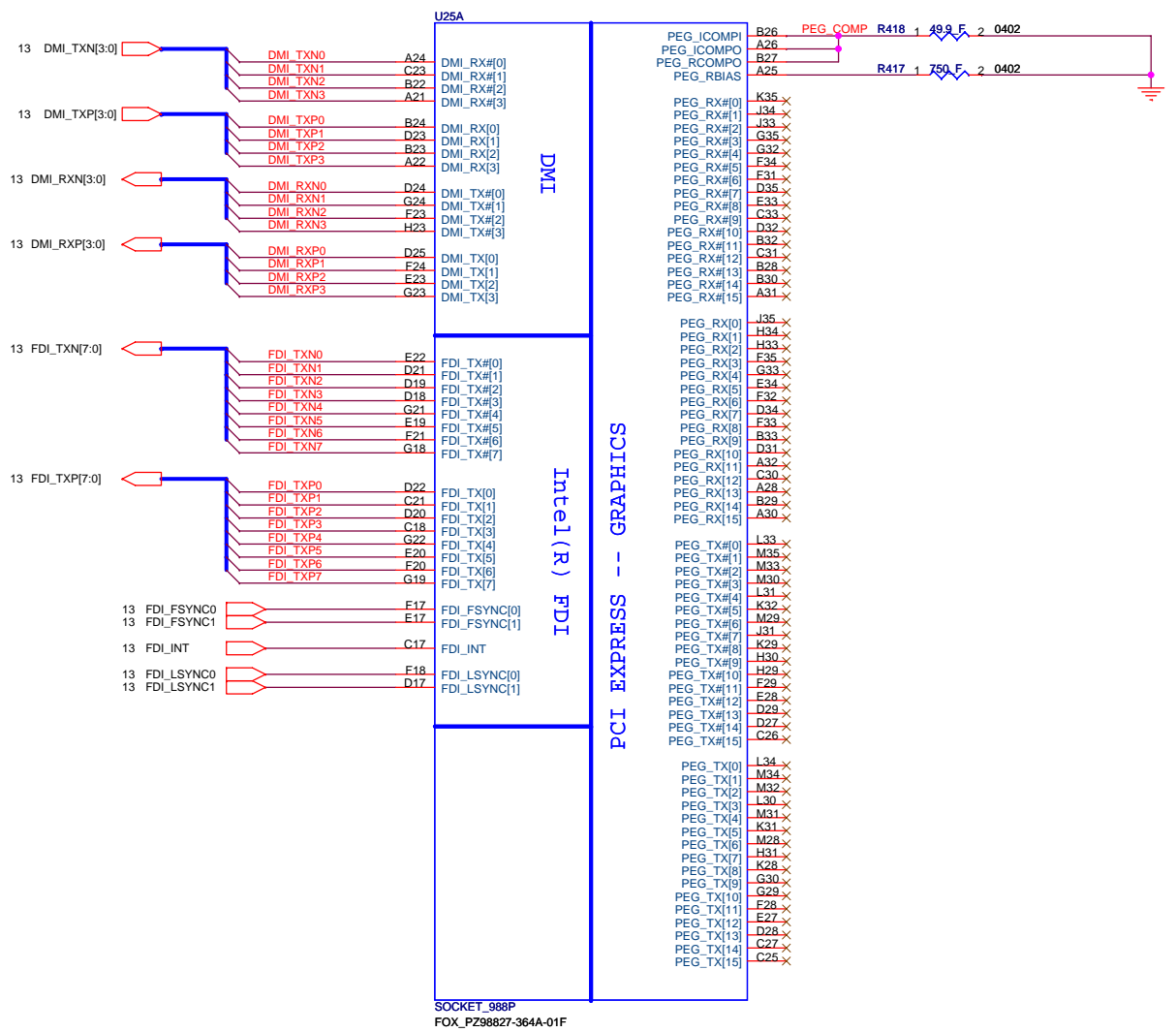
**Project Code & Schematics Subject:** H901 Main Board 6L

<b>PCB P/N:</b>	1P-0099J00-6000 (IRIS)
	1P-0099500-6000 (HANNSTAR)
	1P-0099200-6000 (NANYA)
<b>BT DB P/N:</b>	1P-1099J01-6000 (IRIS)
	1P-1099502-6000 (HANNSTAR)
	1P-1099201-6000 (NANYA)
<b>LED DB P/N:</b>	1P-1099J02-6000 (IRIS)
	1P-1099501-6000 (HANNSTAR)
	1P-1099200-6000 (NANYA)
<b>P/B DB P/N:</b>	1P-1099J00-6000 (IRIS)
	1P-1099500-6000 (HANNSTAR)
	1P-1099202-6000 (NANYA)

P. Leader	Check by	Design by

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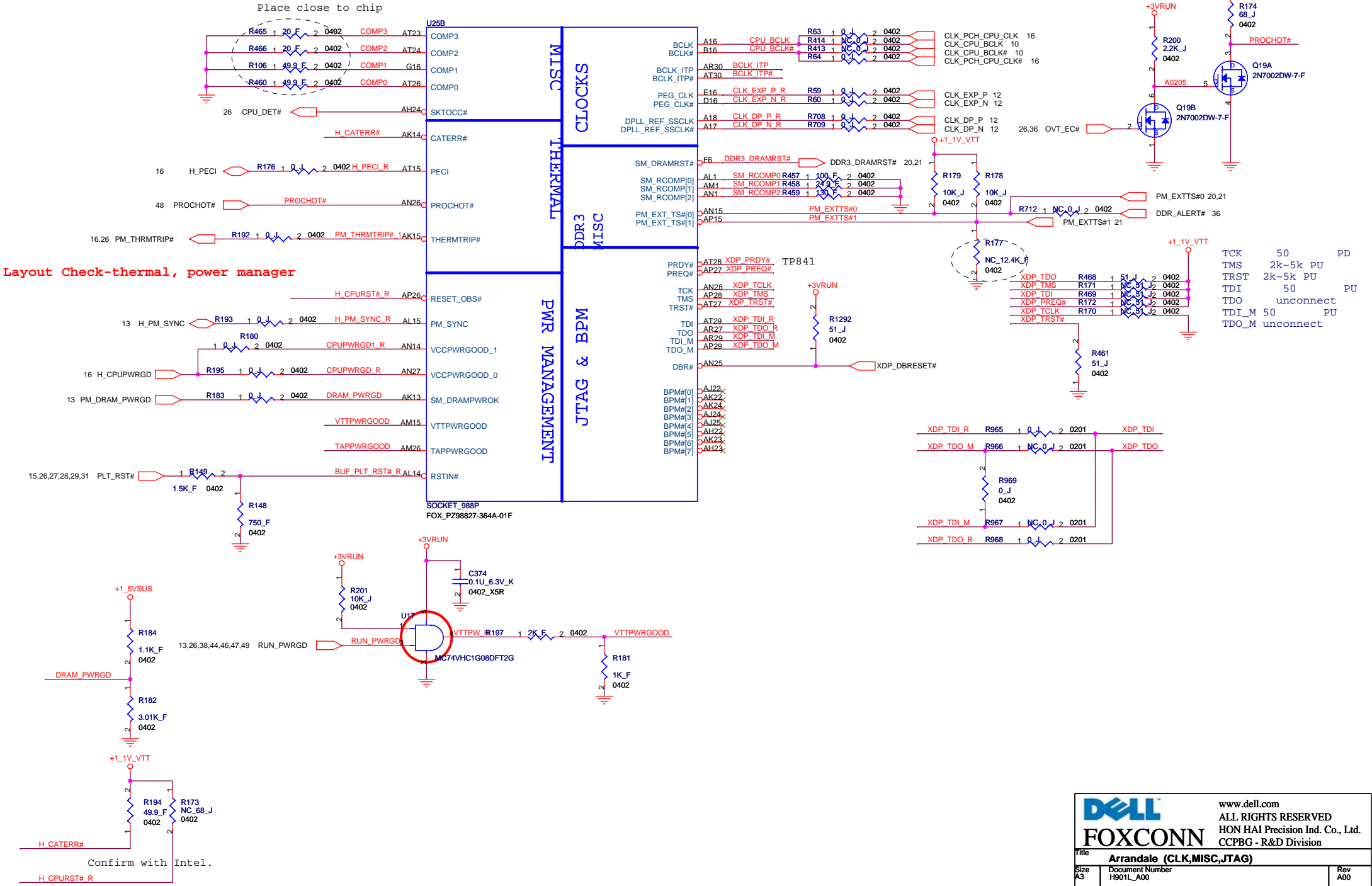


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Title: **Arrandale (DMI,PEG,FDI)**

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Layout Note:  
 Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Width=20mil(MS)  
 Comp1,3 connect with Zo=55 ohm, make trace length shorter than 0.5". Width=5mil(MS)

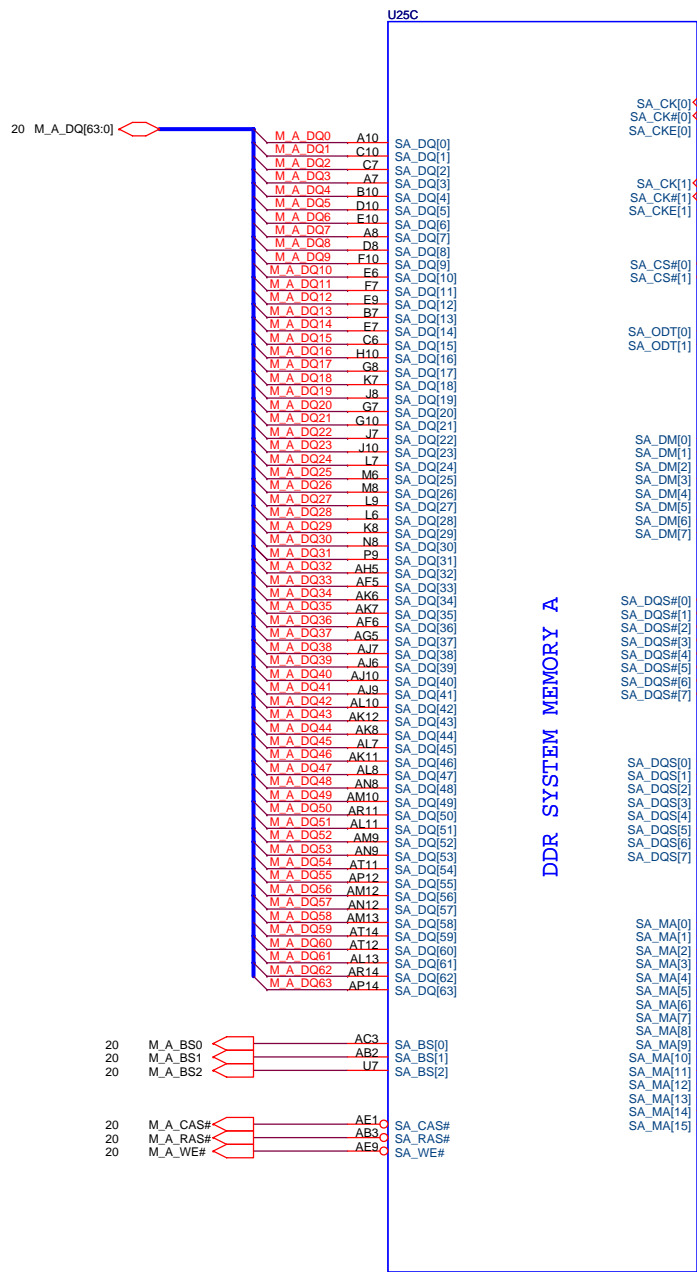


Layout Check-thermal, power manager

Confirm with Intel.  
 H\_CATERR#  
 H\_CPURST#\_R

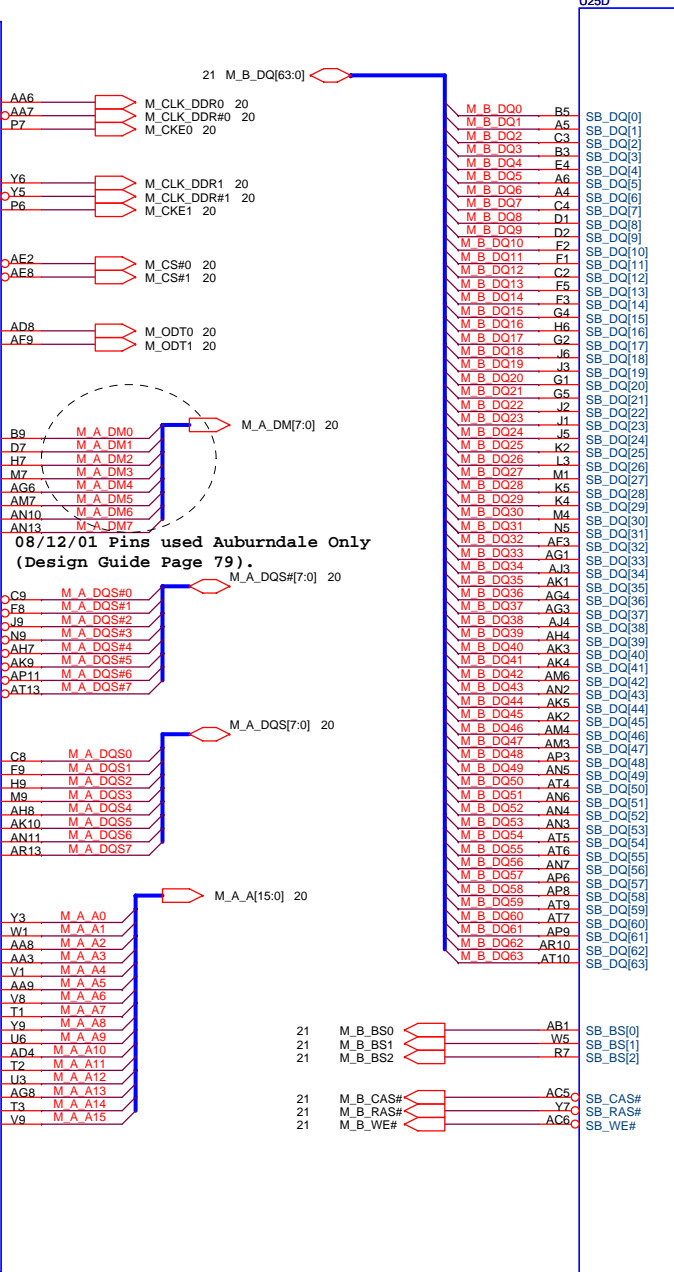
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Title	Arrandale (CLK,MISC,JTAG)	
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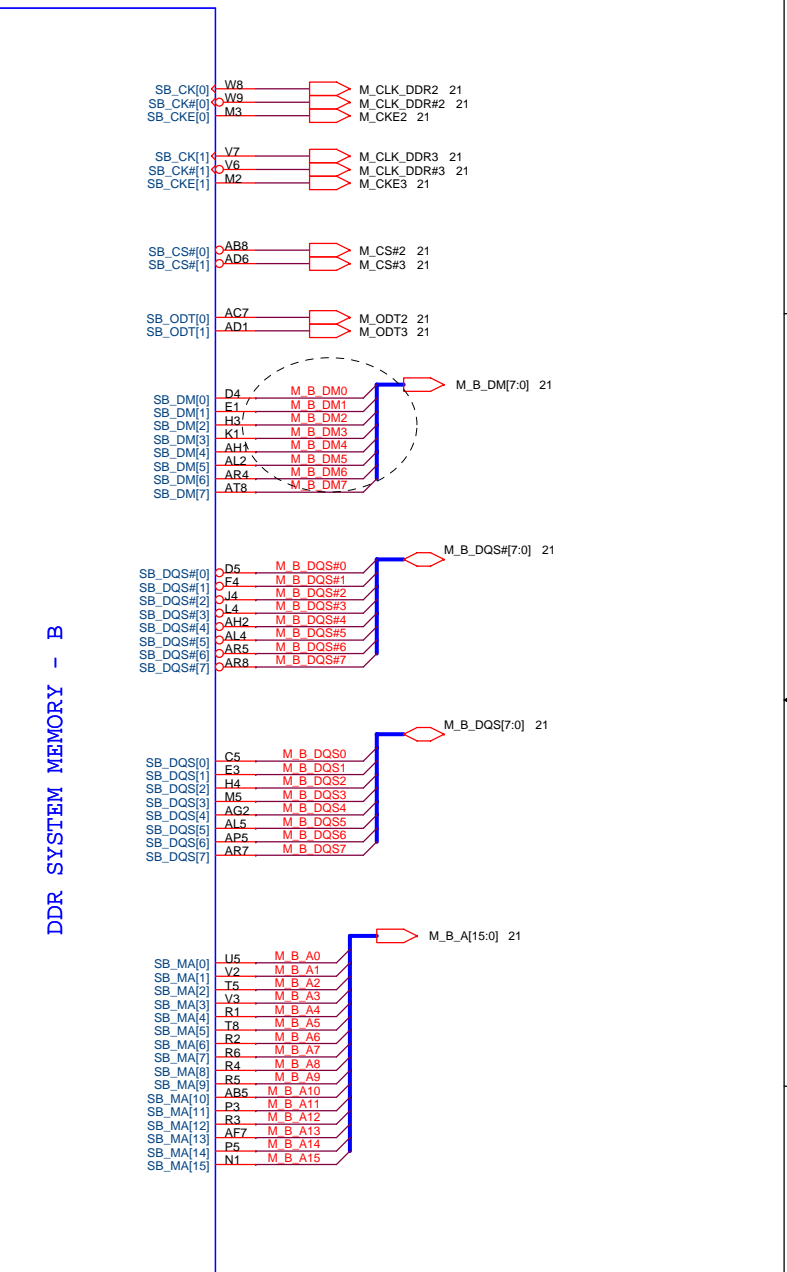
SOCKET\_988P  
FOX\_PZ98827-364A-01F

DDR SYSTEM MEMORY A



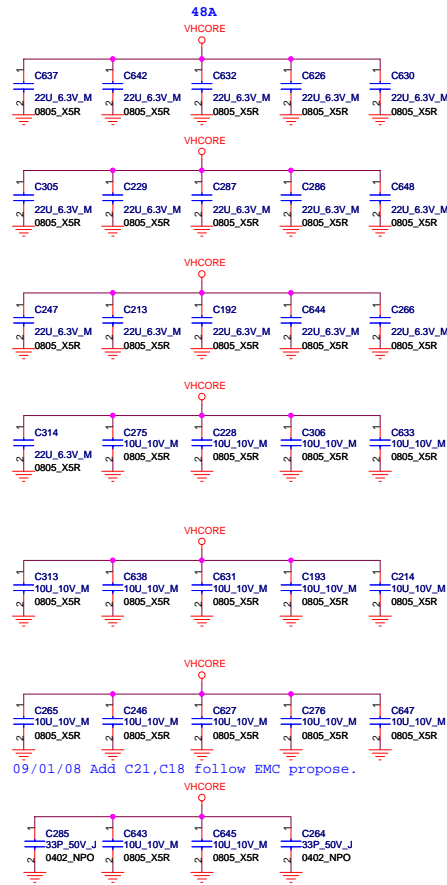
SOCKET\_988P  
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DDR SYSTEM MEMORY - B



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Title: **Arrandale (DDR3)**  
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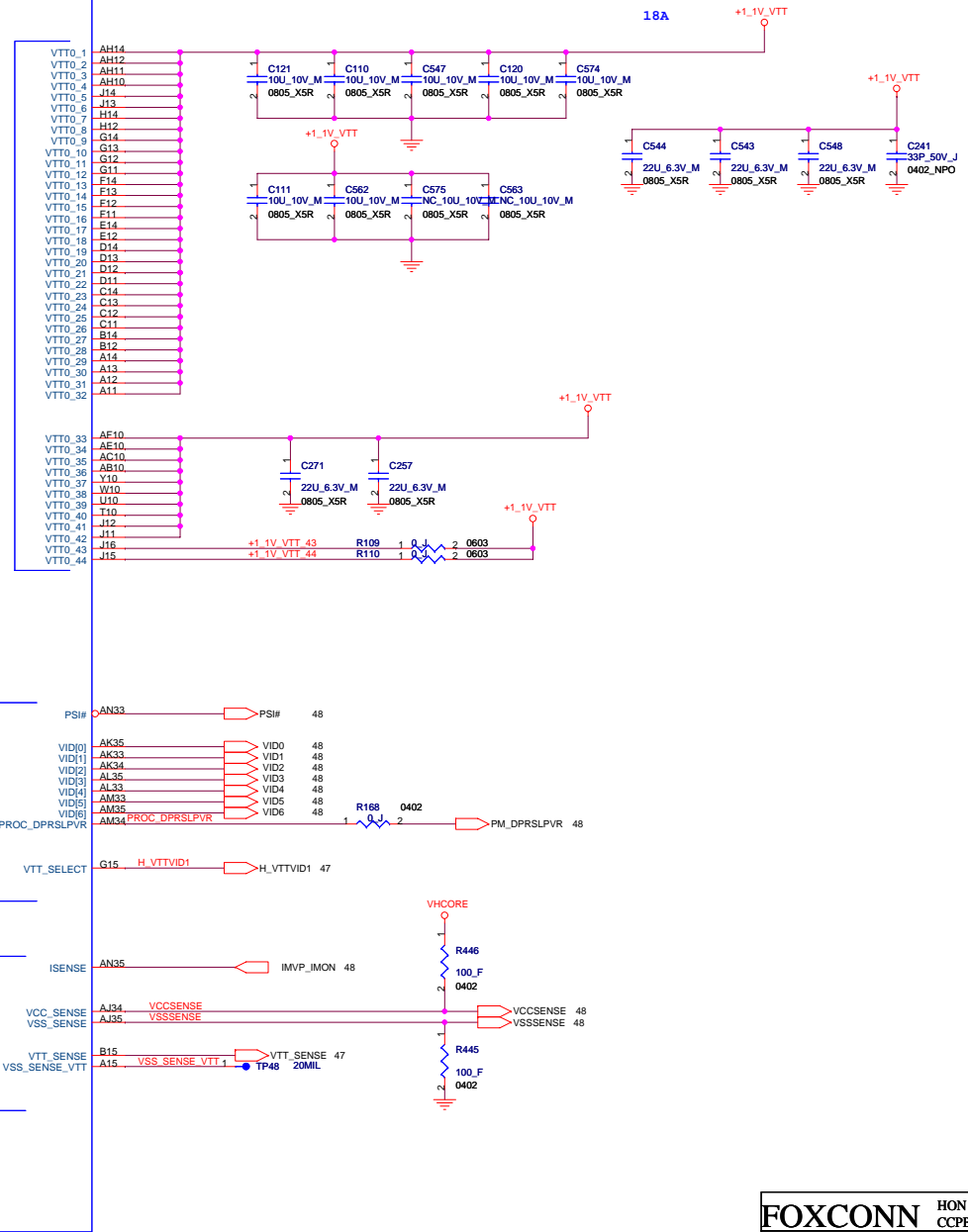


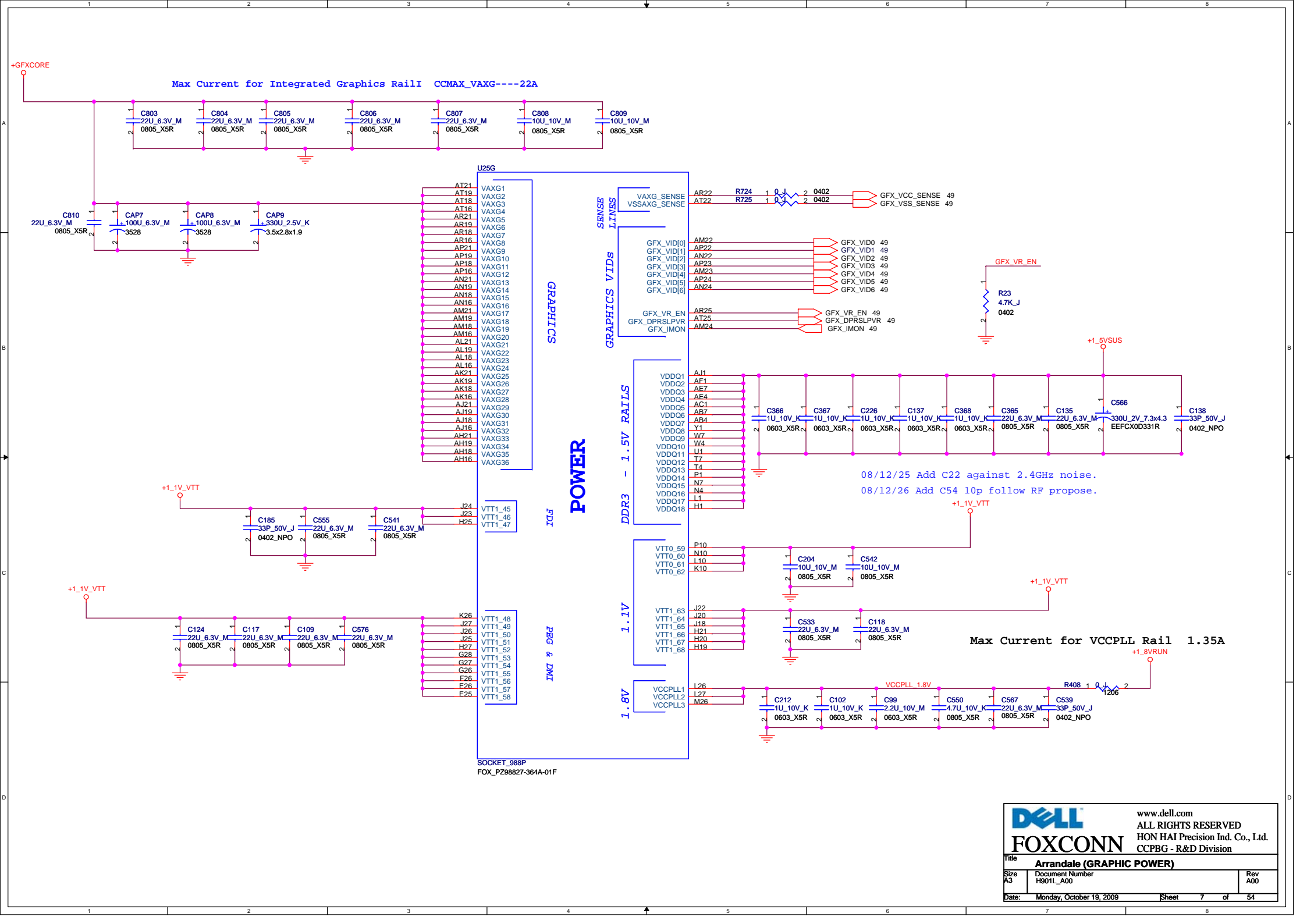
09/01/08 Add C21,C18 follow EMC propose.

- U25F
- AG35 VCC1
  - AG34 VCC2
  - AG33 VCC3
  - AG32 VCC4
  - AG31 VCC5
  - AG30 VCC6
  - AG29 VCC7
  - AG28 VCC8
  - AG27 VCC9
  - AG26 VCC10
  - AF35 VCC11
  - AF34 VCC12
  - AF33 VCC13
  - AF32 VCC14
  - AF31 VCC15
  - AF30 VCC16
  - AF29 VCC17
  - AF28 VCC18
  - AF27 VCC19
  - AF26 VCC20
  - AD35 VCC21
  - AD34 VCC22
  - AD33 VCC23
  - AD32 VCC24
  - AD31 VCC25
  - AD30 VCC26
  - AD29 VCC27
  - AD28 VCC28
  - AD27 VCC29
  - AD26 VCC30
  - AC35 VCC31
  - AC34 VCC32
  - AC33 VCC33
  - AC32 VCC34
  - AC31 VCC35
  - AC30 VCC36
  - AC29 VCC37
  - AC28 VCC38
  - AC27 VCC39
  - AC26 VCC40
  - AA35 VCC41
  - AA34 VCC42
  - AA33 VCC43
  - AA32 VCC44
  - AA31 VCC45
  - AA30 VCC46
  - AA29 VCC47
  - AA28 VCC48
  - AA27 VCC49
  - AA26 VCC50
  - Y35 VCC51
  - Y34 VCC52
  - Y33 VCC53
  - Y32 VCC54
  - X31 VCC55
  - X30 VCC56
  - Y29 VCC57
  - Y28 VCC58
  - Y27 VCC59
  - Y26 VCC60
  - Y25 VCC61
  - Y24 VCC62
  - Y23 VCC63
  - Y22 VCC64
  - V31 VCC65
  - V30 VCC66
  - V29 VCC67
  - V28 VCC68
  - V27 VCC69
  - V26 VCC70
  - U35 VCC71
  - U34 VCC72
  - U33 VCC73
  - U32 VCC74
  - U31 VCC75
  - U30 VCC76
  - U29 VCC77
  - U28 VCC78
  - U27 VCC79
  - U26 VCC80
  - R35 VCC81
  - R34 VCC82
  - R33 VCC83
  - R32 VCC84
  - R31 VCC85
  - R30 VCC86
  - R29 VCC87
  - R28 VCC88
  - R27 VCC89
  - R26 VCC90
  - P35 VCC91
  - P34 VCC92
  - P33 VCC93
  - P32 VCC94
  - P31 VCC95
  - F30 VCC96
  - P29 VCC97
  - P28 VCC98
  - E27 VCC99
  - P26 VCC100

SOCKET\_988P  
FOX\_PZ98827-364A-01F

POWER  
CPU CORE SUPPLY  
1.1V RAIL POWER  
SENSE VIDS





Max Current for Integrated Graphics Rail I CCMAX\_VAXG----22A

U25G

GRAPHICS

POWER

FPD

BEG & DMT

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

1.1V

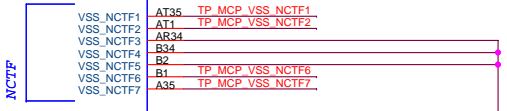
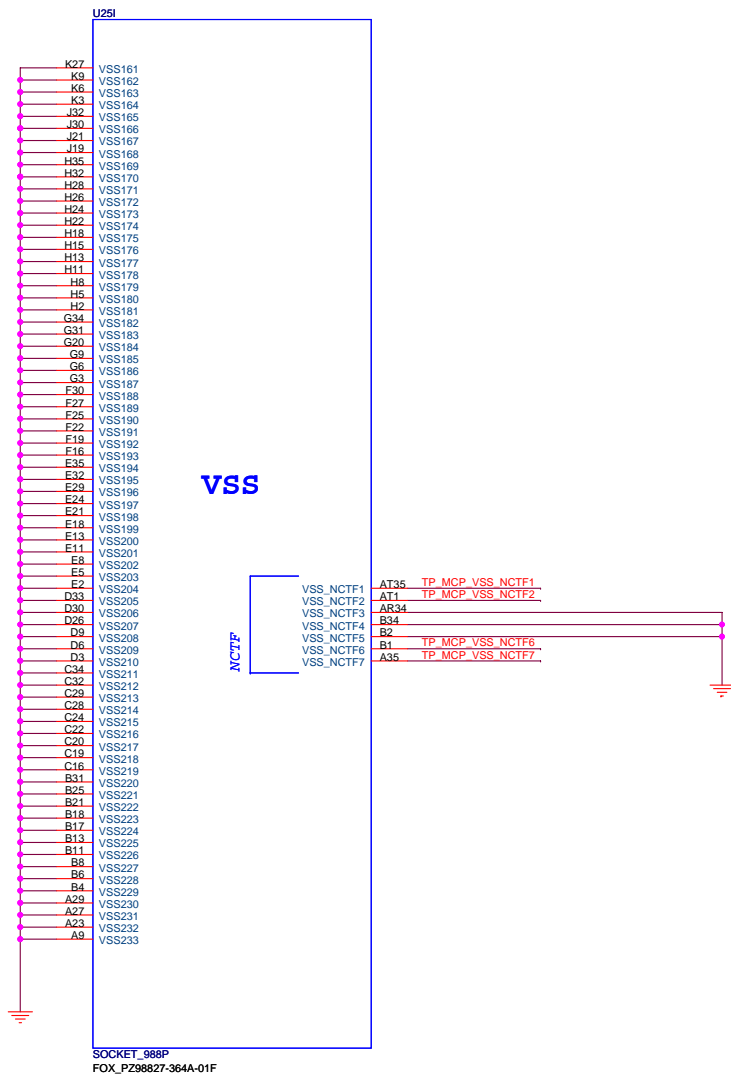
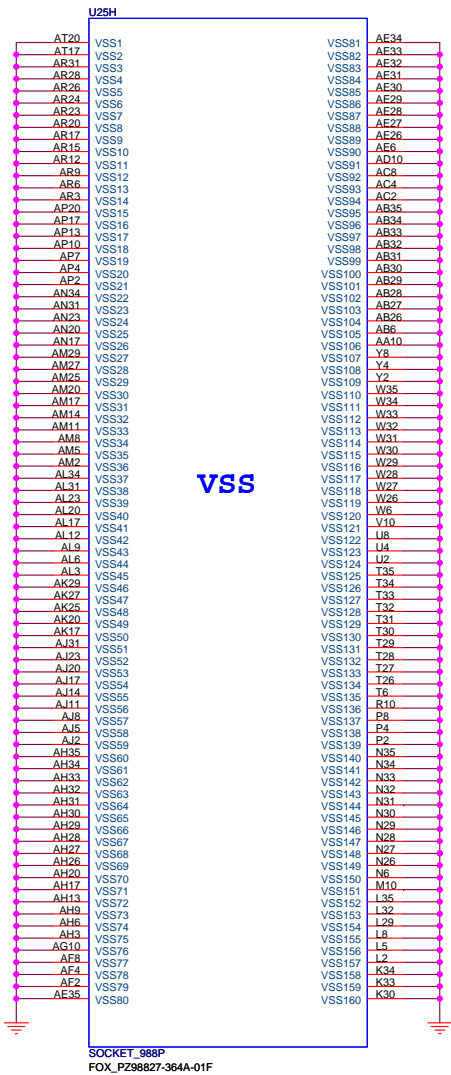
1.8V

SOCKET\_988P  
FOX\_PZ98827-364A-01F

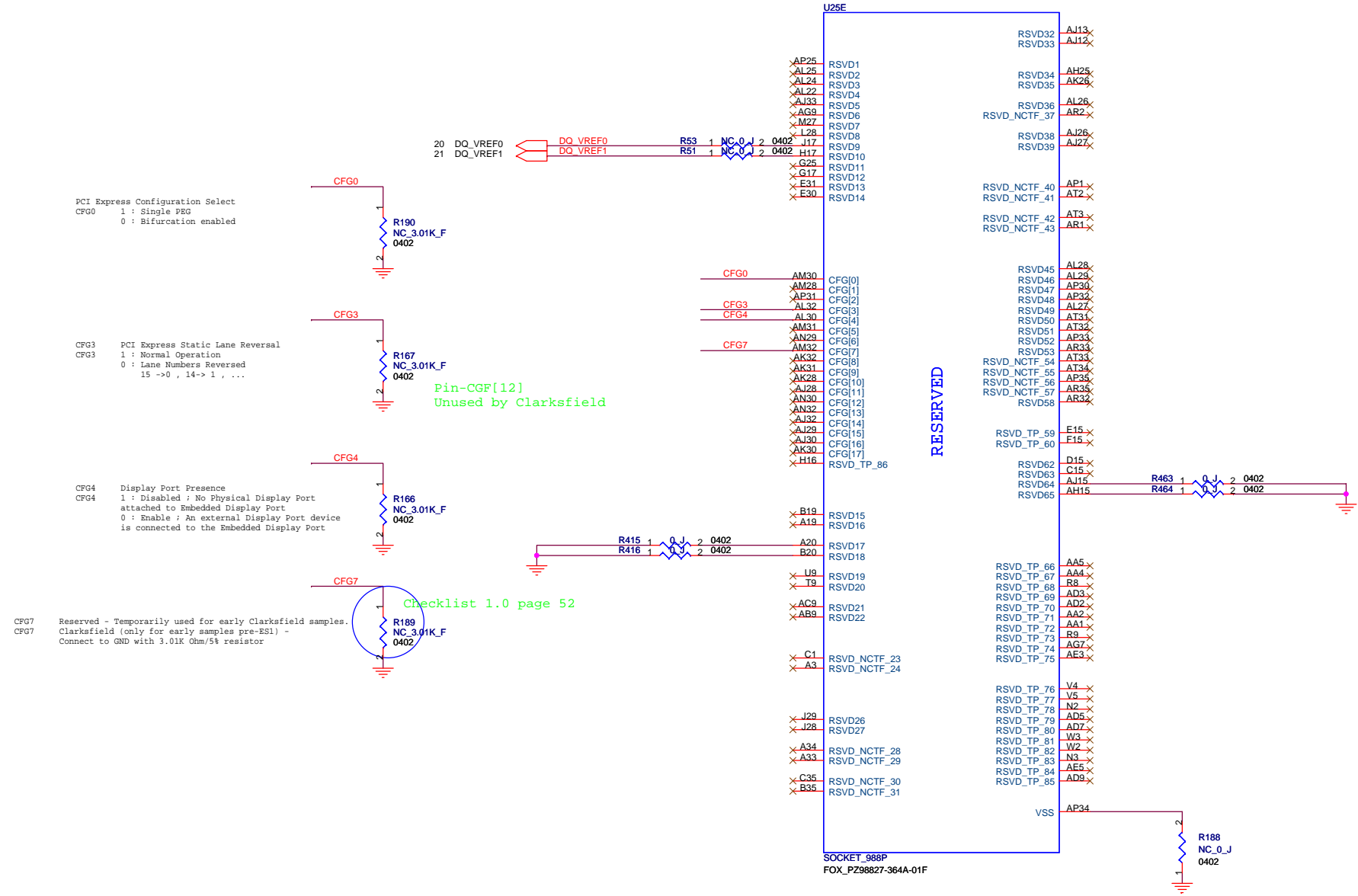
08/12/25 Add C22 against 2.4GHz noise.  
08/12/26 Add C54 10p follow RF propose.

Max Current for VCCPLL Rail 1.35A

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PCI Express Configuration Select  
 CFG0 1 : Single PBG  
 0 : Bifurcation enabled

CFG3 PCI Express Static Lane Reversal  
 CFG3 1 : Normal Operation  
 0 : Lane Numbers Reversed  
 15 -> 0 , 14 -> 1 , ...

CFG4 Display Port Presence  
 CFG4 1 : Disabled ; No Physical Display Port  
 attached to Embedded Display Port  
 0 : Enable ; An external Display Port device  
 is connected to the Embedded Display Port

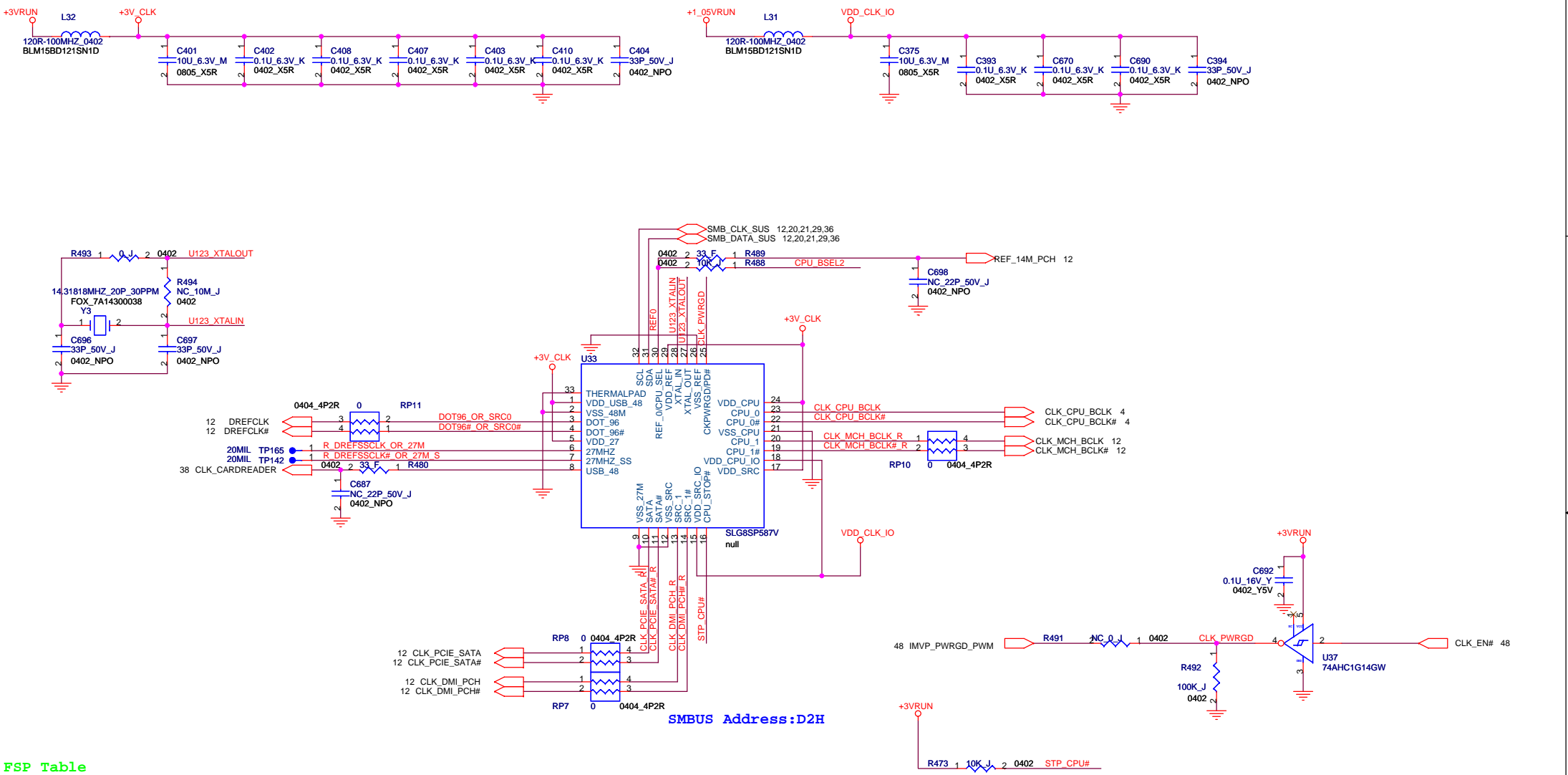
CFG7 Reserved - Temporarily used for early Clarksfield samples.  
 Clarksfield (only for early samples pre-ES1) -  
 Connect to GND with 3.01K Ohm/5% resistor

Pin-CGF[12]  
 Unused by Clarksfield

Checklist 1.0 page 52

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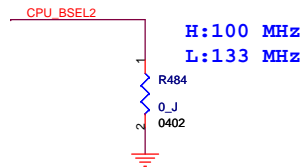
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FSP Table

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

08/12/31 Delete R5497.



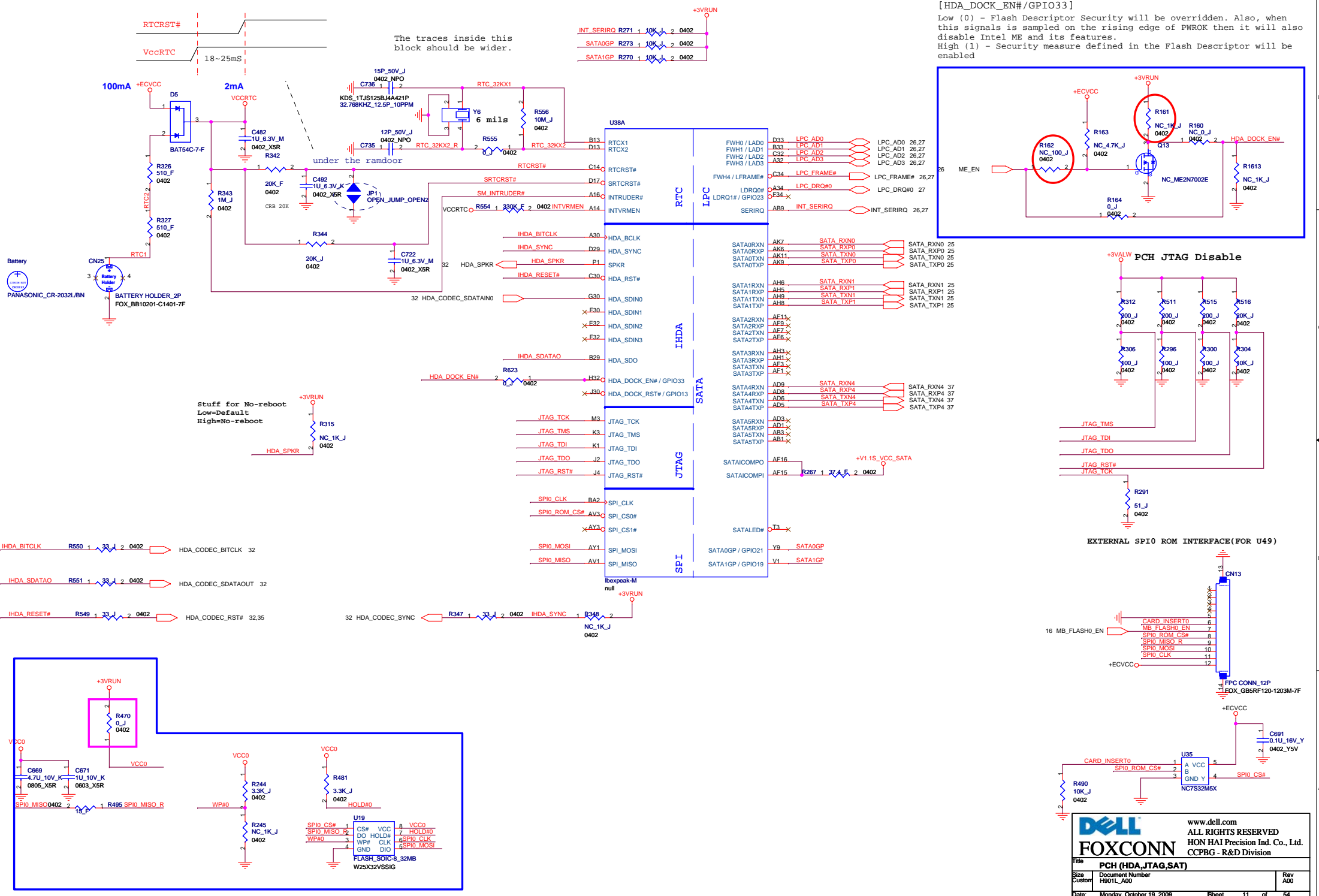
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**FOXCONN**

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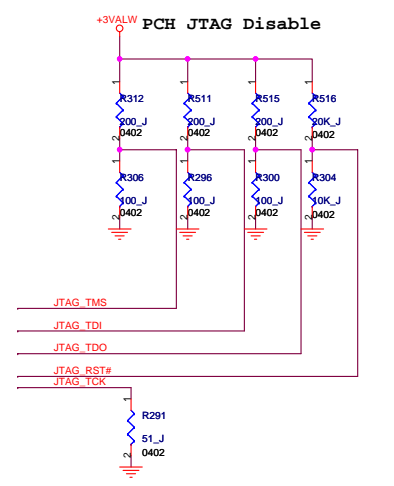
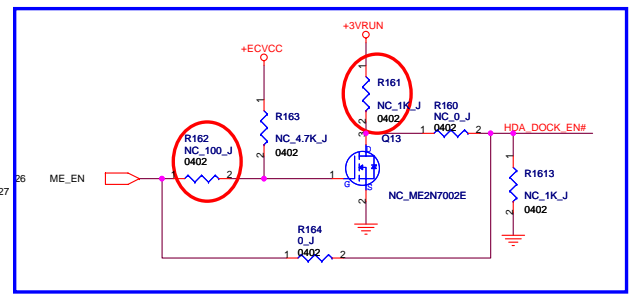
Title: **CLOCK GEN**

Size: A3	Document Number: H901L_A00	Rev: A00
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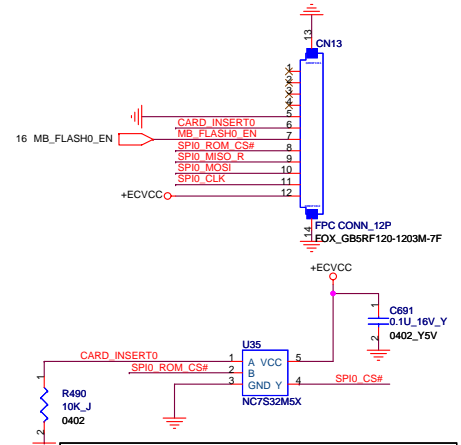
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[HDA\_DOCK\_EN# / GPIO33]  
Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.  
High (1) - Security measure defined in the Flash Descriptor will be enabled



EXTERNAL SPI0 ROM INTERFACE (FOR U49)

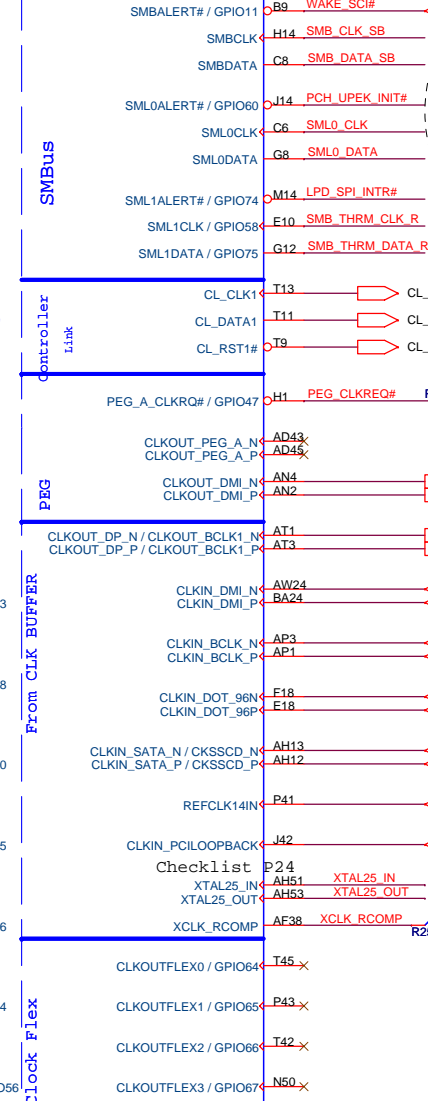
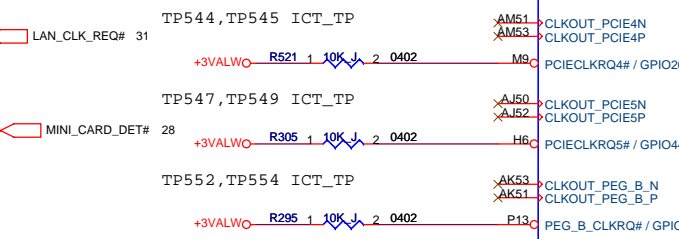
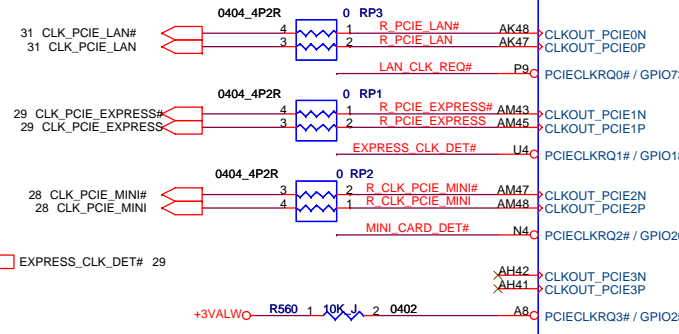
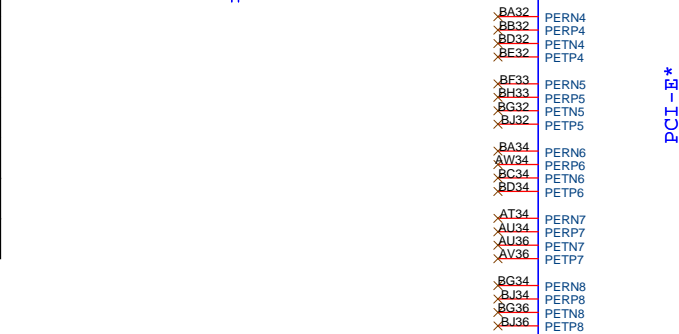
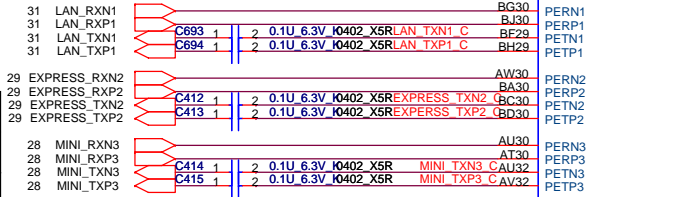


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Title	PCH (HDA, JTAG, SAT)		
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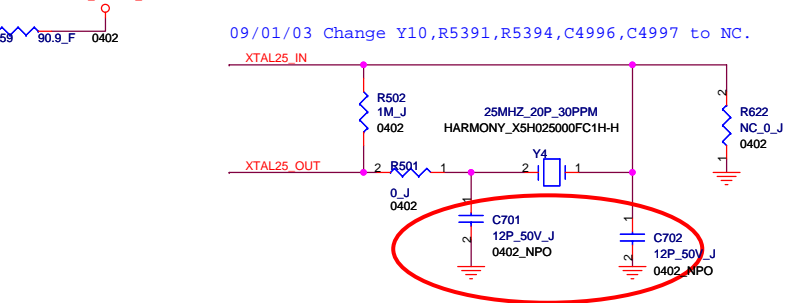
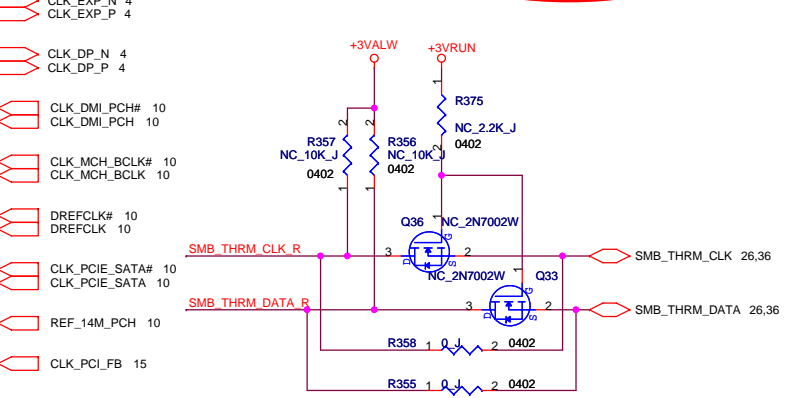
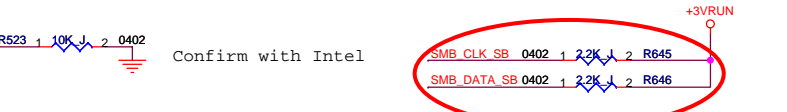
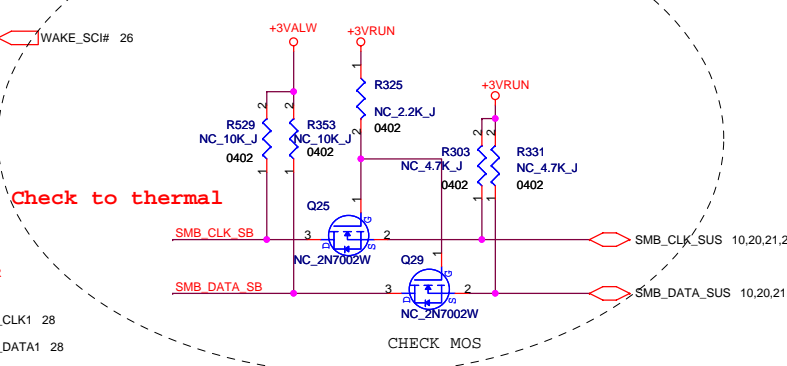
08/12/24 Update PCIe Port follow Mor-side Propose.

PCI-E Port Table

Port	Function
Port1	LAN
Port2	Express Card
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used



SMB\_CLK\_SB R527 1 0 J 2 0402 SMB\_CLK\_SUS  
SMB\_DATA\_SB R336 1 0 J 2 0402 SMB\_DATA\_SUS



08/12/24 Change CLKREQ pull up Power, LAN => +3VSUS, MINICARD=>+3VSUS, TV=> +3VRUN, Mach => +3VRUN.

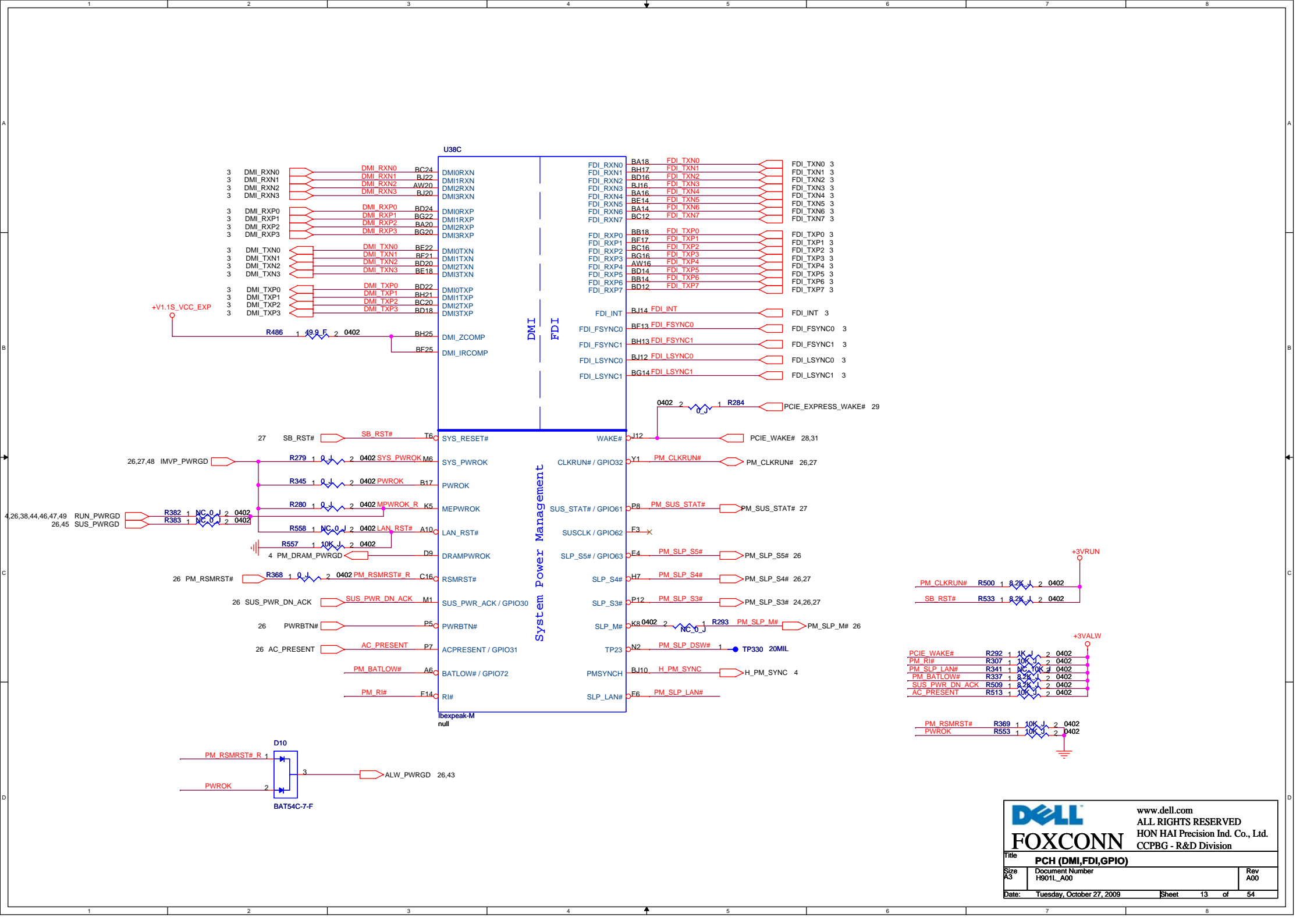
- WAKE\_SCI# R559 1 10K J 2 0402
- PCH\_UPEK\_INIT# R522 1 10K J 2 0402
- LPD\_SPI\_INTR# R517 1 10K J 2 0402
- SML0\_CLK R338 1 2.2K J 2 0402
- SML0\_DATA R339 1 2.2K J 2 0402

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**FOXCONN**

Title: **PCH (PCI-E, SMBUS, CLK)**  
Size: A3  
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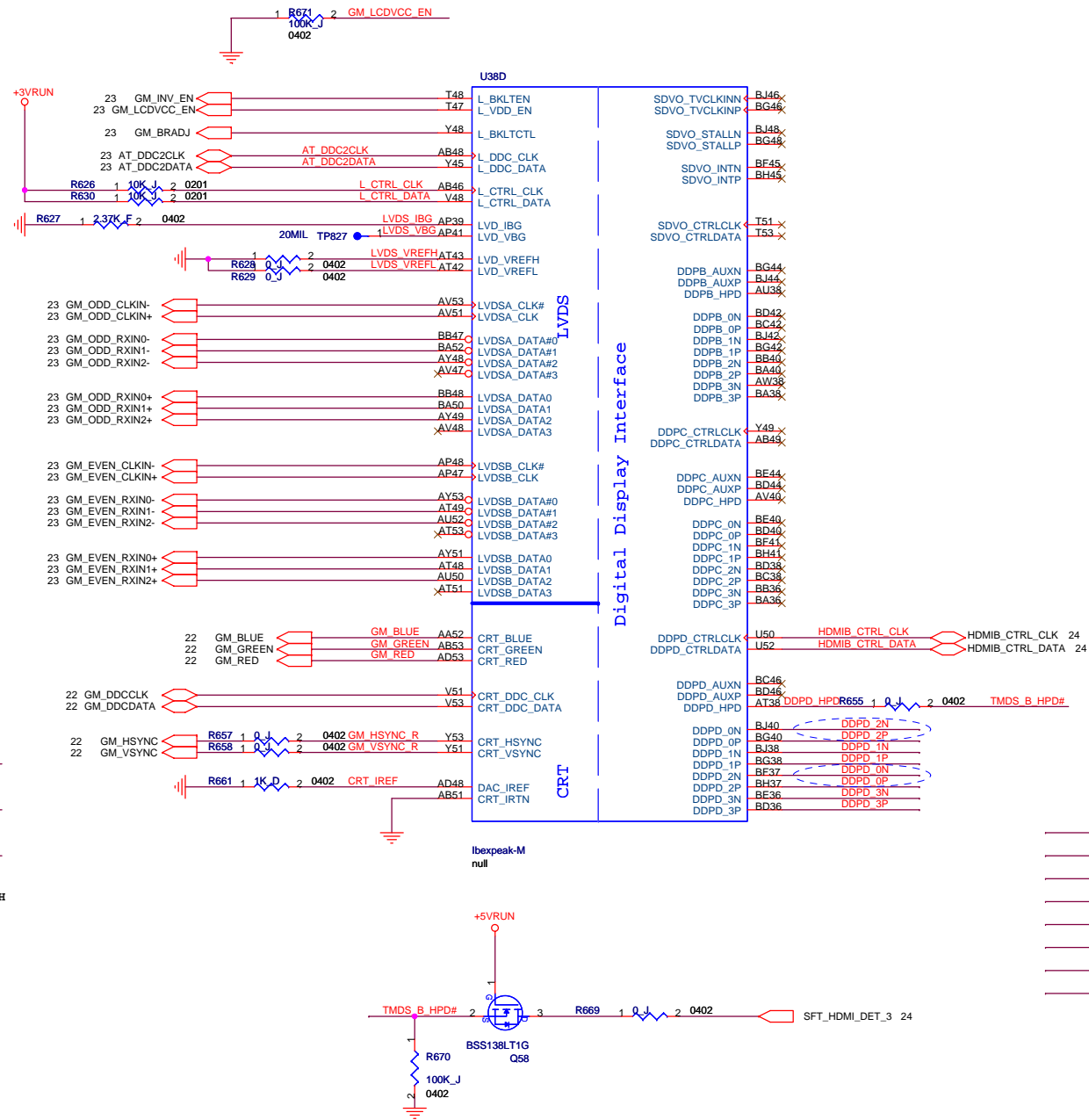
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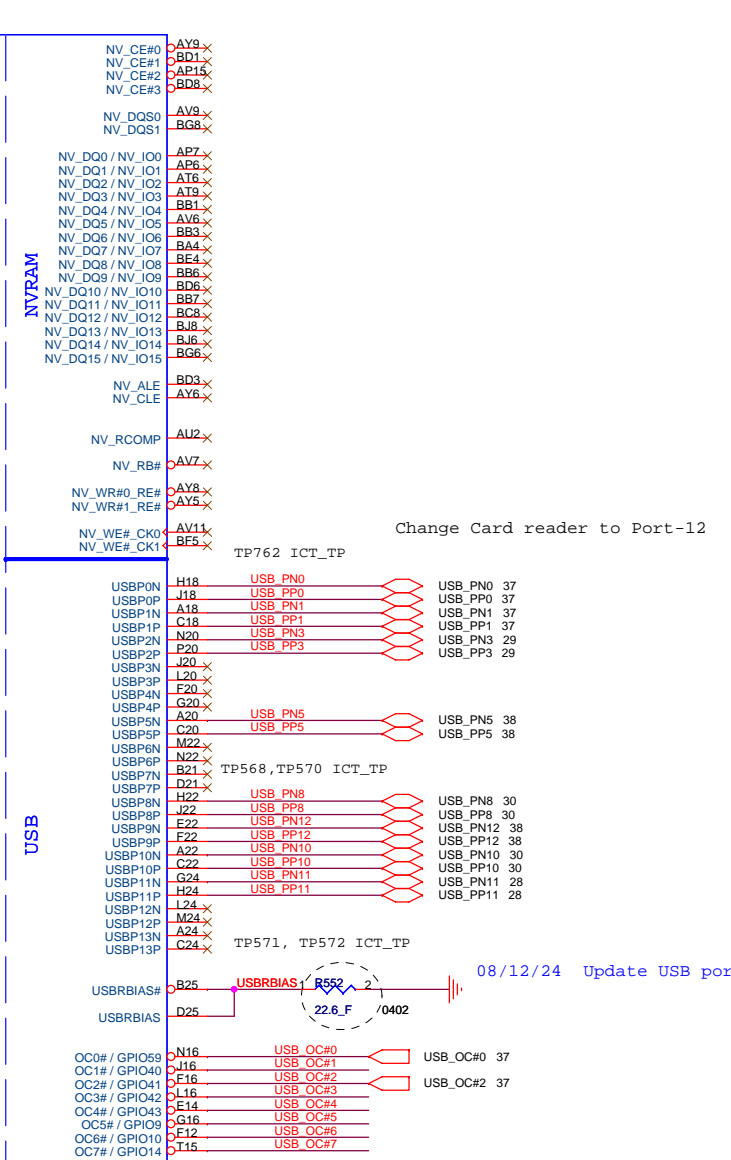
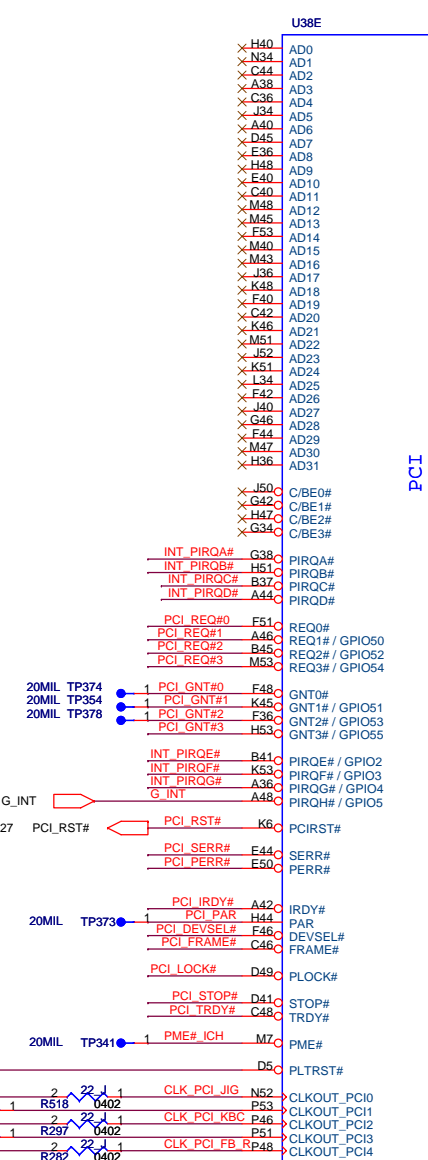
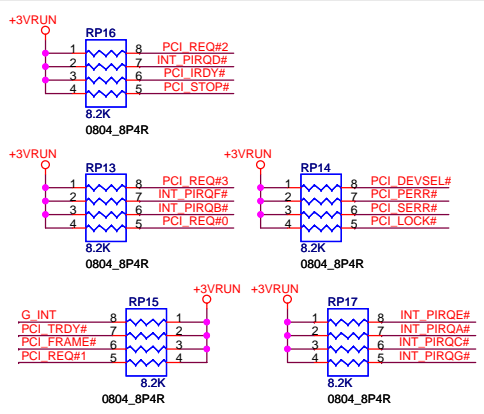
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Title: **PCH (DMI,FDI,GPIO)**

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DDPD_3P	1	2	TMDS_B_CLK	TMDS_B_CLK#	24
C782	0.1U_6.3V_K	0201_X5R	TMDS_B_CLK#	TMDS_B_CLK#	24
DDPD_3N	1	2	TMDS_B_CLK#	TMDS_B_CLK#	24
C783	0.1U_6.3V_K	0201_X5R	TMDS_B_DATA2	TMDS_B_DATA2#	24
DDPD_2P	1	2	TMDS_B_DATA2#	TMDS_B_DATA2#	24
C784	0.1U_6.3V_K	0201_X5R	TMDS_B_DATA1#	TMDS_B_DATA1#	24
DDPD_2N	1	2	TMDS_B_DATA1#	TMDS_B_DATA1#	24
C785	0.1U_6.3V_K	0201_X5R	TMDS_B_DATA0#	TMDS_B_DATA0#	24
DDPD_1P	1	2	TMDS_B_DATA0#	TMDS_B_DATA0#	24
C786	0.1U_6.3V_K	0201_X5R	TMDS_B_DATA0#	TMDS_B_DATA0#	24
DDPD_1N	1	2	TMDS_B_DATA0#	TMDS_B_DATA0#	24
C787	0.1U_6.3V_K	0201_X5R	TMDS_B_DATA0#	TMDS_B_DATA0#	24
DDPD_0P	1	2	TMDS_B_DATA0#	TMDS_B_DATA0#	24
C788	0.1U_6.3V_K	0201_X5R	TMDS_B_DATA0#	TMDS_B_DATA0#	24
DDPD_0N	1	2	TMDS_B_DATA0#	TMDS_B_DATA0#	24
C789	0.1U_6.3V_K	0201_X5R	TMDS_B_DATA0#	TMDS_B_DATA0#	24

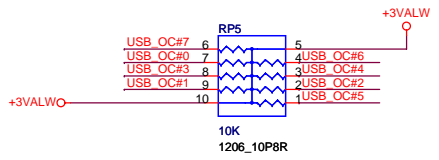
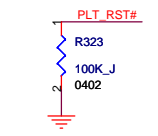
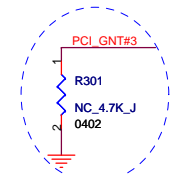


**DMI Termination Voltage**

NV_CLE	Set to Vss when LOW	
	Set to Vcc when HIGH	

**Danbury Technology**  
Disabled when Low  
Enabled when High

USB PORT	Function	OC pin
PORT-0	Ext. Port	
PORT-1	Ext. Port	
PORT-2	EXPRESS CARD	
PORT-3		
PORT-4		
PORT-5	Ext. Port	
PORT-6		
PORT-7		
PORT-8	Bluetooth	
PORT-9	Card reader	
PORT-10	Camera	
PORT-11	WLAN/WiMAX	
PORT-12		
PORT-13		



Check list P39 need to pull up to 3.3VA with 8.3K-10K

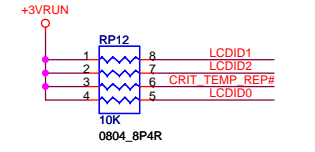
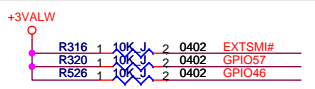
08/12/24 Update USB port.

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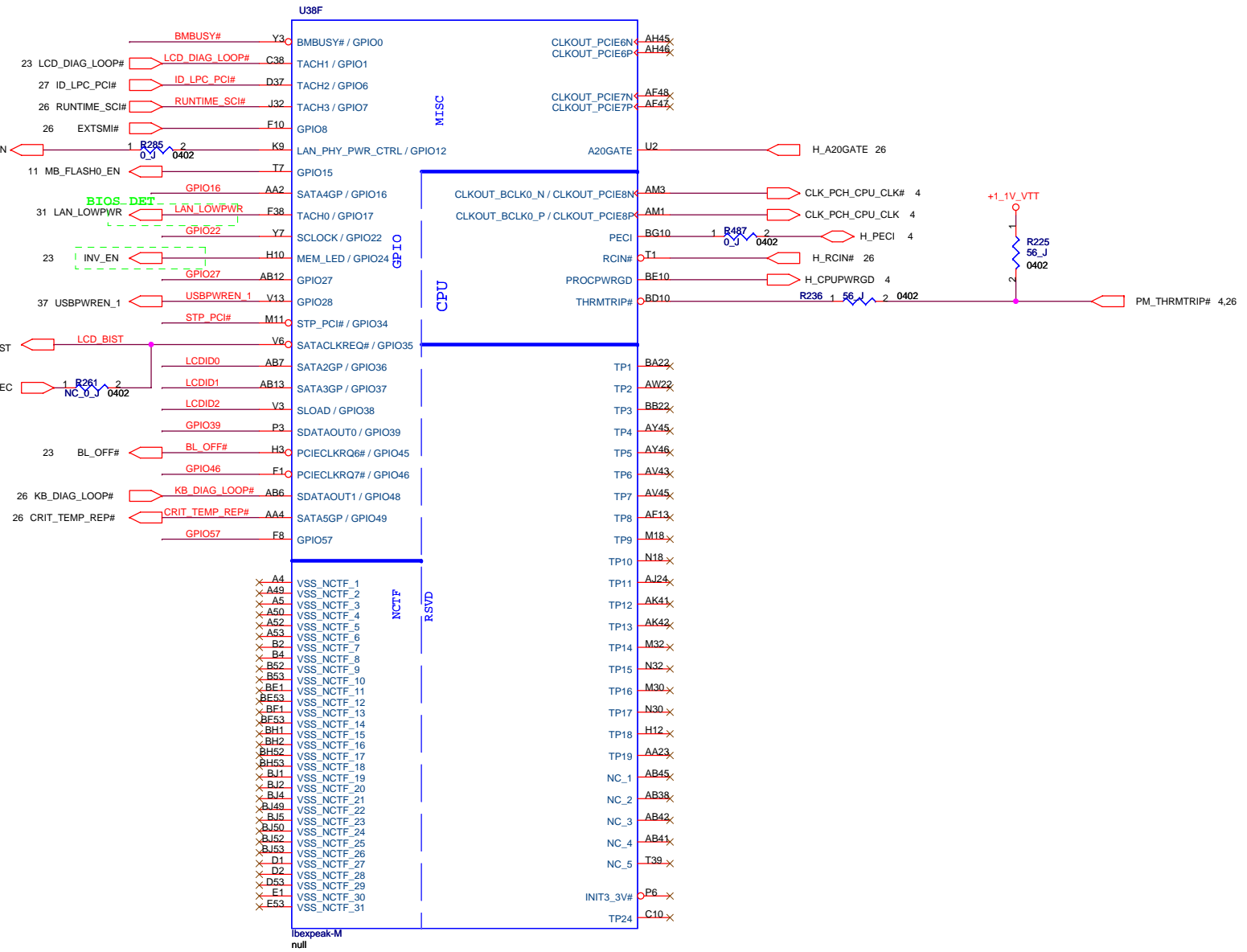
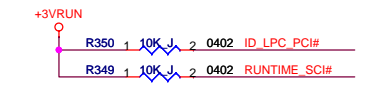
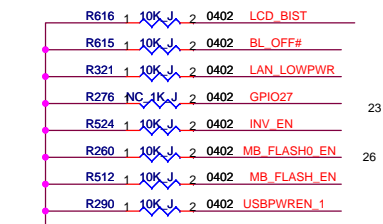
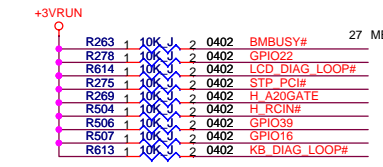
FOXCONN

Title: **PCH (PCI,USB,NVRAM)**

Size: A3	Document Number: H901L_A00	Rev: A00
Date: Monday, October 19, 2009	Sheet 15 of 54	

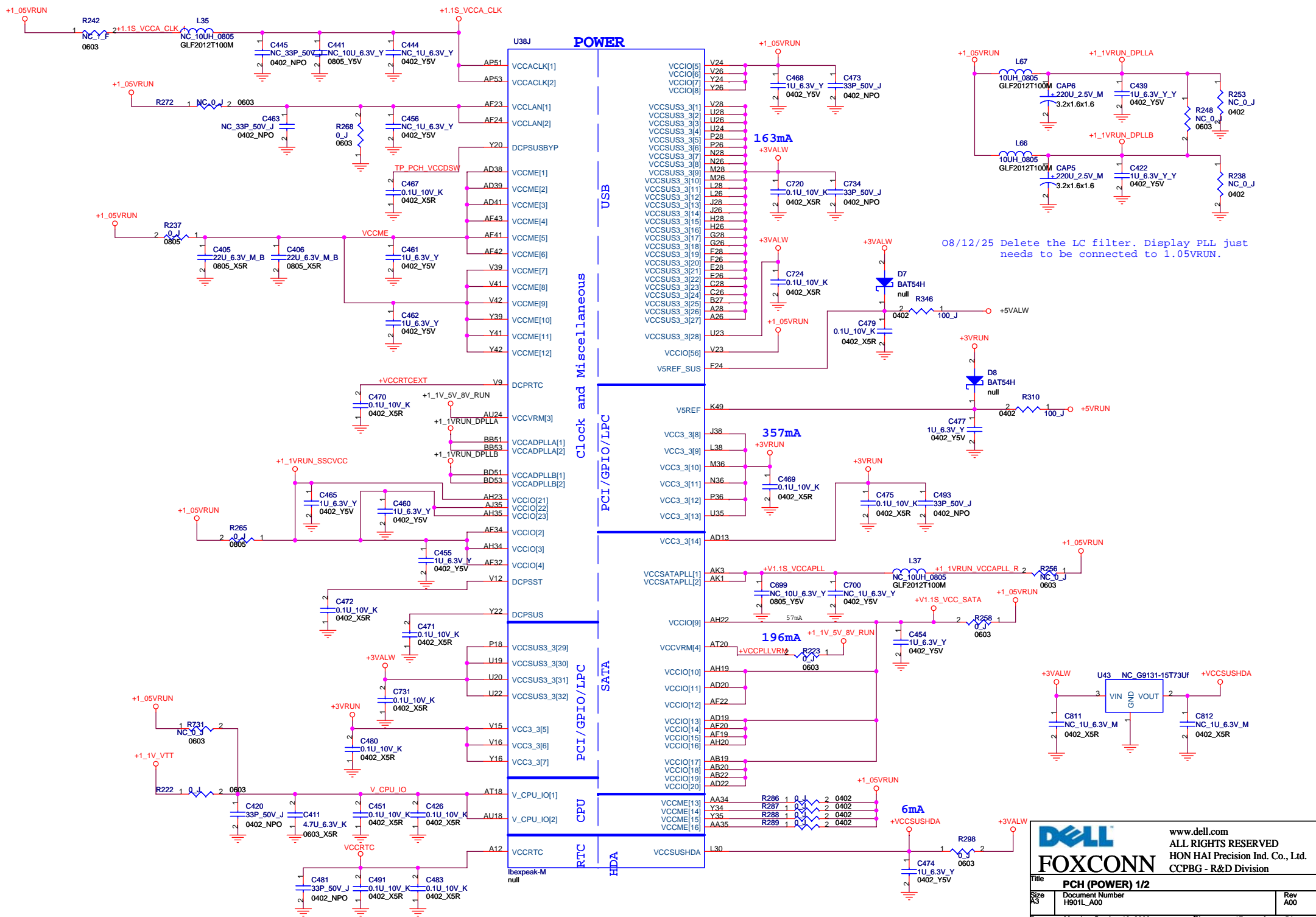


09/01/14 Add R98



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		CCPBG - R&D Division	
Title: <b>PCH (GPIO,VSS_NCTF,RSVD)</b>			
Size: A3	Document Number: H901L_A00	Rev: A00	
Date: Monday, October 19, 2009		Sheet: 16	of: 54





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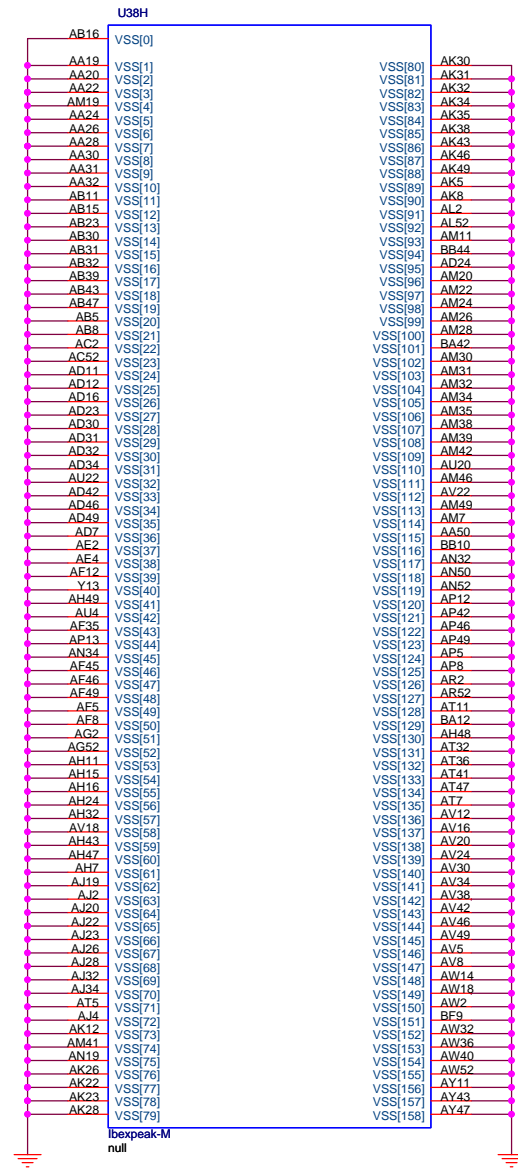
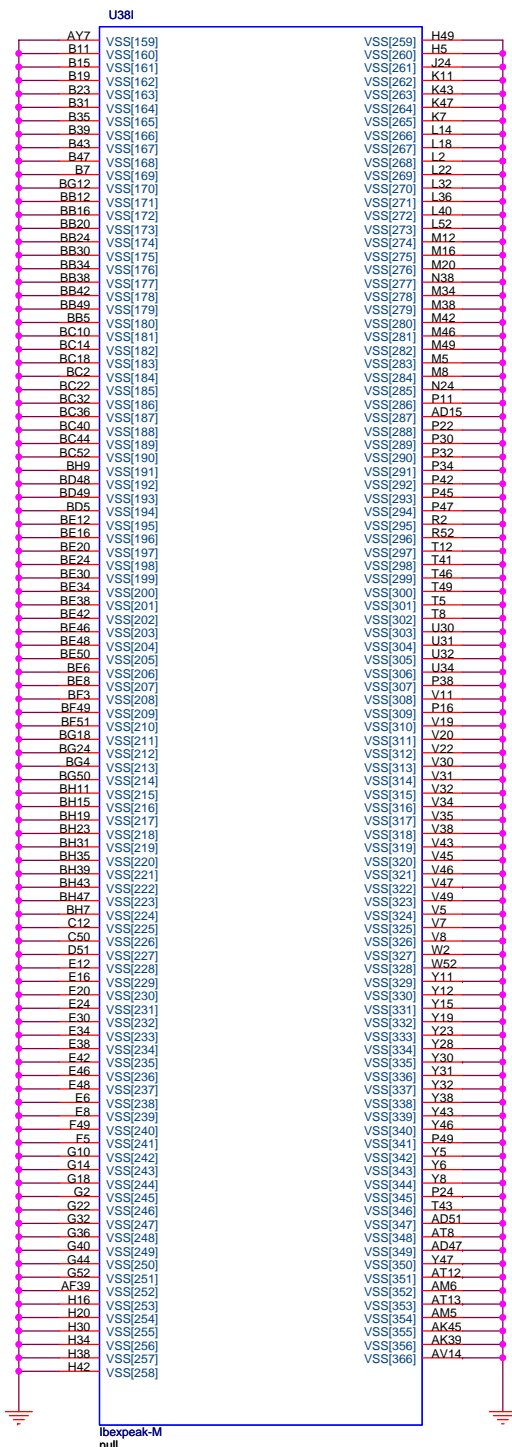
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Title: **PCH (POWER) 1/2**

Size: A3	Document Number: H901L_A00	Rev: A00
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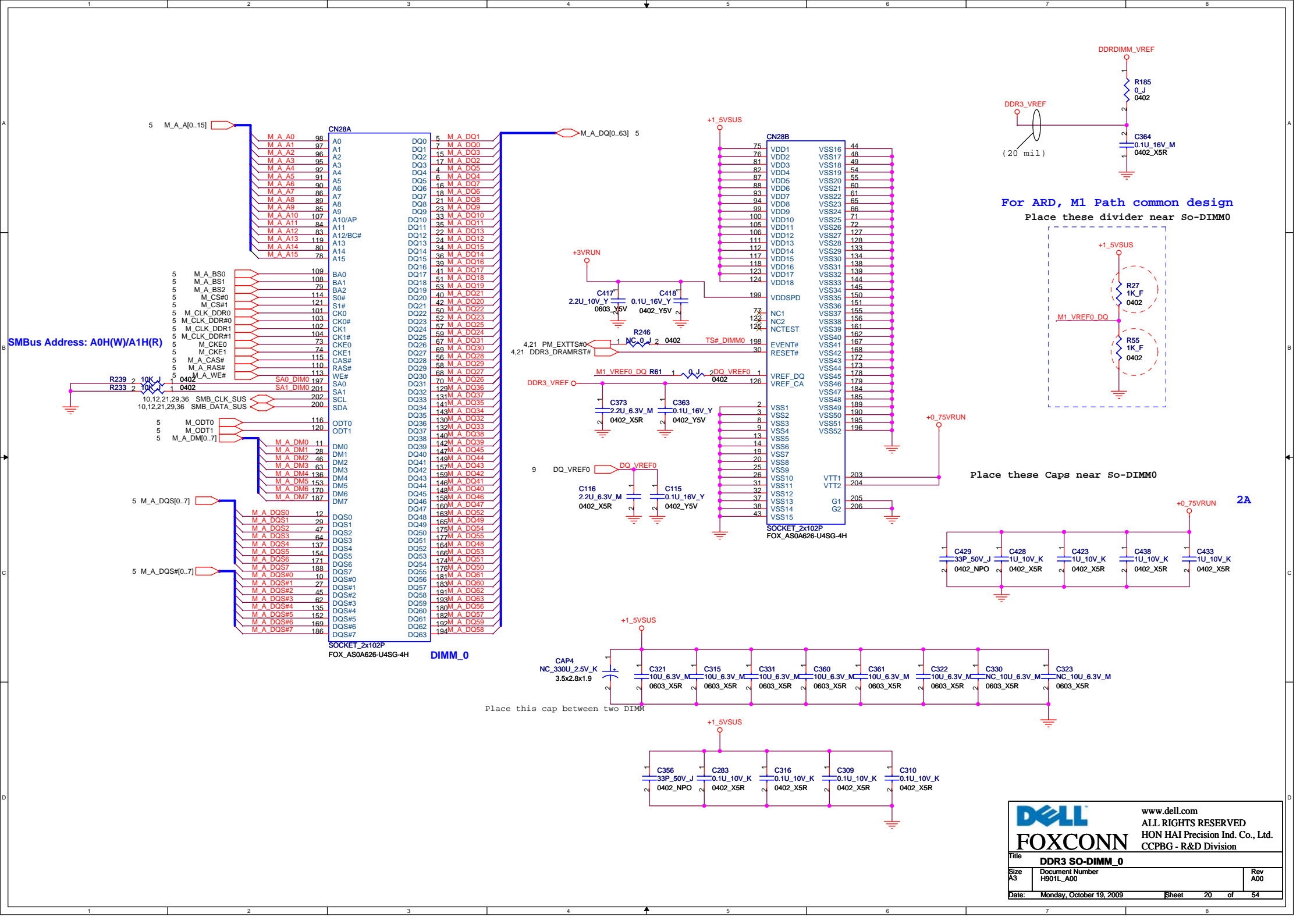
Date: Monday, October 19, 2009 Sheet 17 of 54



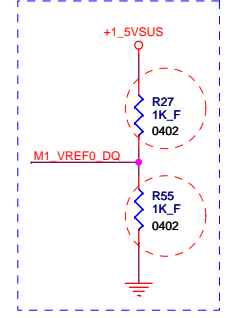


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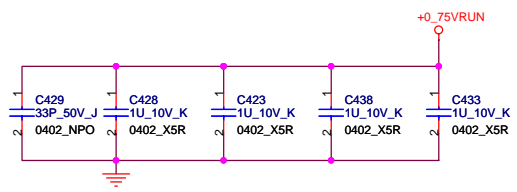
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 Size: A3 Document Number: H901L\_A00 Rev: A00  
 Date: Monday, October 19, 2009 Sheet 19 of 54



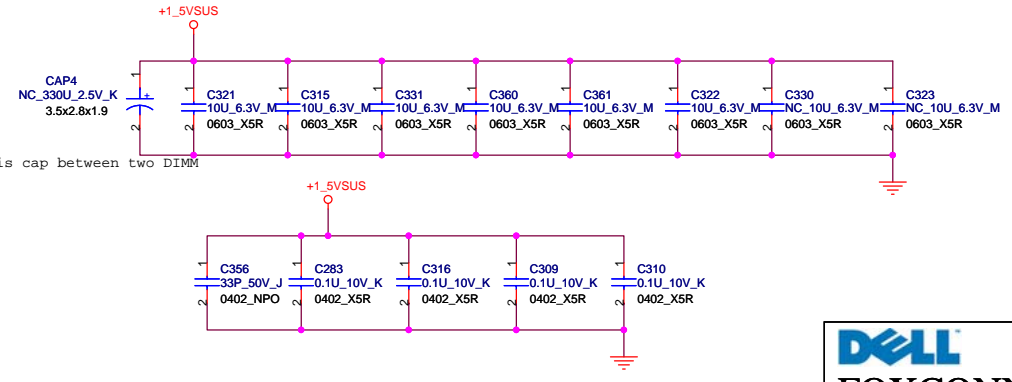
For ARD, M1 Path common design  
Place these divider near So-DIMM0



Place these Caps near So-DIMM0

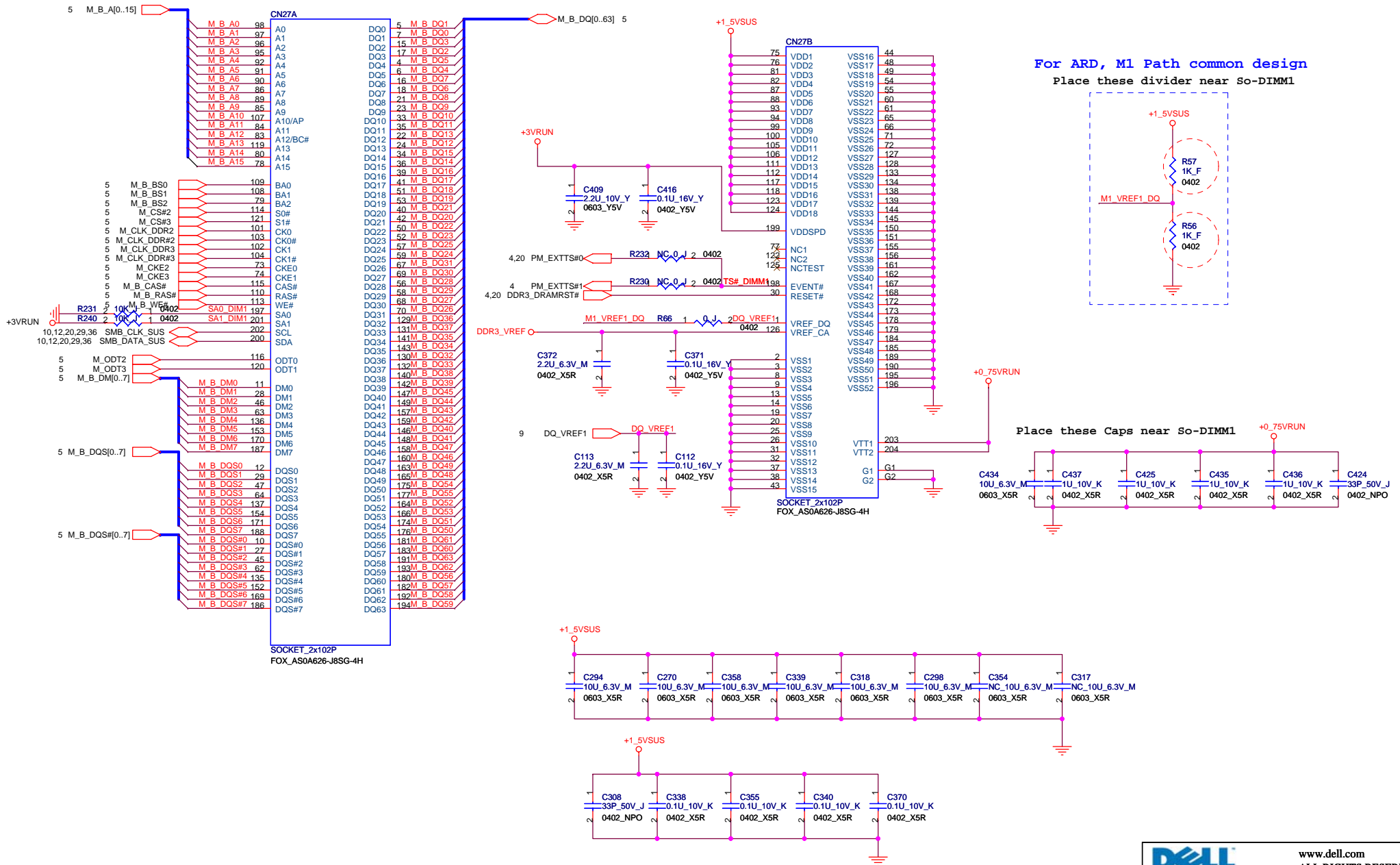


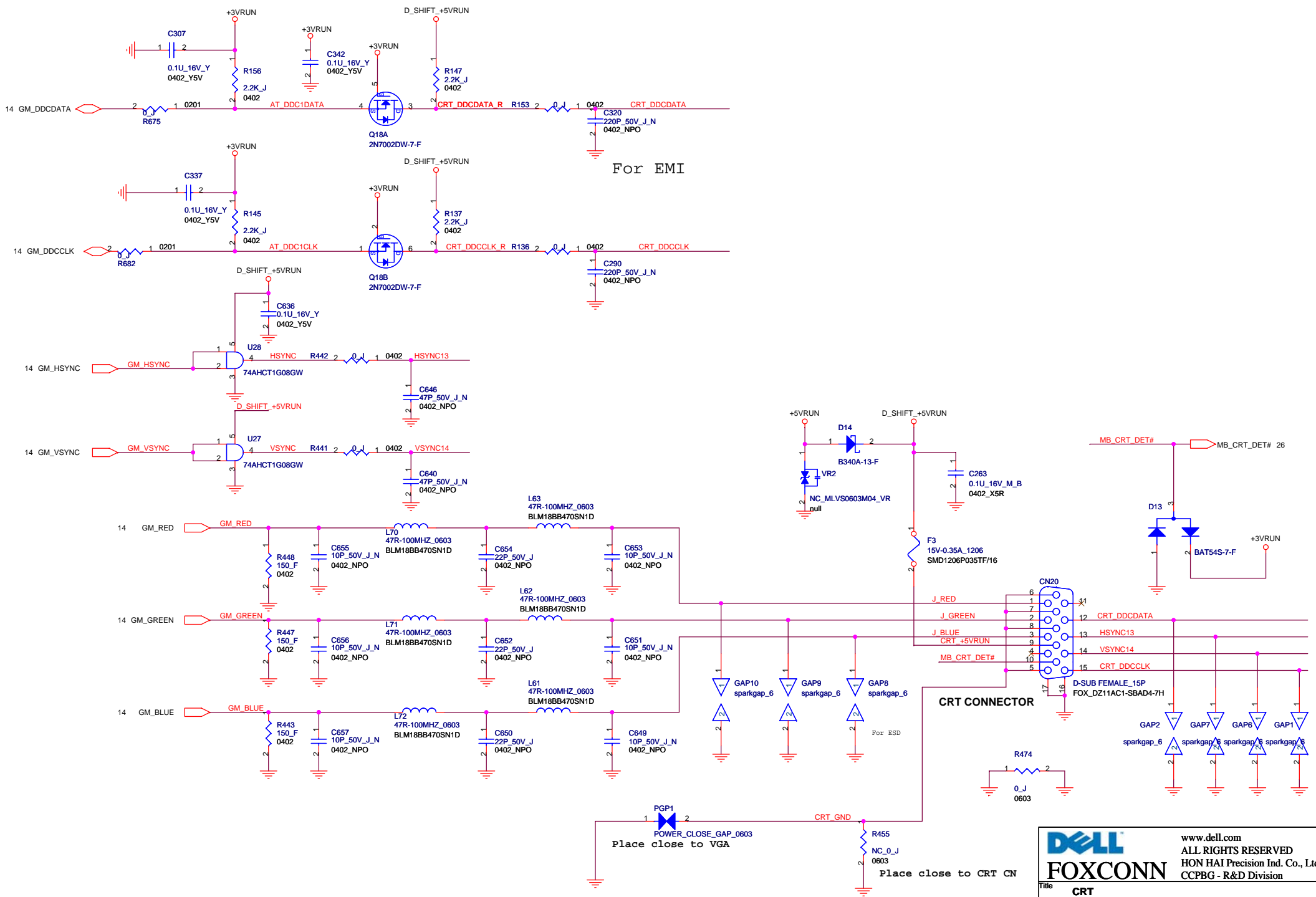
Place this cap between two DIMM



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Title <b>DDR3 SO-DIMM 0</b>		
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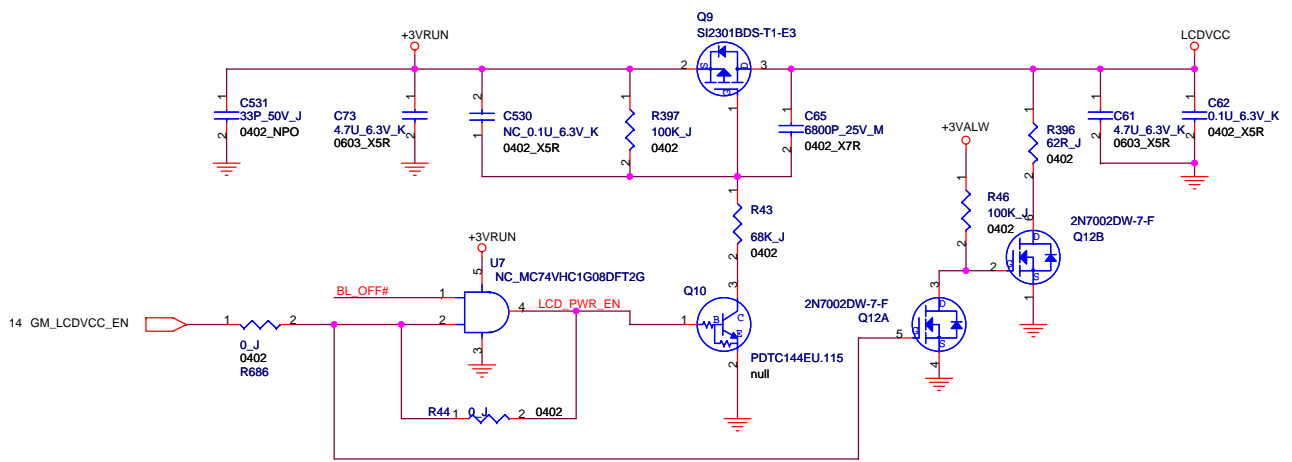
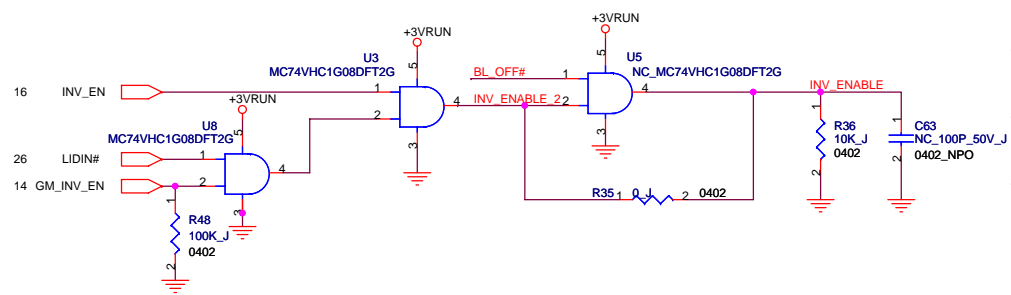
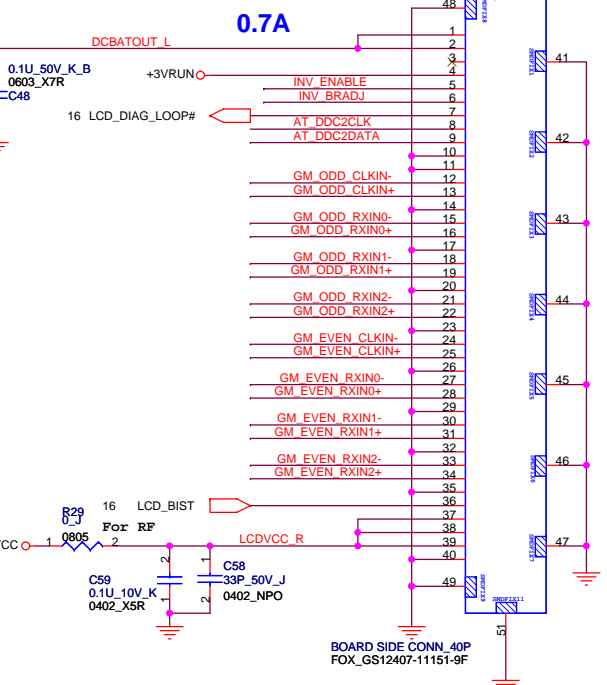
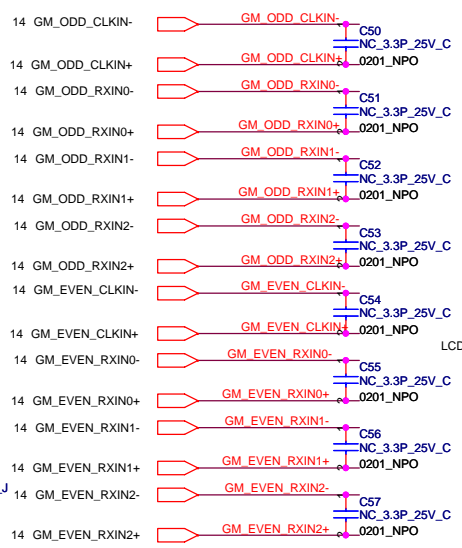
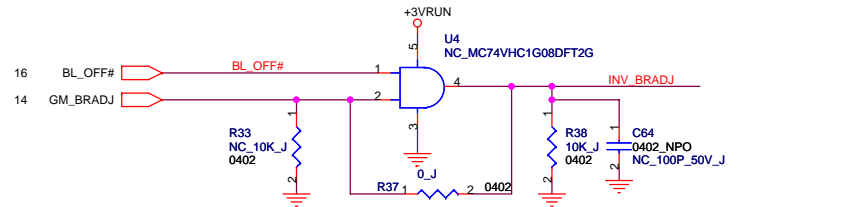
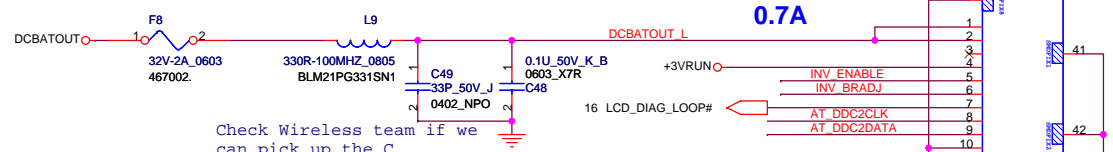
For EMI

PGP1  
POWER\_CLOSE\_GAP\_0603  
Place close to VGA

For ESD

R455  
NC\_0\_J  
0603  
Place close to CRT CN

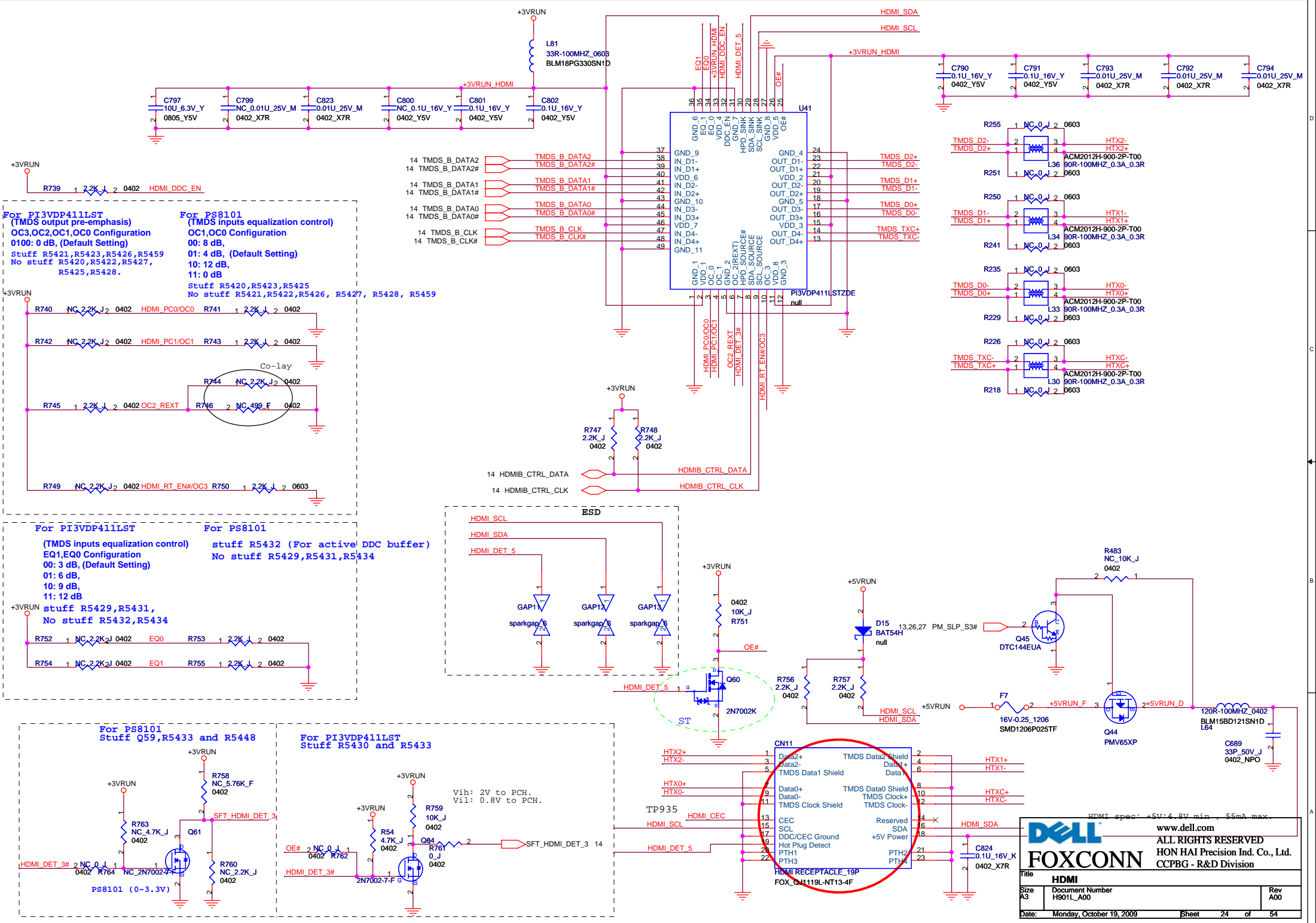
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Title <b>CRT</b>			
Size A3	Document Number H901L_A00	Rev A00	
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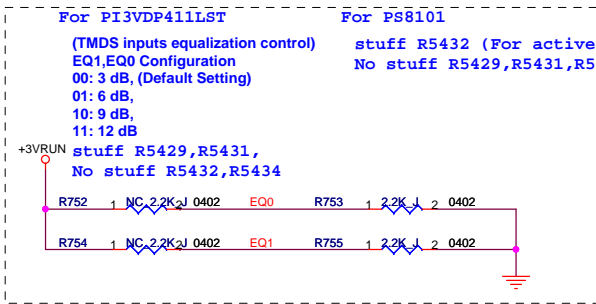
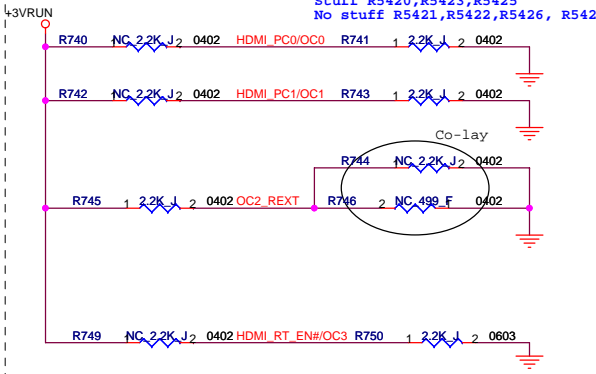
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Title: <b>LVDS</b>		
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**For PI3VDP411LST (TMDS output pre-emphasis)**  
 OC3,OC2,OC1,OC0 Configuration  
 0100: 0 dB, (Default Setting)  
 stuff R5421,R5423,R5426,R5459  
 No stuff R5420,R5422,R5427,  
 R5425,R5428.

**For PS8101 (TMDS inputs equalization control)**  
 OC1,OC0 Configuration  
 00: 8 dB,  
 01: 4 dB, (Default Setting)  
 10: 12 dB,  
 11: 0 dB  
 stuff R5420,R5423,R5425  
 No stuff R5421,R5422,R5426, R5427, R5428, R5459



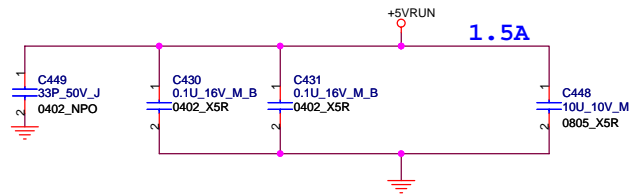
HDMI spec: +5V:4.8V min, 55mA max.

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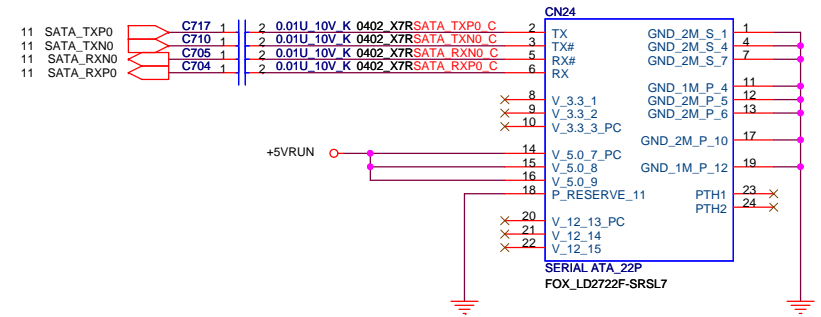
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Title	HDMI	
Size	Document Number	Rev
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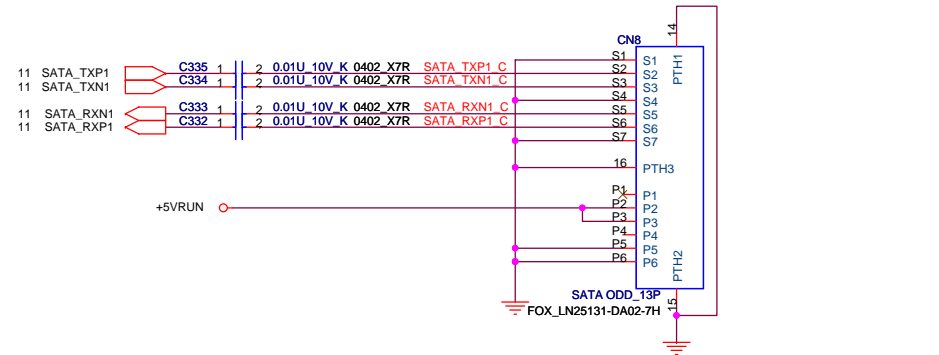




### SATA HDD CONN

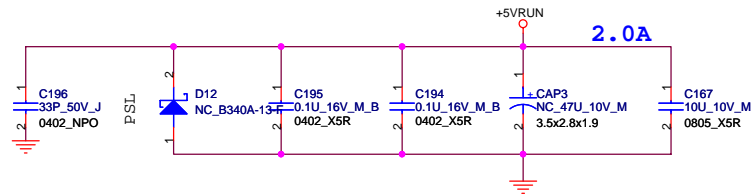


### SATA ODD CONN

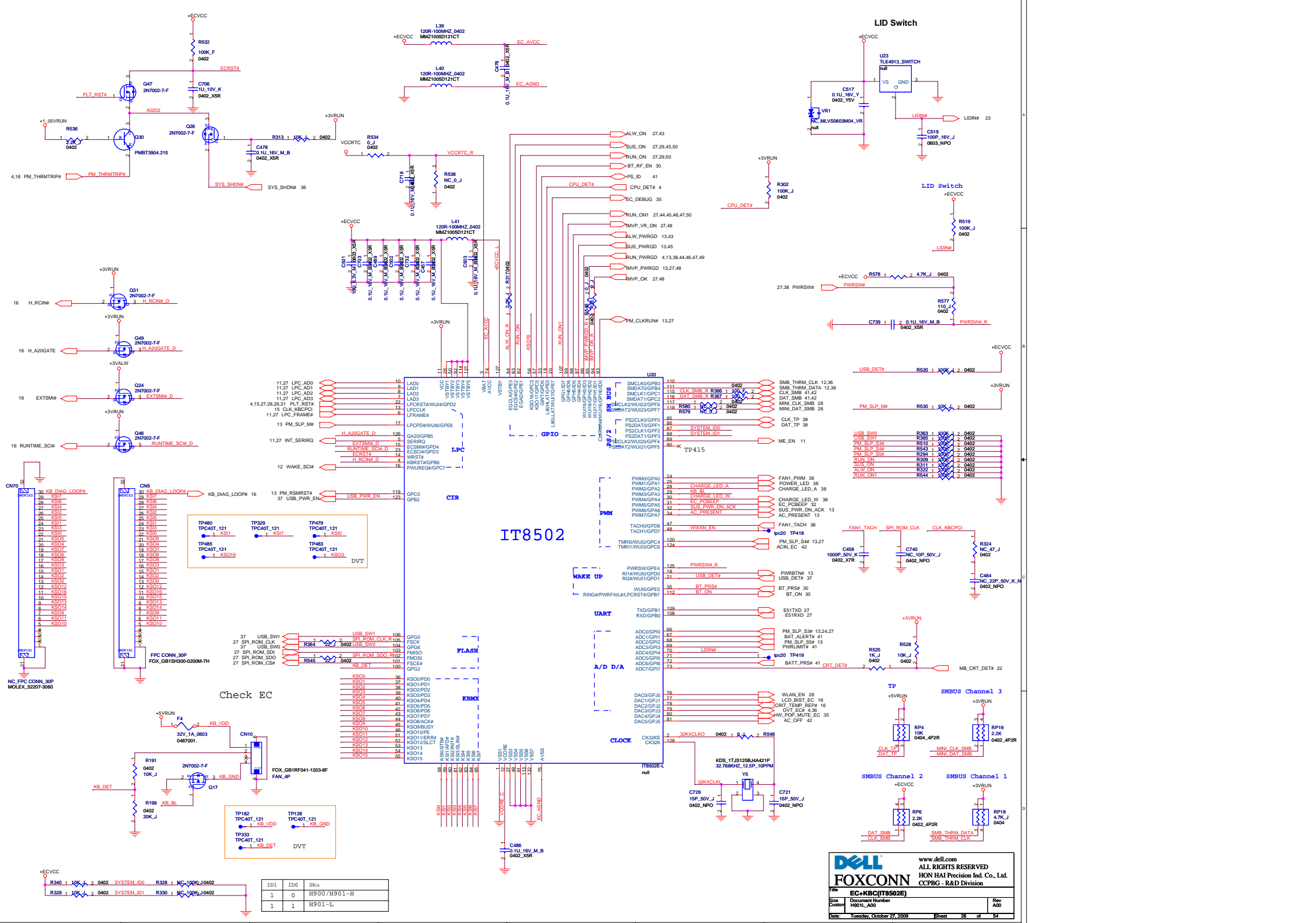


### ODD CON ADAPTER

Add CN68 need 2N-0013009-FKG0 in BOM



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		<b>Title</b> SATA HDD/ODD	
<b>Size</b> A3	<b>Document Number</b> H901L_A00	<b>Rev</b> A00	
<b>Date:</b> Monday, October 19, 2009		<b>Sheet</b> 25	<b>of</b> 54

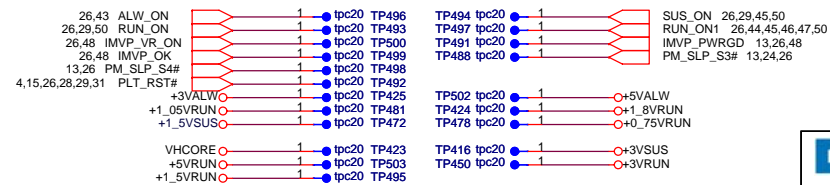
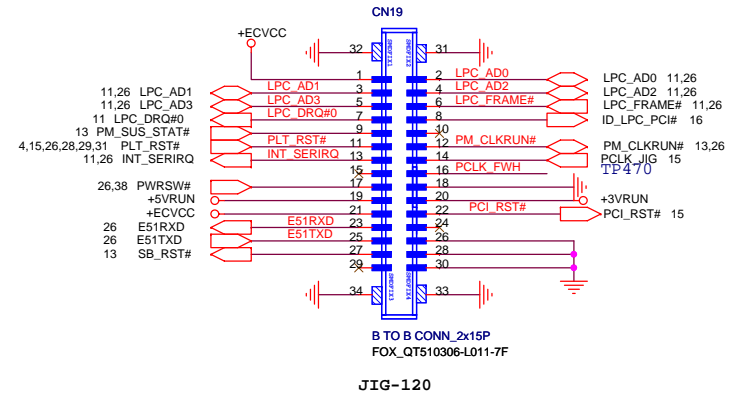
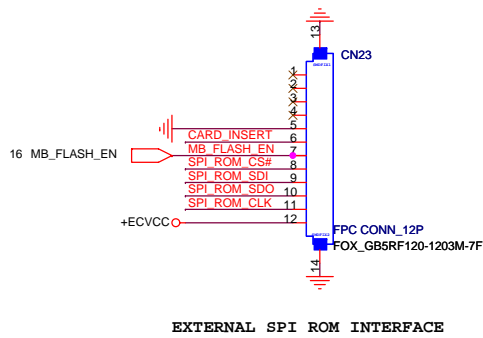
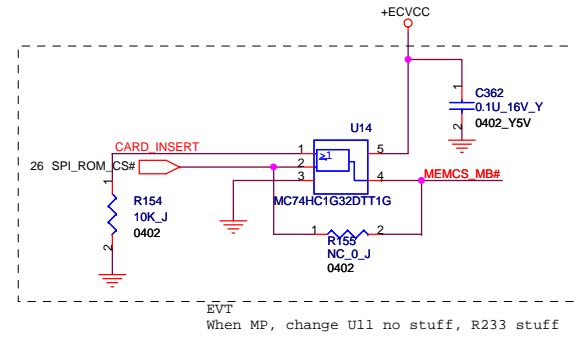
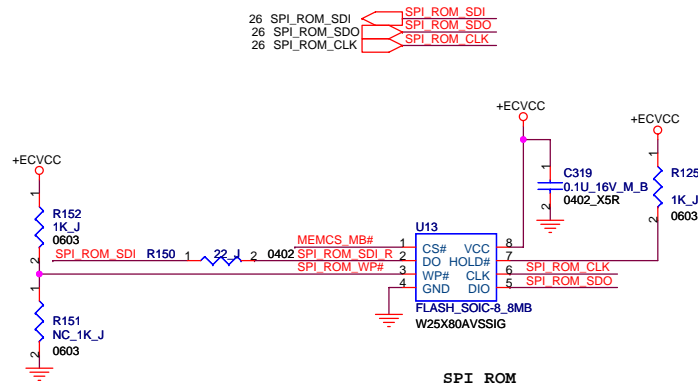


**IT8502**

ID1	ID0	Stk1
1	0	H900/H901-H
1	1	H901-L

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File: **EC-KBC(IT8502E)**  
 Size: H901\_A00  
 Document Number: H901\_A00  
 Date: Tuesday, October 27, 2009  
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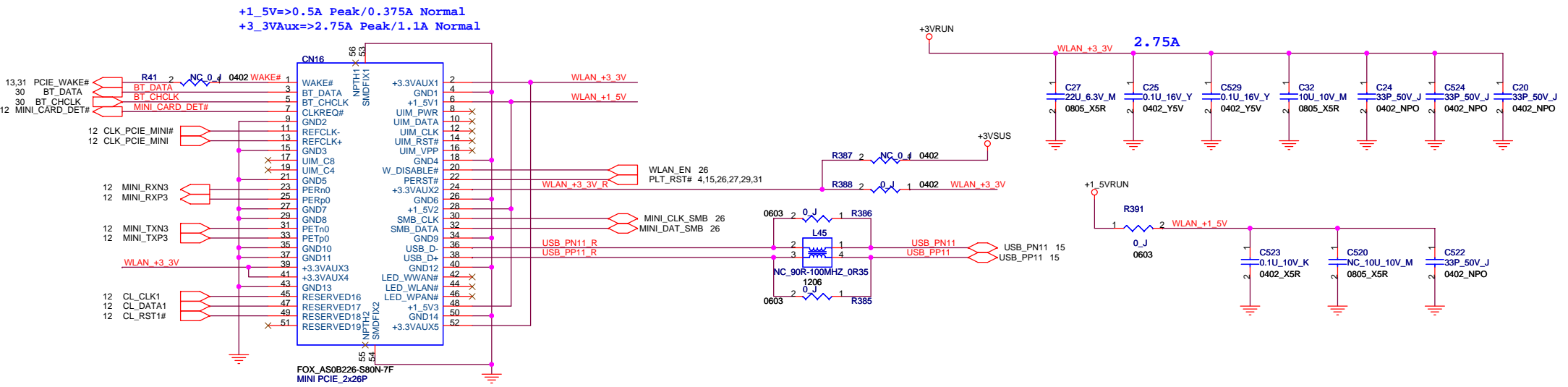


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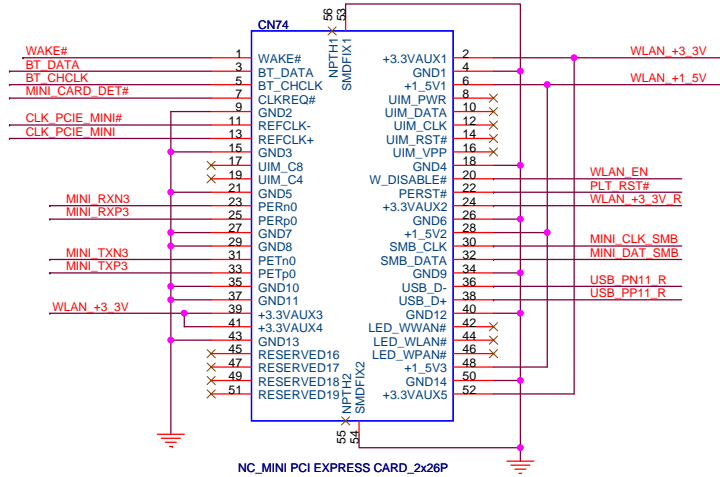
www.dell.com  
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Title: **Flash ROM/SPI**

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Half Mini Card for WLAN or WiMAX

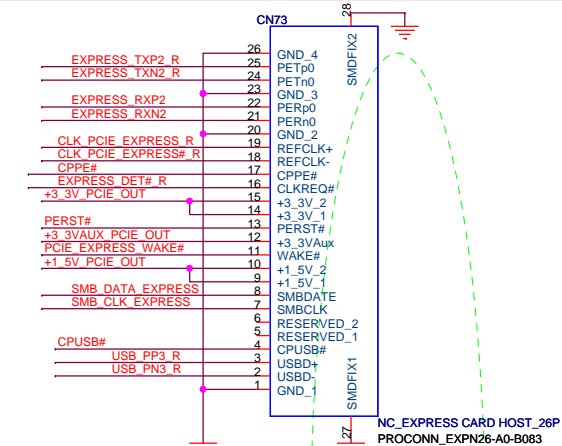
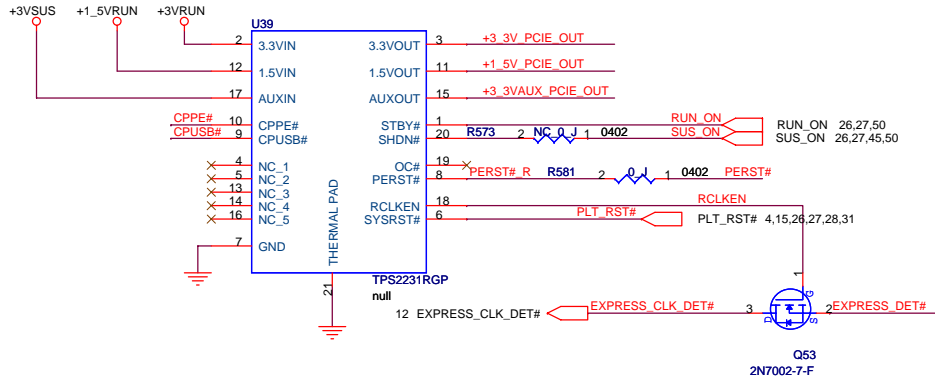


Colay: Half Mini Card CN second source

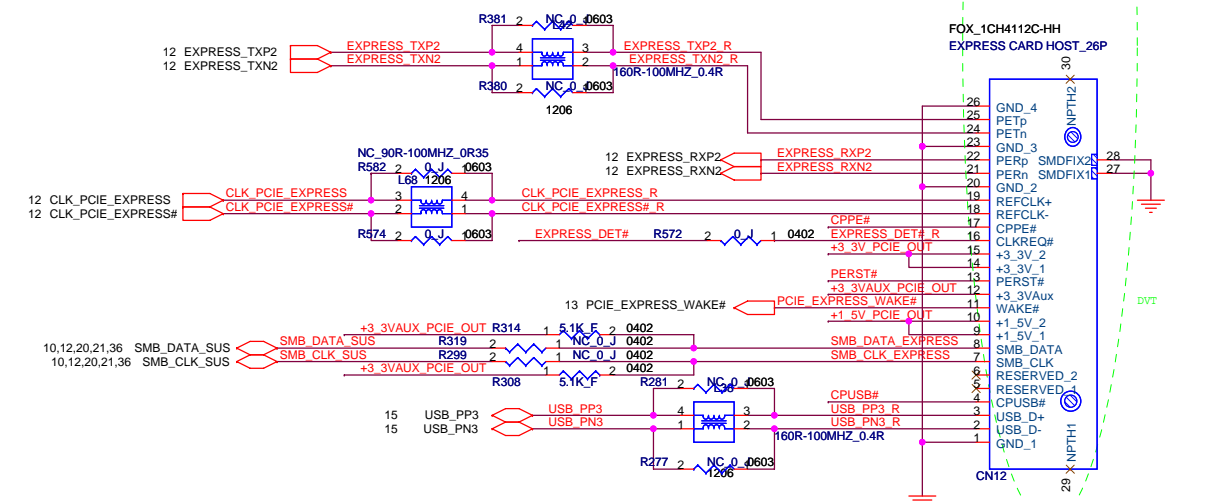
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		<b>FOXCONN</b>	
Title: <b>WLAN/Wimax Mini-PCIE Card</b>			
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Date: Monday, October 19, 2009		Sheet: 28	of: 54

**+1\_5V=>650mA**  
**+3\_3VAux=>275mA**  
**+3\_3V=>1.3A**

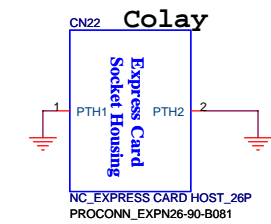
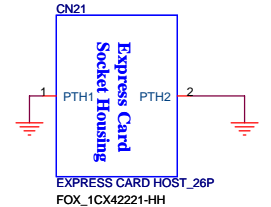
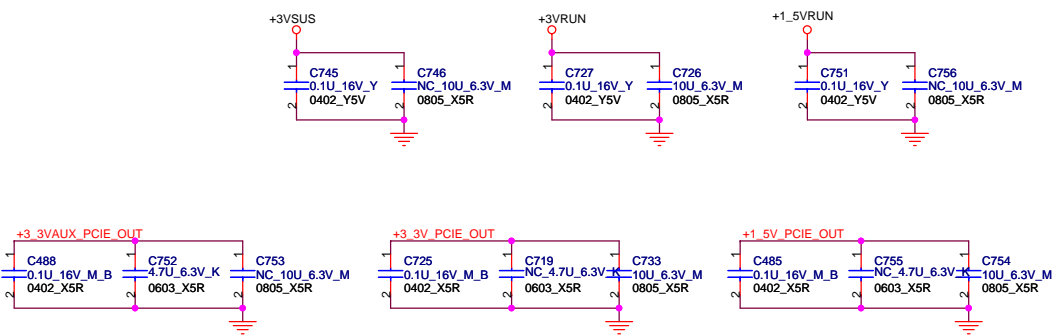
**Express Card Power Switch**



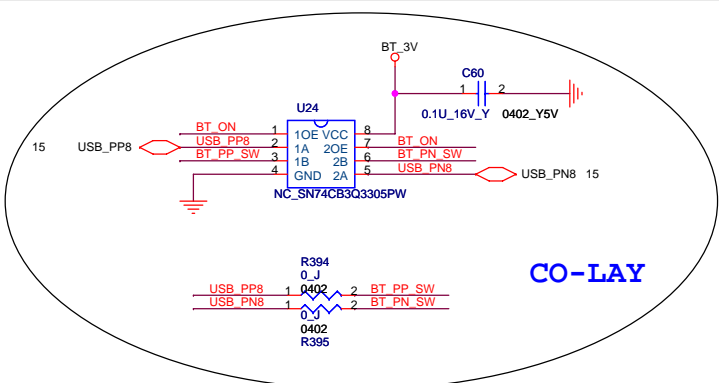
**Colay**



**Express Card Slot.**

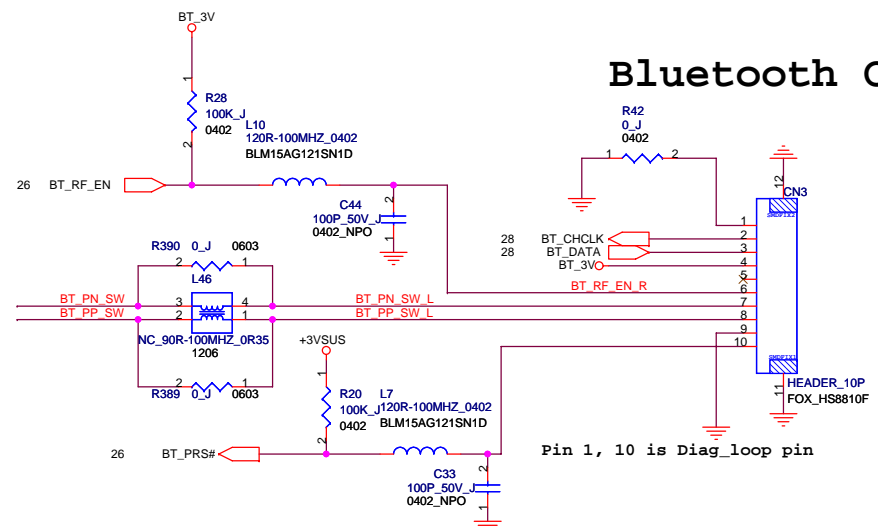
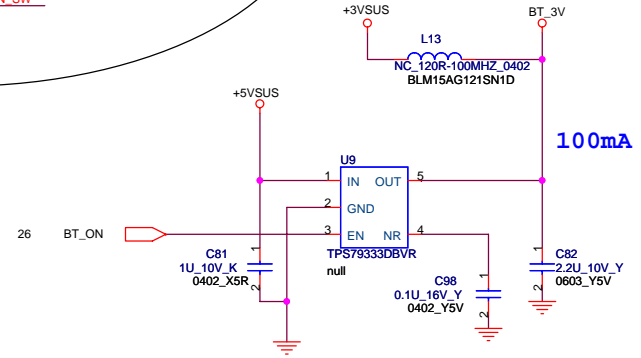


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Title <b>Express card</b>			
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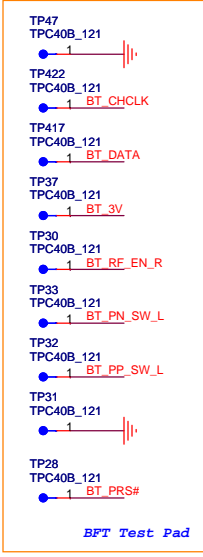


**CO-LAY**

# Bluetooth



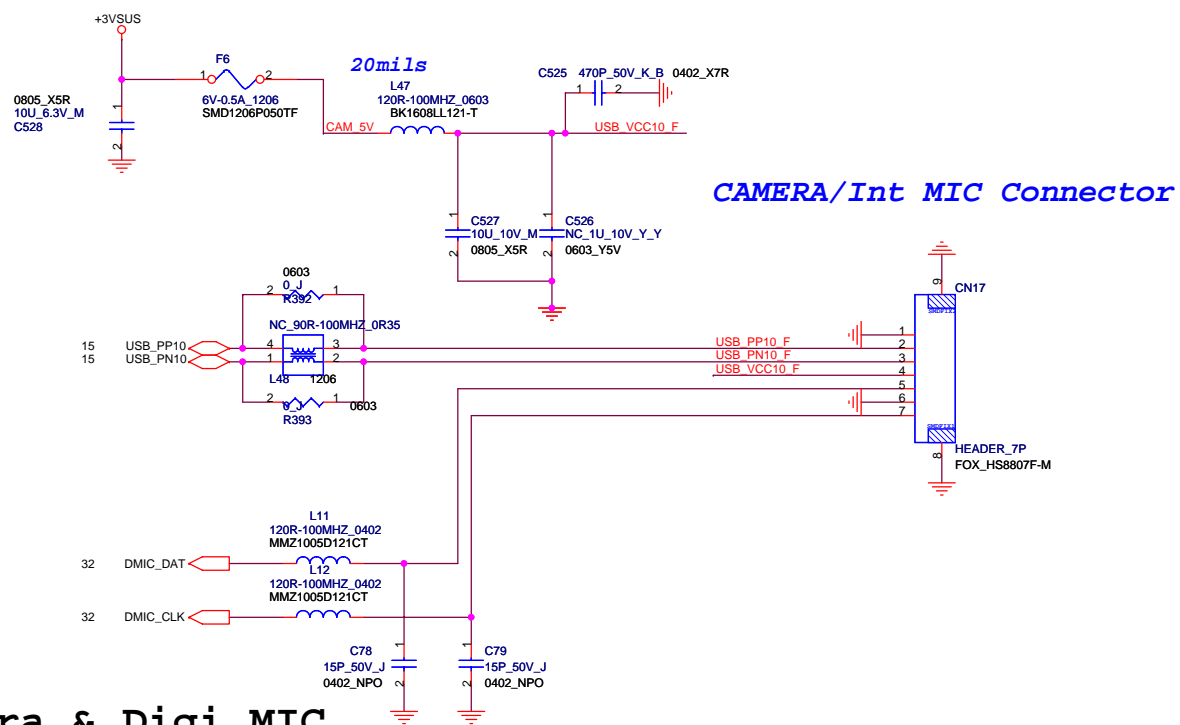
# Bluetooth CONN.



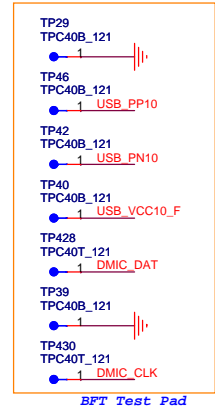
Pin 1, 10 is Diag\_loop pin

BFT Test Pad

# Camera & Digi MIC



# CAMERA/Int MIC Connector



DVT

BFT Test Pad

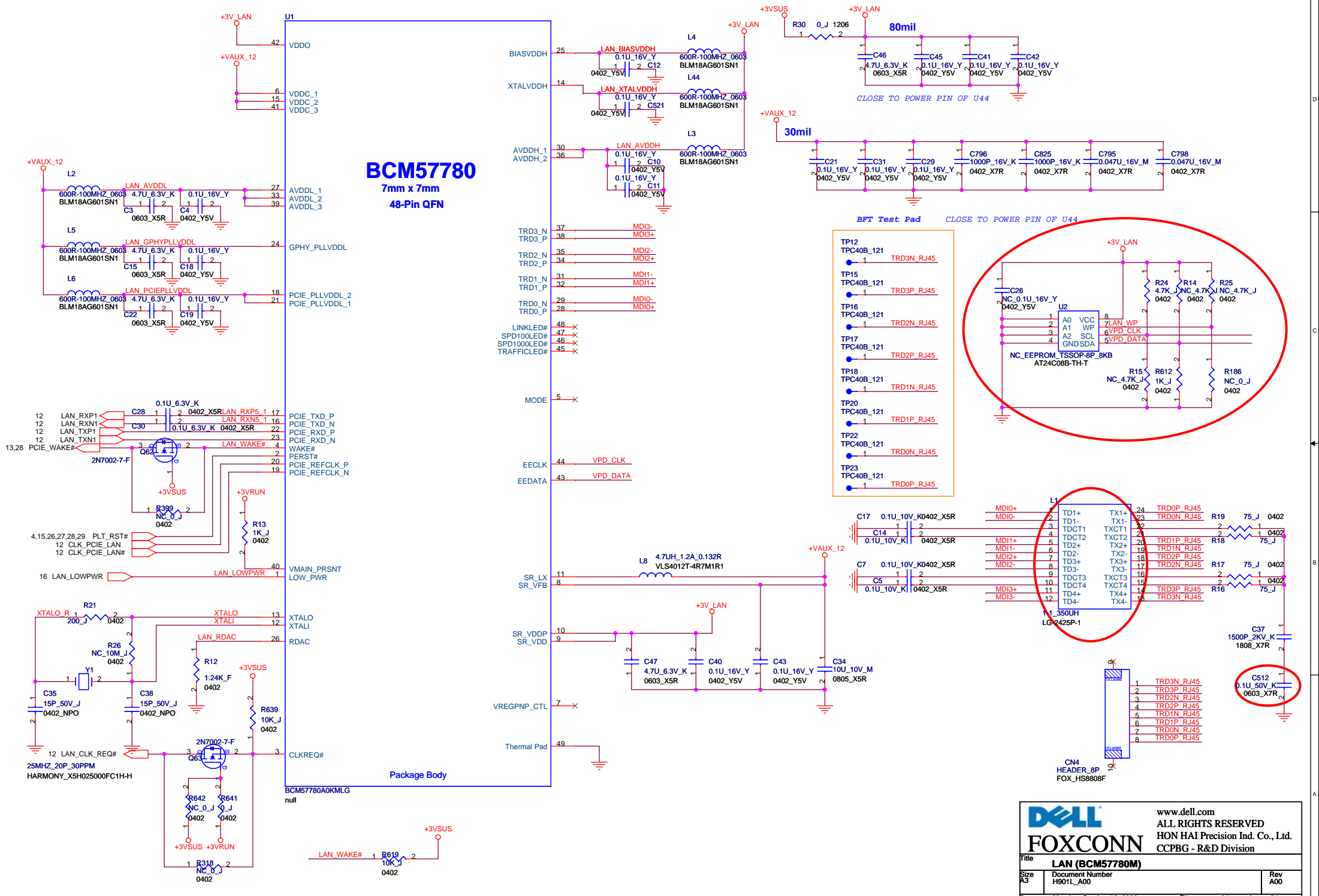
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Title: **BT & CAMERA/Dig MIC CON**

Size: A3	Document Number: H901L_A00	Rev: A00
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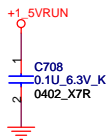
# BCM57780

7mm x 7mm  
48-Pin QFN

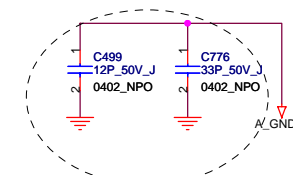
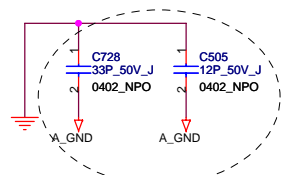
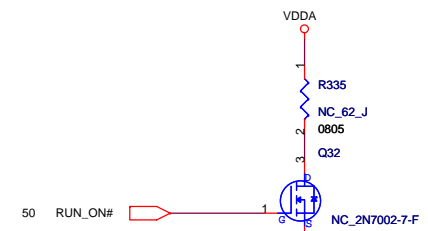
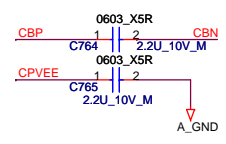
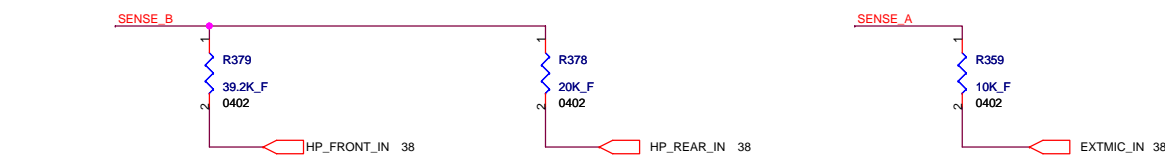
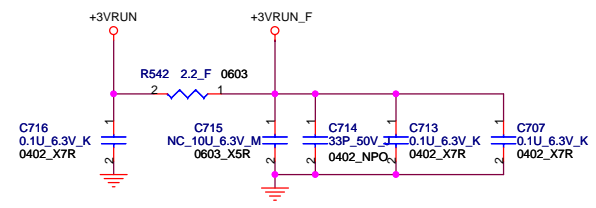
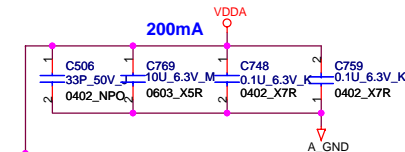
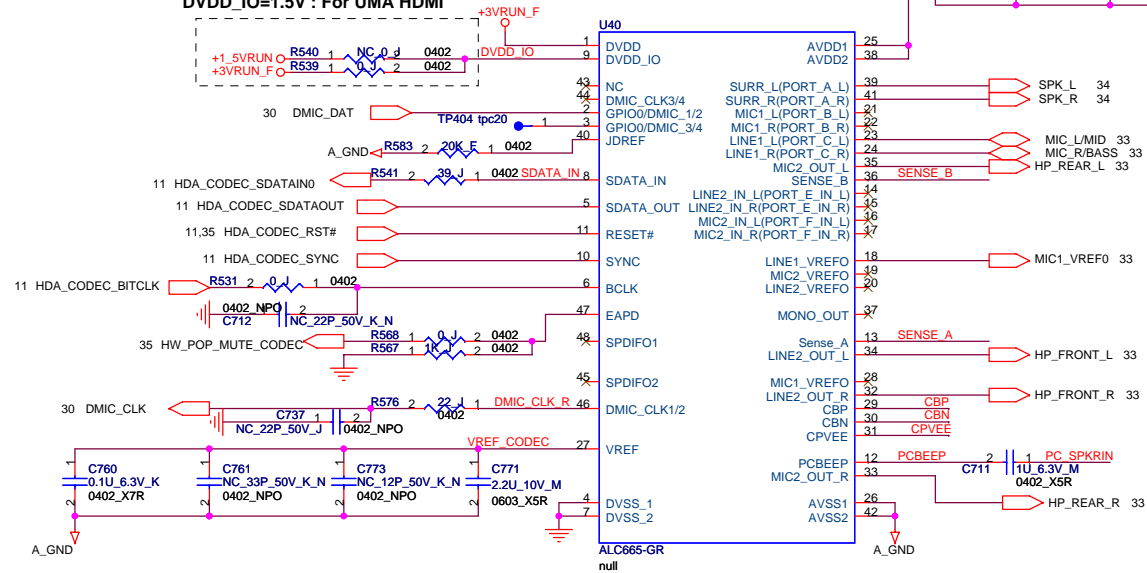


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Title: LAN (BCM57780M)  
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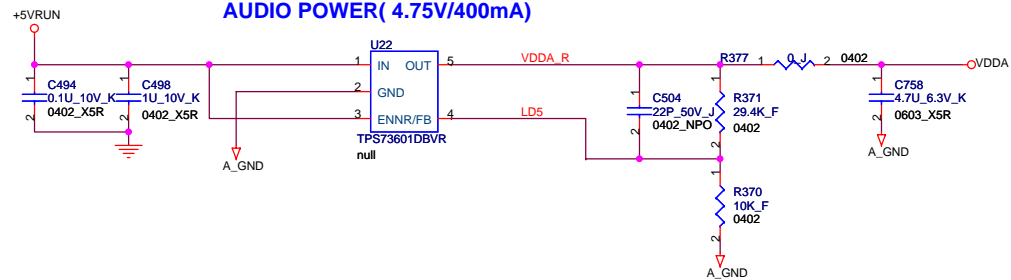


**DVDD\_IO=1.5V : For UMA HDMI**

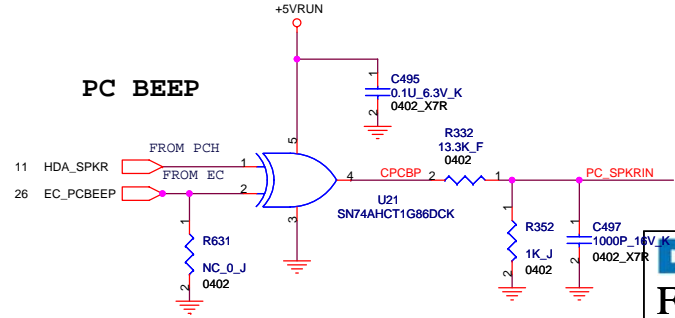


Place these two capacitor together. Place these two capacitor together.

**AUDIO POWER (4.75V/400mA)**



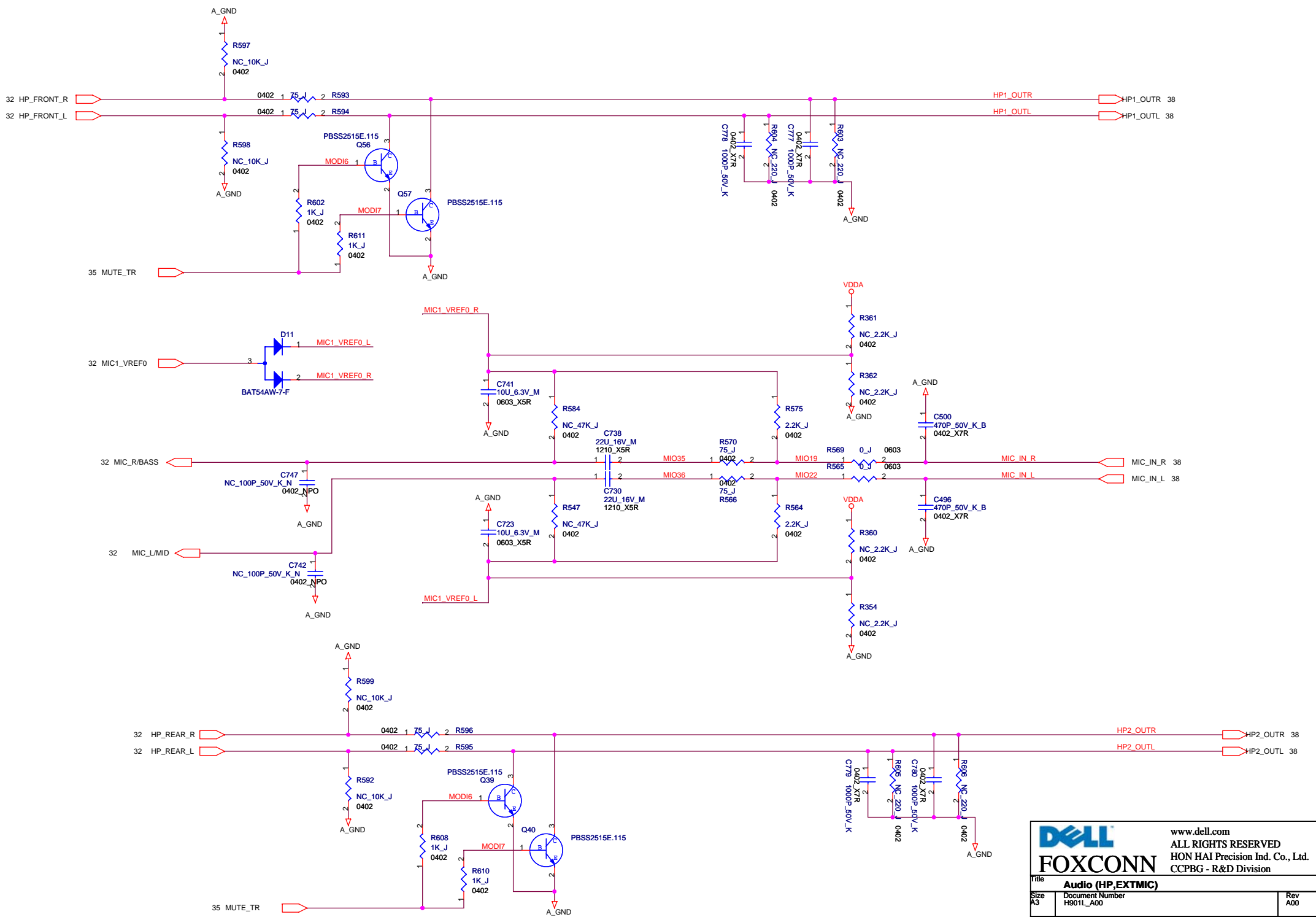
**PC BEEP**

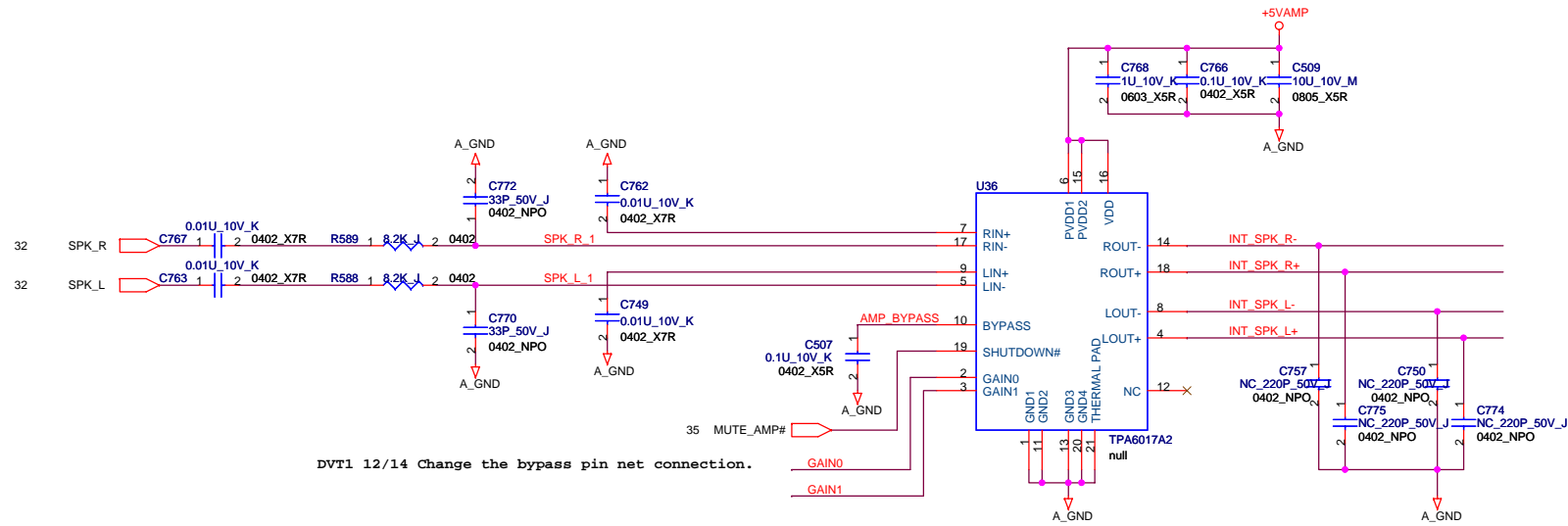
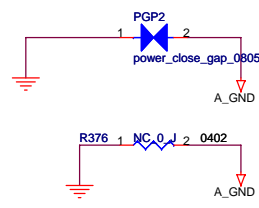
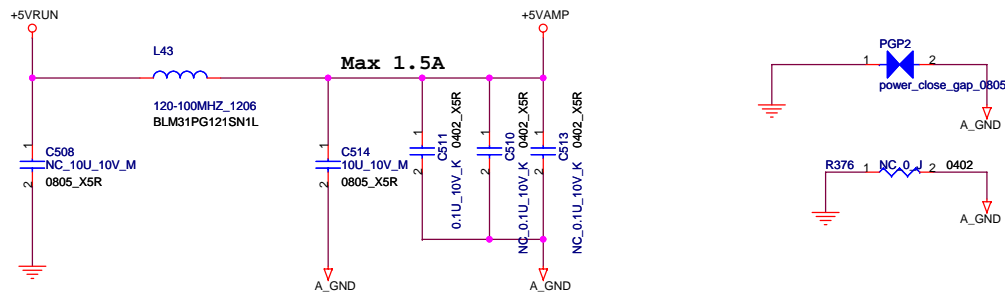


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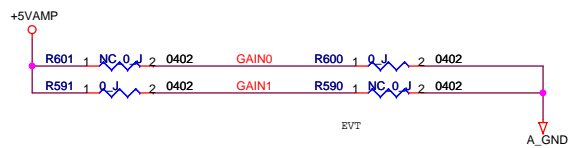
Title	<b>Audio (CODEC &amp; POWER)</b>	
Size	Document Number	Rev
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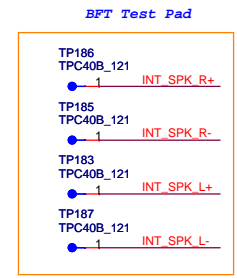
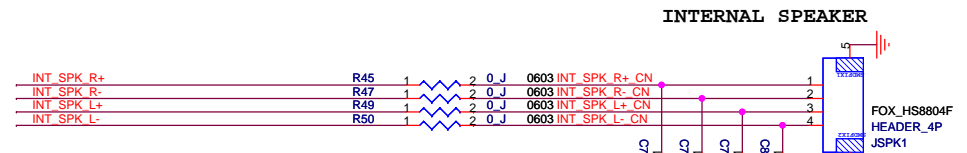
DVT1 12/14 Change the bypass pin net connection.



**SPEAKER AMP**

	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

$dB = 20 \log Gain$   
 If set 10dB, gain is 3.162.  
 $P_o = \{(1.2V_{rms} * 3.162)^2\} / 4 = 3.599 W$

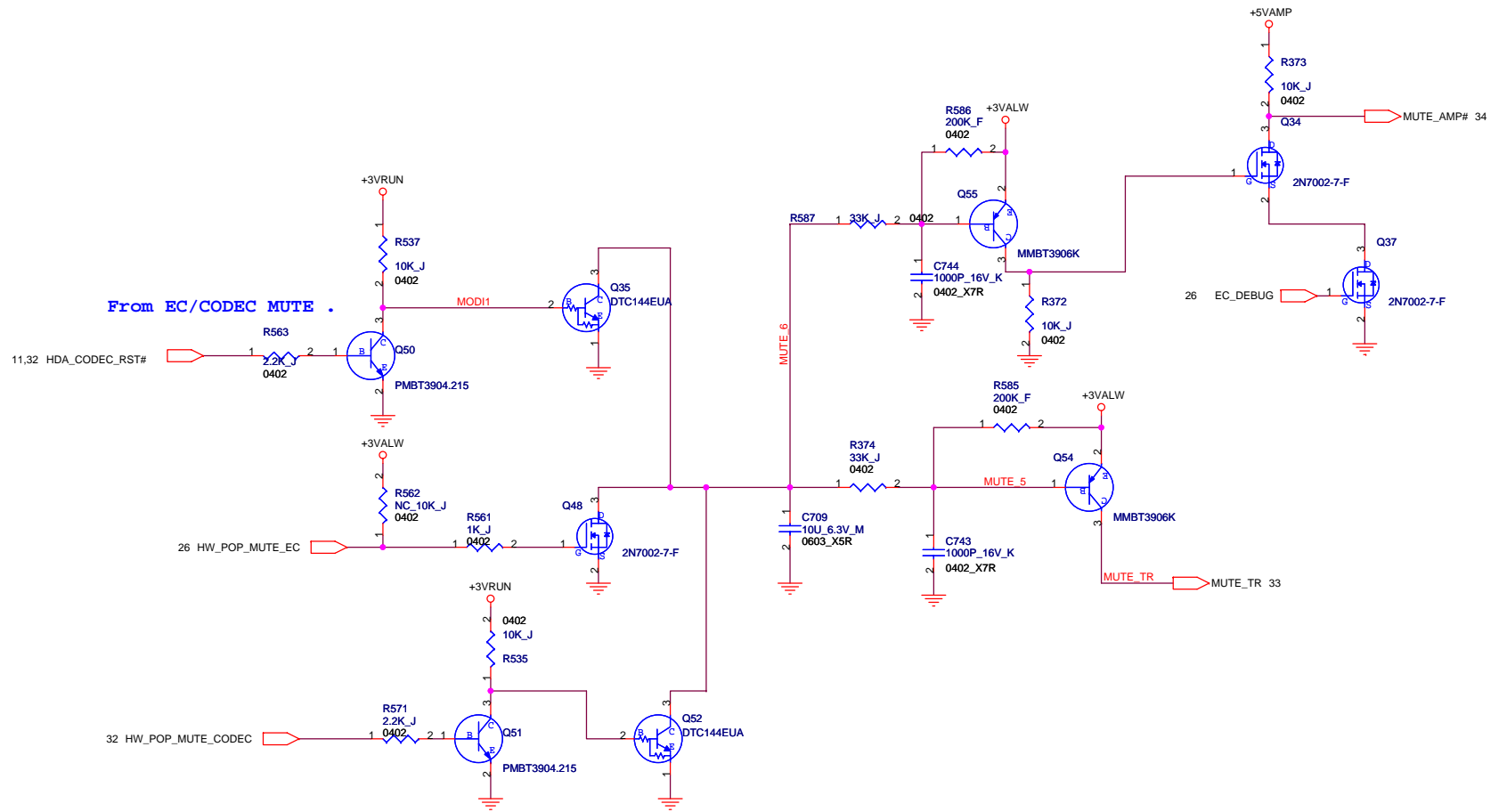




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 Document Number: H901L\_A00  
 Rev: A00

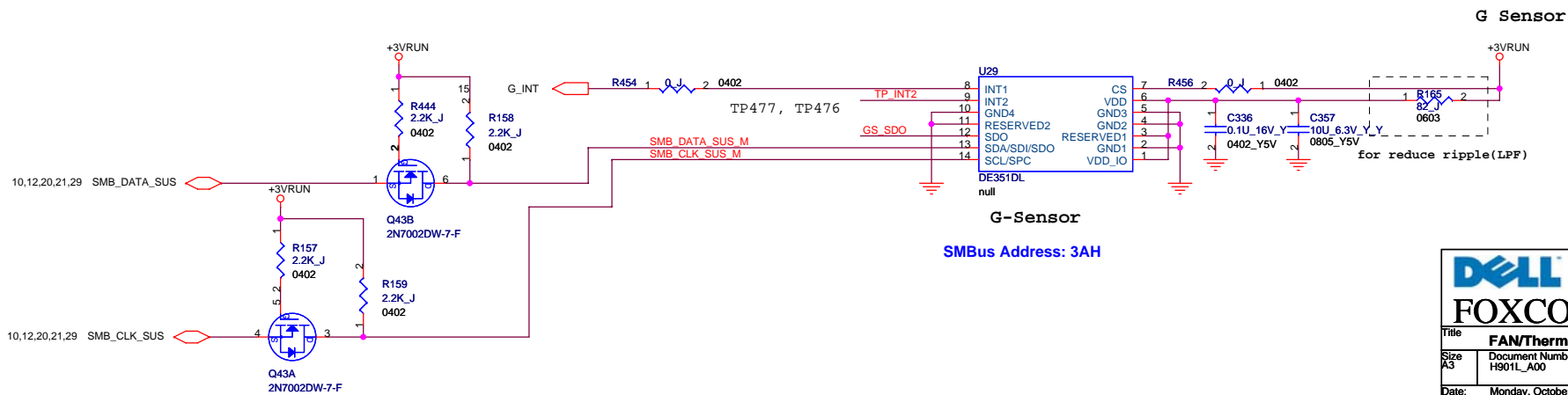
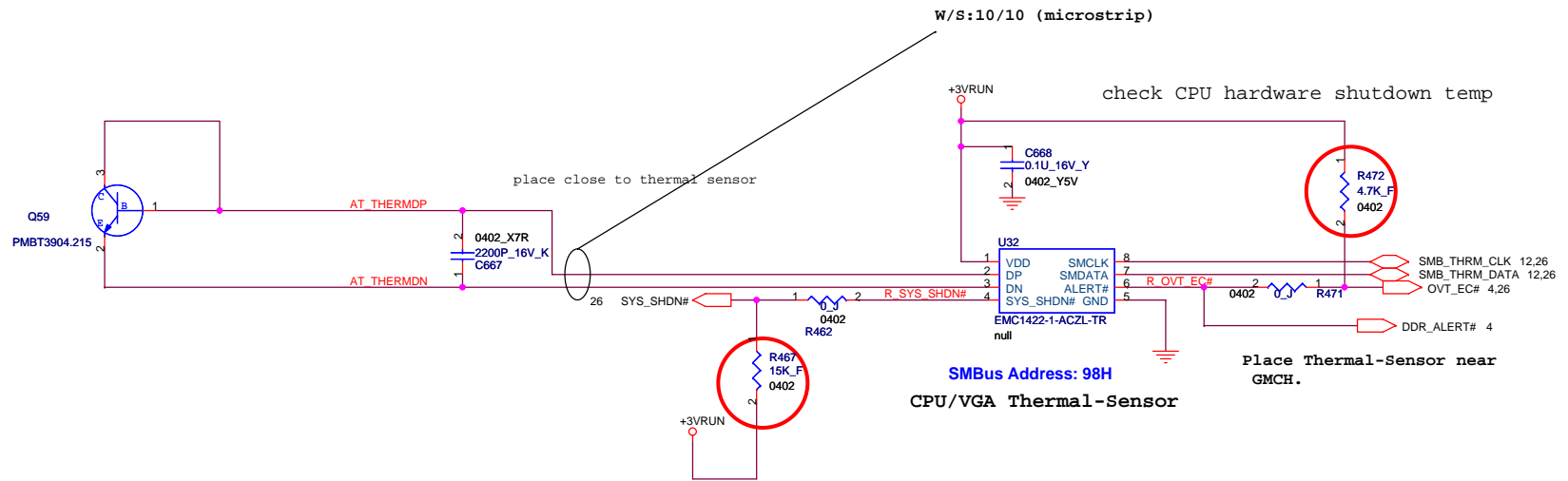
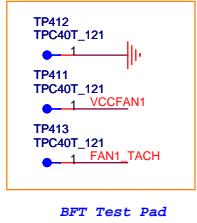
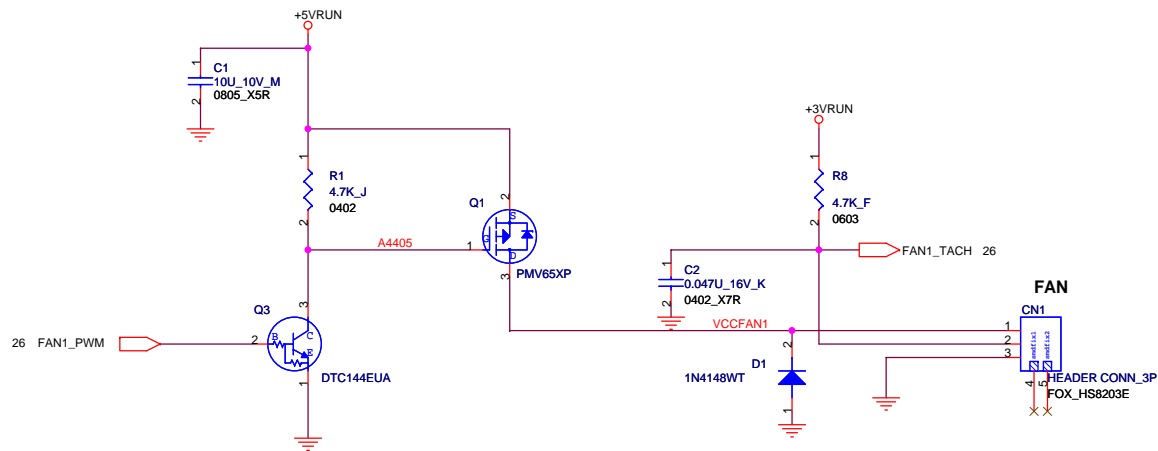
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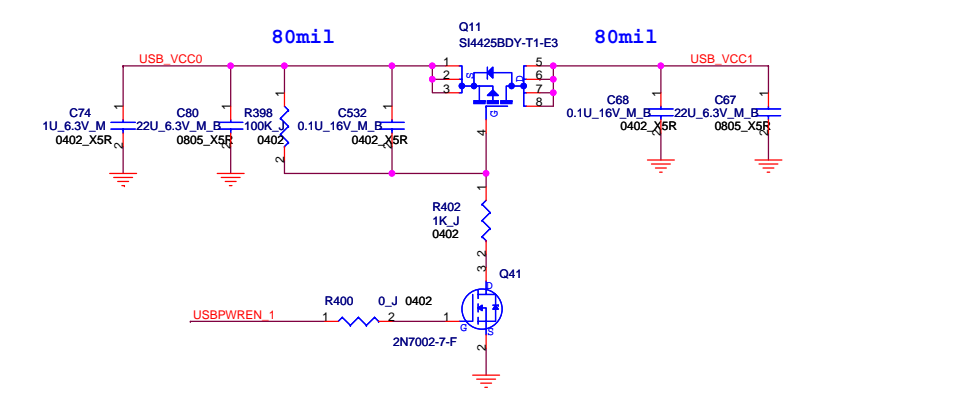
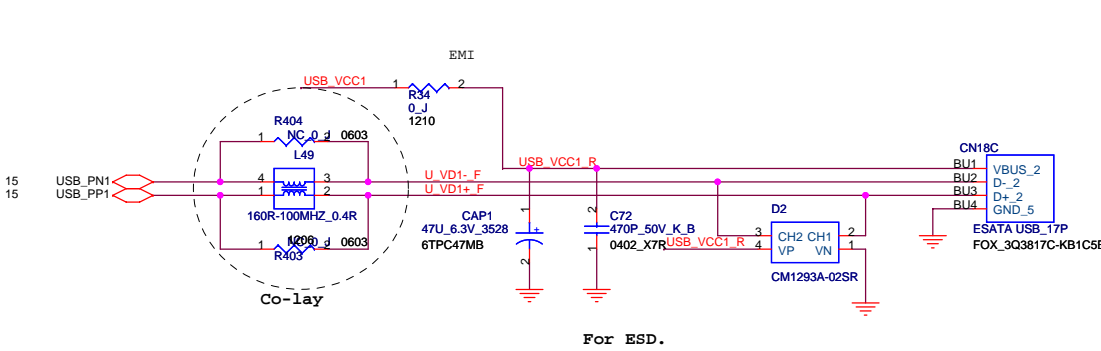
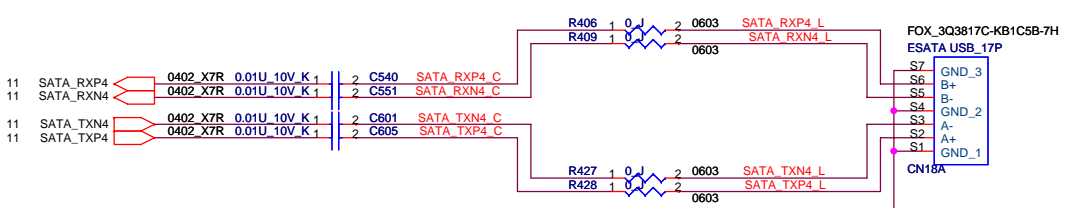
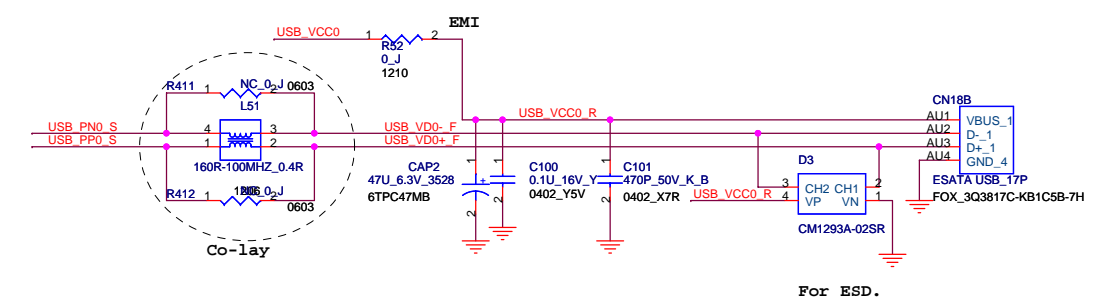
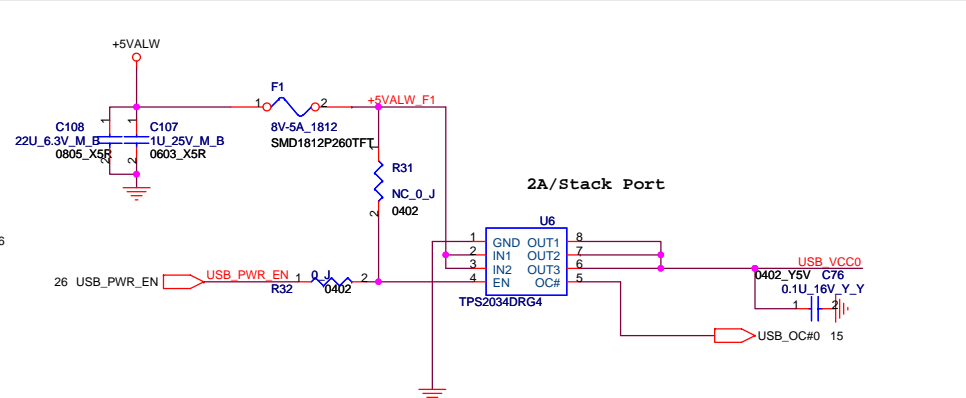
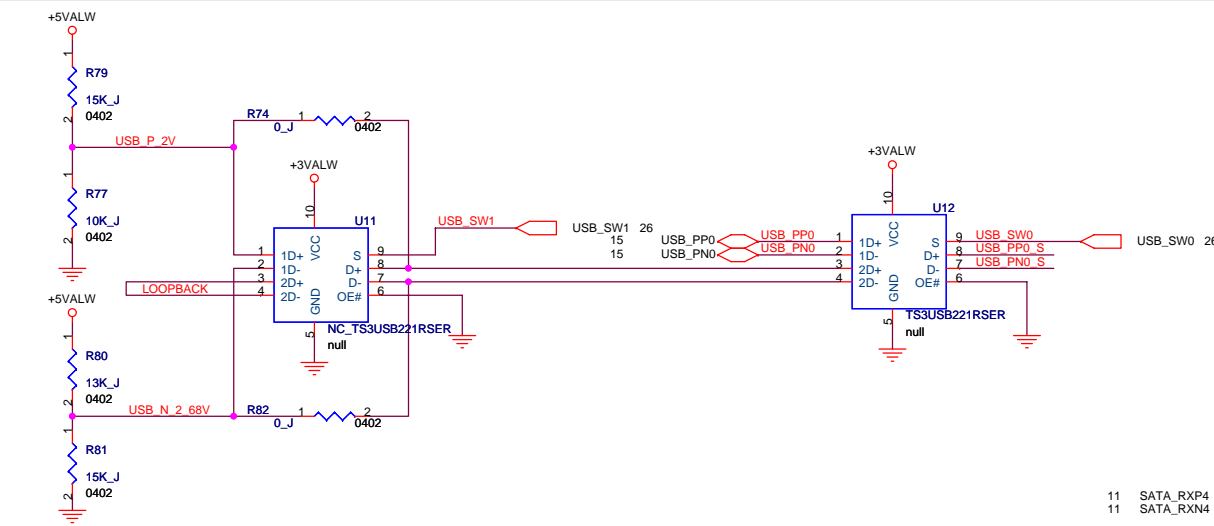
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Size: A3	Document Number: H901L_A00	Rev: A00
Date: Monday, October 19, 2009	Sheet: 35	of: 54



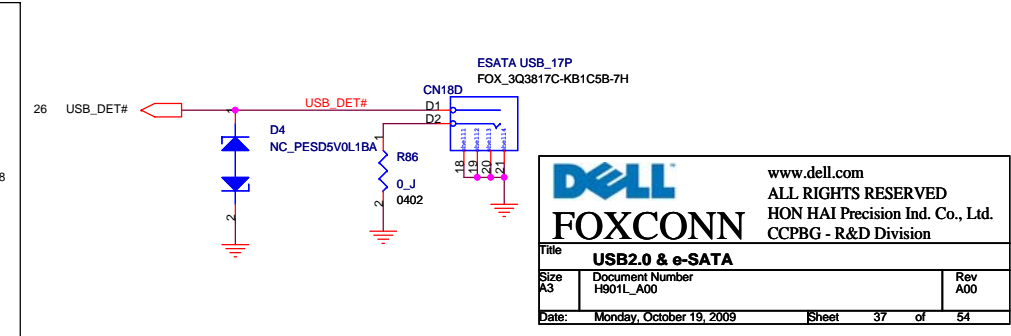
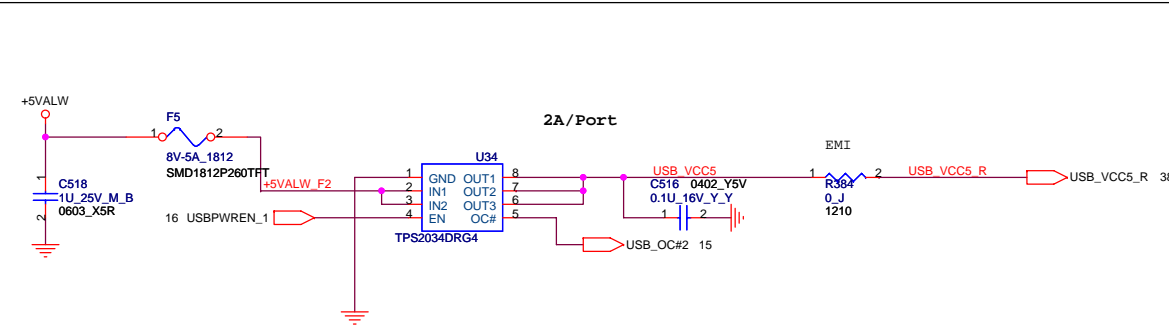
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Title	<b>FAN/Thermal Sensor</b>	
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Date:	Monday, October 19, 2009	Sheet 36 of 54

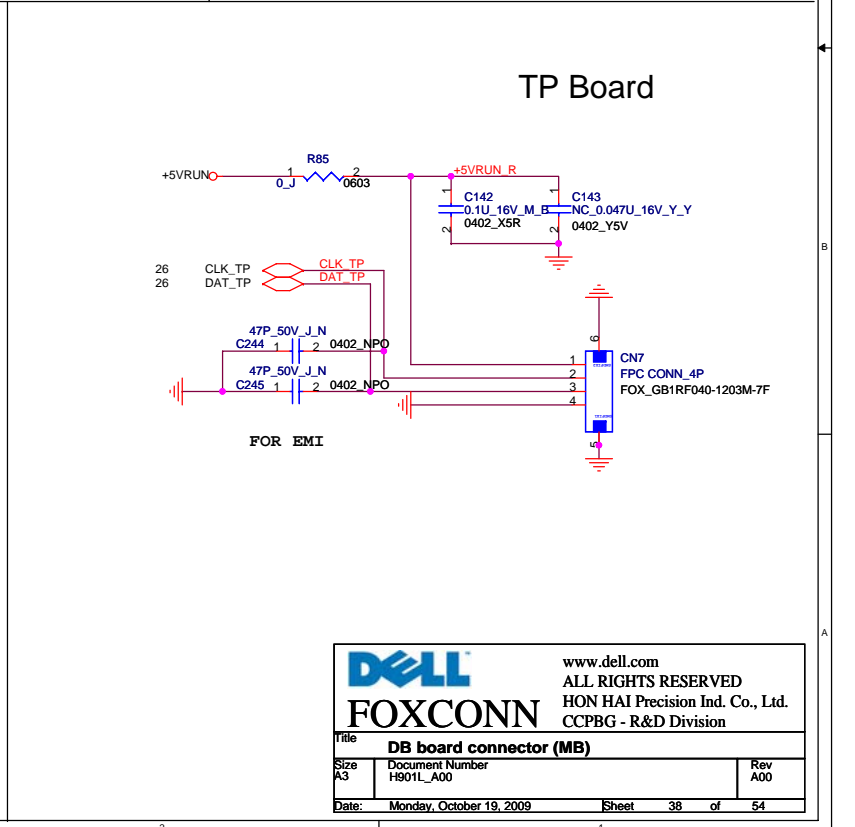
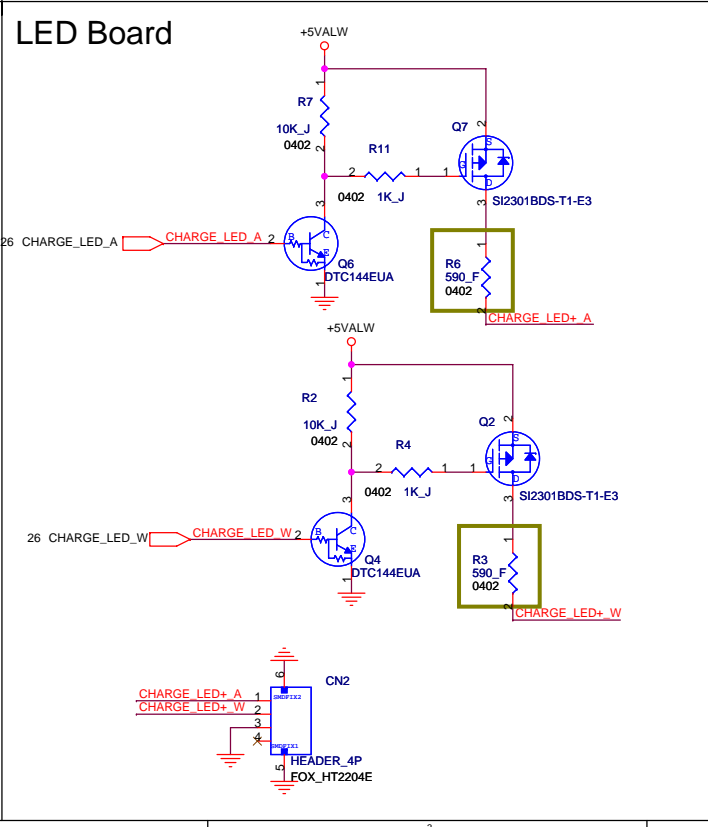
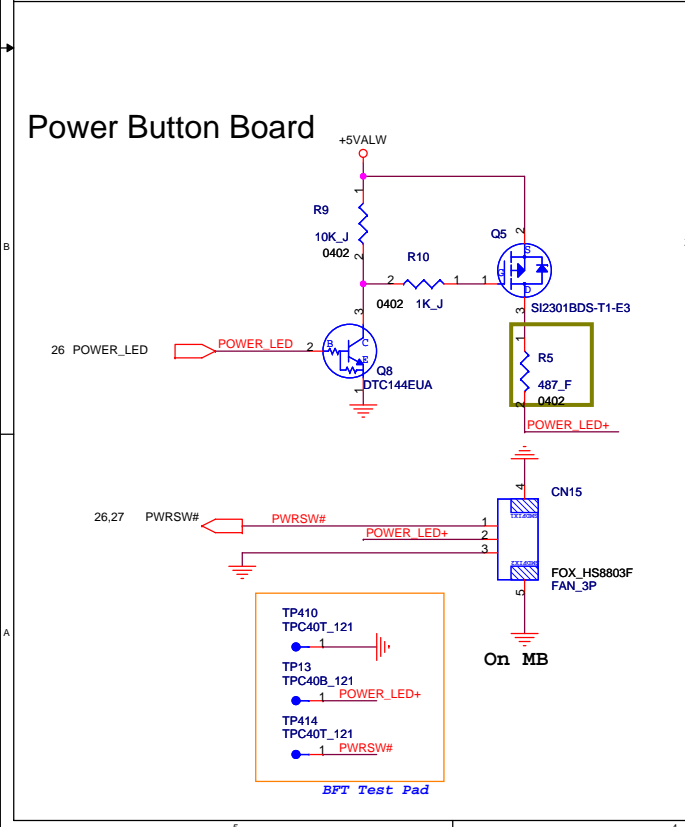
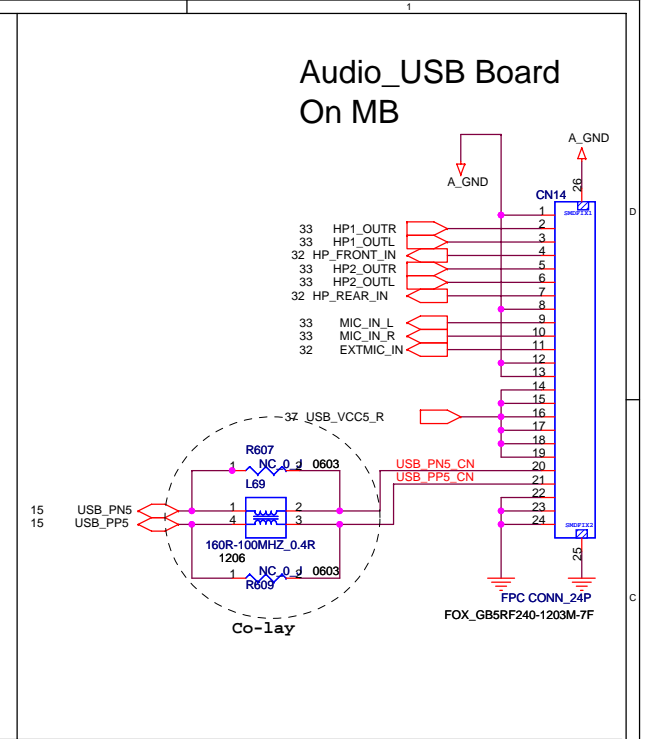
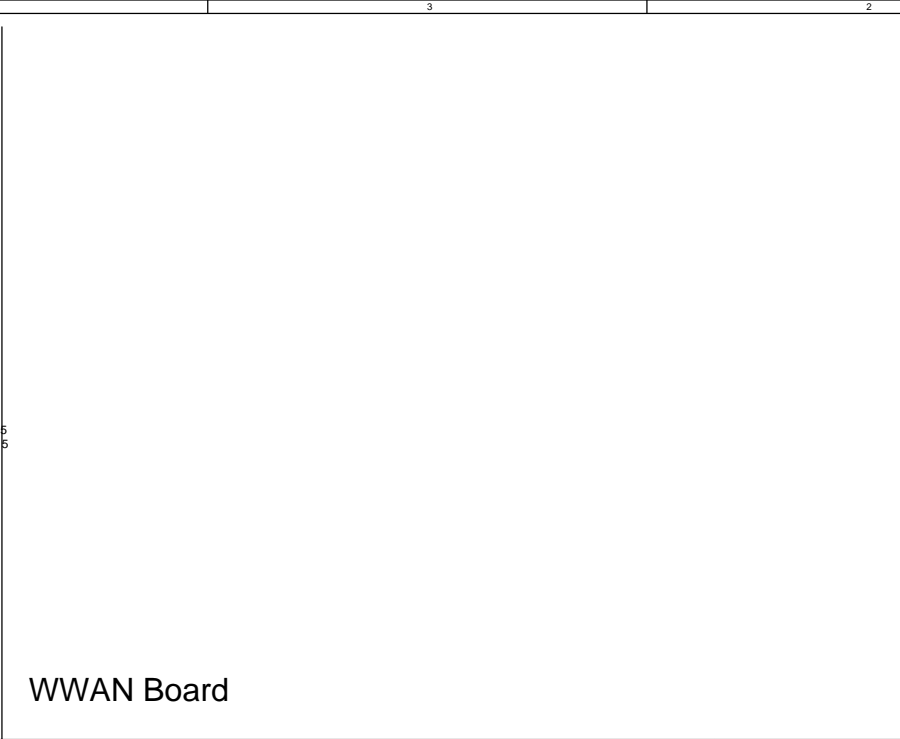
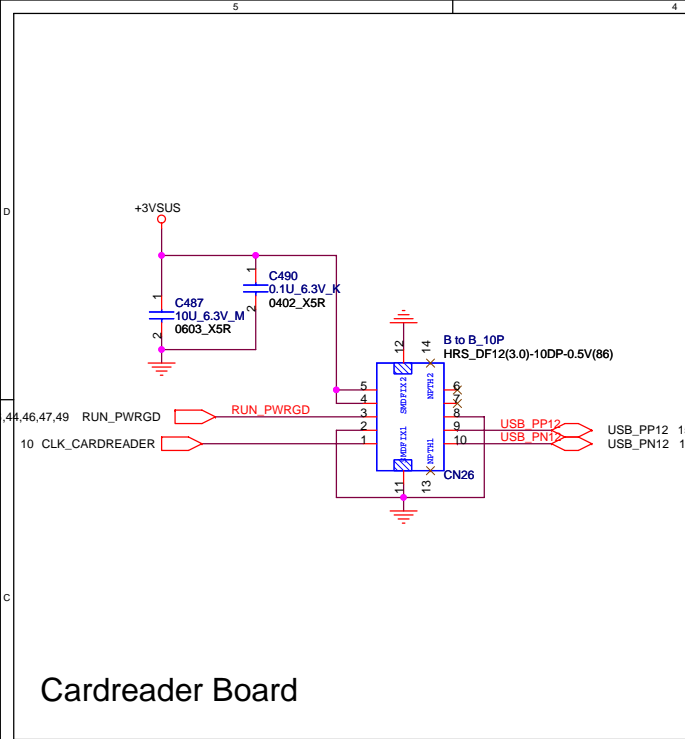


USB + e-SATA on MB



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Title: **USB2.0 & e-SATA**  
 Size: A3 Document Number: H901L\_A00 Rev: A00  
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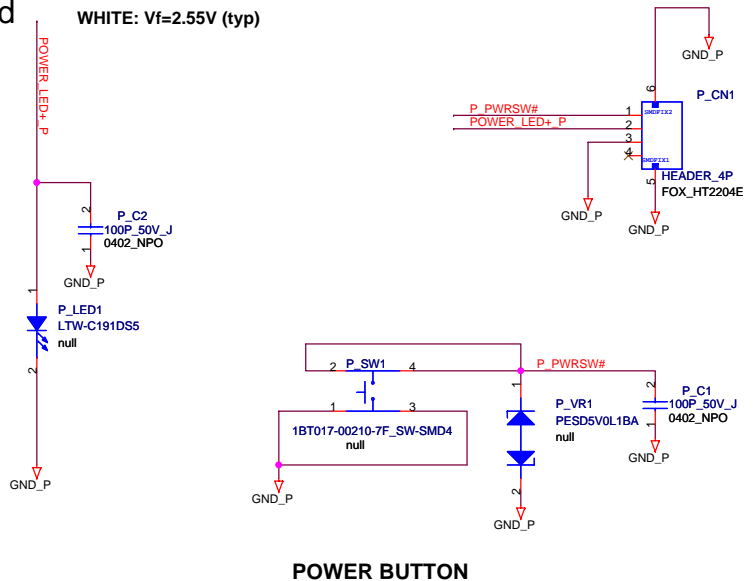


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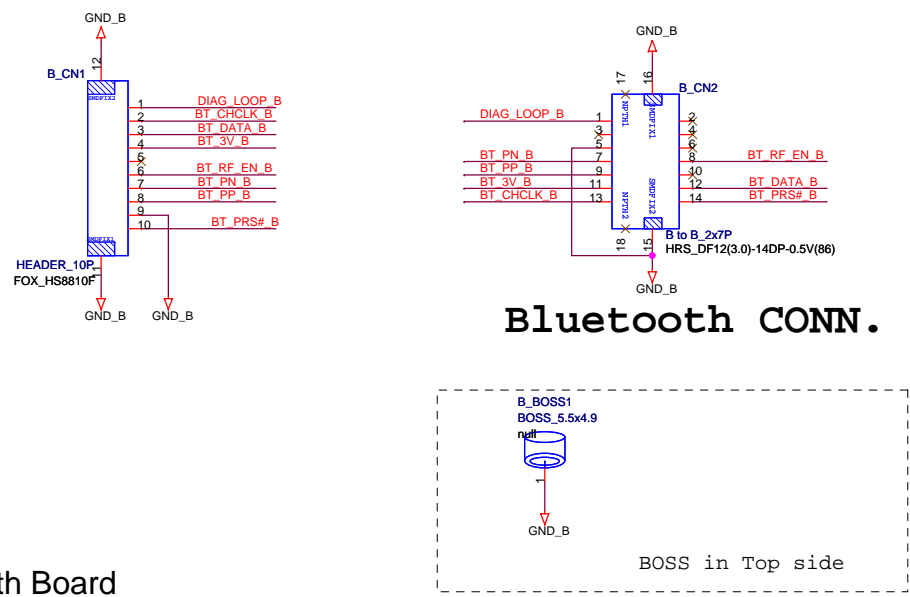
Title: **DB board connector (MB)**

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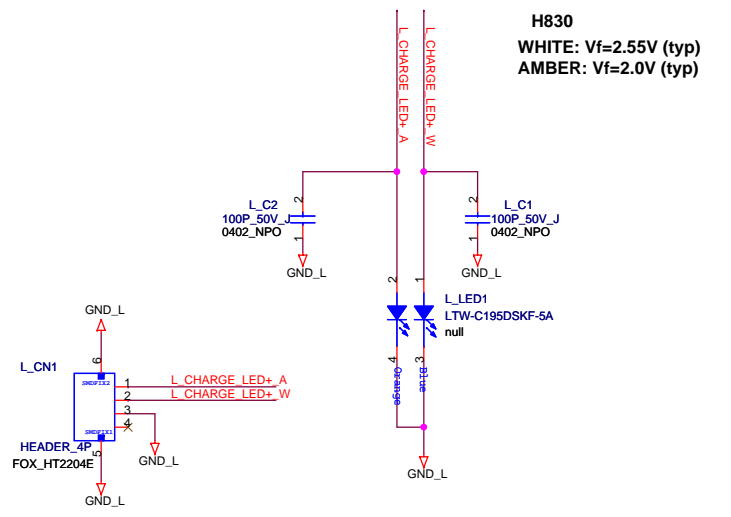
# Power Button Board



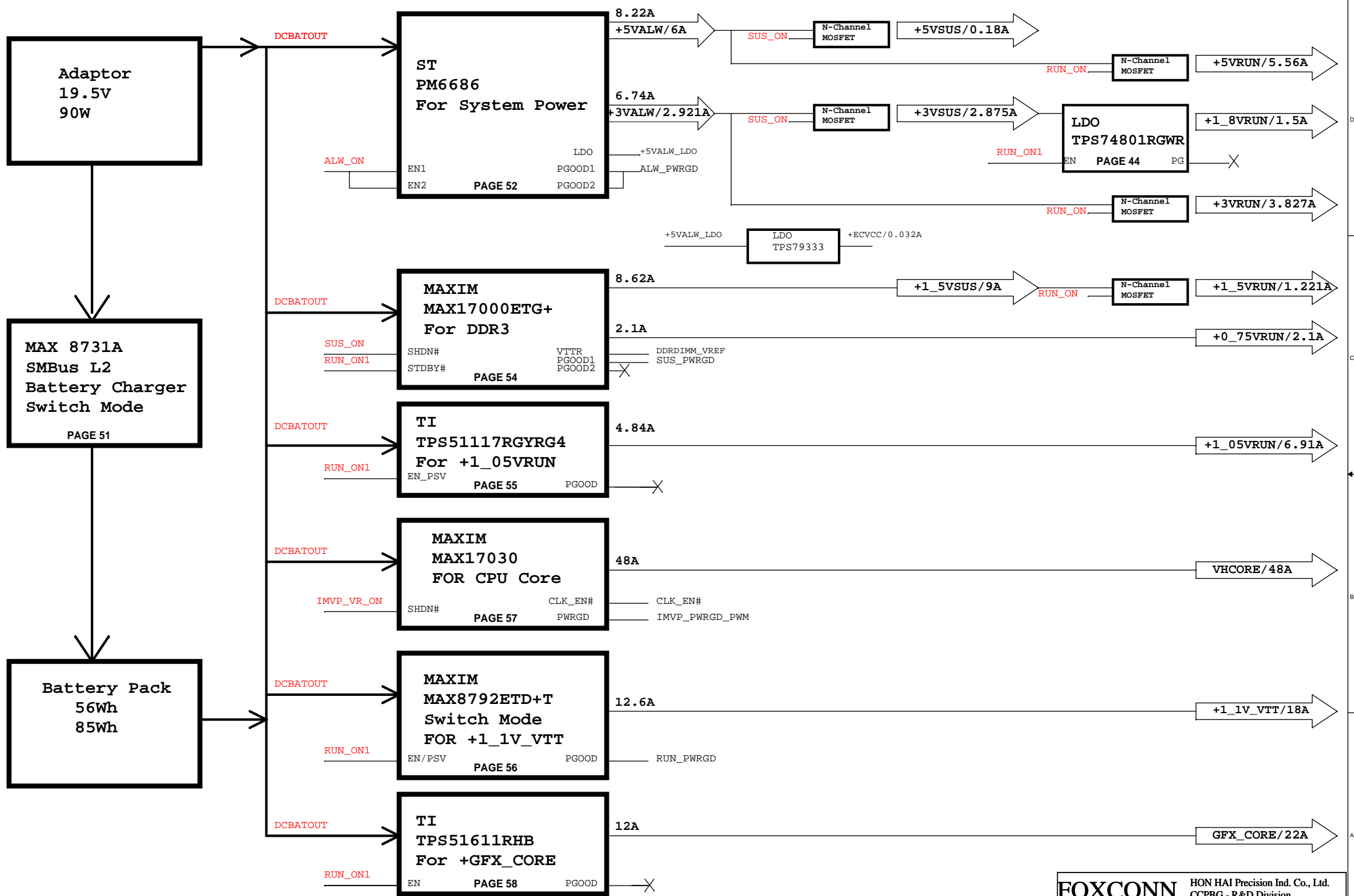
# Bluetooth Board



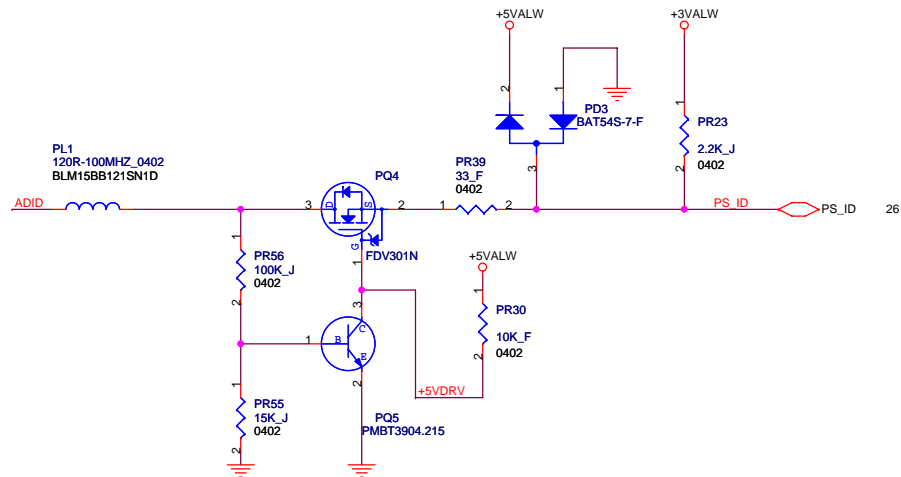
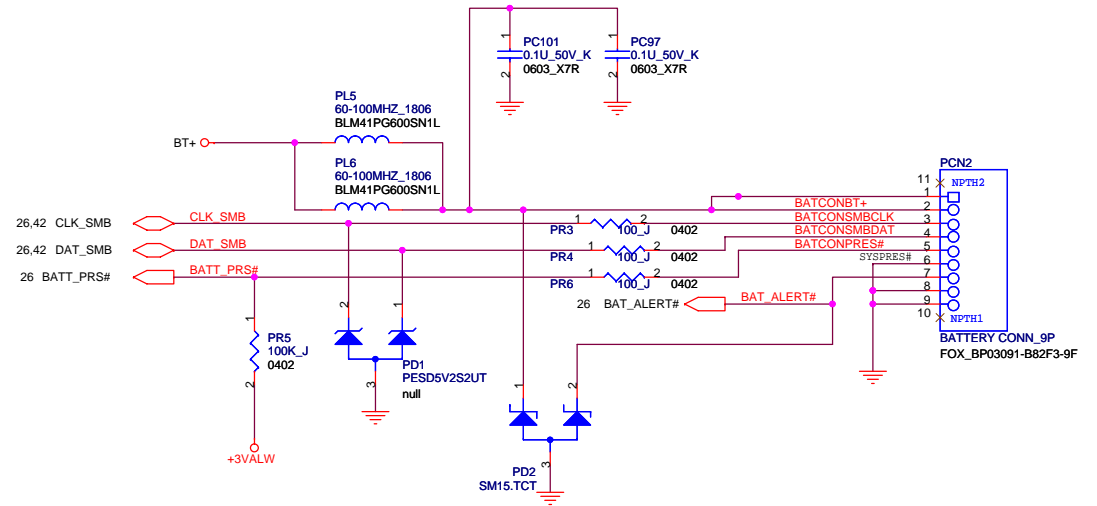
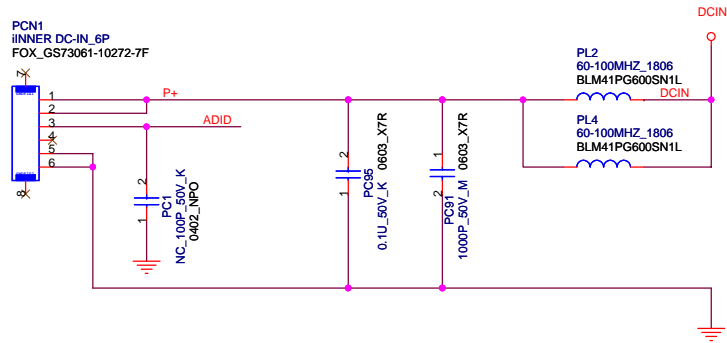
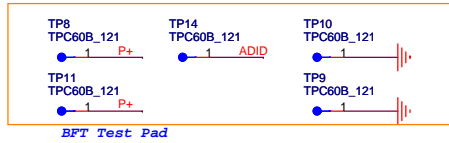
# LED Board

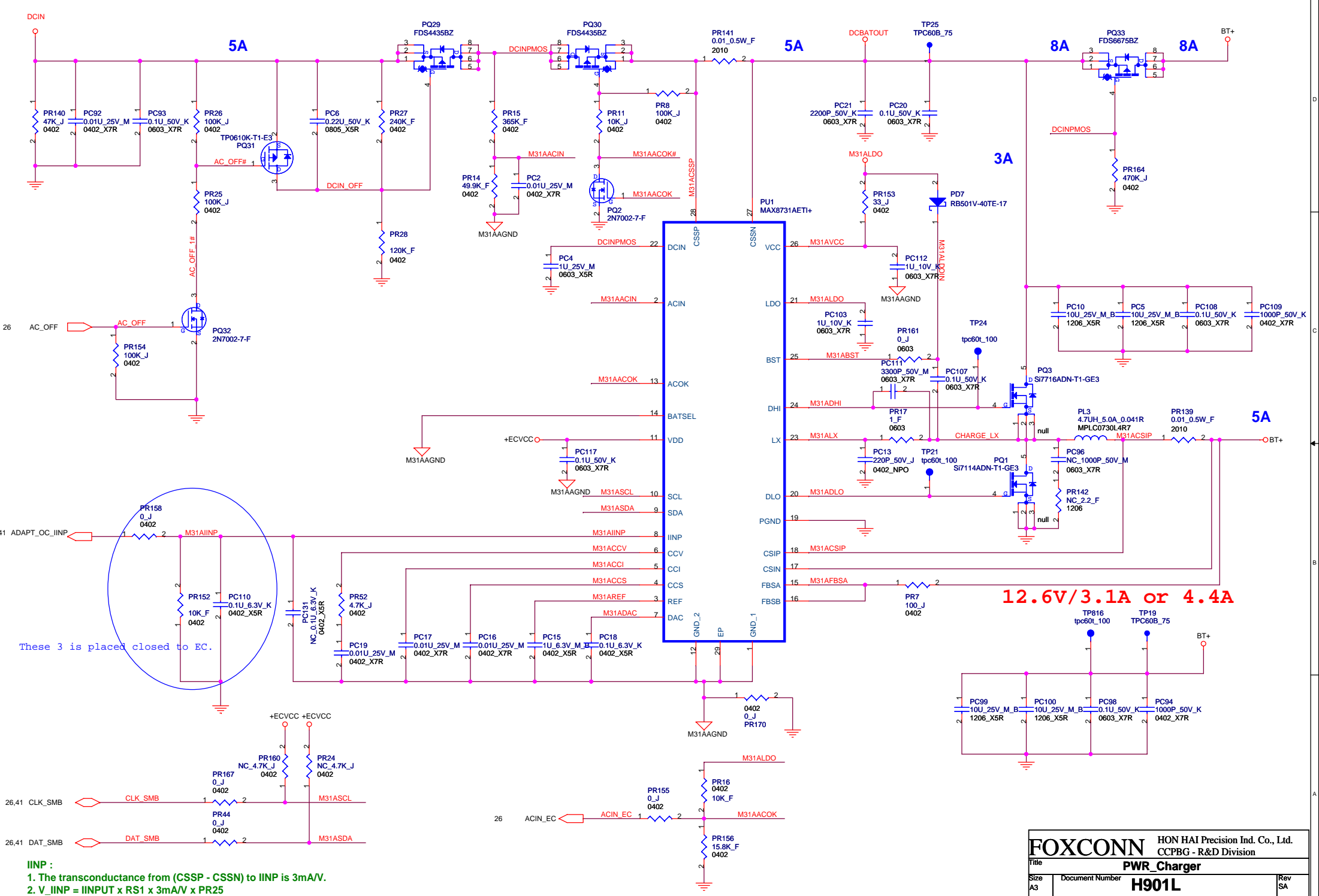


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<b>Title PWR_BTN&amp;LED&amp;BT DB</b>		
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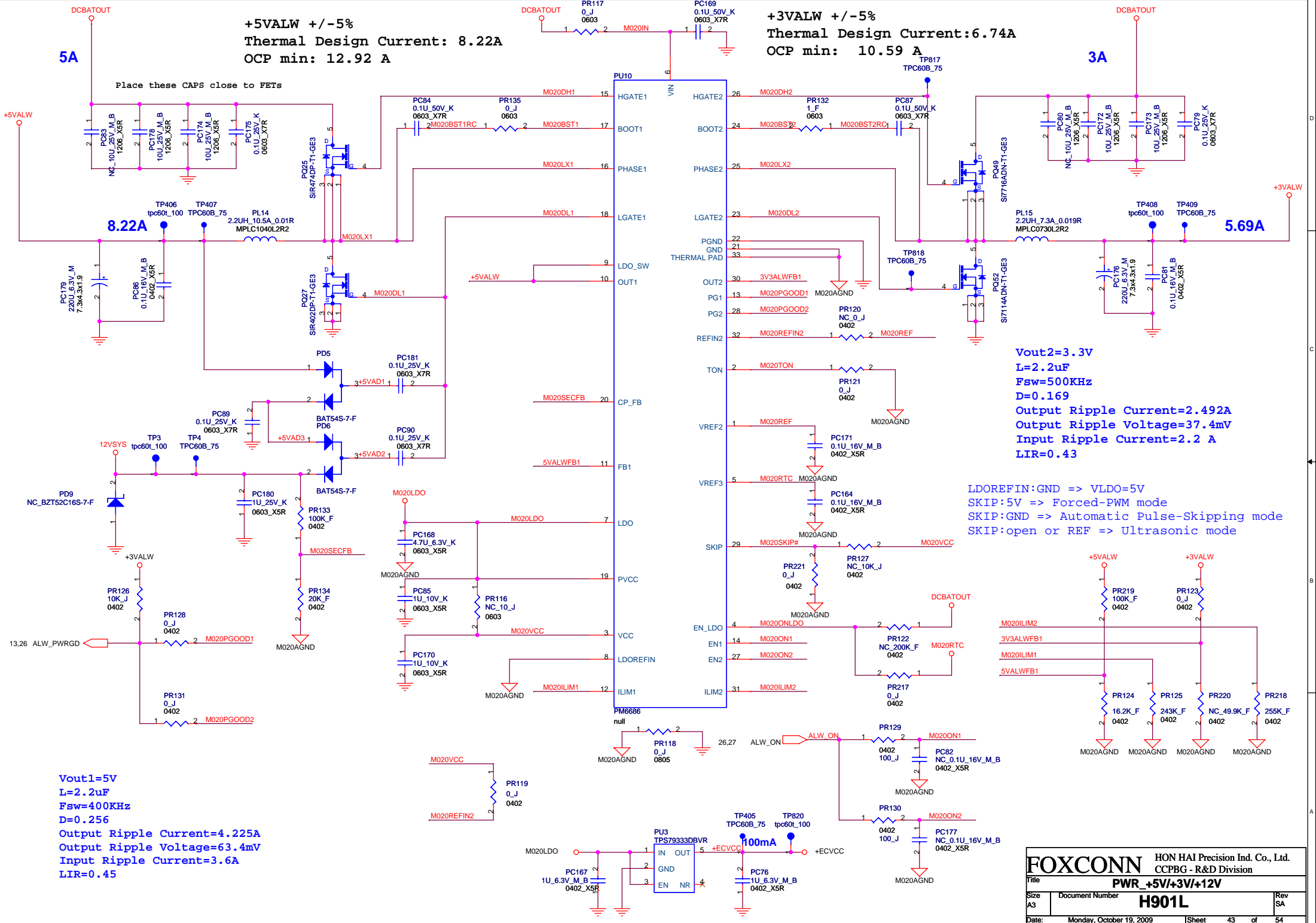


These 3 is placed closed to EC.

12.6V/3.1A or 4.4A

- IINP :**
- The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
  - $V_{IINP} = IINPUT \times RS1 \times 3mA/V \times PR25$

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		PWR Charger	
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**+5VALW +/-5%**  
**Thermal Design Current: 8.22A**  
**OCP min: 12.92 A**

**+3VALW +/-5%**  
**Thermal Design Current: 6.74A**  
**OCP min: 10.59 A**

**3A**

Place these CAPS close to FETs

**8.22A**

**5.69A**

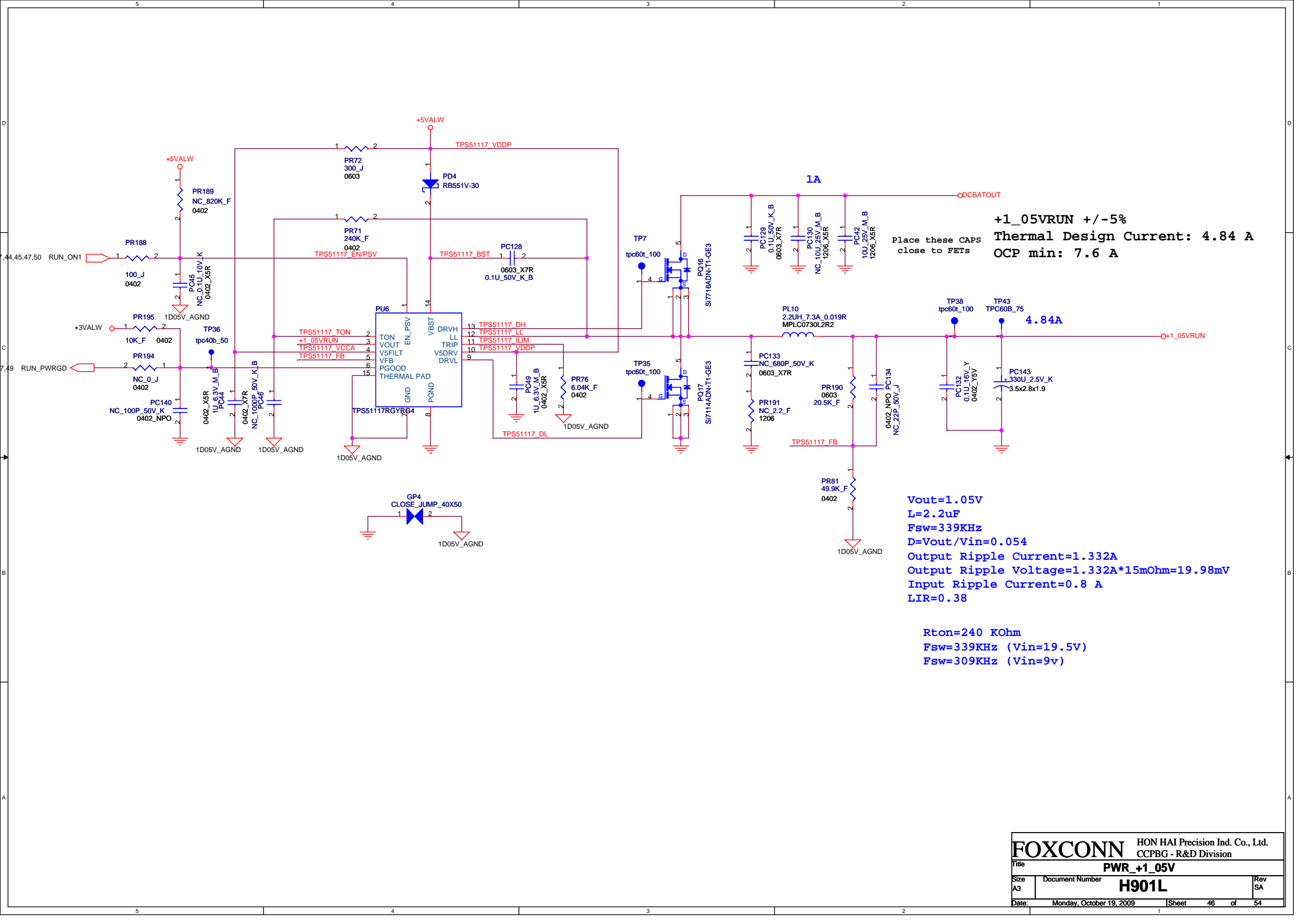
**Vout2=3.3V**  
**L=2.2uF**  
**Fsw=500KHz**  
**D=0.169**  
**Output Ripple Current=2.492A**  
**Output Ripple Voltage=37.4mV**  
**Input Ripple Current=2.2 A**  
**LIR=0.43**

LDOREFIN:GND => VLDO=5V  
 SKIP:5V => Forced-PWM mode  
 SKIP:GND => Automatic Pulse-Skipping mode  
 SKIP:open or REF => Ultrasonic mode

**Vout1=5V**  
**L=2.2uF**  
**Fsw=400KHz**  
**D=0.256**  
**Output Ripple Current=4.225A**  
**Output Ripple Voltage=63.4mV**  
**Input Ripple Current=3.6A**  
**LIR=0.45**







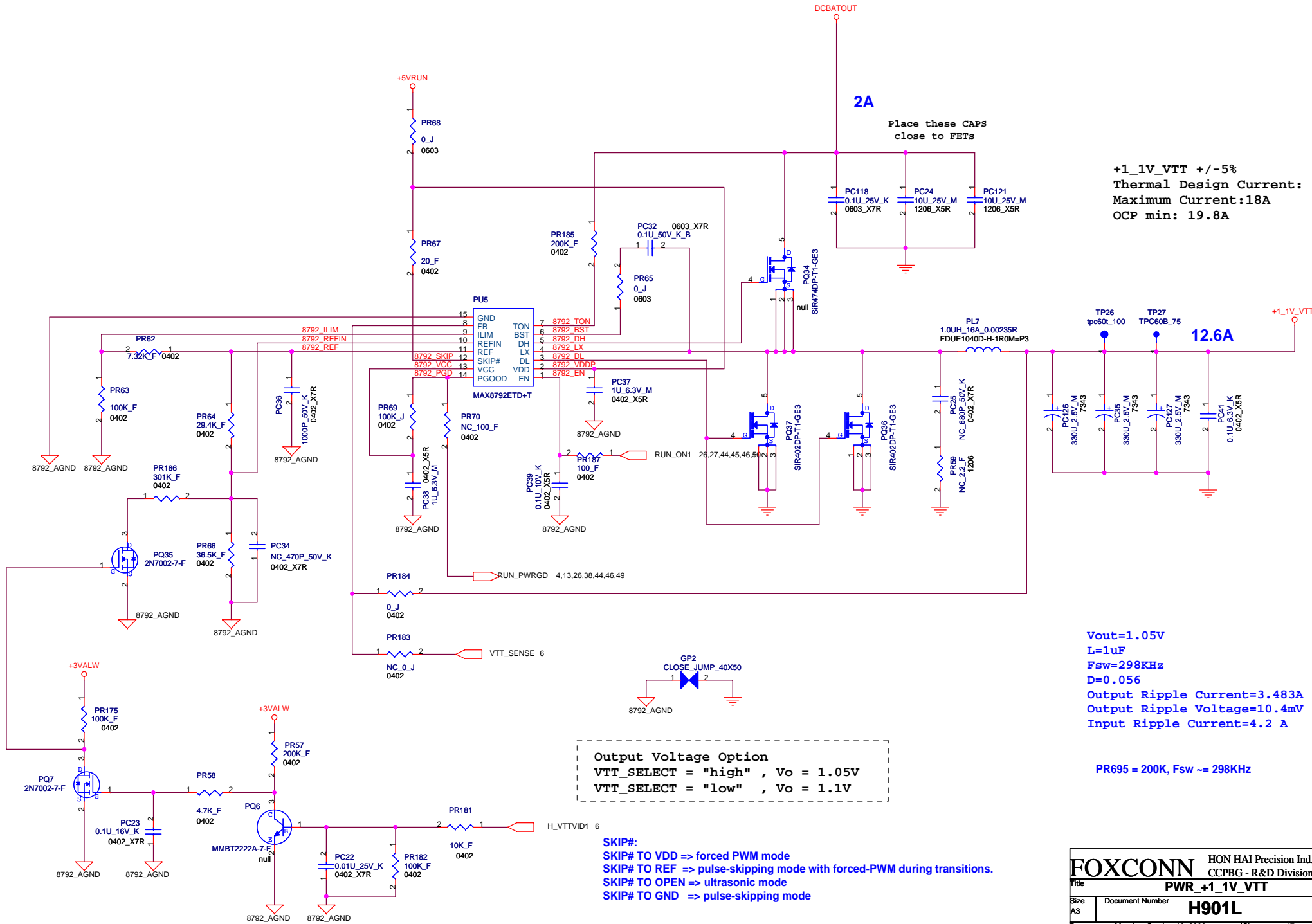
**+1.05VRUN +/-5%**  
**Thermal Design Current: 4.84 A**  
**OCP min: 7.6 A**

Place these CAPS close to FETs

**4.84A**

**Vout=1.05V**  
**L=2.2uF**  
**Fsw=339KHz**  
**D=Vout/Vin=0.054**  
**Output Ripple Current=1.332A**  
**Output Ripple Voltage=1.332A\*15mOhm=19.98mV**  
**Input Ripple Current=0.8 A**  
**LIR=0.38**

**Rton=240 KOhm**  
**Fsw=339KHz (Vin=19.5V)**  
**Fsw=309KHz (Vin=9v)**



+1\_1V\_VTT +/-5%  
 Thermal Design Current: 12.6A  
 Maximum Current: 18A  
 OCP min: 19.8A

12.6A

Vout=1.05V  
 L=1uF  
 Fsw=298KHz  
 D=0.056  
 Output Ripple Current=3.483A  
 Output Ripple Voltage=10.4mV  
 Input Ripple Current=4.2 A

PR695 = 200K, Fsw ~ 298KHz

Output Voltage Option  
 VTT\_SELECT = "high" , Vo = 1.05V  
 VTT\_SELECT = "low" , Vo = 1.1V

SKIP#:  
 SKIP# TO VDD => forced PWM mode  
 SKIP# TO REF => pulse-skipping mode with forced-PWM during transitions.  
 SKIP# TO OPEN => ultrasonic mode  
 SKIP# TO GND => pulse-skipping mode

Arrandale SV CPU  
 V(HFM):0.95V  
 V(LFM):0.875V  
 LL:-1.9mOhm  
 Icc\_max:48A  
 Icc\_TDC:32 A  
 I(DYNAMIC):TBD

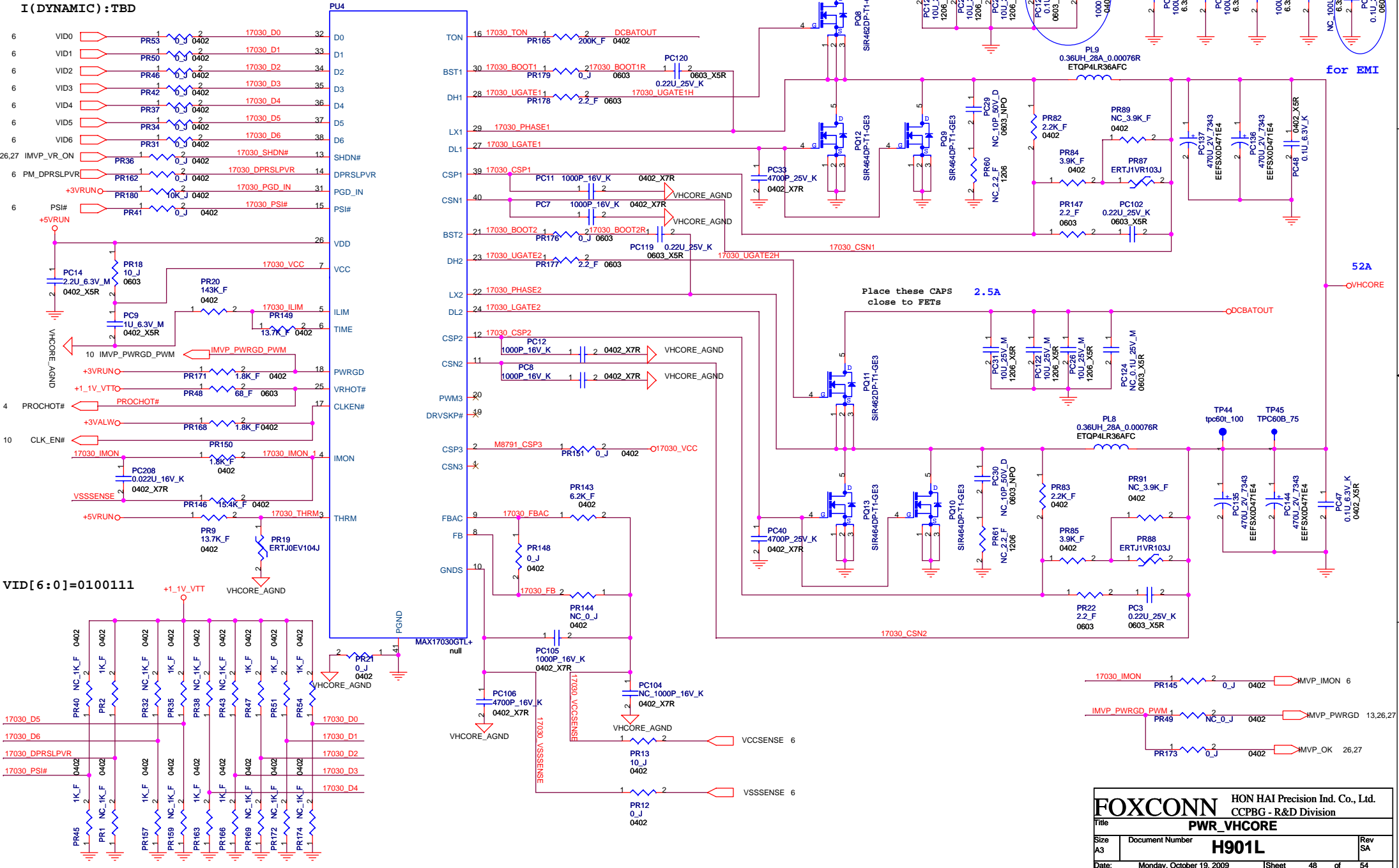
VID[5:3] for CSC, CRB default '100' = 50A (Iccmax)  
 VID[2:0] for MSID (To differentiate XE CPU from SV CPU)  
 DPRSLPVR='1' for IMVP6.5  
 Others are RSVD  
 Both PH and PD resistors are required to reserve for all 9 signals

OCP setting:60A(30A per phase).  
 PR149=13.7K Ohm

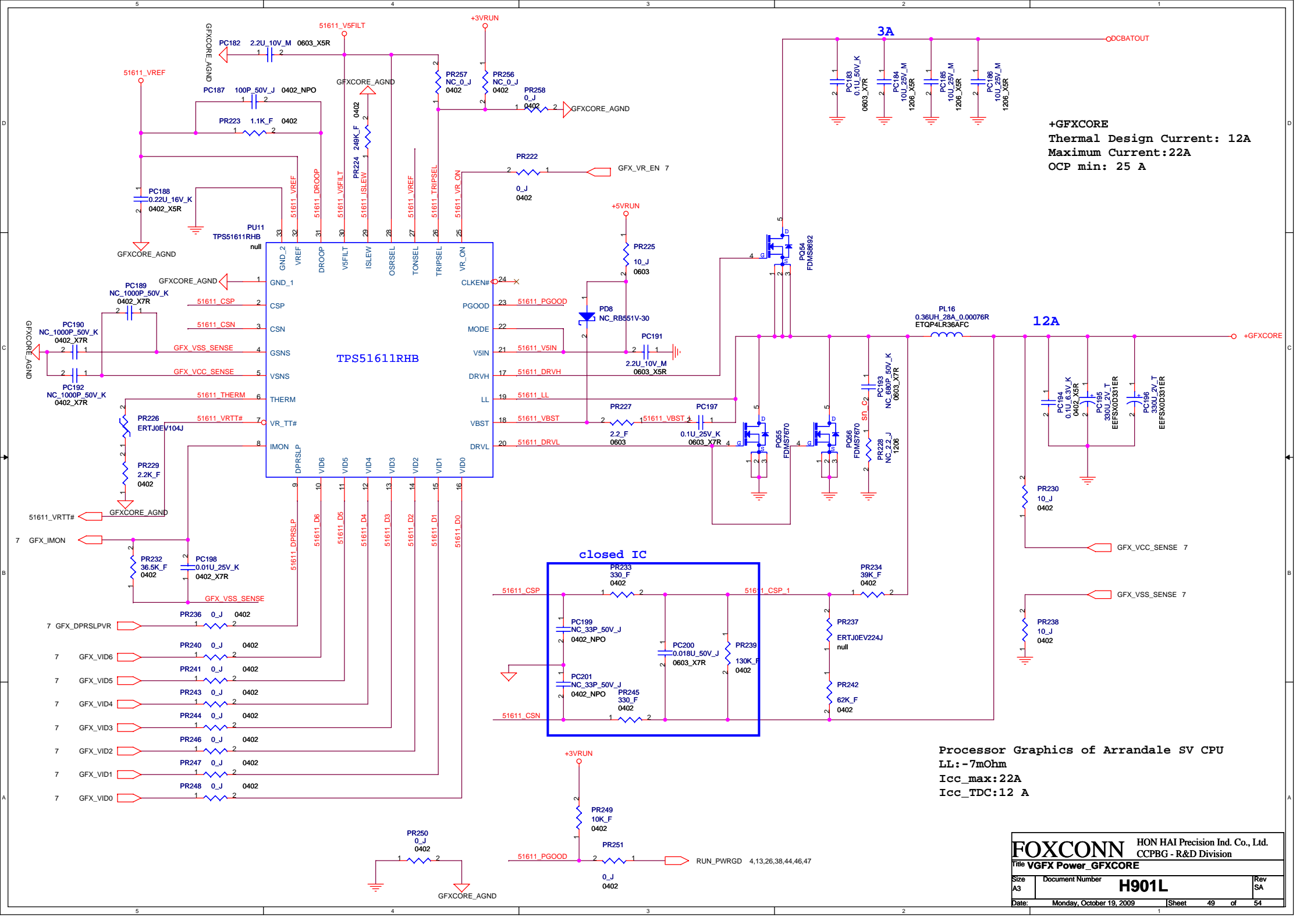
Place these CAPS close to FETs

2.5A  
 for EMI

Place these CAPS close to VCORE input

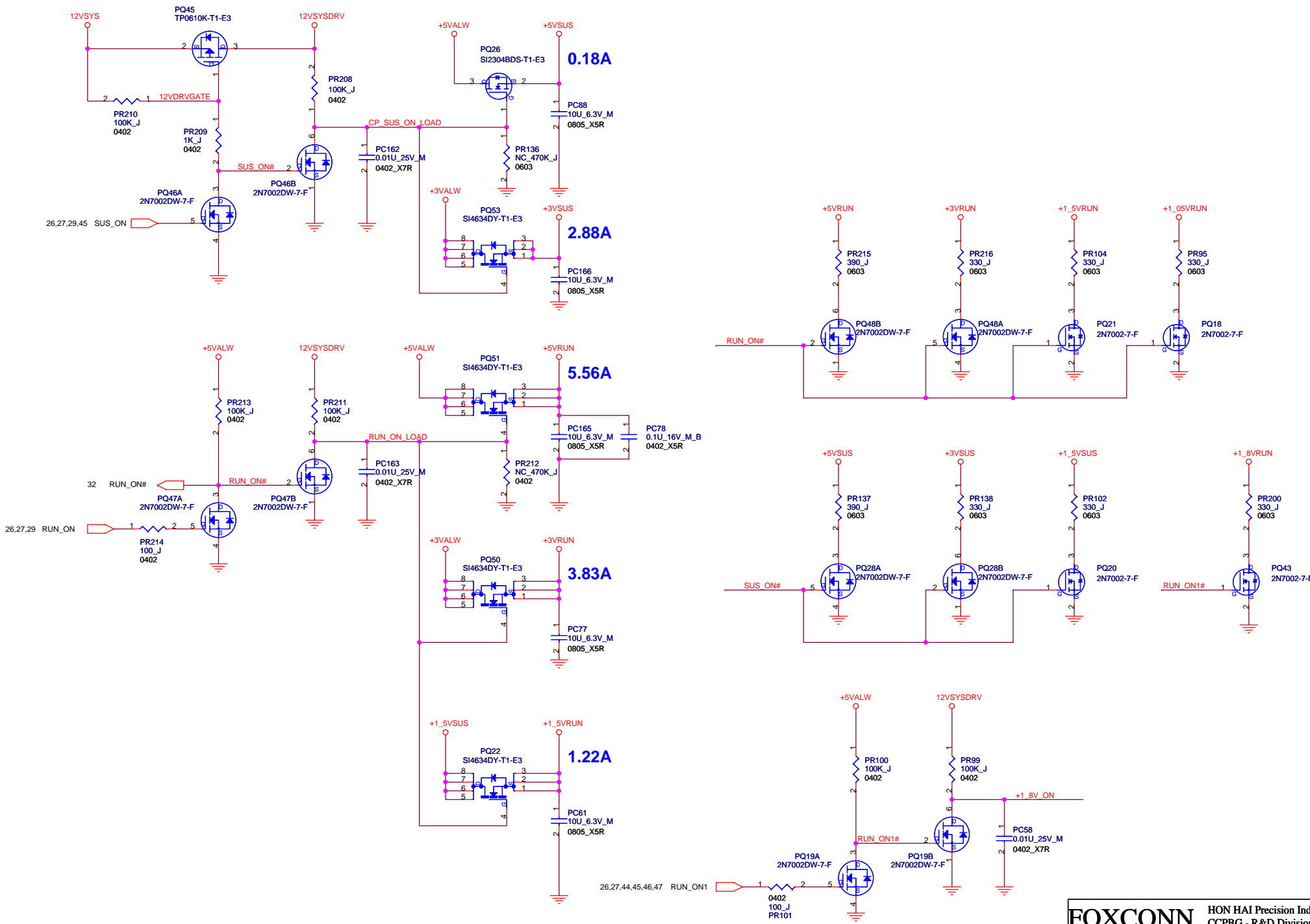


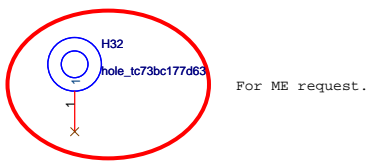
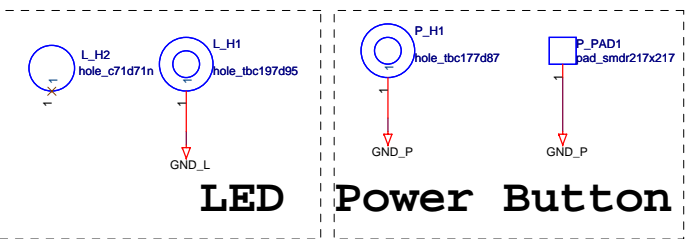
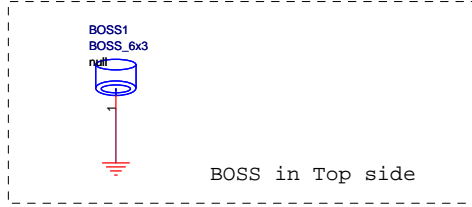
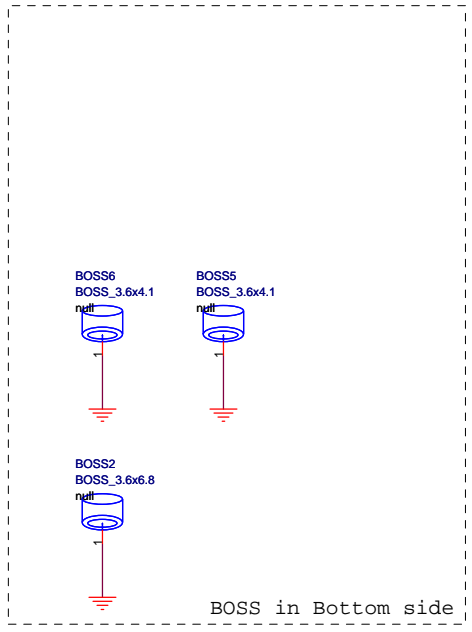
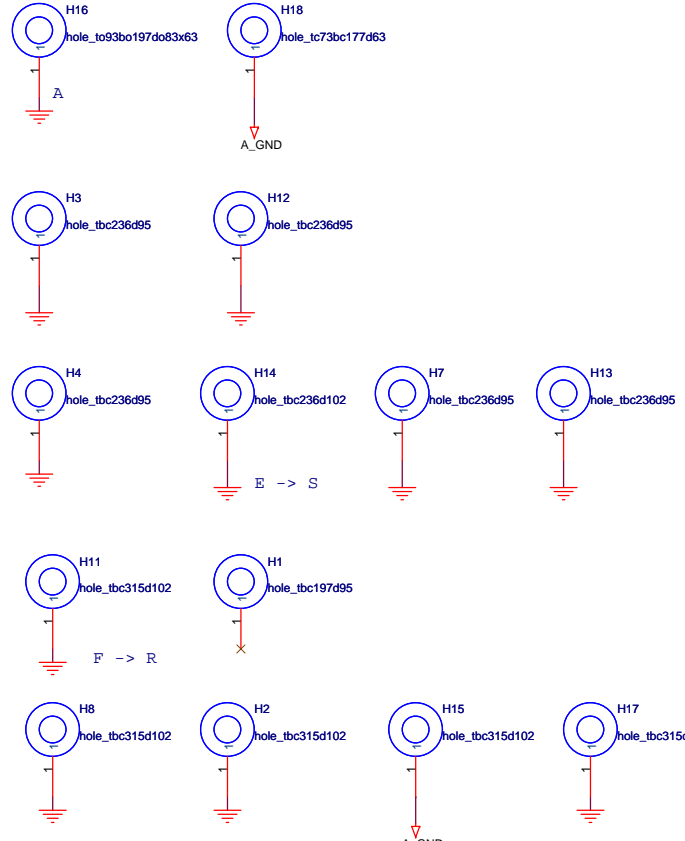
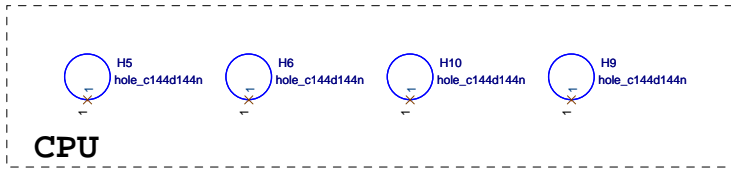
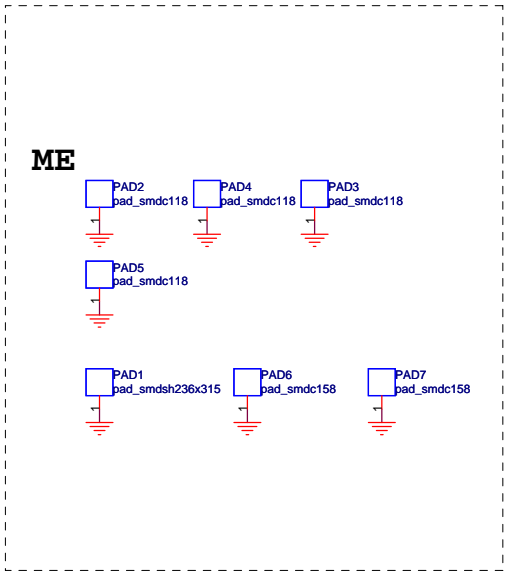




**+GFXCORE**  
 Thermal Design Current: 12A  
 Maximum Current: 22A  
 OCP min: 25 A

Processor Graphics of Arrandale SV CPU  
 LL: -7mOhm  
 Icc\_max: 22A  
 Icc\_TDC: 12 A





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Title <b>HOLE</b>			
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## H901L EVT

(2009/06/08)

P.39 Add Q62, Q63, R619, and R639 10K ohm and del D16 & D17 for leakage issue.

(2009/06/23)

P. 4 NC R712 0 ohm for DDR\_alert# noise.

(2009/06/25)

P.11 Change RTC battery P/N from 1M-BCR2032-LB00 to 1M-BCR2032-LB01.

(2009/07/01)

P.51 Add H32 for ME request.

(2009/07/14)

P.12 Add R645 & R646 2.2K ohm for SMBUS PH.

P.31 Change C35 & C38 from 18pF to 15pF for Crystal vendor recommend.

(2009/07/15)

P.22 Add C655, C656, C657 10pF, and L70, L71, L72 47R, change L61, L62, L63 from 33R to 47R for CRT.

(2009/07/16)

P.13 Add R293 0 ohm NC for SLP\_M#.

P.30 Change C33 and C44 from NPO 10% to 5% for PUR recommend.

P.39 Change P\_C1, P\_C2, L\_C1, L\_C2 from 10pF NPO 10% to 5% for PUR recommend.

P.32 Change C499 and C505 from 12pF NPO 10% to 5% for PUR recommend.

P.11 Change C735 from 12pF NPO 10% to 5% for PUR recommend.

P.30 Change C78 and C79 from 15pF NPO 10% to 5% for PUR recommend.

P.11 Change C736 from 15pF NPO 10% to 5% for PUR recommend.

P.38 Change C244 and C245 from 47pF NPO 10% to 5% for PUR recommend.

(2009/07/17)

P.13 Add R763 10K ohm PH for HDMI.

P.31 Add C512 0.1uF for Hipot test.

## H901L DVT

(2009/07/23)

P.36 Change R467 from 33K to 15K ohm and R472 from 15K to 4.7K ohm for Thermal recommend.

(2009/07/28)

P.24 Change HDMI connector from 2N-0019003-FKGO to 2N-0019002-MKGO

(2009/08/20)

P.28 Delete R27

P.31 Change L1 to LANKOM.

P.18 Delete R257

## H901L PVT

(2009/09/3)

P. 20 & 21 Change CN27 & CN28 to tray for L6 recommend.

P. 25 Change CN25 & CN8 to tray for L6 recommend.

P. 29 Change CN73 Part number for CIS recommend.

P. 20 Add R27 & R55 1K ohm for Intel M1 DDR solution.

P. 21 Add R56 & R57 1K ohm for Intel M1 DDR solution.

## H901L X-Build

(2009/09/16)

P.12 Change C701 & C702 from 18pF to 12pF for Crystal vendor recommend.

P.22 Add R474 0 ohm for EMI solution.

## H901L X-Build

(2009/09/18)

P.31 Add R612 1K ohm .

P.31 Delete C26

P.31 Delete U2


P.31 Delete R14

P.31 Delete R186

(2009/10/14)

P.29 Add L38 , L42 & L69

P.29 Delete R277, R281, R380, R381, R607, R609 for EMI

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<b>History (1)</b>			
Title	H901L_A00		
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# H900 Power Change History

Number	Date	Page	Title	Issue	Description	Version
1	2009/07/02	P.48	V_CORE	Chage exposed GND and VDD capacitor of VCORE to PGND.	Change PC14.2 from AGND to PGND. Change PU4.41 from AGND to PGND. Change PR21.2 from PGND to AGND.	X01
2	2009/07/02	P.48	V_CORE	Add feedback capacitor to improve GND noise for system with battery only can't power ON issue.	Add PC7: 1000pF 16V X7R(1C-2B20102-K001) . Add PC8: 1000pF 16V X7R(1C-2B20102-K001) . Add PC11: 1000pF 16V X7R(1C-2B20102-K001) . Add PC12: 1000pF 16V X7R(1C-2B20102-K001) .	X01
3	2009/07/02	P.48	V_CORE	Change boost resistor to reduce ring of Mosfet.	Change PR178 from 0 Ohm 0603 5%(1R-0000000-J300) to 2.2 Ohm 0603 1%(1R-000022X-F300) Change PR177 from 0 Ohm 0603 5%(1R-0000000-J300) to 2.2 Ohm 0603 1%(1R-000022X-F300)	X01
4	2009/07/08	P.49	+GFX_CORE	Delete some capacitors from TI suggestion. Fine tune load line and IMON setting.	Del PC190,PC192,PC189,PC199,PC201. Change PR223 from 3K 0402 1%(1R-0000302-F200) to 1.2K 0402 1%(1R-0000122-F200) Change PR232 from 10K 0402 1%(1R-0000103-F200) to 45.3K 0402 1%(1R-0004532-F200) Change PC198 from 3300P 50V 0402 10%(1C-2B20332-K000) to 0.47uF 6.3V 0402 10%(1C-2B20474-K000)	X01
5	2009/07/08	P.48	V_CORE	Modify DCR feedback and IMON setting. Change L-S Mosfet to SIR464 to improve efficiency.	Change PR84 and PR85 from 1.69K 0402 1%(1R-0001691-F200) to 3.9K 0402 1%(1R-0003901-F200) Change PR150 from 10K 0402 1%(1R-0000103-F200)to 1.8K 0402 1%(1R-0000182-F200) Change PC208 from 0.1uF 6.3V 0402(1C-2B20104-K101) to 0.022uF 16V 0402 X7R (1C-2B20223-K000) Change PR146 from 12K 0402 1%(1R-0000123-F200) to 15.4K 0402 1%(1R-0001542-F200) Change PQ9,PQ10,PQ12,PQ13 from SIR466(17-S1R466D-PT00) to SIR464(17-S1R464D-PT00)	X01
6	2009/07/10	P.42	Charger	Slow down P-Mos turn on to reduce inrush current of AC adapter.	Change PR28 from 100K 0402 5%(1R-0000104-J200) to 120K 0402 1%(1R-0000124-F200)	X01
7	2009/07/16	P.49	+GFX_CORE	Add a L-S Mosfet for GFX_CORE	Add PQ56:FDMS7670 (17-FDMS767-0000)	X01
8	2009/07/16	P.49	+GFX_CORE	Change GFX_CORE setting from vender's suggestion	Change PR224 from 124K 0402 1%(1R-0001243-F200) to 249K 0402 1%(1R-0002493-F200) Change PU11.33 to PGND. Change PU11.1 to AGND. Add a reserve PR258 between PU11.26 to AGND. Change PR234 from 82.5K 0402 1%(1R-0008252-F200) to 52.3K 0402 1%(1R-0005232-F200) Change PR242 from 63.4K 0402 1%(1R-0006342-F200) to 62K 0402 1%(1R-0000623-F200) Change PR239 from 51K 0402 1%(1R-0000513-F200) to 68K 0402 1%(1R-0000683-F200) Change PR223 from 1.2K 0402 1% (1R-0000122-F200) to 910 0402 1%(1R-0000911-F200)	X01
9	2009/07/20	P.50	Other power plane	Add discharge path for 1_5VRUN and 1_05VRUN	Add PR104:330 Ohm 0603 5%(1R-0000331-J300) Add PR95:330 Ohm 0603 5%(1R-0000331-J300) Add PQ21:2N7002-7-F SOT-23(17-2N70027-F000) Add PQ18:2N7002-7-F SOT-23(17-2N70027-F000)	X01

# H900 Power Change History

Number	Date	Page	Title	Issue	Description	Version
10	2009/08/21	P.49	GFX_CORE	Modify GFX_CORE setting(Load line,IMON and OCP).	Change PR234 from 52.3K to 36.5K 0402 1%(1R-0003652-F200) Change PR242 from 62K to 49.9K 0402 1%(1R-0004992-F200) Change PR239 from 68K to 47K 0402 1%(1R-0000473-F200) Change PC200 from 0.015uF to 0.022uF 50V 0603 X7R(1C-2B30223-K001) Change PR223 from 910 Ohm to 768 Ohm 0402 1%(1R-0007683-F200) Delete PR256: 0 Ohm 0402 5%(1R-0000000-J200) Add PR258: 0 Ohm 0402 5%(1R-0000000-J200) Change PR232 from 39K,5%,0402 to 54.9K,1%,0402(1R-0005492-F200) Change PC198 from 3300pF 16V to 0.01uF,25V,10%,0402(1C-2B20103-K000)	X01
11	2009/09/03	P.48	VCORE	Adding 2 capacitor for EMI.	Add PC125:0.1uF 25V X5R(1C-2B30104-M000) Add PC138:1000pF 50V X7R(1C-2B20102-K000)	X02
12	2009/09/07	P.49	GFX_CORE	Modify GFX_CORE setting from TI's suggestion.	Change PR234 to 39kohm 0402 1% Change PR242 to 62kohm 0402 1% Change PR239 to 130kohm 0402 1% Change PC200 to 18nF 0603 50V 5% X7R Change PR223 to 1.1kohm 0402 1% Change PR232 to 36.5kohm 0402 1% Change PC198 to 10nF 0402 25V 10% X7R	X02
13	2009/10/19	P.48	VCORE	Add a capacitor(0.1uF) on DCBATOUT rail for EMI.	Add PC139:0.1uF 25V X5R(1C-2B30104-M000)	