Compal Confidential

NAT02 M/B Schematics Document

Intel Clarksfield Processor with DDRIII + Ibex Peak-M + Madison Pro

2009-08-20

REV:0.1

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Block Diagram
Compal confidential
Model : NAT02

FFS
+3VS
P.13

FAN
+5VS
+3VS
P.13

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
48MHZ to CardReader page 12

PCH XDP
page 22

CPU XDP
133MHz
page 05

Intel
Arrandale/ Clarksfield
(DIS)
+CPU_CORE
+1.1VS_VTT
Processor
rPGA988A
page 4,5,6,7,8,9

PCI-E 2.0x16
5GT/s PER LANE
100MHz

PEG(DIS)

Memory BUS(DDRIII)
Dual Channel
1.5V DDRIII 800/1066/1333
6.4G/8.5G/10.6G
100M/133M/166M(CFD)

DDRIII-DIMM X2
BANK 0, 1, 2, 3, 4 ,5 ,6 ,7 ,8
+1.5V
+0.75VS
P.10,11

CRT CONN
+5VS
P.34

VGA

LVDS CONN
+LCDVDD
+3.3V_ALW
P.34

LVDS

DP CONN
+5VS
P.36

DPB

HDMI CONN
+5VS
P.35

DPA

AMD
Madison Pro
29 x 29 mm
+1.1VS
P.37,38,39,40,41

VRAM 64Mx16
P.42,43

DMI x4
100MHz
1GB/s x4

Intel
Ibex Peak-M
PCH
+1.05VS
page 14,15,16,17
18,19,20,21,22

100MHz

PCI-Express x 8 (ABD PCIE1 2.5GT/S CKD PCIE1/2 2.5/5GT/S)

USBx14 3.3V 48MHz
SATA x 6 100MHz
(GEN1 1.5GT/S ,GEN2 3GT/S)
HD Audio 3.3V 24MHz
SPI

Right Front Side.
USB Port X1
+5V_ALW
P.29
To Card-reader subboard

Right behind side.
USB Port1 X1
+5V_ALW
P.29
To Single USB subboard

Bluetooth
P.29

Touch Screen
P.31

Camera
P.29

Charge USB/E-SATA Ports X1
+5VALW
P.29

port 5

SPI ROM x1
2MB
page 14

LPC BUS
+3VS
33MHz

To Card-reader subboard
P.29

8 IN 1 CONN
+3VS

IEEE1394

CardBus
OZ888GS0
+3VS
+1.8VS

Express Card
P.27

PCI Express BUS

RJ45

RTL8111DL
+3VALW
P.23

ENE KBC
KB926QFD3
+RTC_CELL
+3VALW
P.30

SB3526
+3VS
page 31
To Cap Sensor subboard

SPI

Int.KBD & BL
P.31

Touch Pad
P.31

Flash ROM
128KB
P.30
16Mx1sector

port 4
E-ODD
+3VS
+5VS
P.28

port 1
S-HDD-2
+5VS
P.28

port 0
S-HDD-1
+5VS
P.28

Azalia Codec
92HD73C
+3VS
+VDDA
P.24

AMP
MAX9736A
B+
P.25

Speaker

AMP
MAX9736A
B+
P.25

Subwoofer

AMP
MAX4411x2
P.24

Dig. MIC
P.29

HeadPhone & MIC Jack
+3VS

PCIE3
Mini Card 3
TV Tuner
+3VS
+1.5VS
P.27
USB[x]

PCIE2
Mini Card 2
WLAN
+3VS
+1.5VS
P.26
USB[x]

PCIE1
Mini Card 1
WWAN
+3VS
+1.5VS
P.26
USB[x]

DC/DC Interface
P.32

BATT IN
P.53

VCORE
P.52

1.5V/0.75V
P.49

Power Sequence

1.1VS_VTT
P.50

CHARGER
P.46

3V/5V
P.47

DC IN
P.45

GPU/1.1V
P.51

1.05V/1.8V
P.48

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+GPU_CORE	Core voltage for GPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.1VS	1.1V power rail for PCIE of GUP	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
B+_BIAS	B+ always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	VGA	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
X00	M96	0	0 V	0 V	0.100 V
X01	M96	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
X02	M96	18K +/- 1%	0.436 V	0.503 V	0.538 V
MP	M96	33K +/- 1%	0.712 V	0.819 V	0.875 V
X00	Madison	56K +/- 1%	1.036 V	1.185 V	1.264 V
X01	Madison	100K +/- 1%	1.453 V	1.650 V	1.759 V
X02	Madison	200K +/- 1%	1.935 V	2.200 V	2.341 V
MP	Madison	NC	2.500 V	3.300 V	3.300 V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
WWAN	
WLAN	
Express Card	
VGA thermal sensor	

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3191AKLFT, SLG8SP585)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
Free Fall Sensor	
CPU XDP	
PCH XDP	
XDCP_ISL90727	0101 110Xb
XDCP_ISL90728	0111 110Xb

USB Port Table

USB Port	Device
0	USB&ESATA
1	Reader/BD
2	USB board
3	WPAN
4	WLAN
5	WWAN
6	NC
7	NC
8	Express
9	Touch screen
10	Bluetooth
11	Camera

BTO Option Table

BTO Item	BOM Structure

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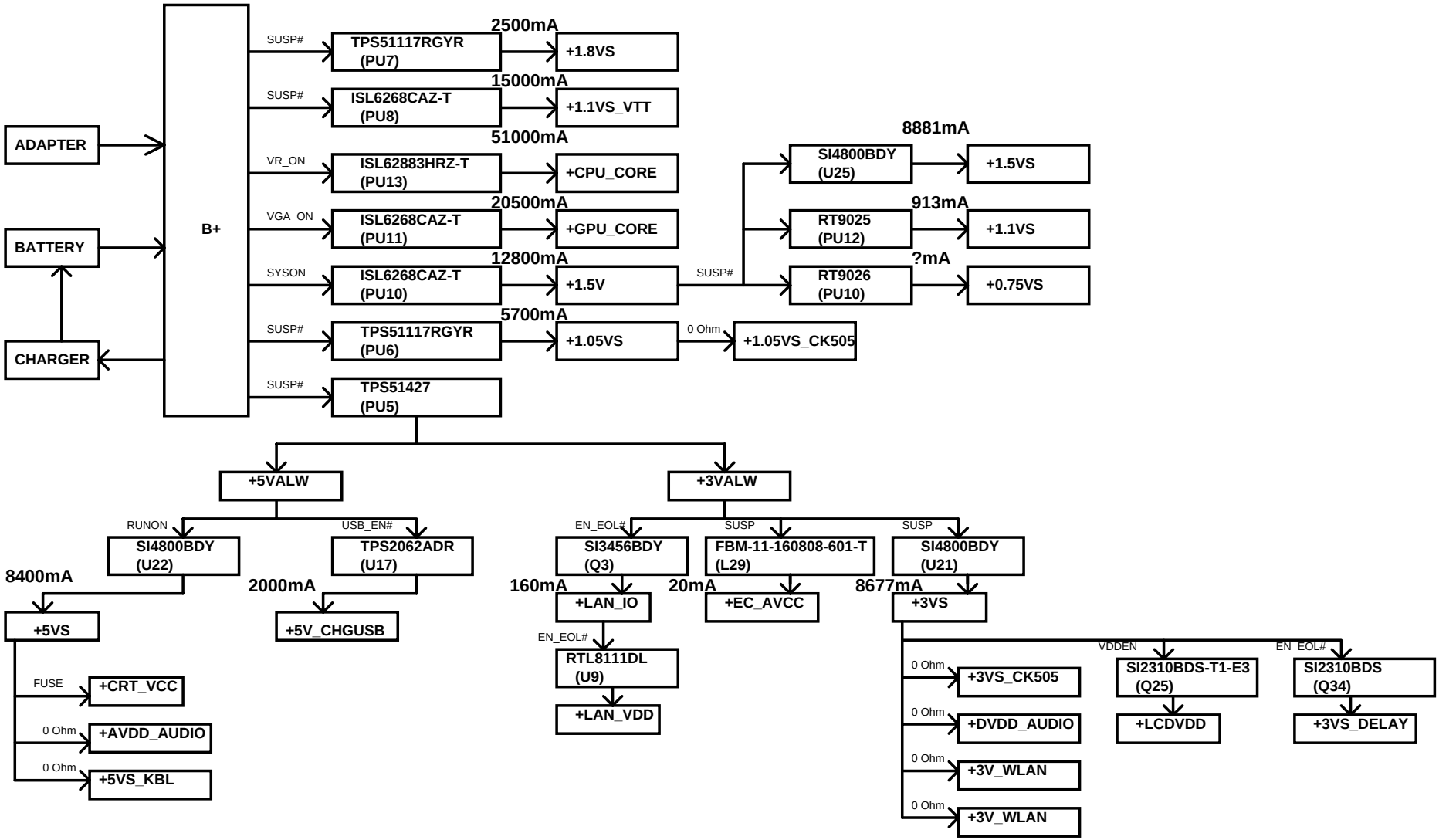

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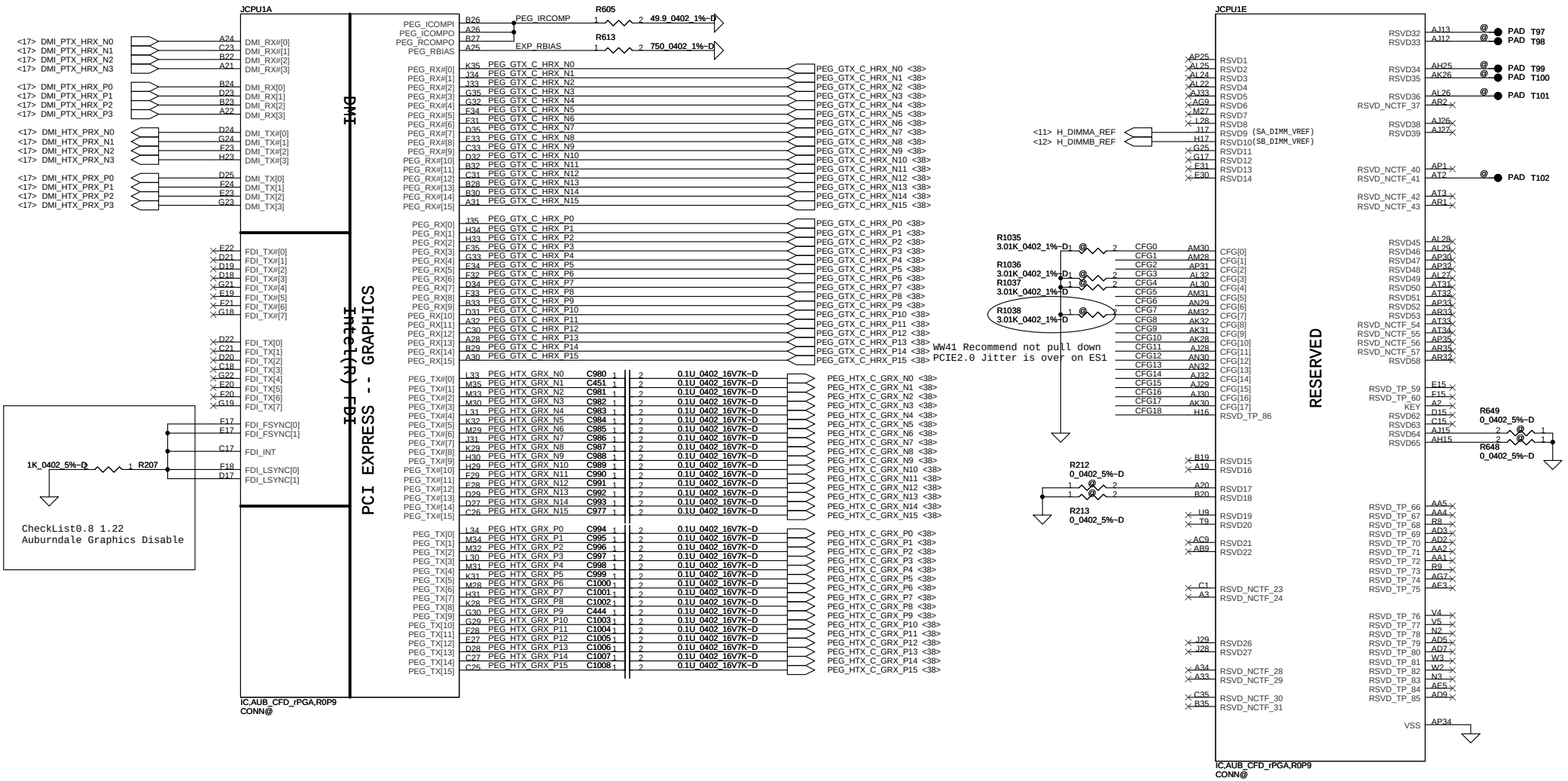

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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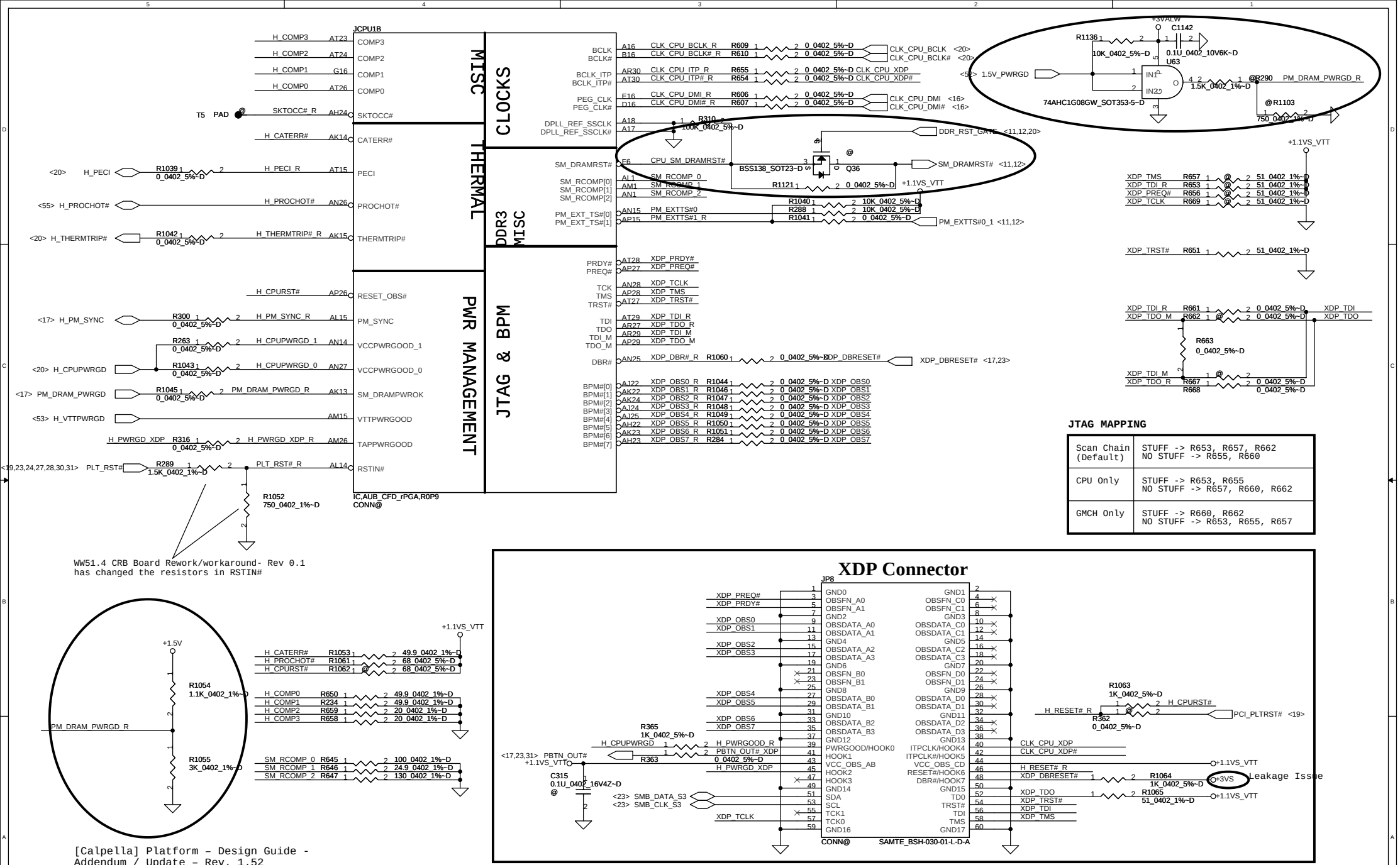

JTAG MAPPING

Scan Chain (Default)	STUFF -> R653, R657, R662 NO STUFF -> R655, R660
CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
GMCH Only	STUFF -> R660, R662 NO STUFF -> R653, R655, R657

WW51.4 CRB Board Rework/workaround- Rev 0.1
has changed the resistors in RSTIN#

[Calpella] Platform – Design Guide -
Addendum / Update – Rev. 1.52

XDP Connector

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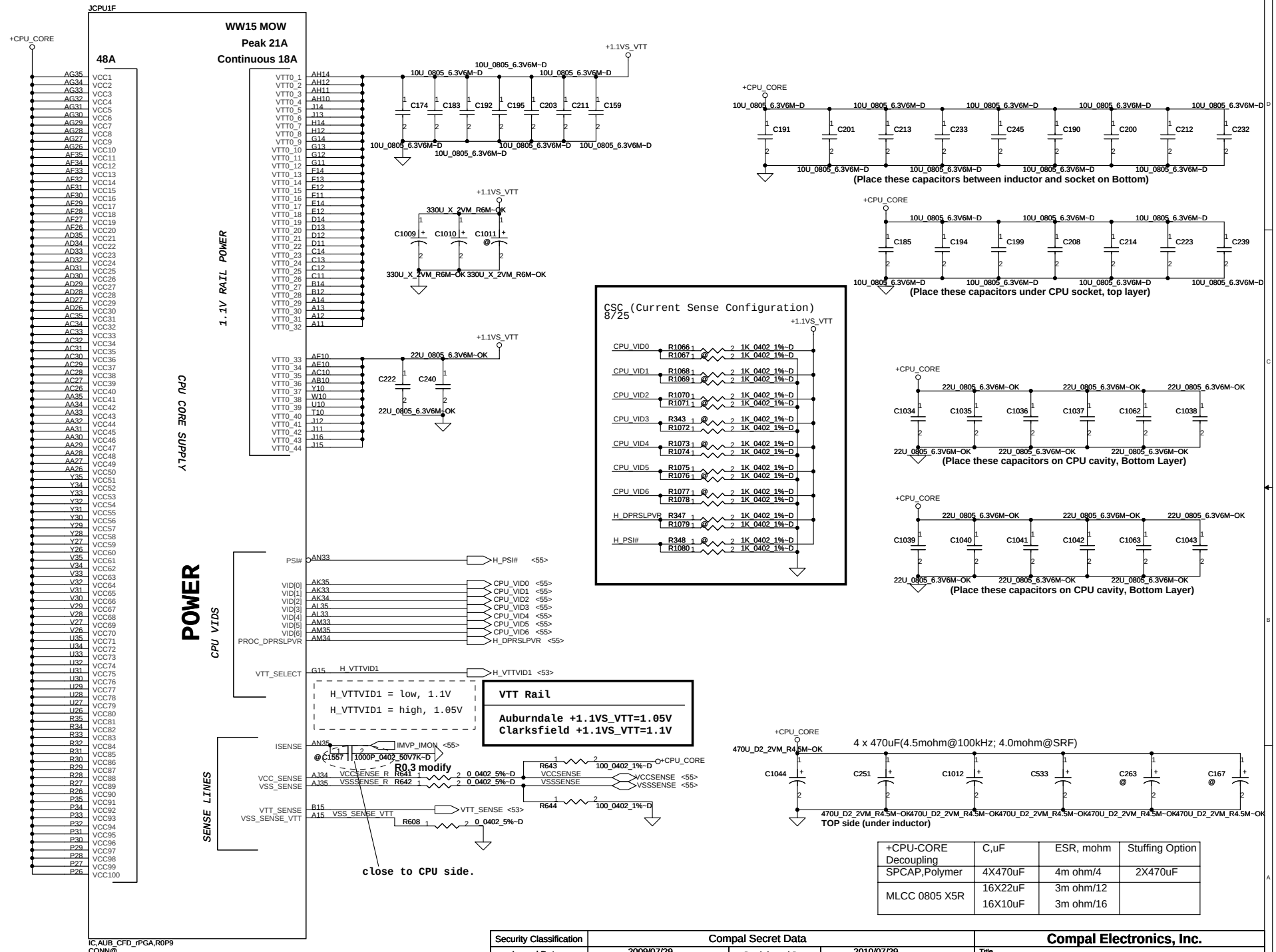

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

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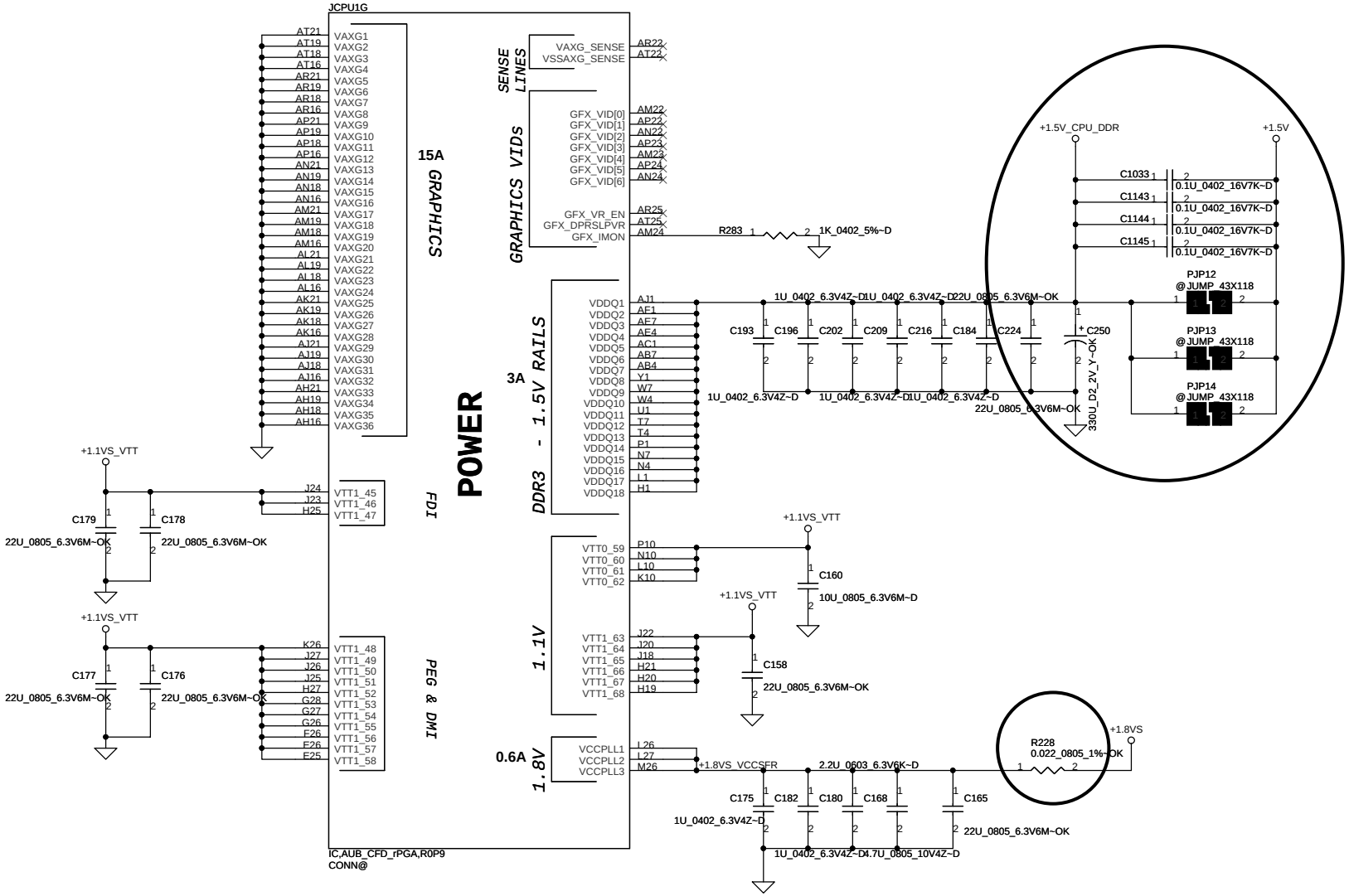

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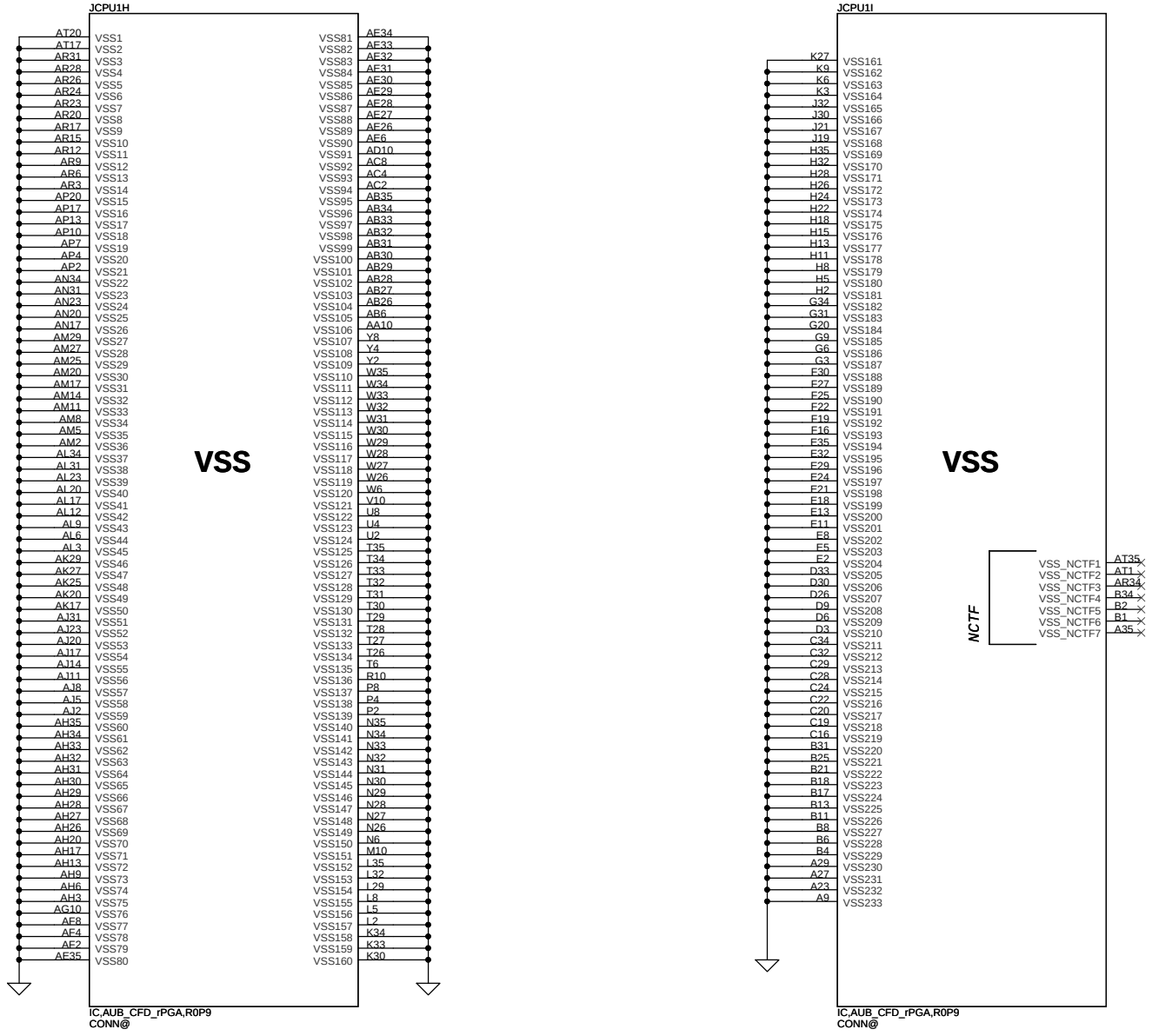

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M1 Circuit

M2 Circuit

M3 Circuit

2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

JDIMM1

FOX_AS0A626-U4RN-7F
CONN@

DDR3 SO-DIMM A
Standard Type

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M1 Circuit

+1.5V

R1230 1K_0402_1%~D

+V_DDR3_DIMMB_REF

+V_DDR3_DIMMB_REF

R1231 1K_0402_1%~D

DDR_RST_GATE <6,11,20>

+V_DDR3_DIMMB_REF

Q44 @BSS138_SOT23~D

H_DIMMB_REF <5>

@ R321 100K_0402_5%~D

2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

M1 Circuit

+V_DDR3_DIMMB_REF — R166 0_0402_5%~D — VREF_DQB

M3 Circuit

<5> H_DIMMB_REF — R165 @ 0_0402_5%~D

VREF_POT1_R — R186 @ 0_0402_5%~D

C110 2.2U_0805_16V4Z~D

C122 0.1U_0402_16V4Z~D

<7> DDR_B_DQS#[0..7]

<7> DDR_B_D[0..63]

<7> DDR_B_DM[0..7]

<7> DDR_B_DQS[0..7]

<7> DDR_B_MA[0..15]

<11,16,23> PCH_SMBCLK — PCH_SMBCLK

<11,16,23> PCH_SMBDATA — PCH_SMBDATA

M2 Circuit

+3V

+1.5V

@C156 1U_0402_6.3V4Z~D

@U8 ISL90728WIE627Z-TK_SC70-6

VDD RH GND RW SCL SDA

@R196 12.1K_0402_1%~D

@R197 12.1K_0402_1%~D

VREF_RW_POT1

+5VALW

@U46B LM358DT_SO8

@R193 2.2_0402_5%~D

VREF_POT1_R

@ R194 10_0402_5%~D

C128 1U_0402_6.3V4Z~D @

VREF_OPAMP_POT1

PCH_SMBCLK

PCH_SMBDATA

PP_S4GT_Q_1

<11> PP_S4GT — PP_S4GT — @ Q49 2N7002LT1G_SOT23-3

Layout Note: Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

10U_0805_6.3V6M~D 10U_0805_6.3V6M~D 0.1U_0402_16V4Z~D 0.1U_0402_16V4Z~D

C172 C188 C206 C173 C189 C207 C1047 C1048 C1049 C1050 C198 330U_D2_2V_Y~OK

10U_0805_6.3V6M~D

10U_0805_6.3V6M~D 10U_0805_6.3V6M~D 10U_0805_6.3V6M~D 0.1U_0402_16V4Z~D 0.1U_0402_16V4Z~D

Layout Note: Place near JDIMM2.203 & JDIMM2.204

+0.75VS

1U_0603_10V4Z~D

C1018 C282 C283 C1019 C298

1U_0603_10V4Z~D 10U_0805_6.3V6M~D

1U_0603_10V4Z~D 1U_0603_10V4Z~D

JDIMM2

	VREF_DQ	1	VSS1	2	
	VSS2	3	DQ4	4	DDR_B_D4
DDR_B_D0	DQ0	5	DQ5	6	DDR_B_D5
DDR_B_D1	DQ1	7	VSS3	8	
	VSS4	9	DQS#0	10	DDR_B_DQS#0
DDR_B_DM0	DM0	11	DQS0	12	DDR_B_DQS0
	VSS5	13	VSS6	14	
DDR_B_D2	DQ2	15	DQ6	16	DDR_B_D6
DDR_B_D3	DQ3	17	DQ7	18	DDR_B_D7
	VSS7	19	VSS8	20	
DDR_B_D8	DQ8	21	DQ12	22	DDR_B_D12
DDR_B_D9	DQ9	23	DQ13	24	DDR_B_D13
	VSS9	25	VSS10	26	
DDR_B_DQS#1	DQS#1	27	DM1	28	DDR_B_DM1
DDR_B_DQS1	DQS1	29	RESET#	30	SM_DRAMRST#
	VSS11	31	VSS12	32	SM_DRAMRST# <6,11>
DDR_B_D10	DQ10	33	DQ14	34	DDR_B_D14
DDR_B_D11	DQ11	35	DQ15	36	DDR_B_D15
	VSS13	37	VSS14	38	
DDR_B_D16	DQ16	39	DQ20	40	DDR_B_D20
DDR_B_D17	DQ17	41	DQ21	42	DDR_B_D21
	VSS15	43	VSS16	44	
DDR_B_DQS#2	DQS#2	45	DM2	46	DDR_B_DM2
DDR_B_DQS2	DQS2	47	VSS17	48	
	VSS18	49	DQ22	50	DDR_B_D22
DDR_B_D18	DQ18	51	DQ23	52	DDR_B_D23
DDR_B_D19	DQ19	53	VSS19	54	
	VSS20	55	DQ28	56	DDR_B_D28
DDR_B_D24	DQ24	57	DQ29	58	DDR_B_D29
DDR_B_D25	DQ25	59	VSS21	60	
	VSS22	61	DQS#3	62	DDR_B_DQS#3
DDR_B_DM3	DM3	63	DQS3	64	DDR_B_DQS3
	VSS23	65	VSS24	66	
DDR_B_D26	DQ26	67	DQ30	68	DDR_B_D30
DDR_B_D27	DQ27	69	DQ31	70	DDR_B_D31
	VSS25	71	VSS26	72	
<7> DDR_B_CKE0 DDR_B_CKE0	CKE0	73	CKE1	74	DDR_B_CKE1 DDR_B_CKE1 <7>
	VDD1	75	VDD2	76	
	NC1	77	A15	78	DDR_B_MA15
<7> DDR_B_BS2 DDR_B_BS2	BA2	79	A14	80	DDR_B_MA14
	VDD3	81	VDD4	82	
DDR_B_MA12	A12/BC#	83	A11	84	DDR_B_MA11
DDR_B_MA9	A9	85	A7	86	DDR_B_MA7
	VDD5	87	VDD6	88	
DDR_B_MA8	A8	89	A6	90	DDR_B_MA6
DDR_B_MA5	A5	91	A4	92	DDR_B_MA4
	VDD7	93	VDD8	94	
DDR_B_MA3	A3	95	A2	96	DDR_B_MA2
DDR_B_MA1	A1	97	A0	98	DDR_B_MA0
	VDD9	99	VDD10	100	
<7> DDR_B_CLK0 DDR_B_CLK0	CK0	101	CK1	102	DDR_B_CLK1 DDR_B_CLK1 <7>
<7> DDR_B_CLK0# DDR_B_CLK0#	CK0#	103	CK1#	104	DDR_B_CLK1# DDR_B_CLK1# <7>
	VDD11	105	VDD12	106	
DDR_B_MA10	A10/AP	107	BA1	108	DDR_B_BS1 DDR_B_BS1 <7>
<7> DDR_B_BS0 DDR_B_BS0	BA0	109	RAS#	110	DDR_B_RAS# DDR_B_RAS# <7>
	VDD13	111	VDD14	112	
DDR_B_WE#	WE#	113	S0#	114	DDR_B_CS0# DDR_B_CS0# <7>
<7> DDR_B_WE# <7> DDR_B_CAS# DDR_B_CAS#	CAS#	115	ODT0	116	DDR_B_ODT0 DDR_B_ODT0 <7>
	VDD15	117	VDD16	118	
DDR_B_MA13	A13	119	ODT1	120	DDR_B_ODT1 DDR_B_ODT1 <7>
<7> DDR_B_CS1# DDR_B_CS1#	S1#	121	NC2	122	
	VDD17	123	VDD18	124	
	NCTEST	125	VREF_CA	126	DDR_VREF_CA_DIMMB R1058 0_0402_5%~D
	VSS27	127	VSS28	128	
DDR_B_D32	DQ32	129	DQ36	130	DDR_B_D36
DDR_B_D33	DQ33	131	DQ37	132	DDR_B_D37
	VSS29	133	VSS30	134	
DDR_B_DQS#4	DQS#4	135	DM4	136	DDR_B_DM4
DDR_B_DQS4	DQS4	137	VSS31	138	
	VSS32	139	DQ38	140	DDR_B_D38
DDR_B_D34	DQ34	141	DQ39	142	DDR_B_D39
DDR_B_D35	DQ35	143	VSS33	144	
	VSS34	145	DQ44	146	DDR_B_D44
DDR_B_D40	DQ40	147	DQ45	148	DDR_B_D45
DDR_B_D41	DQ41	149	VSS35	150	
	VSS36	151	DQS#5	152	DDR_B_DQS#5
DDR_B_DM5	DM5	153	DQS5	154	DDR_B_DQS5
	VSS37	155	VSS38	156	
DDR_B_D42	DQ42	157	DQ46	158	DDR_B_D46
DDR_B_D43	DQ43	159	DQ47	160	DDR_B_D47
	VSS39	161	VSS40	162	
DDR_B_D48	DQ48	163	DQ52	164	DDR_B_D52
DDR_B_D49	DQ49	165	DQ53	166	DDR_B_D53
	VSS41	167	VSS42	168	
DDR_B_DQS#6	DQS#6	169	DM6	170	DDR_B_DM6
DDR_B_DQS6	DQS6	171	VSS43	172	
	VSS44	173	DQ54	174	DDR_B_D54
DDR_B_D50	DQ50	175	DQ55	176	DDR_B_D55
DDR_B_D51	DQ51	177	VSS45	178	
	VSS46	179	DQ60	180	DDR_B_D60
DDR_B_D56	DQ56	181	DQ61	182	DDR_B_D61
DDR_B_D57	DQ57	183	VSS47	184	
	VSS48	185	DQS#7	186	DDR_B_DQS#7
DDR_B_DM7	DM7	187	DQS7	188	DDR_B_DQS7
	VSS49	189	VSS50	190	
DDR_B_D58	DQ58	191	DQ62	192	DDR_B_D62
DDR_B_D59	DQ59	193	DQ63	194	DDR_B_D63
	VSS51	195	VSS52	196	
	SA0	197	EVENT#	198	PM_EXTTS#0_1 PM_EXTTS#0_1 <6,11>
	VDDSPD	199	SDA	200	SMBDATA SMBDATA <11,13,14,16>
	SA1	201	SCL	202	SMBCLK SMBCLK <11,13,14,16>
	VTT1	203	VTT2	204	+0.75VS
	G1	205	G2	206	

FOX_AS0A626-U8RN-7F CONN@

+1.5V — R1059 10K_0402_5%~D — +3VSO — R1082 10K_0402_5%~D

C1020 2.2U_0603_6.3V4Z~D

C277 0.1U_0402_16V4Z~D

+V_DDR3_DIMMB_REF2

DDR_VREF_CA_DIMMB R1058 0_0402_5%~D

C231 2.2U_0603_6.3V4Z~D

C221 0.1U_0402_16V4Z~D

M1 Circuit

+1.5V

R1249 1K_0402_1%~D

+V_DDR3_DIMMB_REF2

+V_DDR3_DIMMB_REF2

R1250 1K_0402_1%~D

DDR3 SO-DIMM B Standard Type

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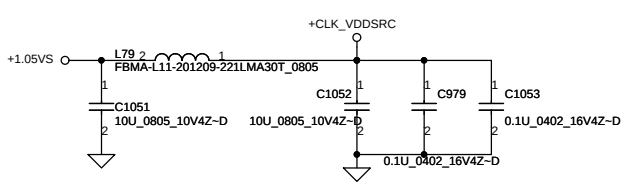
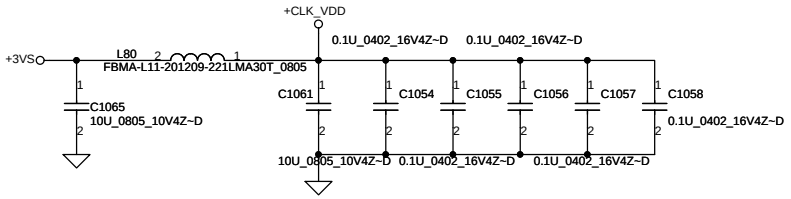
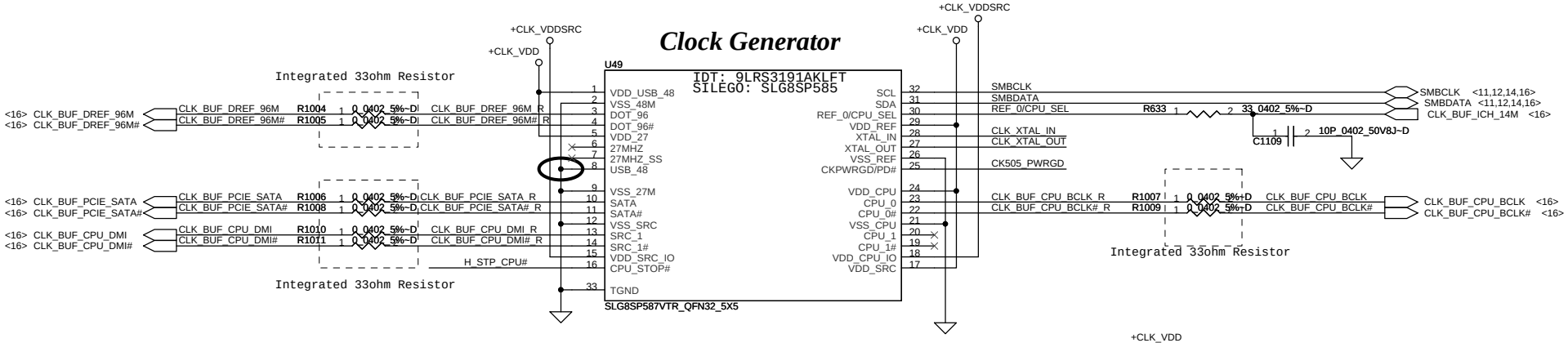
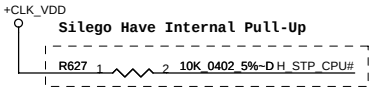
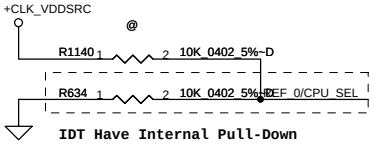




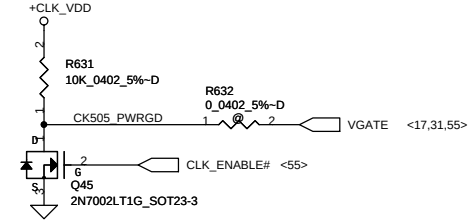
Clock Generator

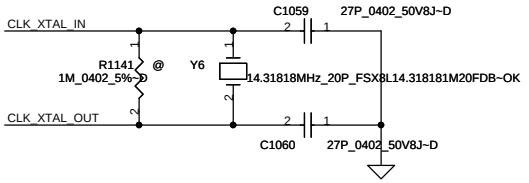






PIN 30	CPU_0	CPU_1
0(Default)	133MHz	133MHz
1	100MHz	100MHz





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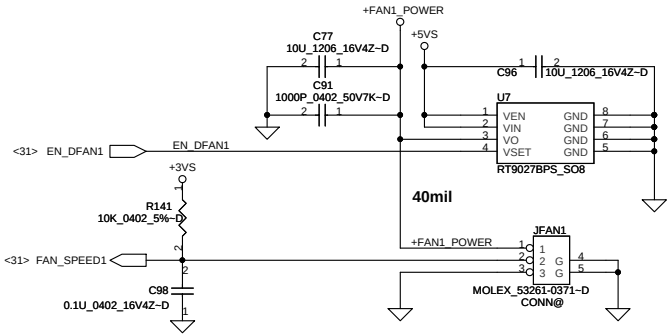
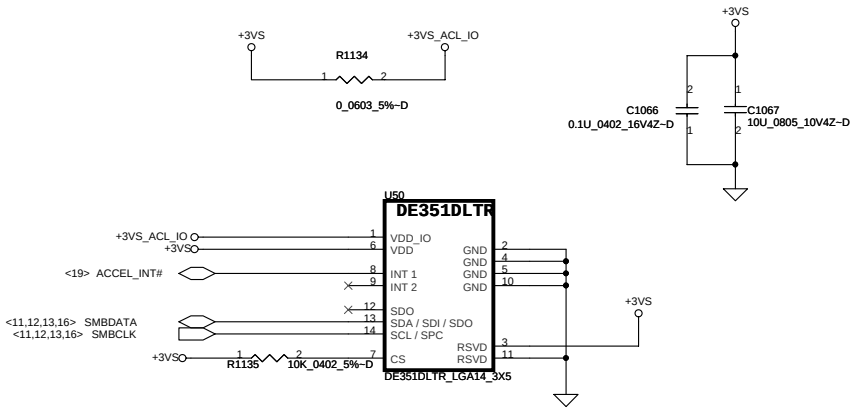
FAN Control circuit



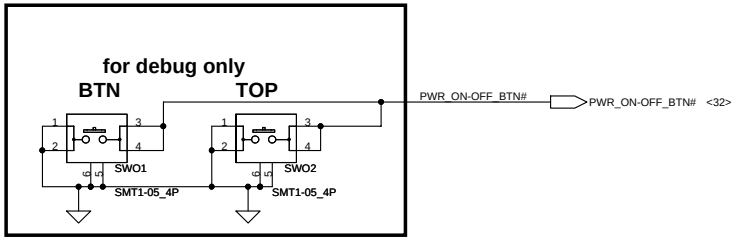
Free Fall Sensor



Must be placed in the center of the system.

P/N : SA000039C00 (S IC DE351DLTR LGA 14P MOTION SENSOR)

Power Button



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+RTCVCC R46 20K_0402_1%~D PCH_RTCRST# RC Delay 18~25mS close to RAM door CMOS1 @ C15 1U_0603_10V6K~D

+RTCVCC R36 20K_0402_1%~D PCH_SRTCRST# RC Delay 18~25mS close to RAM door ME1 @ C13 1U_0603_10V6K~D

C398 18P_0402_50V8J~D PCH_RTCX1 X2 NC OSC NC OSC 32.768KHZ_12.5PF_Q13MC14610002 R1100 10M_0402_5%~D C402 18P_0402_50V8J~D PCH_RTCX2

U47A REV1.0

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14

+RTCVCC R64 1M_0402_5%~D SM_INTRUDER# R51 330K_0402_5%~D PCH_INTVRMEN

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

LPC: FWH0 / LAD0 D33 LPC_AD0, FWH1 / LAD1 B33 LPC_AD1, FWH2 / LAD2 C32 LPC_AD2, FWH3 / LAD3 A32 LPC_AD3, FWH4 / LFRAME# C34 LPC_FRAME#, LDRQ0# A34, LDRQ1# / GPIO23 E34, SERIRQ AB9 SERIRQ

IHDA: HDA_BITCLK_PCH A30, HDA_SYNC_PCH D29, PCH_SPKR P1, PCH_RST_PCH# C30, HDA_SDIN0 G30, HDA_SDIN1 E30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDOUT_PCH B29

HDA for AUDIO
<25> HDA_BITCLK_AUDIO R1083 33_0402_5%~D HDA_BITCLK_PCH
<25> HDA_SYNC_AUDIO R1084 33_0402_5%~D HDA_SYNC_PCH
<25> HDA_RST_AUDIO# R1085 33_0402_5%~D HDA_RST_PCH#
<25> HDA_SDOUT_AUDIO R1086 33_0402_5%~D HDA_SDOUT_PCH

<31,32> TOUCHKEY_TINT R1024 0_0402_5%~D R1232 @ 1K_0402_5%~D H32 HDA_DOCK_EN# / GPIO33, J30 HDA_DOCK_RST# / GPIO13

GPIO33 pull down only for ME disable

SATA: SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9; SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8; SATA2RXN AE11, SATA2RXP AF9, SATA2TXN AE7, SATA2TXP AF6; SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AE3, SATA3TXP AE1; SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5; SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1

SATA_ITX_DRX_N0 0.01U_0402_16V7K~D C961 SATA_ITX_DRX_P0 0.01U_0402_16V7K~D C962
SATA_IRX_DTX_N0 <29> SATA_IRX_DTX_P0 <29> SATA_ITX_C_DRX_N0 <29> SATA_ITX_C_DRX_P0 <29>
SATA for HDD1

SATA_ITX_DRX_N1 C963 0.01U_0402_16V7K~D SATA_ITX_DRX_P1 C964 0.01U_0402_16V7K~D
SATA_IRX_DTX_N1 <29> SATA_IRX_DTX_P1 <29> SATA_ITX_C_DRX_N1 <29> SATA_ITX_C_DRX_P1 <29>
SATA for HDD2
R0.3 depop

From PCH EDS 5.16, SATA port2 & 3 are not available in all sku.

SATA_ITX_DRX_N4 C965 0.01U_0402_16V7K~D SATA_ITX_DRX_P4 C966 0.01U_0402_16V7K~D
SATA_IRX_DTX_N4 <29> SATA_IRX_DTX_P4 <29> SATA_ITX_C_DRX_N4 <29> SATA_ITX_C_DRX_P4 <29>
SATA for ODD
R0.3 depop

SATA_ITX_DRX_N5 C967 0.01U_0402_16V7K~D SATA_ITX_DRX_P5 C968 0.01U_0402_16V7K~D
SATA_IRX_DTX_N5 <30> SATA_IRX_DTX_P5 <30> SATA_ITX_C_DRX_N5 <30> SATA_ITX_C_DRX_P5 <30>
SATA for eSATA

SATAICOMPO AF16, SATAICOMPI AF15 SATA_COMP R139 37.4_0402_1%~OK +1.05VS

HDA_BITCLK_AUDIO C1110 @ 10P_0402_50V8J~D

JTAG: <23> PCH_JTAG_TCK M3, <23> PCH_JTAG_TMS K3, <23> PCH_JTAG_TDI K1, <23> PCH_JTAG_TDO J2, <23> PCH_JTAG_RST# J4

SPI: PCH_SPI_CLK_1 R584 0_0402_5%~D PCH_SPI_CLK BA2, PCH_SPI_CS0# R571 15_0402_5%~D PCH_SPI_CS0#_R AV3, SPI_CS1# AY3, PCH_SPI_MOSI_1 R575 15_0402_5%~D PCH_SPI_MOSI AY1, PCH_SPI_MISO_1 R565 33_0402_5%~D PCH_SPI_MISO AV1

SATALED# T3 PCH_SATALED# R129 10K_0402_5%~D +3VS
SATA0GP / GPIO21 Y9, SATA1GP / GPIO19 V1

R77 @ 10K_0402_5%~D +3VS
R116 @ 10K_0402_5%~D

PCH_GPIO21 <23>
PCH_GPIO19 <23>
R111 10K_0402_5%~D
R82 10K_0402_5%~D

IBEXPEAK-M_FCBGA1071~D

+3VS R1120 1K_0402_5%~D PCH_SPKR SERIRQ R115 10K_0402_5%~D

+3V +1.05VS

R1130 @ 51_0402_1%~D
R1101 200_0402_5%~D
PCH_JTAG_TMS R1102 100_0402_1%~D
R1131 @ 51_0402_1%~D
R1104 200_0402_5%~D
PCH_JTAG_TDO R1105 100_0402_1%~D
R1132 @ 51_0402_1%~D
R1106 200_0402_5%~D
PCH_JTAG_TDI R1107 100_0402_1%~D
R1133 @ 51_0402_1%~D
R1108 20K_0402_1%~D
PCH_JTAG_RST# R1109 10K_0402_5%~D

2008 Intel MOW36/MOW50

TDO:
Reserved on ES1 Sample
Mount R1104, R1105 on ES2 Sample

MP mount R1130, R1131, R1132, R1133 and remove others

+3VS R1110 3.3K_0402_5%~D PCH_SPI_CS0# PCH_SPI_MISO_1 SPI_WP1# U29 CS# SO WP# GND VCC HOLD# SCLK SI SPI_HOLD1# 3.3K_0402_5%~D R1122 +3VS PCH_SPI_CLK_1 PCH_SPI_MOSI_1
MX25L1605AM2C-12G_SO8

SPI Flash (16Mbit/2Mbyte)

+3VS PCH_SPI_MOSI R173 @ 1K_0402_5%~D enable iTPM: SPI_MOSI High

PCH_JTAG_TCK R1111 4.7K_0402_5%~D CRB 1.0 Change to 4.7K

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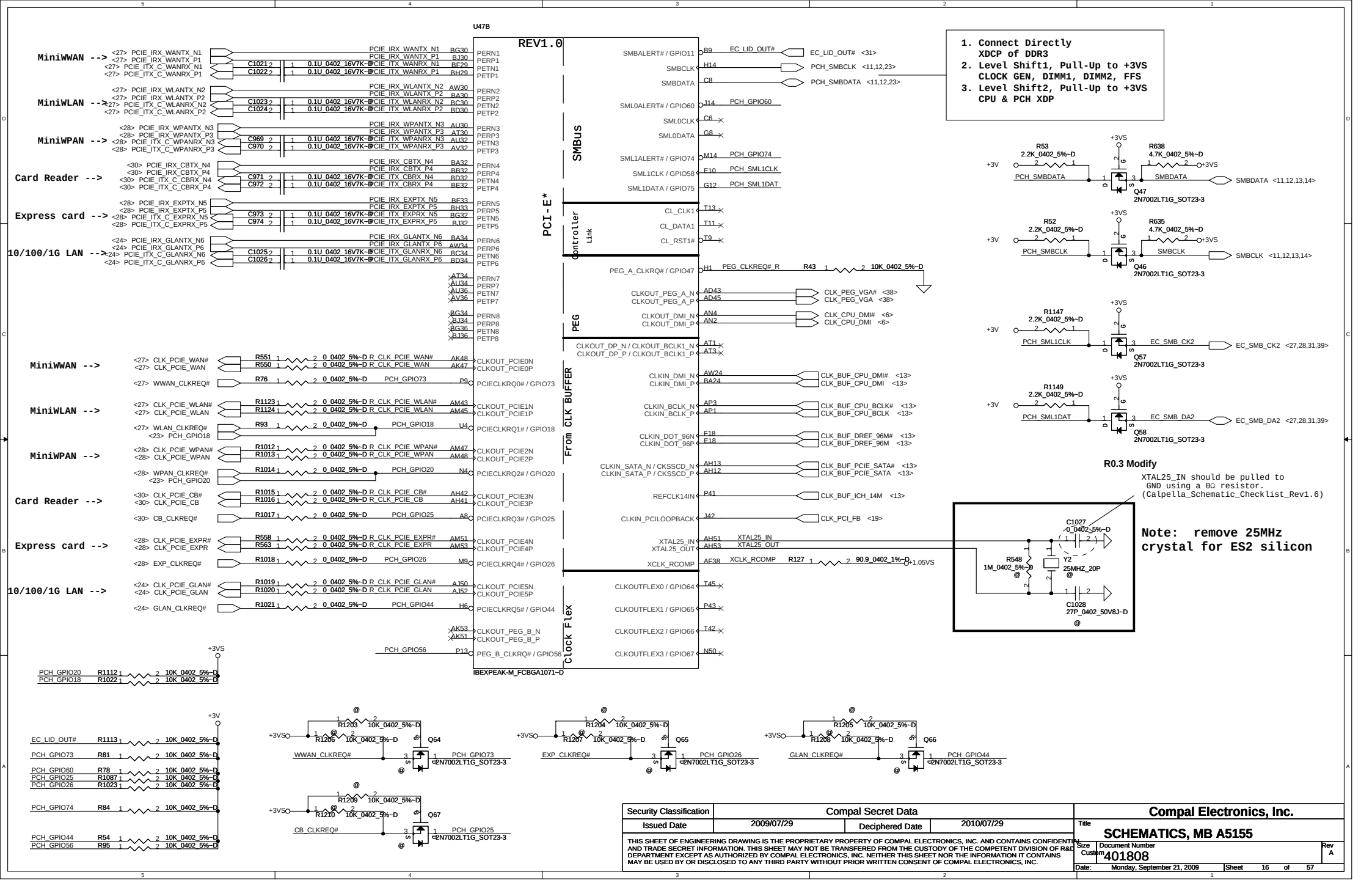

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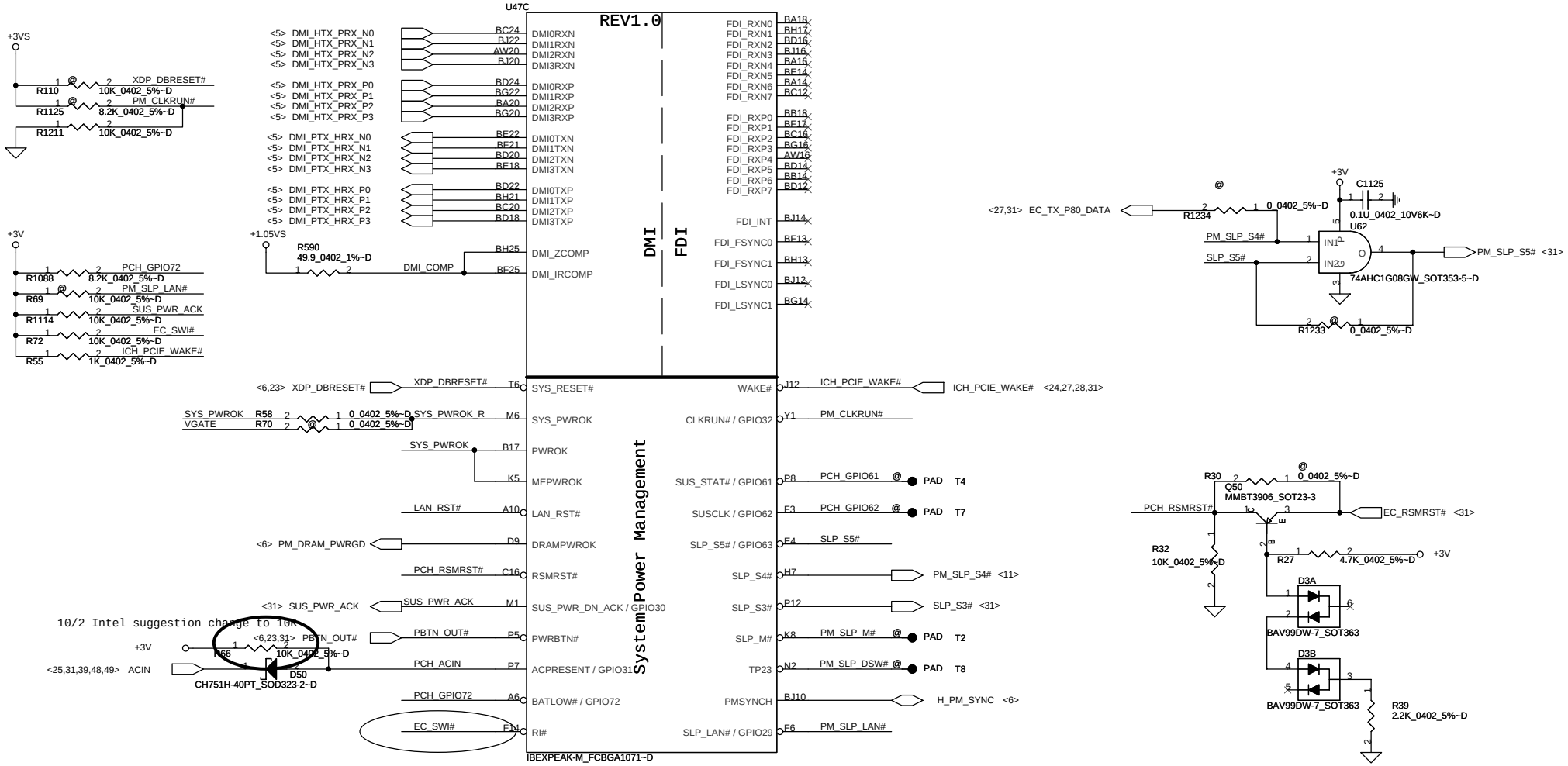

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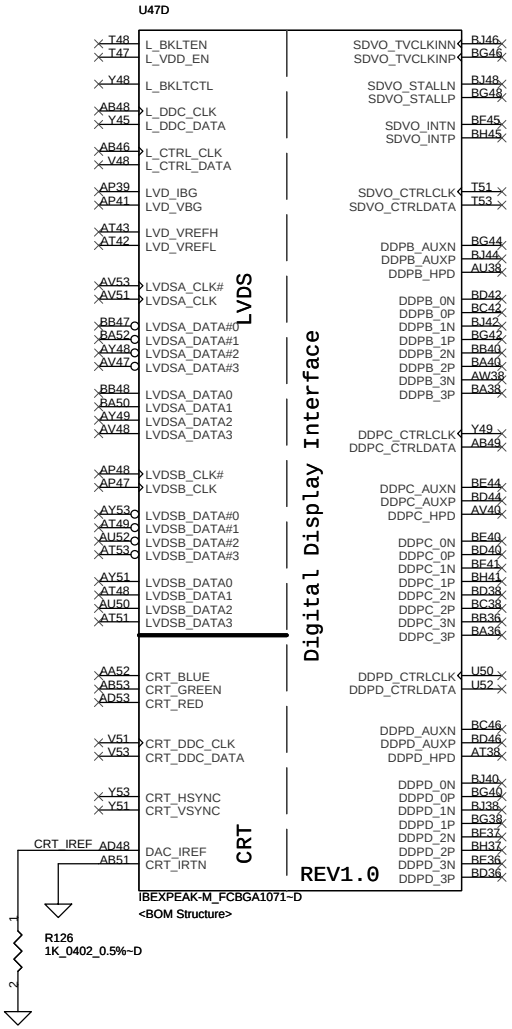

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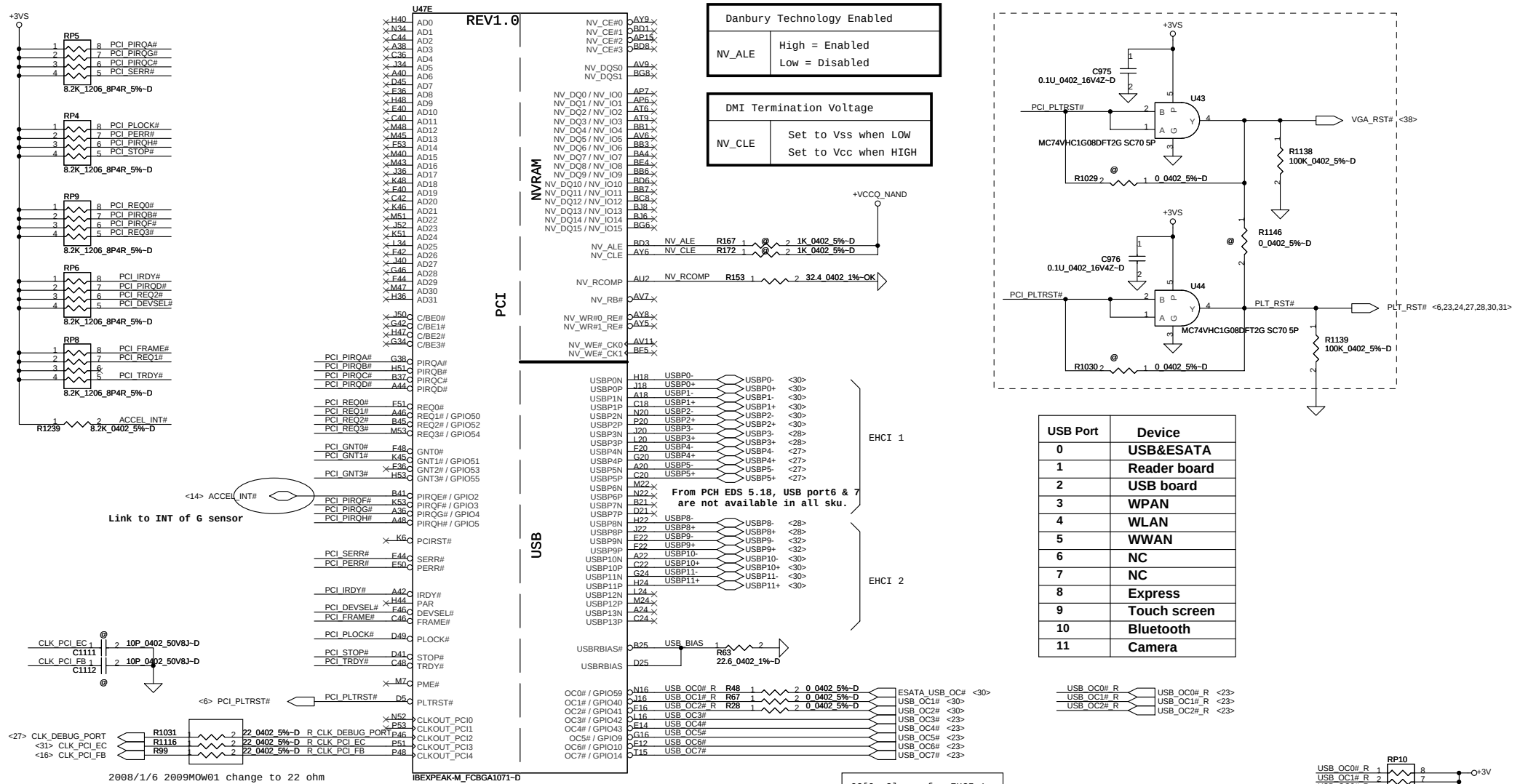

USB Port	Device
0	USB&ESATA
1	Reader board
2	USB board
3	WPAN
4	WLAN
5	WWAN
6	NC
7	NC
8	Express
9	Touch screen
10	Bluetooth
11	Camera

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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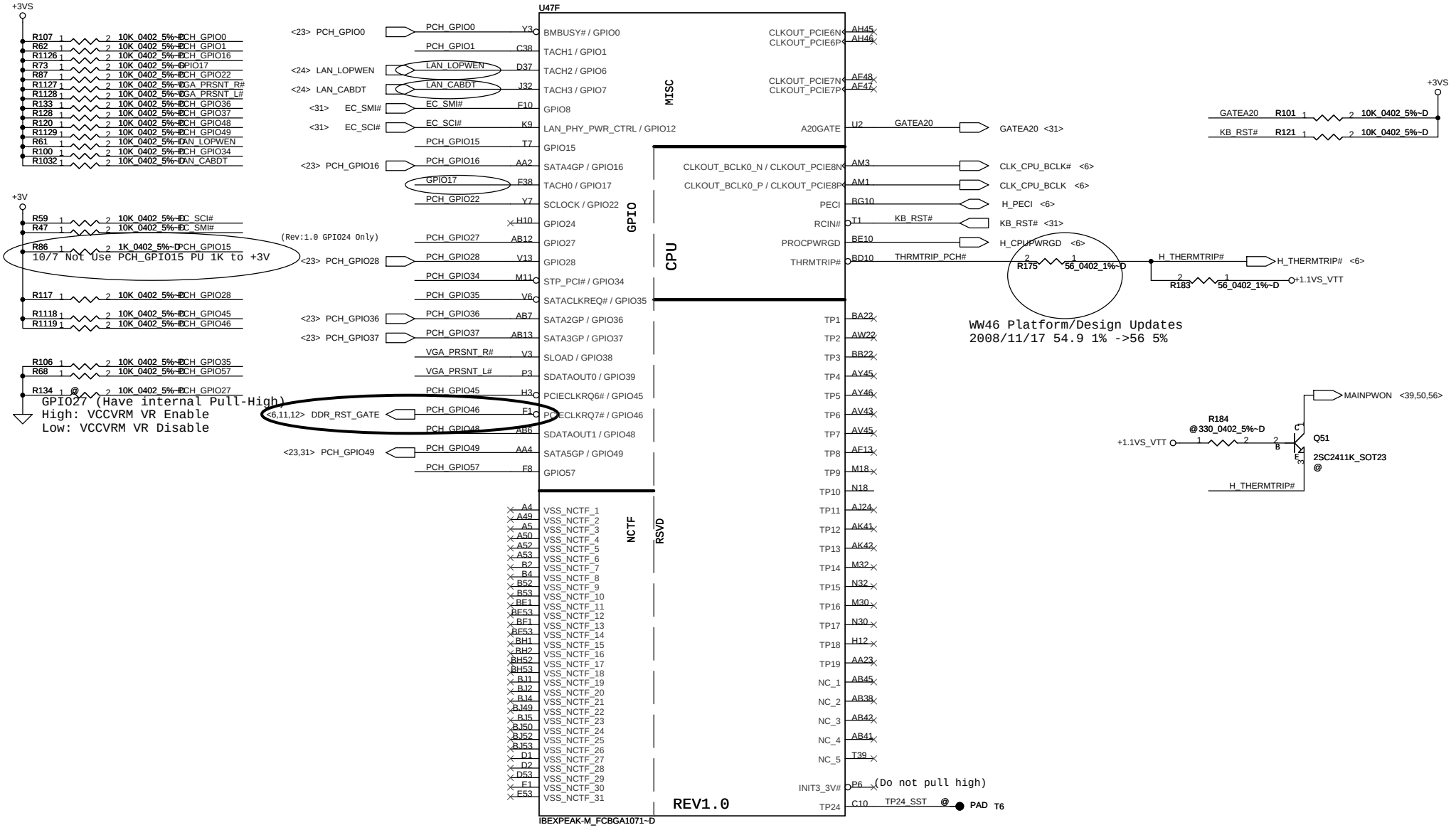

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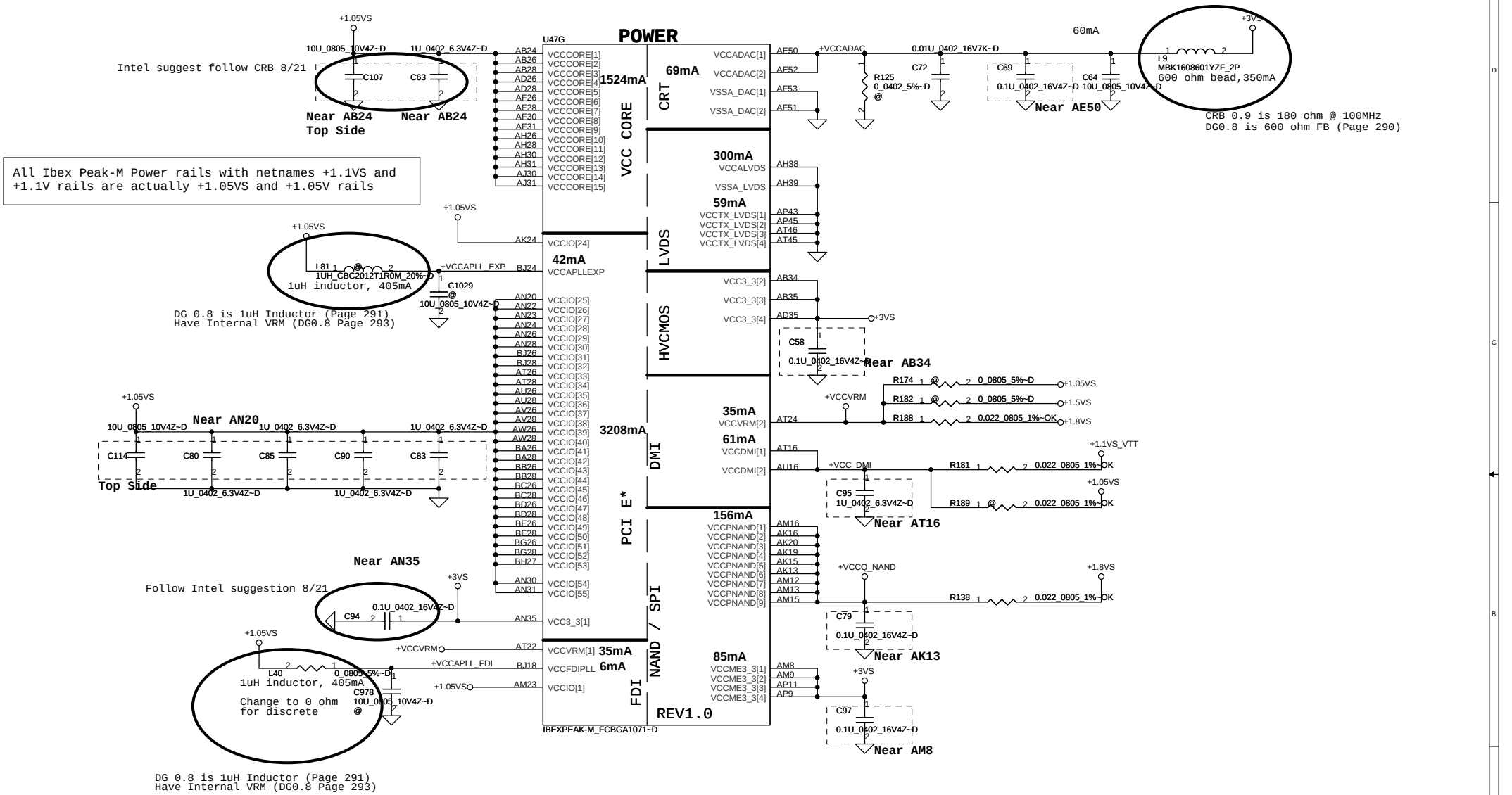

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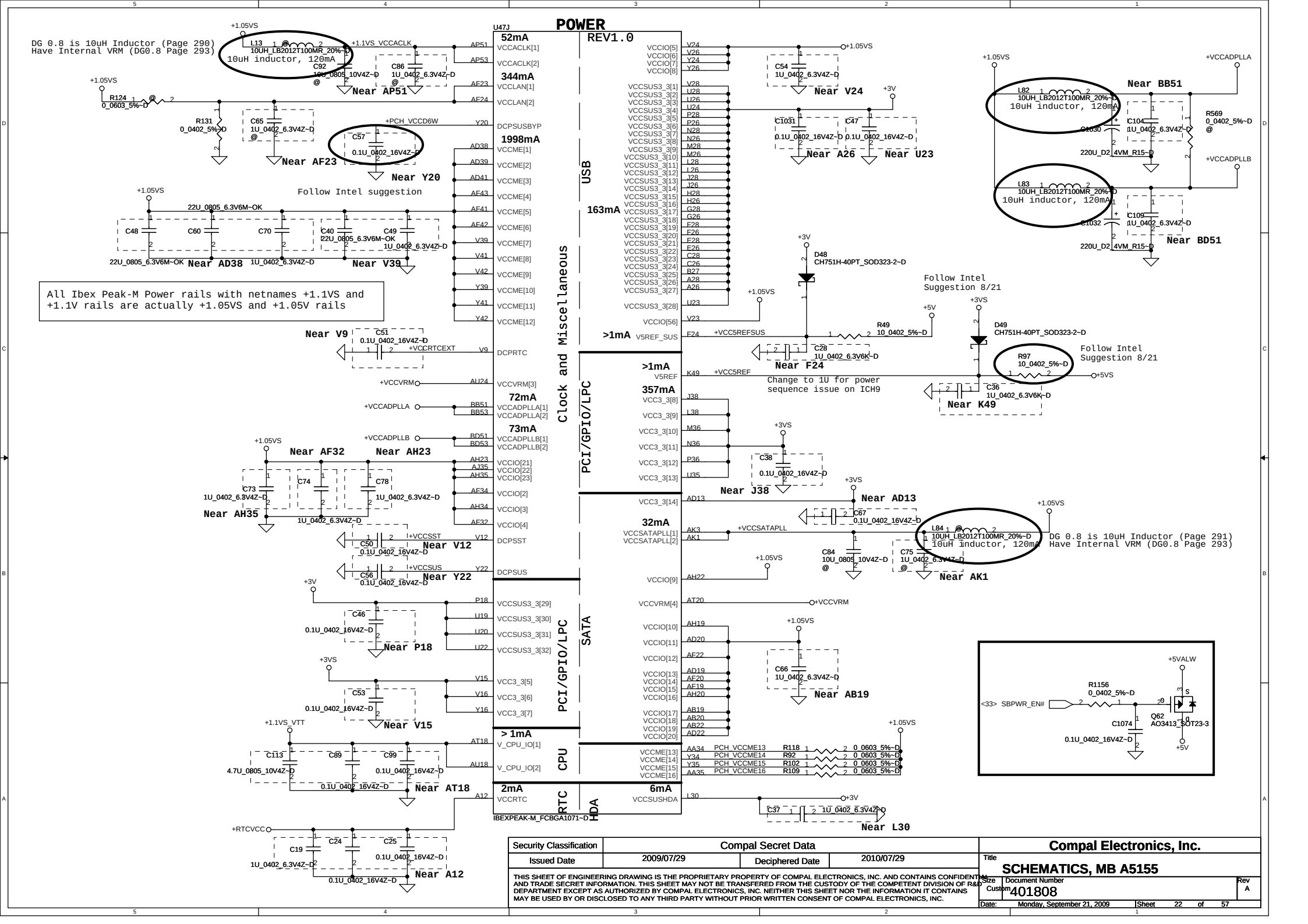

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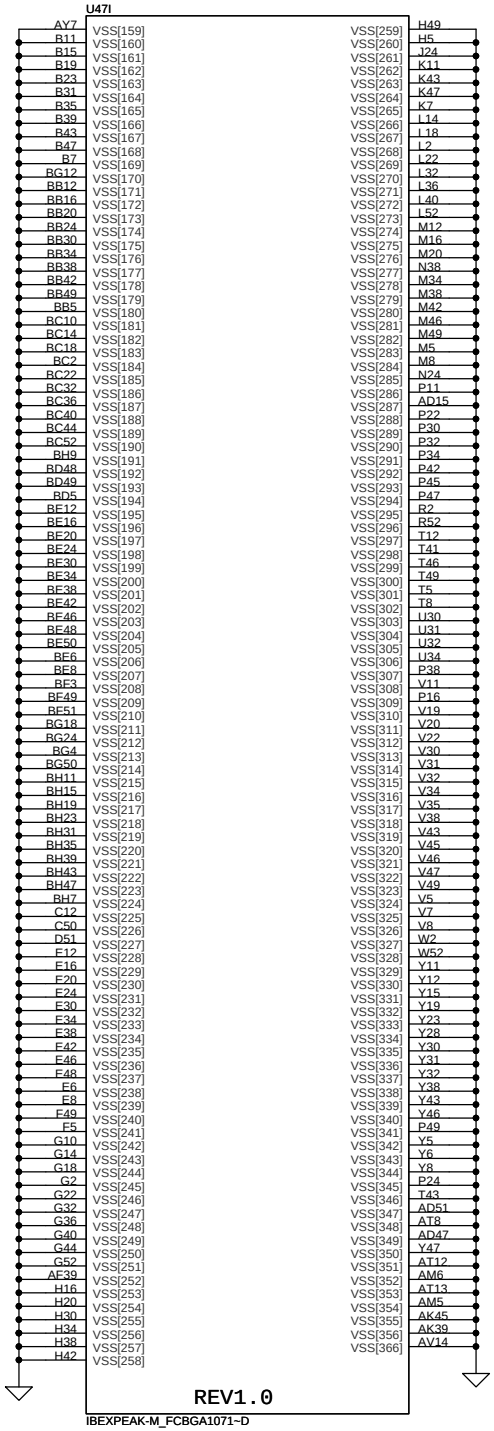
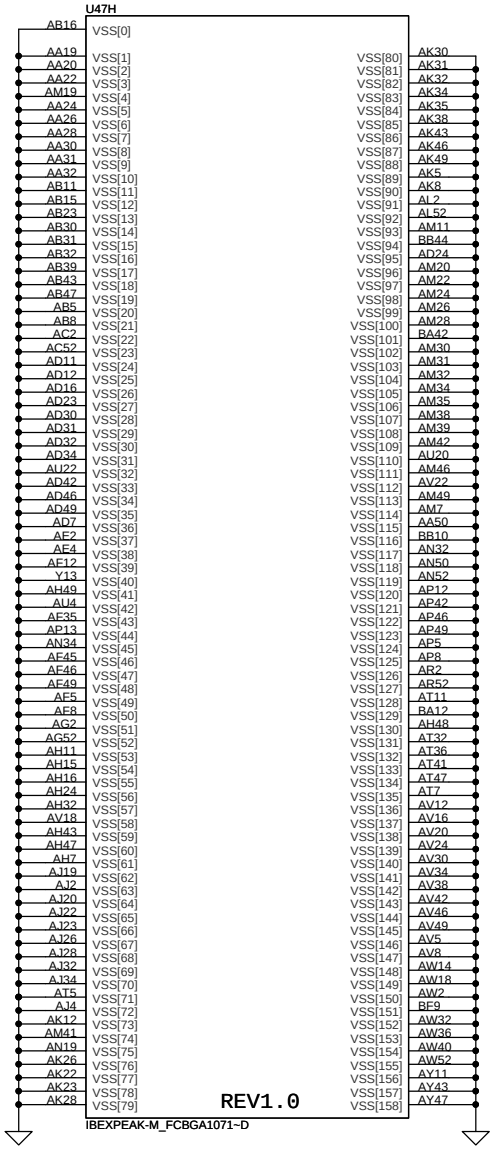
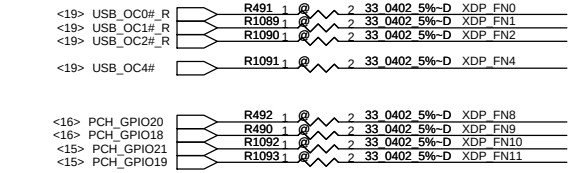
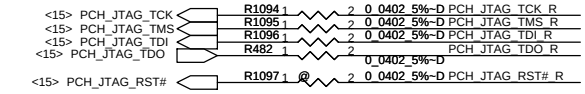
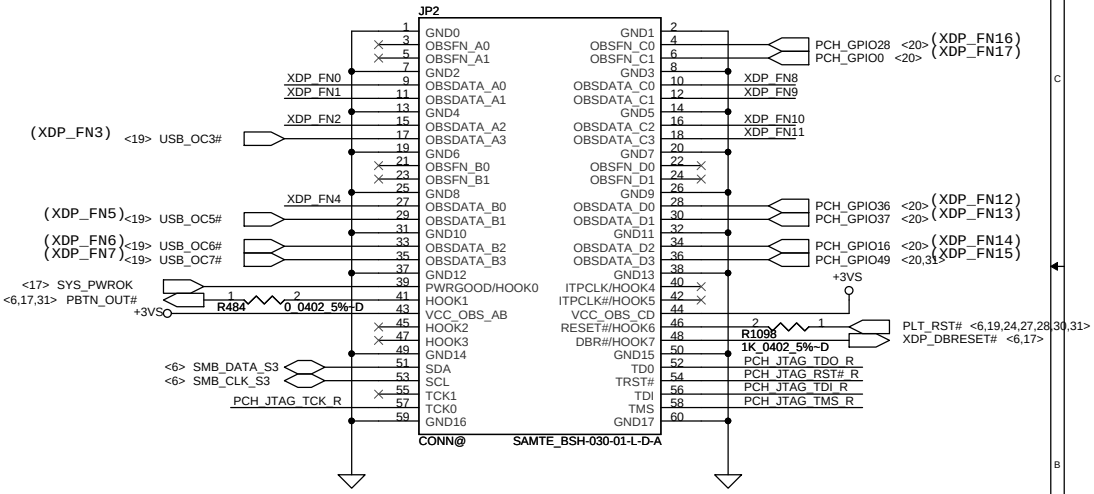
PCH XDP Port

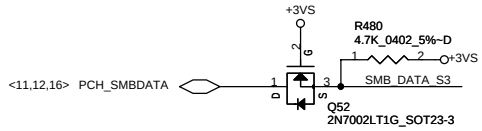












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LEDS1-0	0 0	0 1	1 0	1 1
LED0	Tx / Rx	Tx / Rx	Tx	LINK10 / ACT
LED1	LINK100	LINK10 /100 / 1000	LINK	LINK100 / ACT
LED2	LINK10	LINK10 / 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 / ACT

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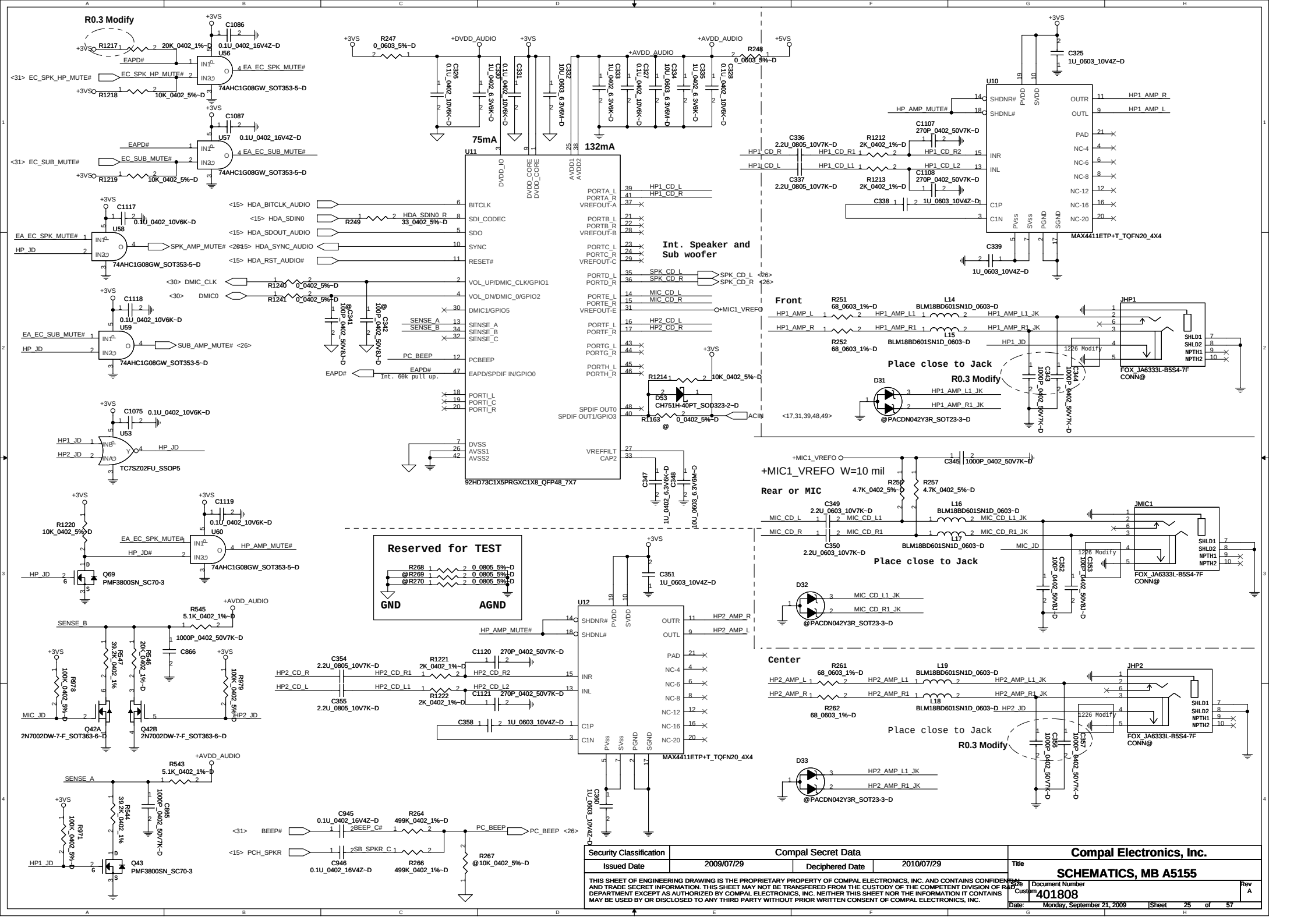

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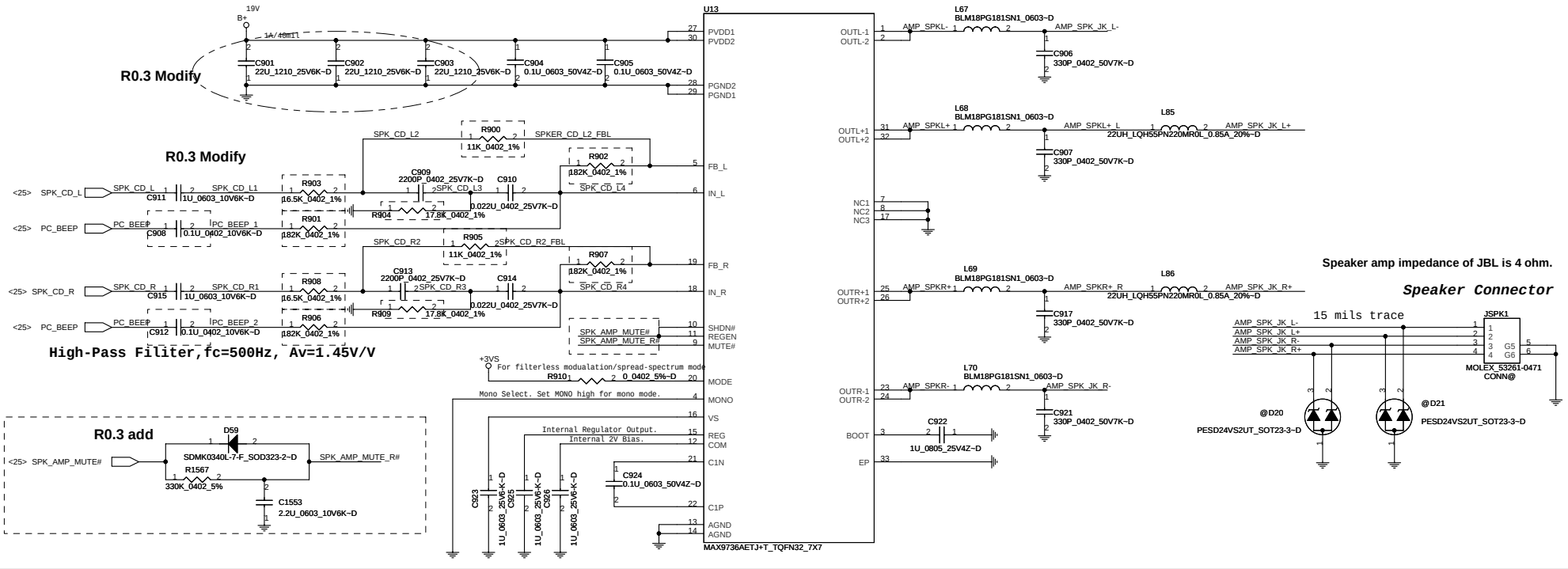

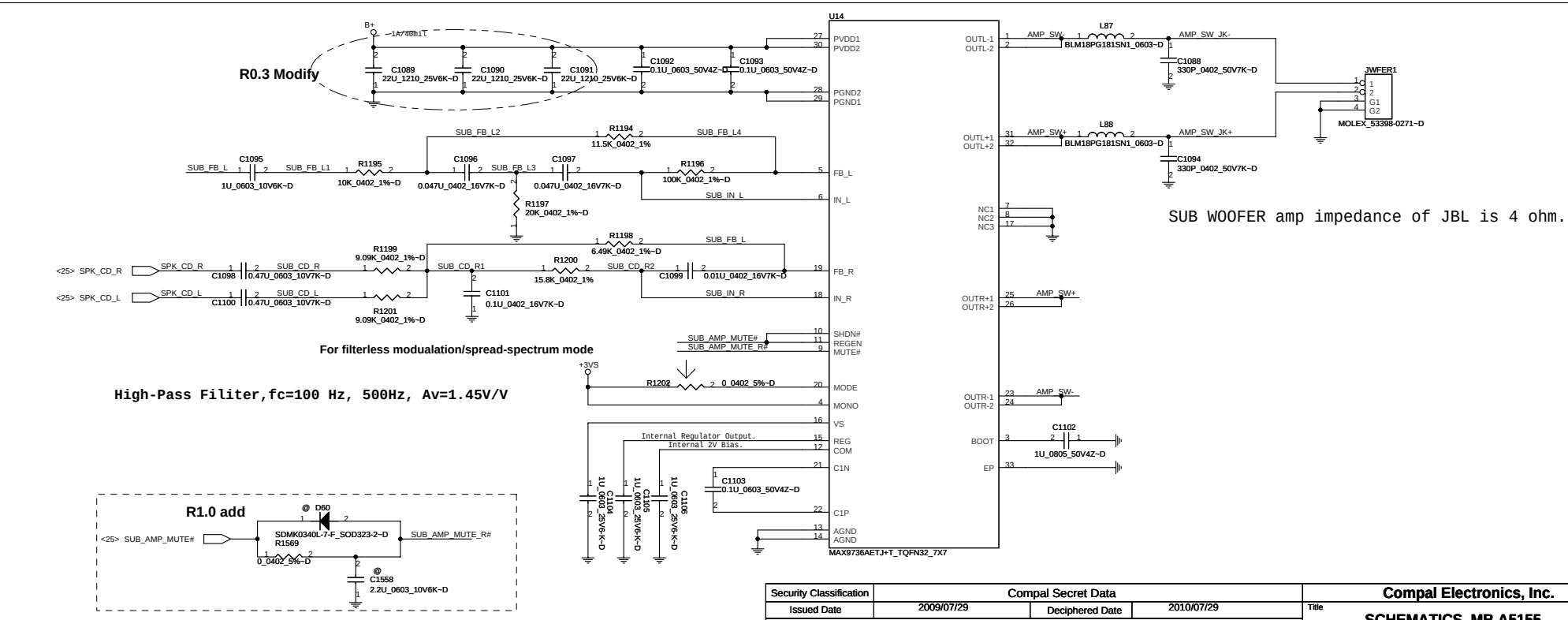

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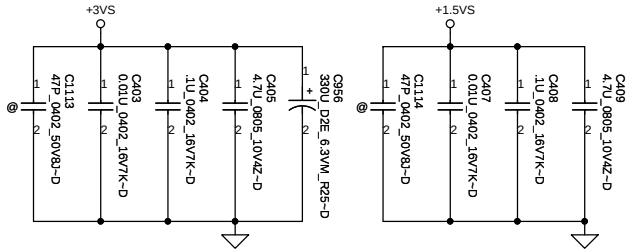
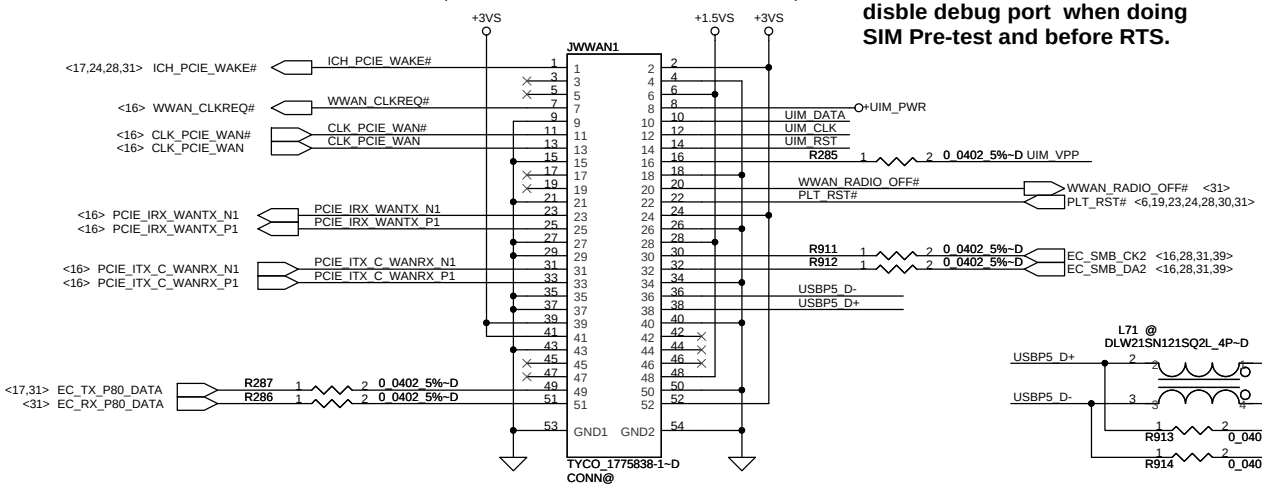
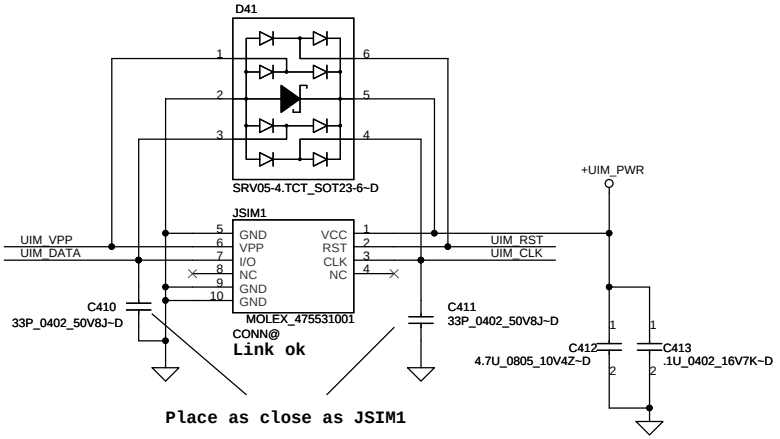
WWAN

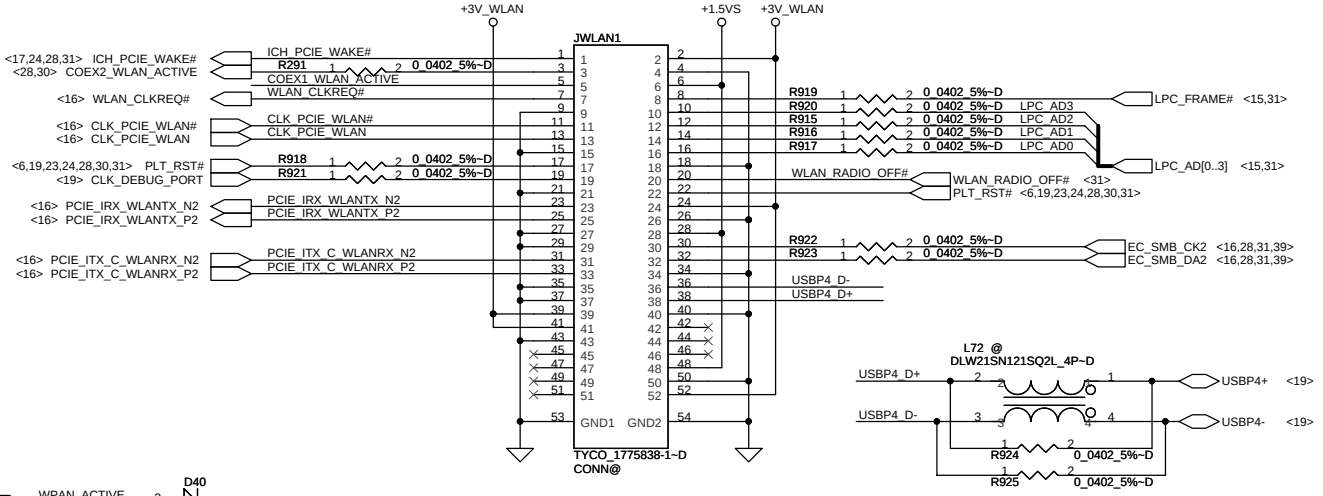


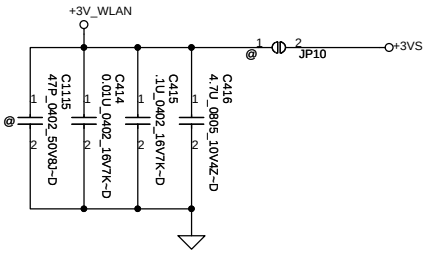
Don't forget to remove R287 or disble debug port when doing SIM Pre-test and before RTS.

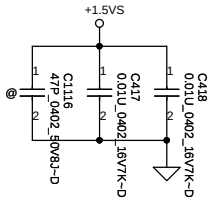


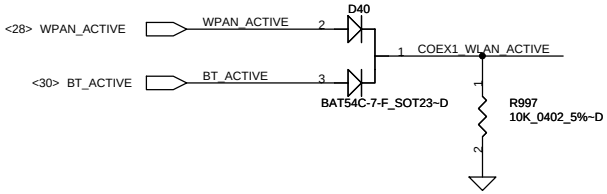


WLAN









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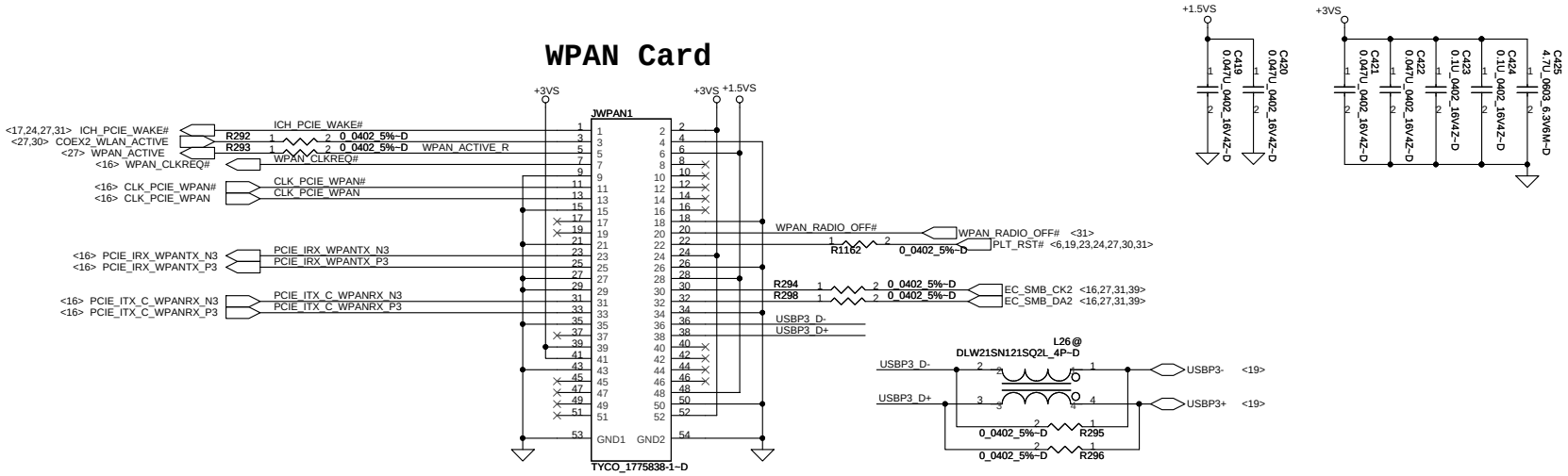
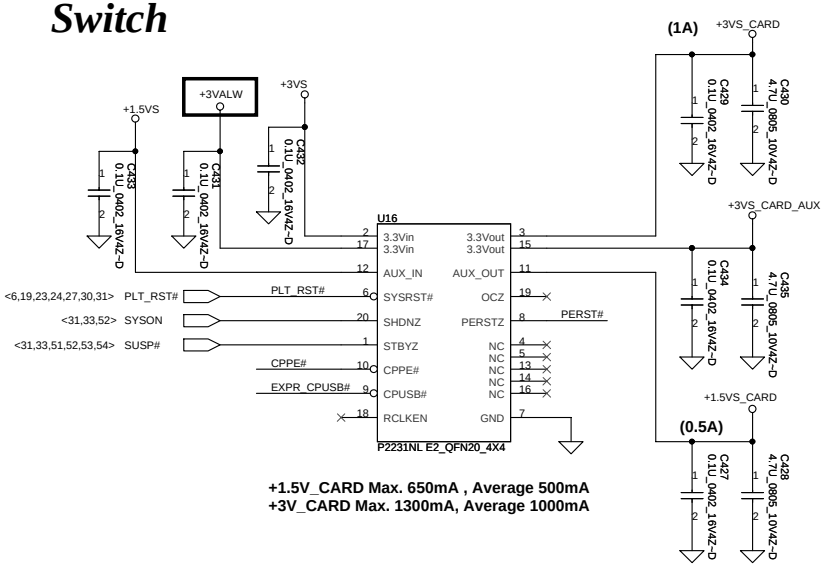
WPAN Card

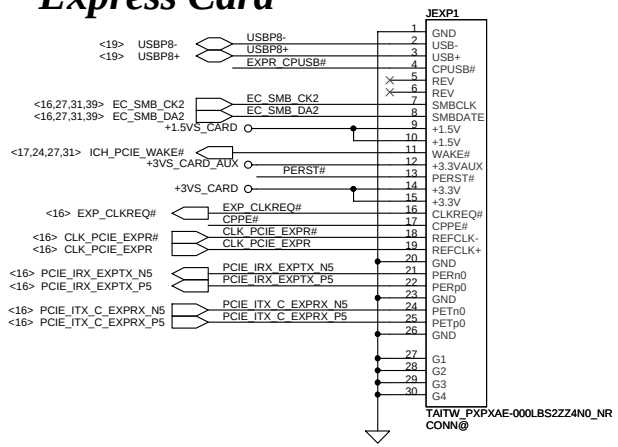


Express Card Power Switch



+1.5V_CARD Max. 650mA , Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

Express Card



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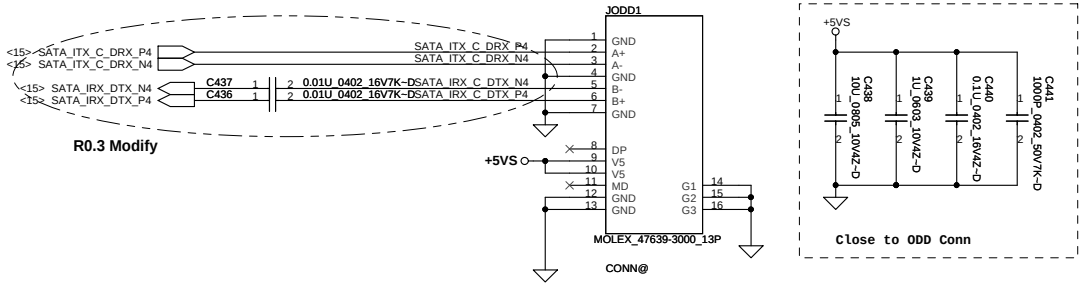
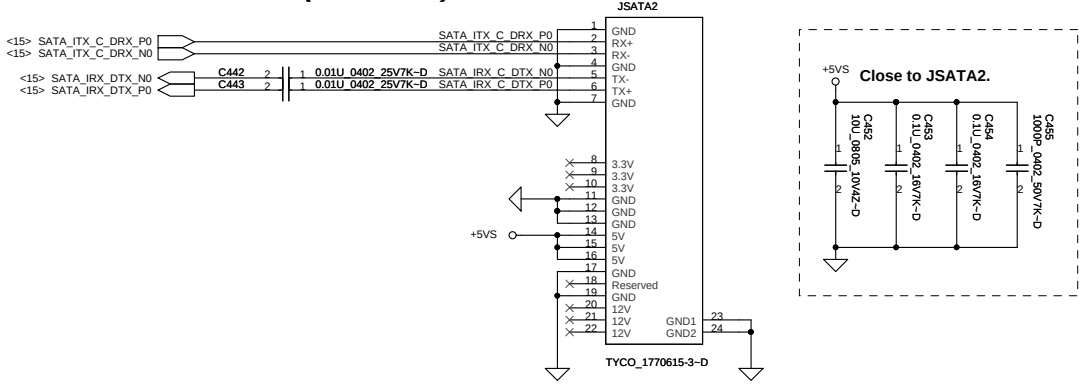
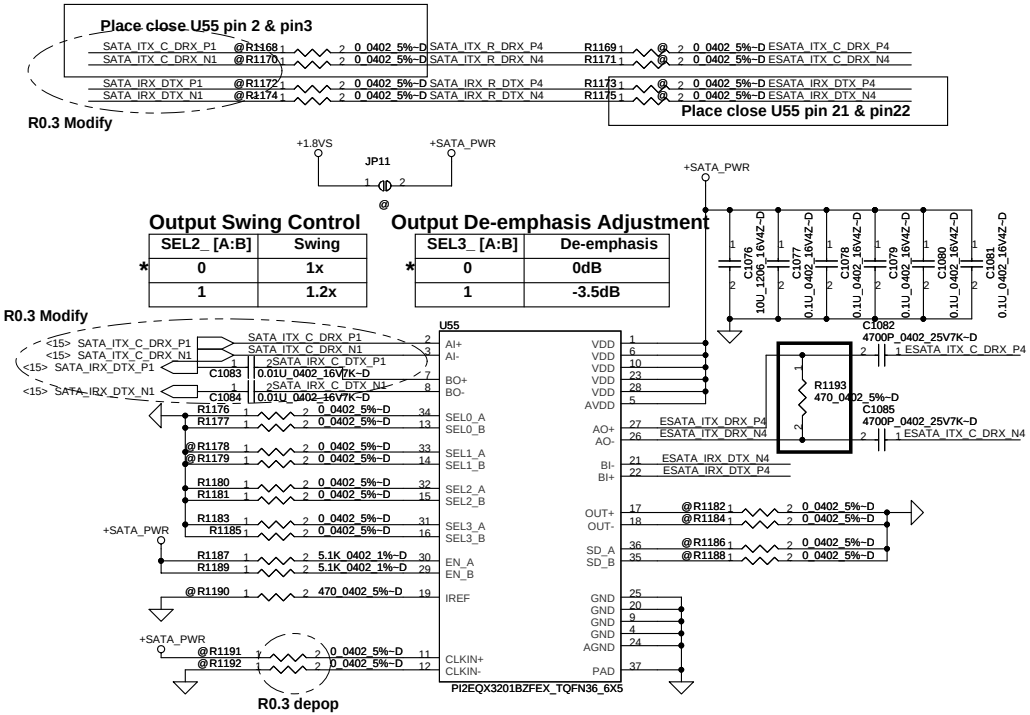
SATA ODD CONN



SATA HDD (On board)





R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

Output Swing Control

	SEL2_ [A:B]	Swing
*	0	1x
	1	1.2x

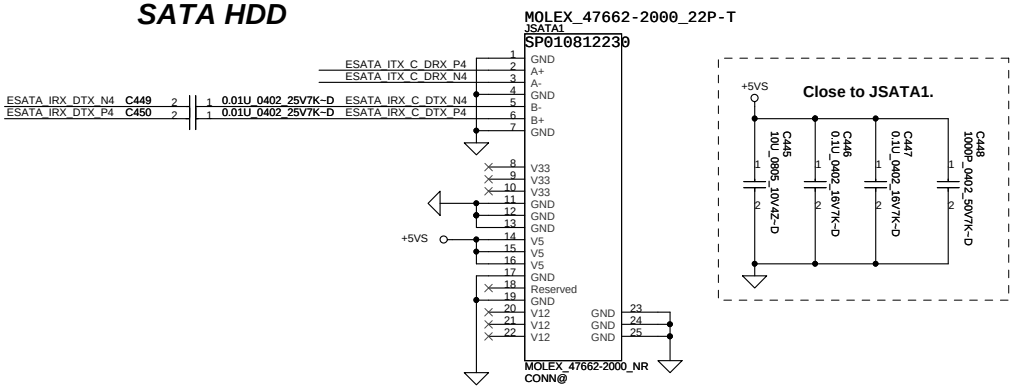
Output De-emphasis Adjustment

	SEL3_ [A:B]	De-emphasis
*	0	0dB
	1	-3.5dB

Equalizer Selection

	SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
*	0	0	no equalization
	0	1	[0:2.5dB] @ 1.6 GHz
	1	0	[2.5:4.5dB] @ 1.6 GHz
	1	1	[4.5:6.5dB] @ 1.6 GHz

SATA HDD



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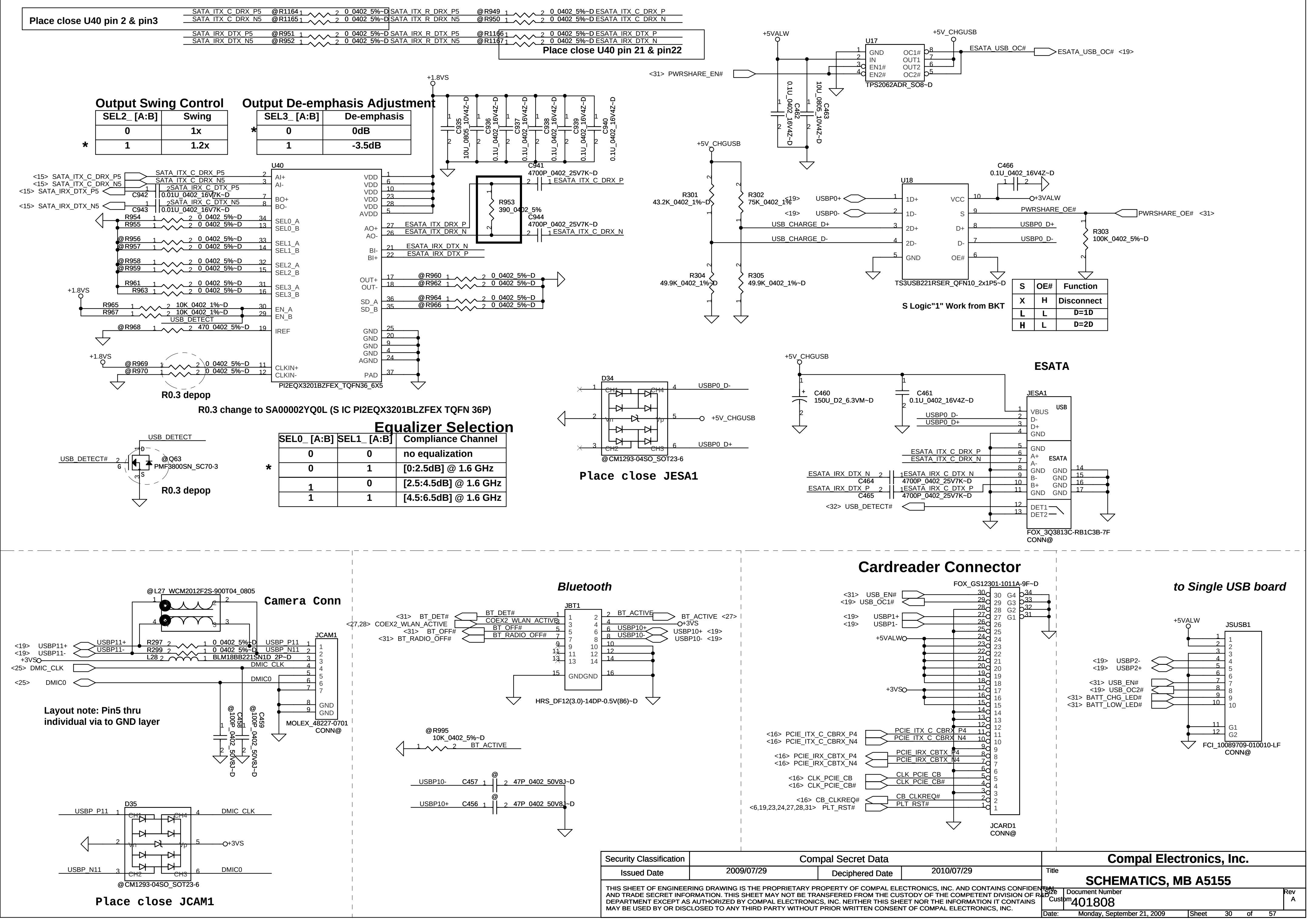

Output Swing Control

SEL2_[A:B]	Swing
0	1x
* 1	1.2x

Output De-emphasis Adjustment

SEL3_[A:B]	De-emphasis
* 0	0dB
1	-3.5dB

Equalizer Selection

SEL0_[A:B]	SEL1_[A:B]	Compliance Channel
0	0	no equalization
* 0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

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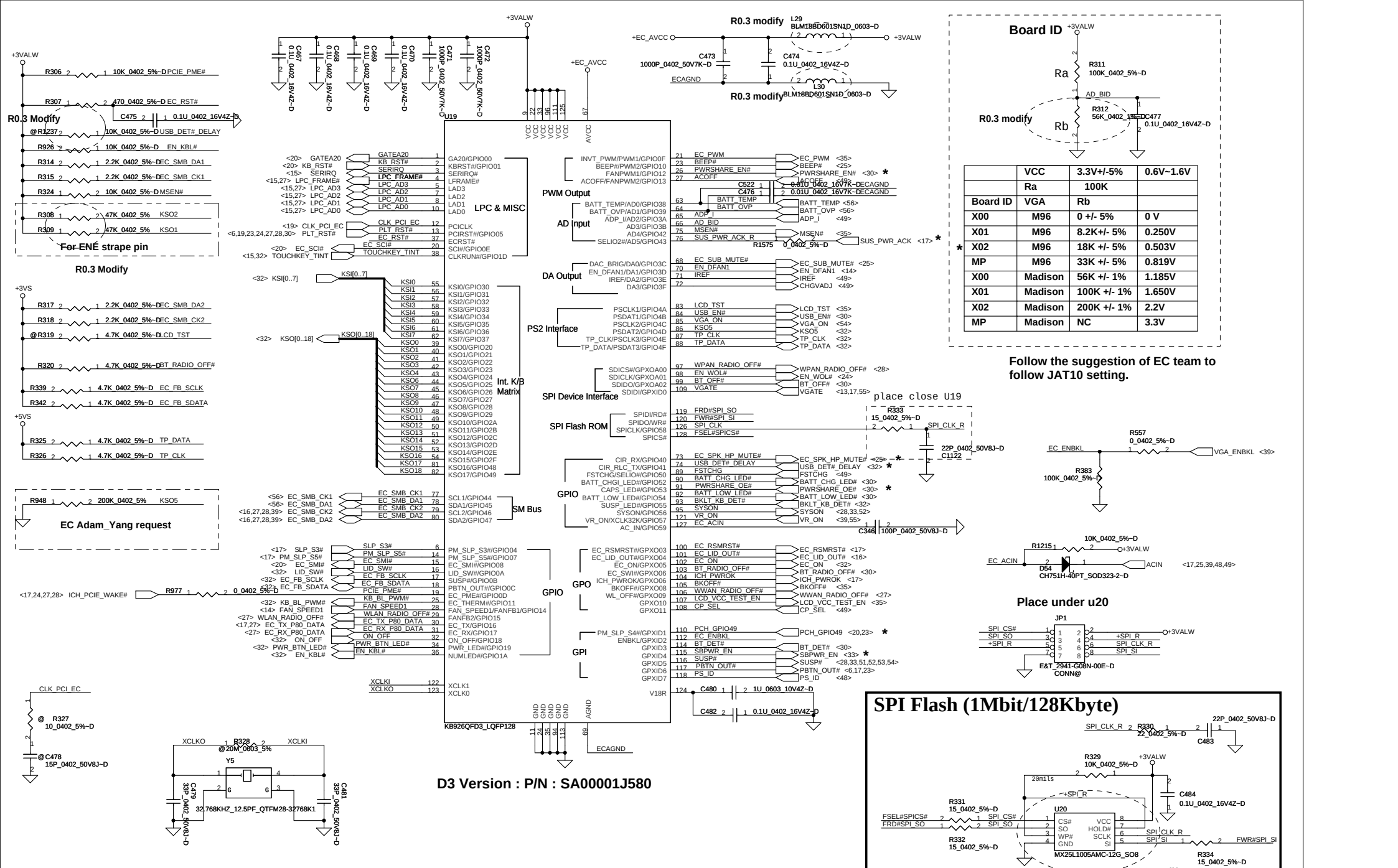

	VCC	3.3V+/-5%	0.6V~1.6V
	Ra	100K	
Board ID	VGA	Rb	
X00	M96	0 +/- 5%	0 V
X01	M96	8.2K+/- 5%	0.250V
* X02	M96	18K +/- 5%	0.503V
MP	M96	33K +/- 5%	0.819V
X00	Madison	56K +/- 1%	1.185V
X01	Madison	100K +/- 1%	1.650V
X02	Madison	200K +/- 1%	2.2V
MP	Madison	NC	3.3V

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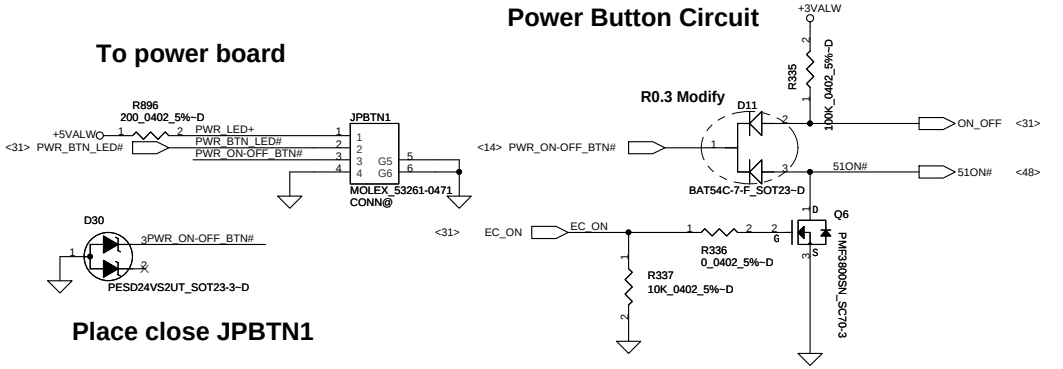
Power Button Circuit

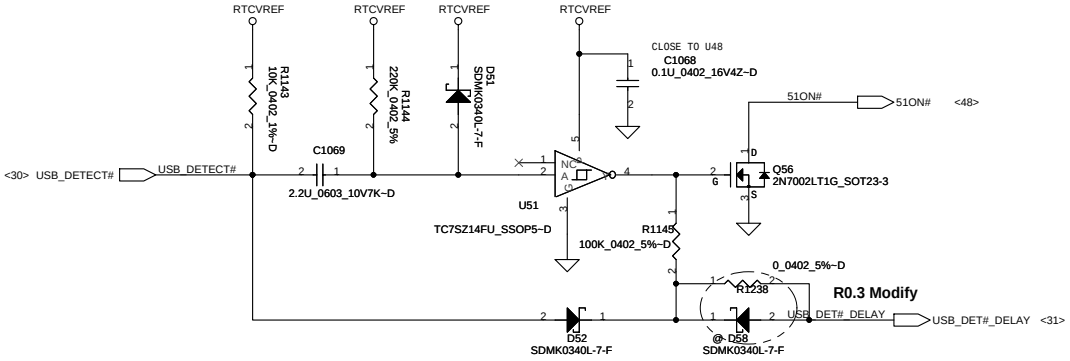
To power board



Place close JPBTN1

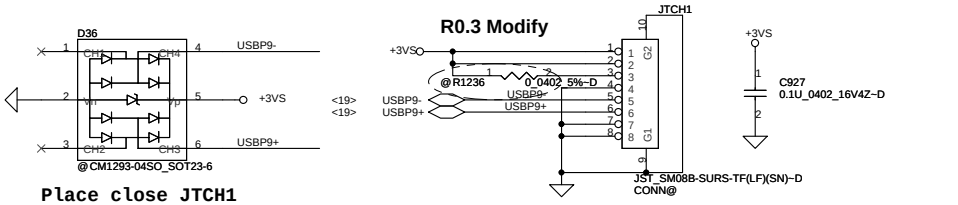
INT_KB_Conn.1

For EMI

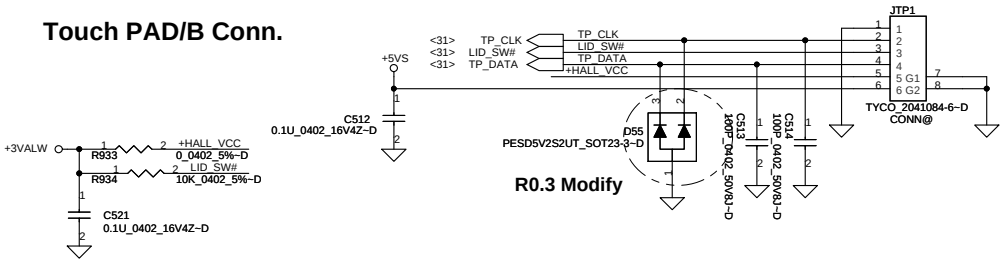


Power share

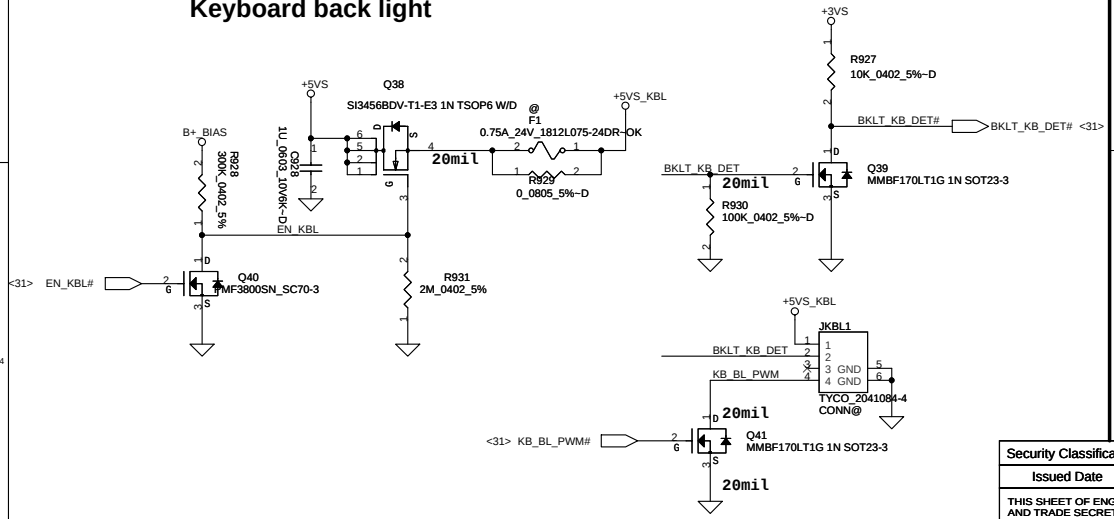
Touch Screen Connector



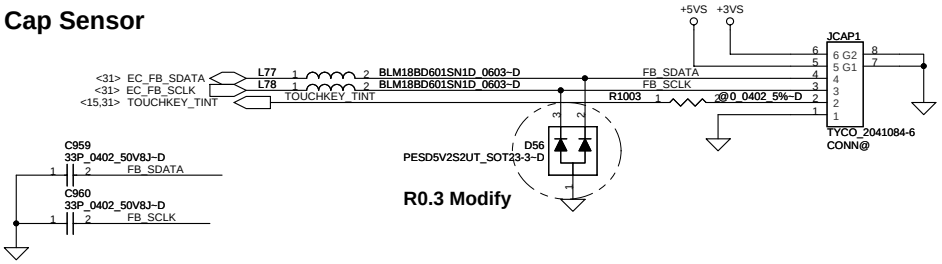
Touch PAD/B Conn.



Keyboard back light



Cap Sensor



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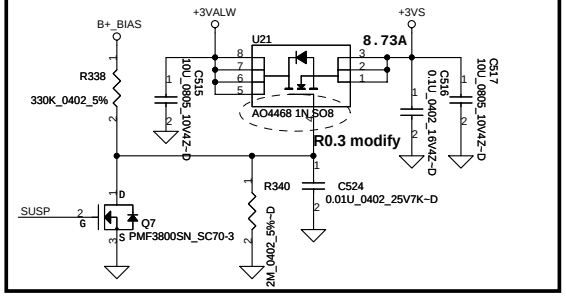
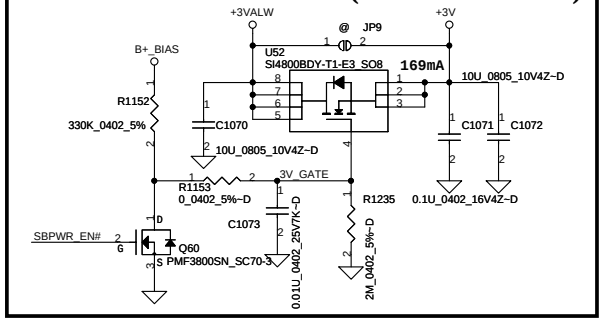
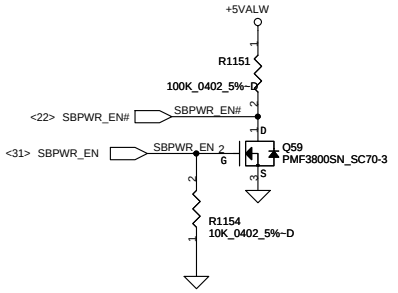
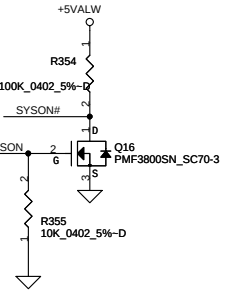
+3VALW to +3VS Transfer



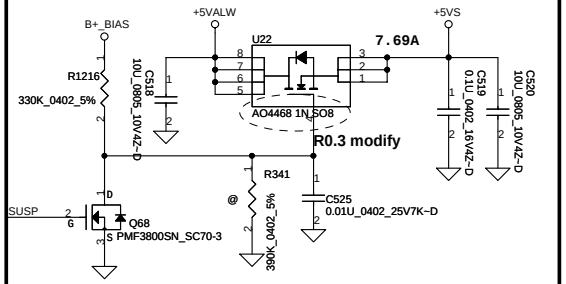
+3VALW to +3V Transfer (PCH AUX Power)

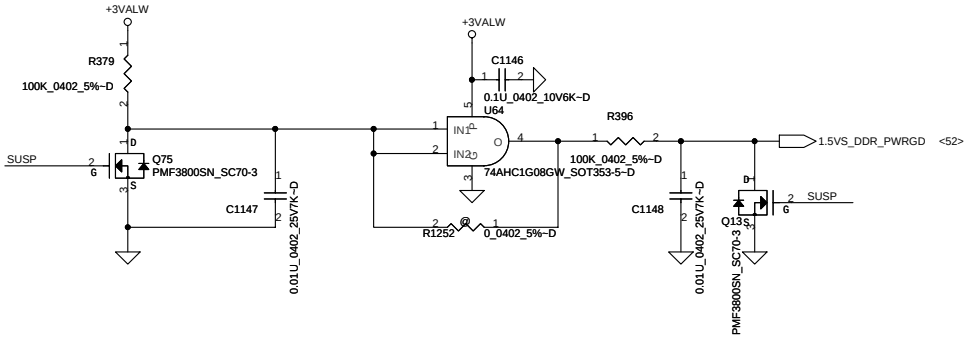


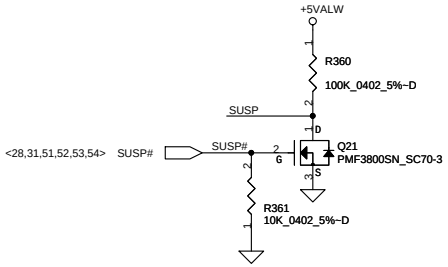




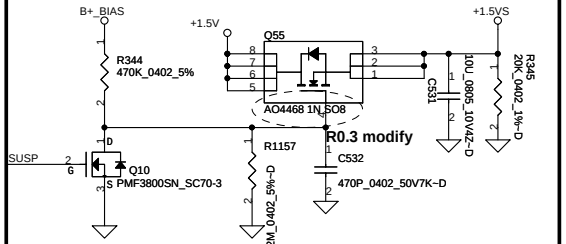
+5VALW to +5VS Transfer



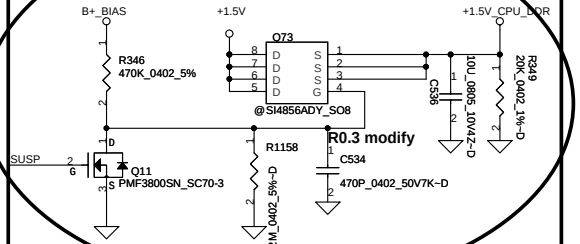




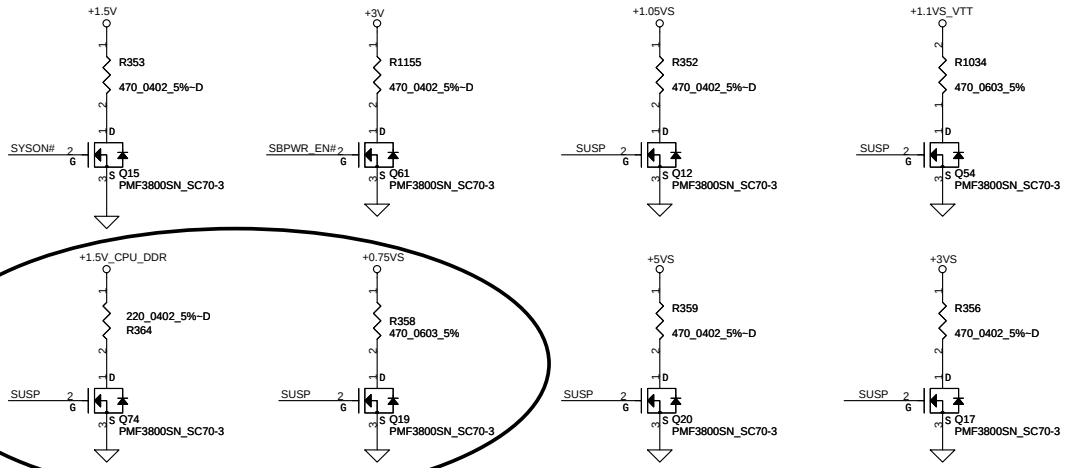
+1.5V to +1.5VS Transfer



+1.5V to +1.5VS_DDR Transfer



Discharge Circuit



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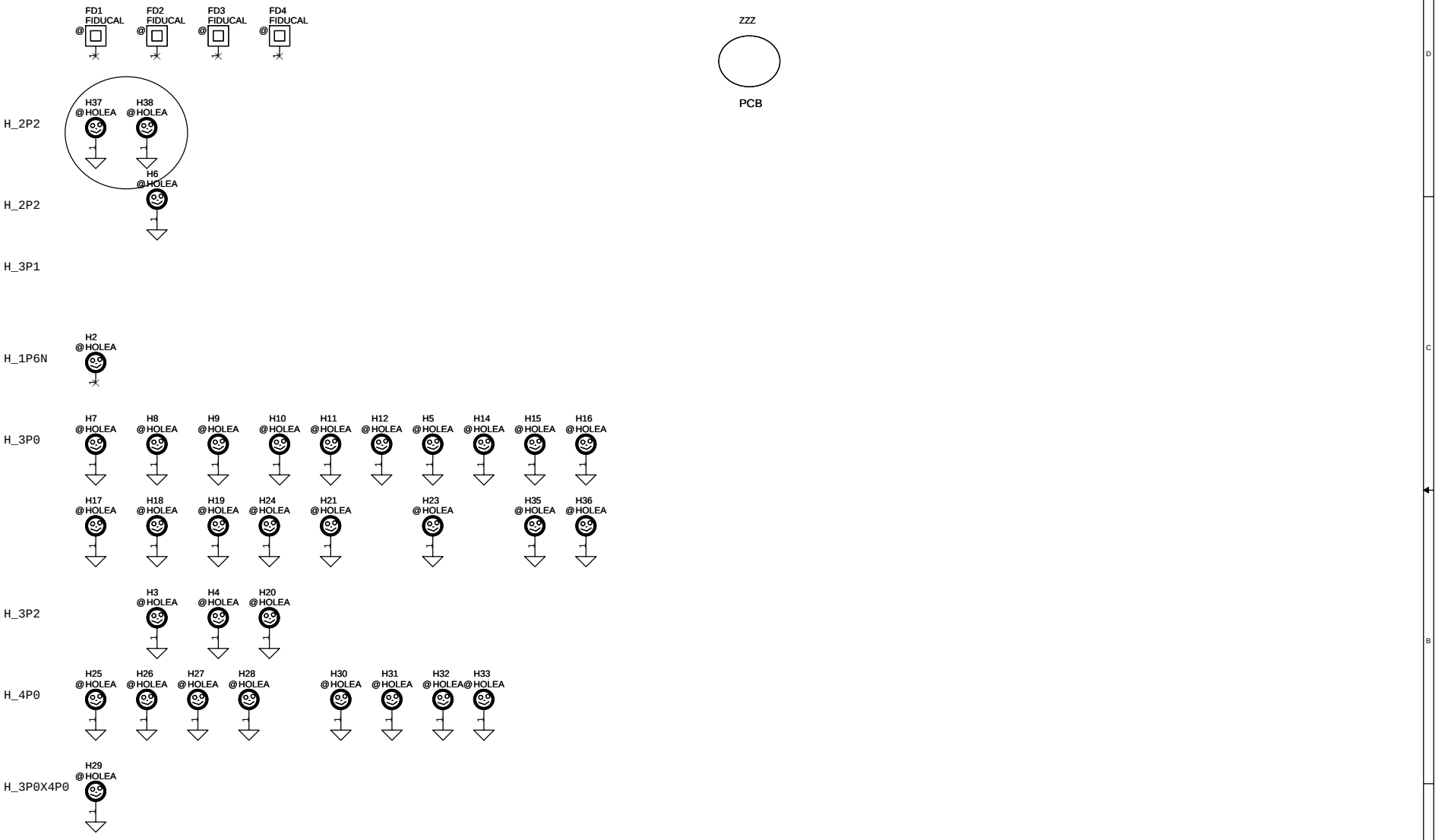

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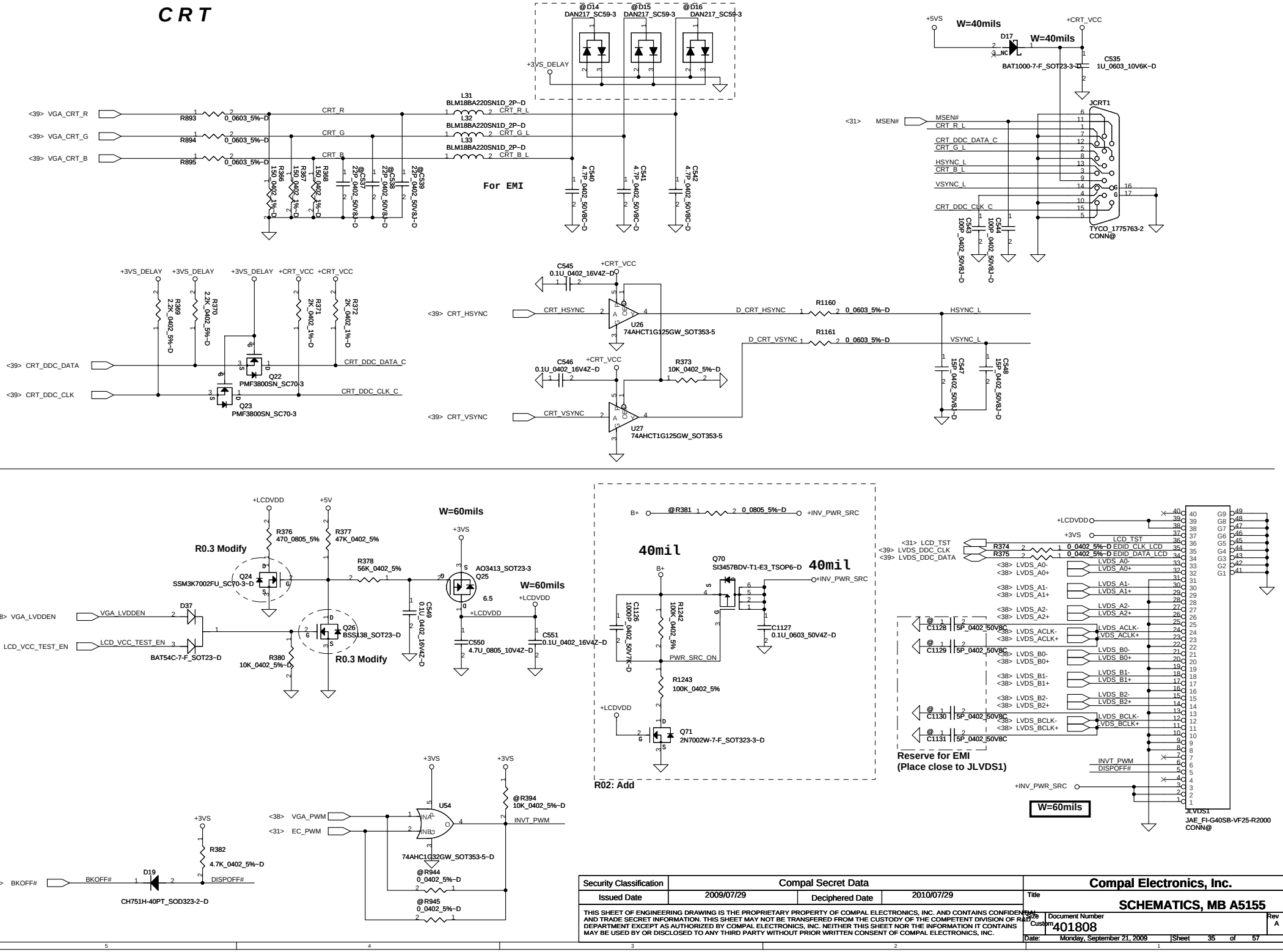
CRT



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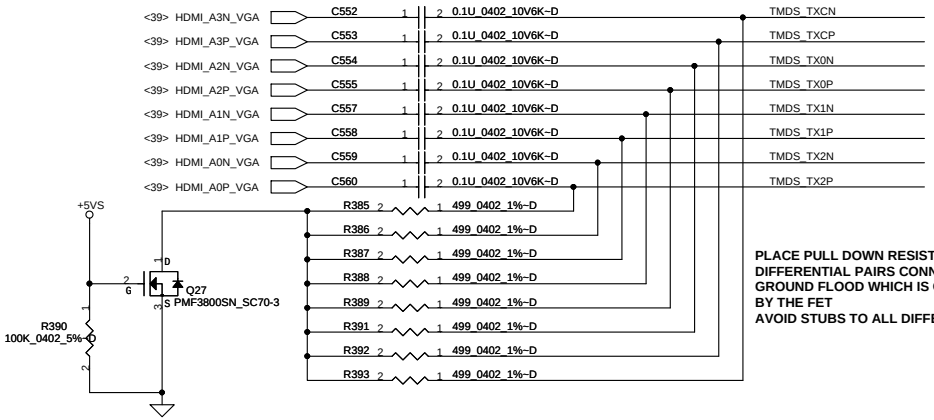
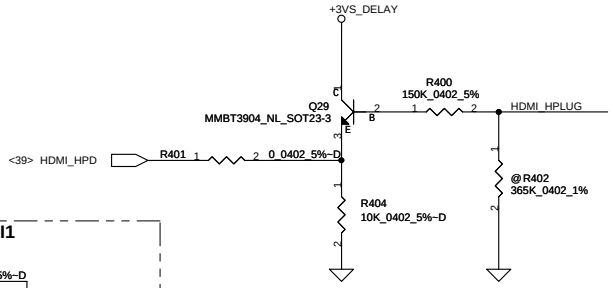
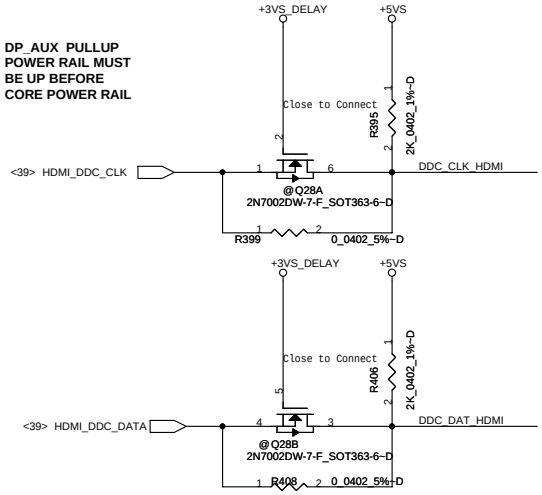
PLACE AC CAP
CLOSE TO CONNECTOR



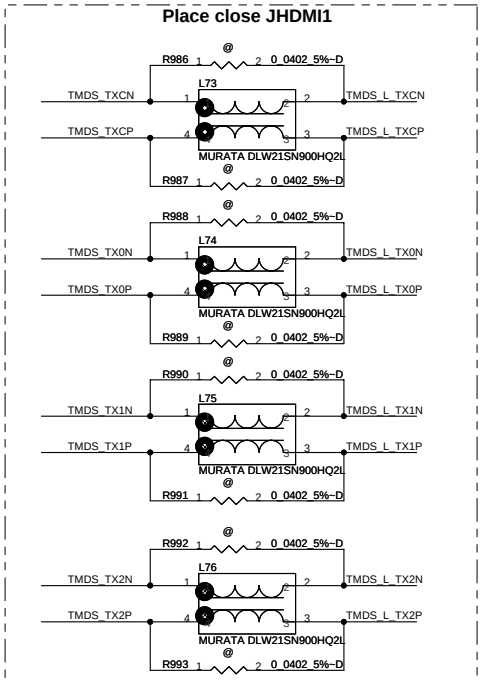
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

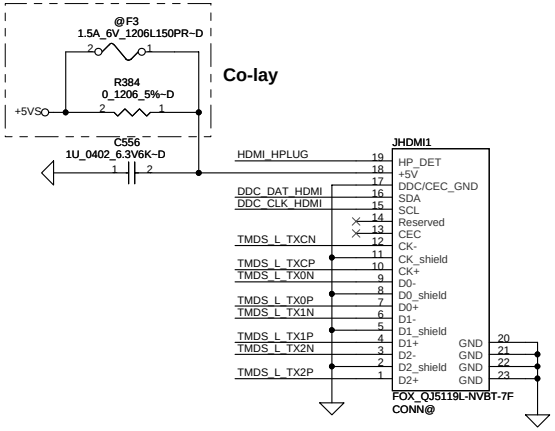


DP_AUX PULLUP
POWER RAIL MUST
BE UP BEFORE
CORE POWER RAIL



Place close JHDMI1





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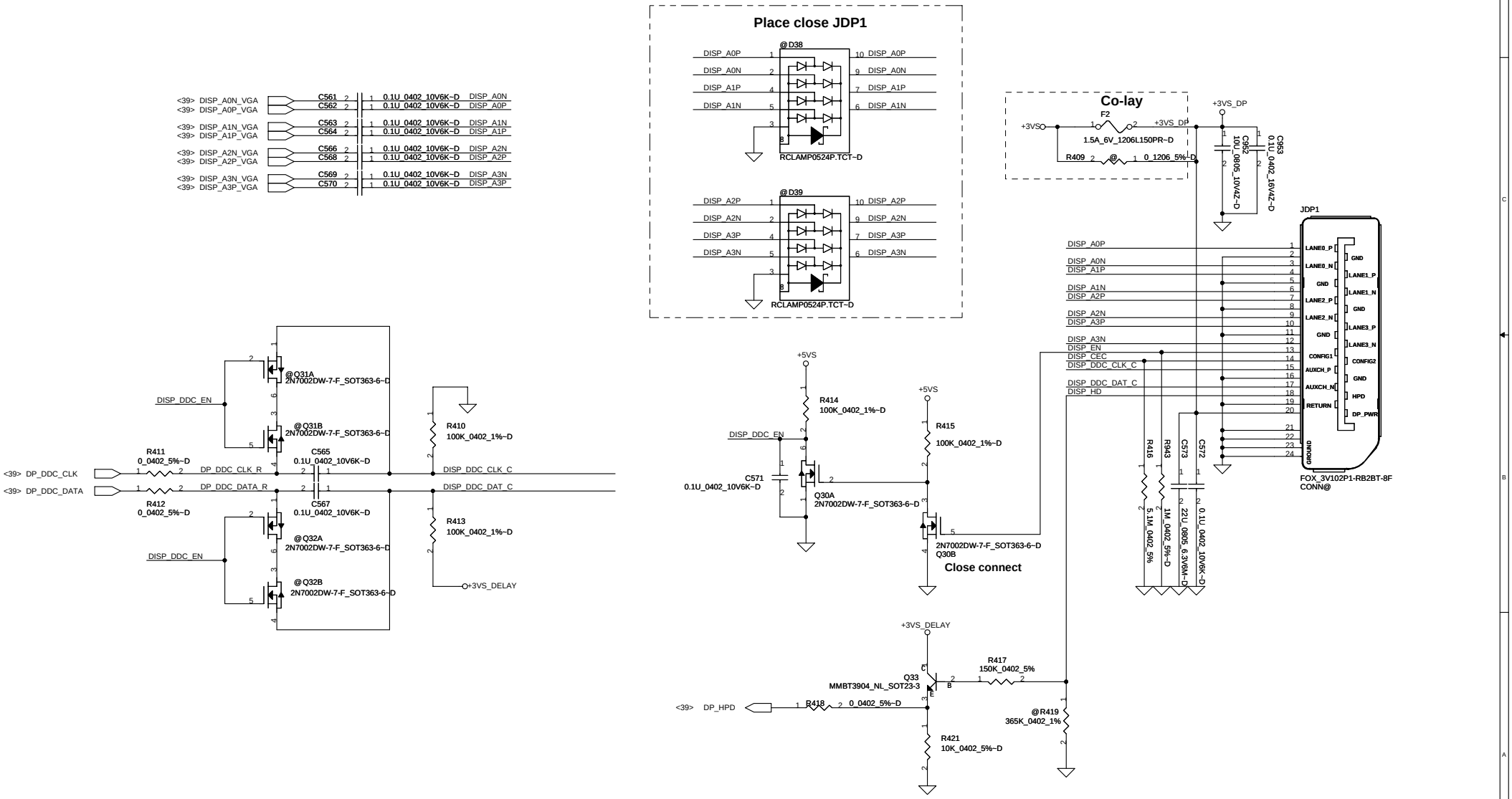

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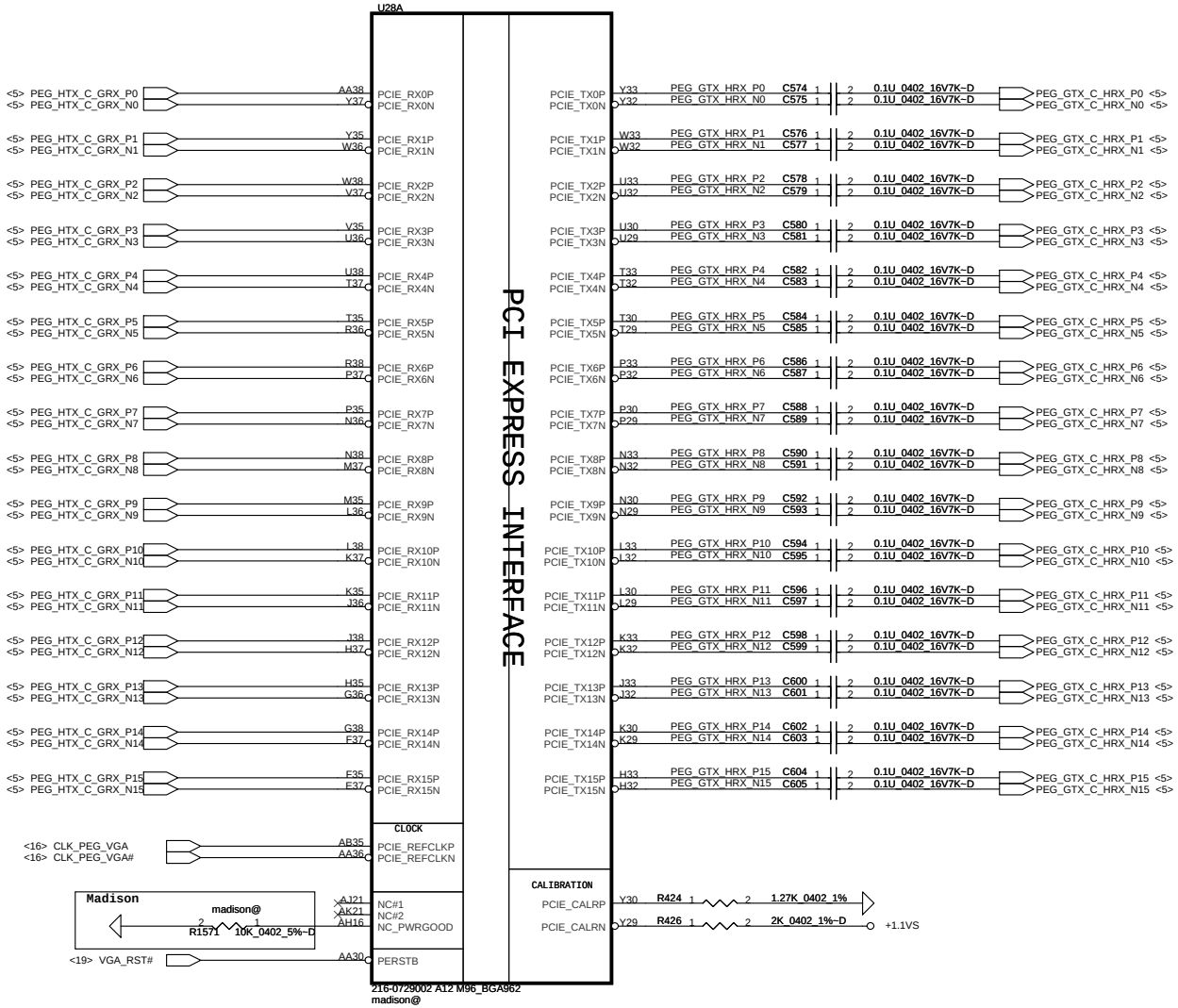

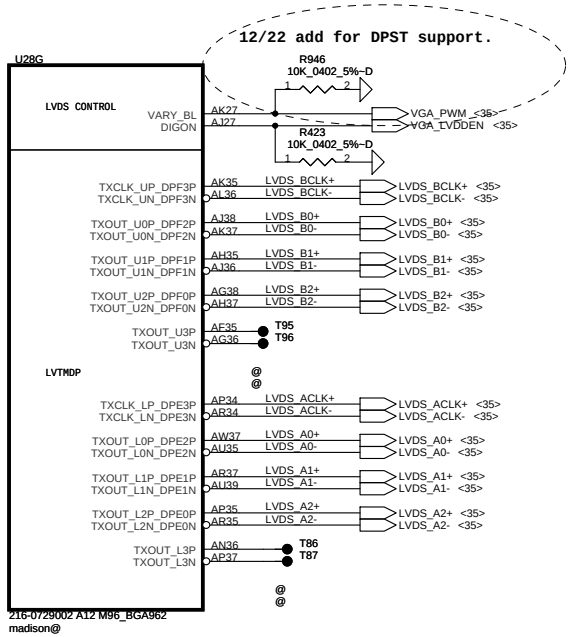

Madison P/N : SA00003M30L (S IC 216-0772000 MADISON PRO FCBGA GPU)

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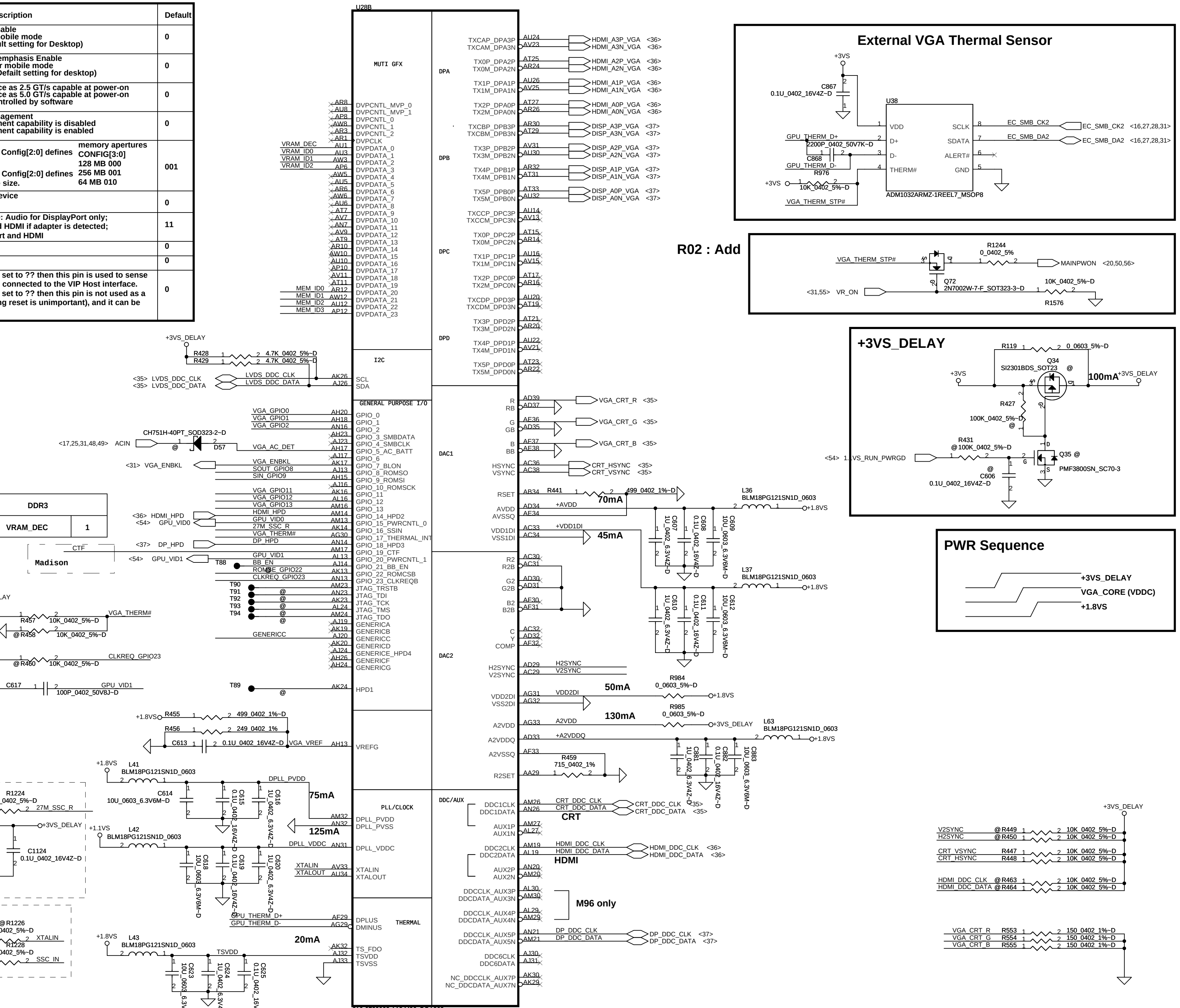
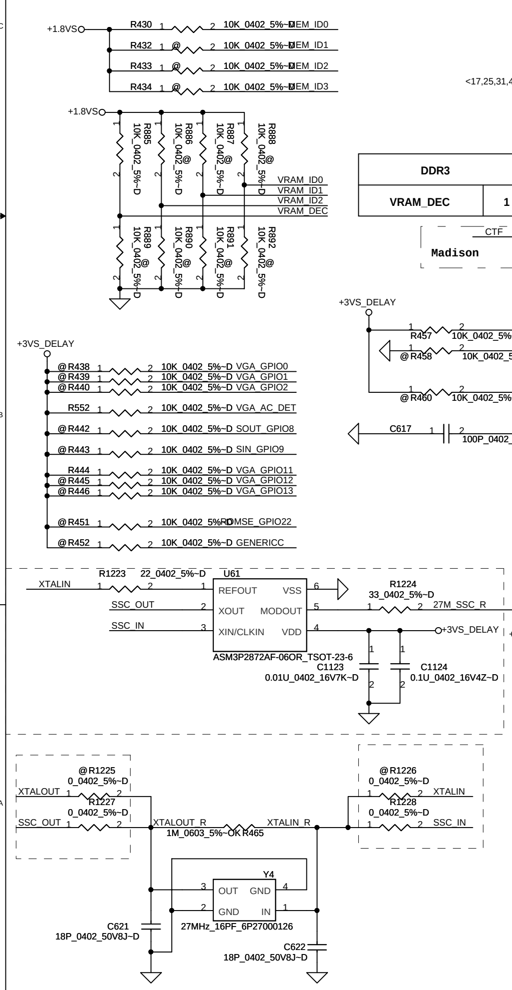
Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF _CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE _STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location / VRAM	MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3
Samsung	O	O	O	O
HYNIX	1	O	O	O





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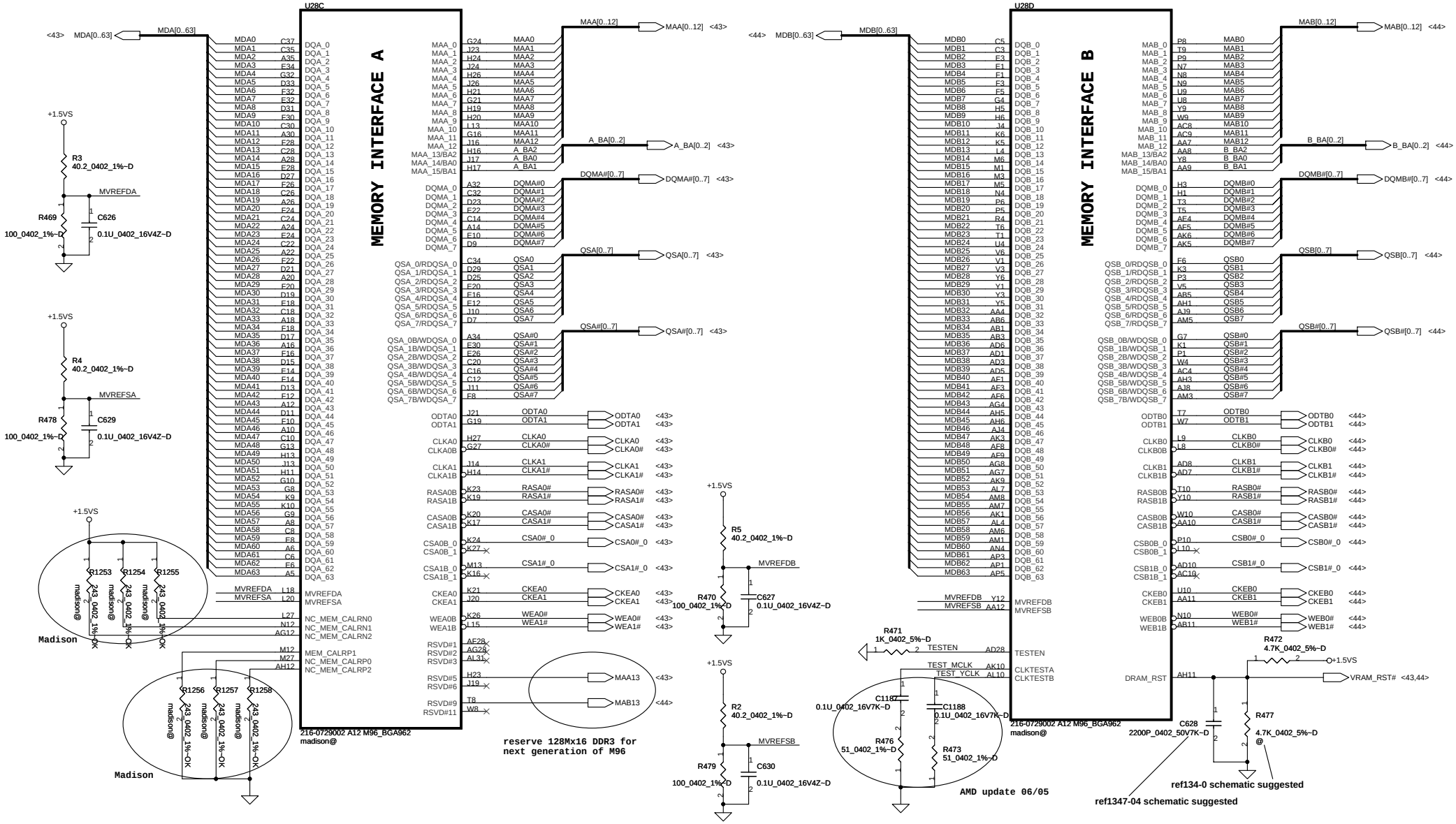

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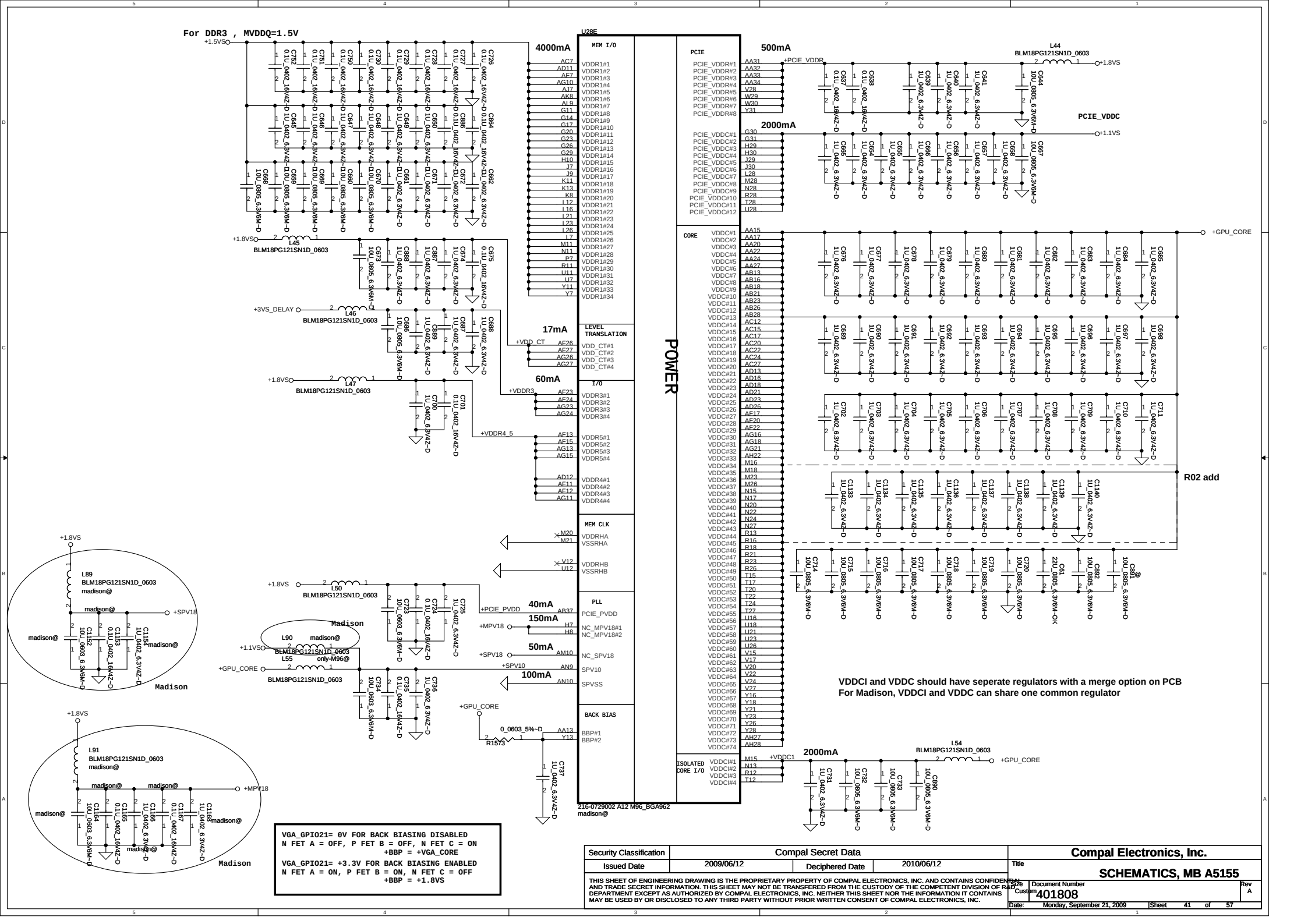

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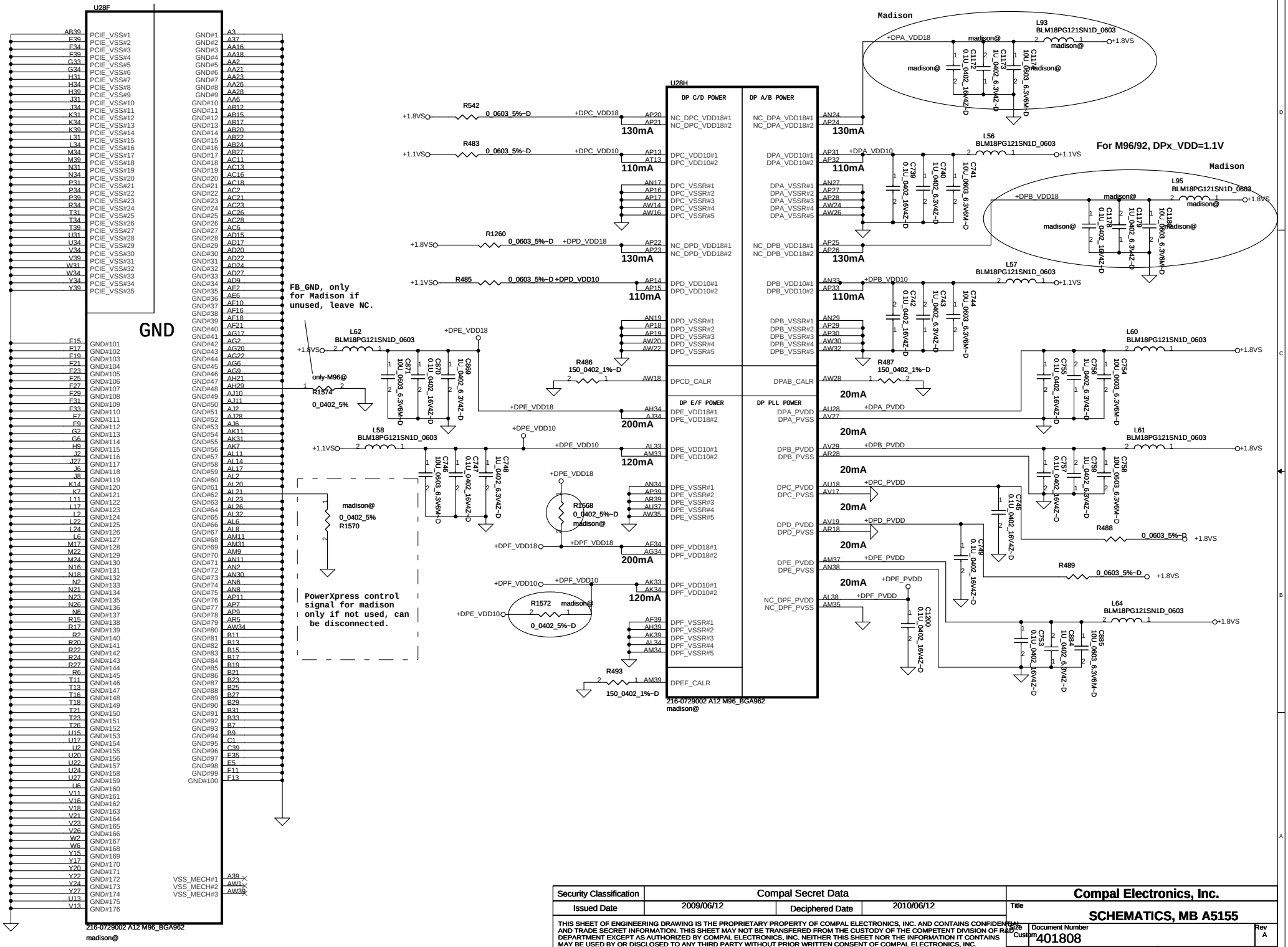

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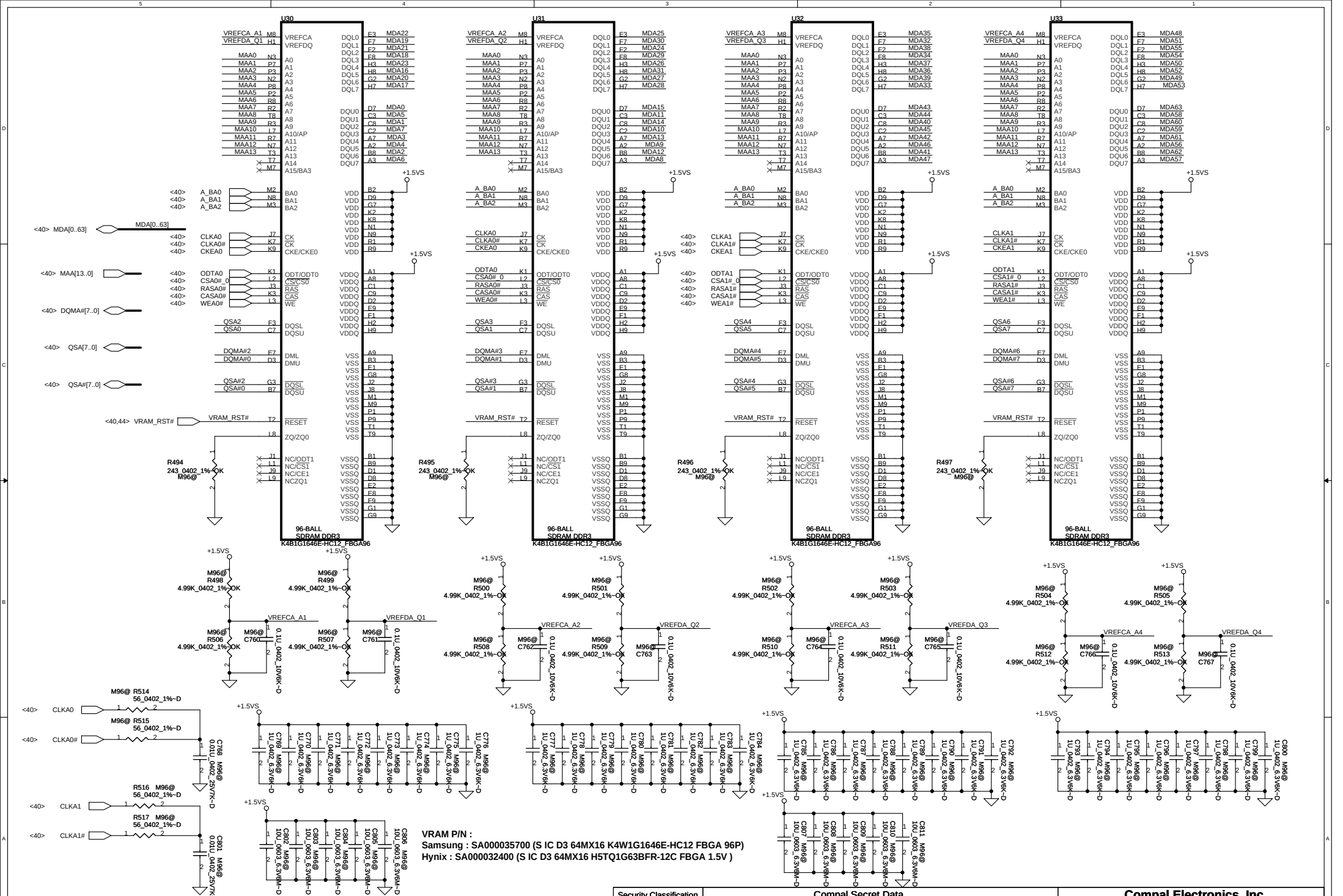

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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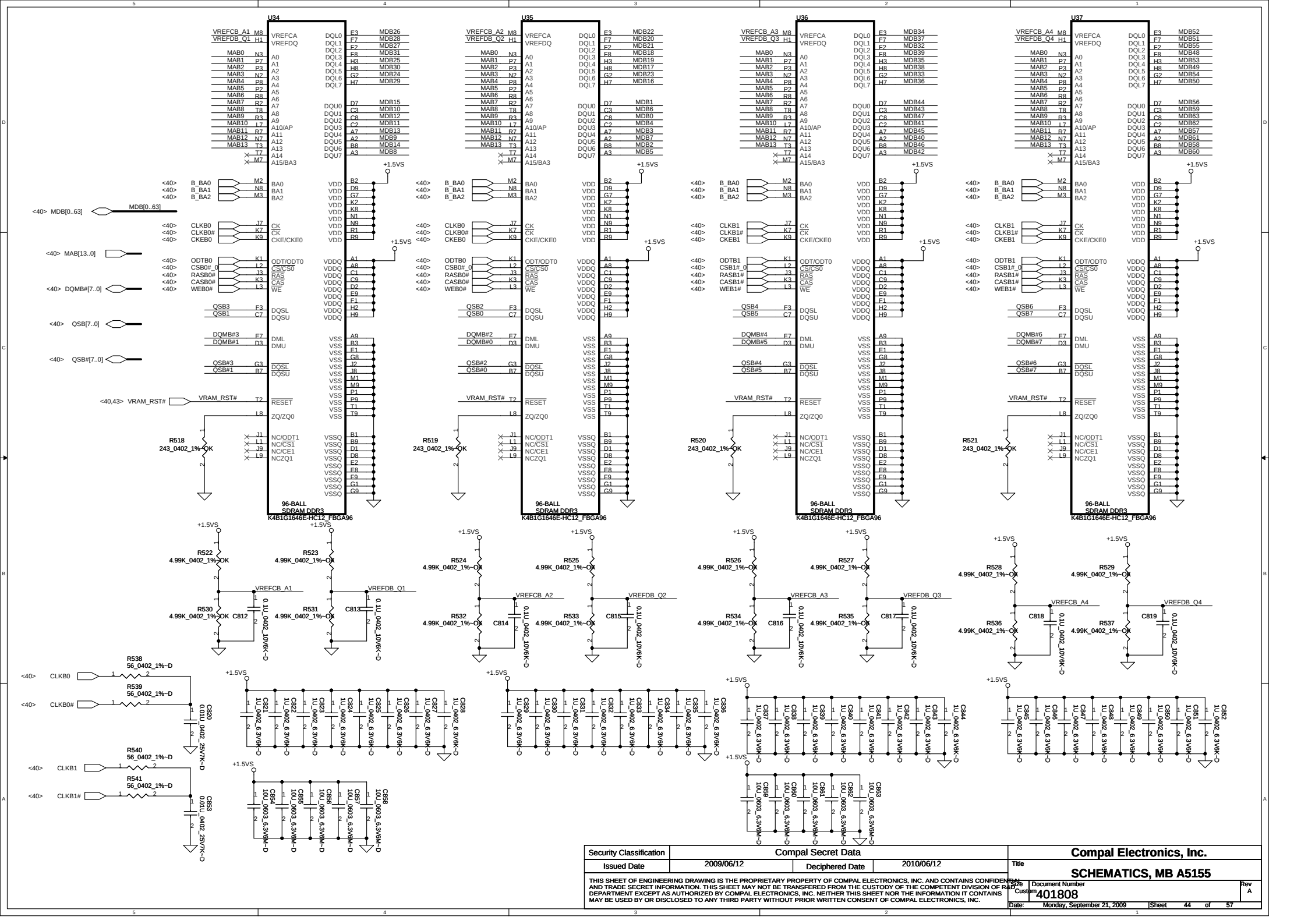

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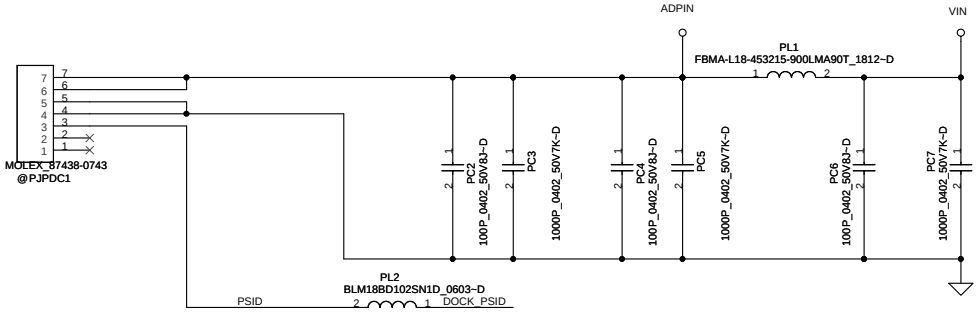

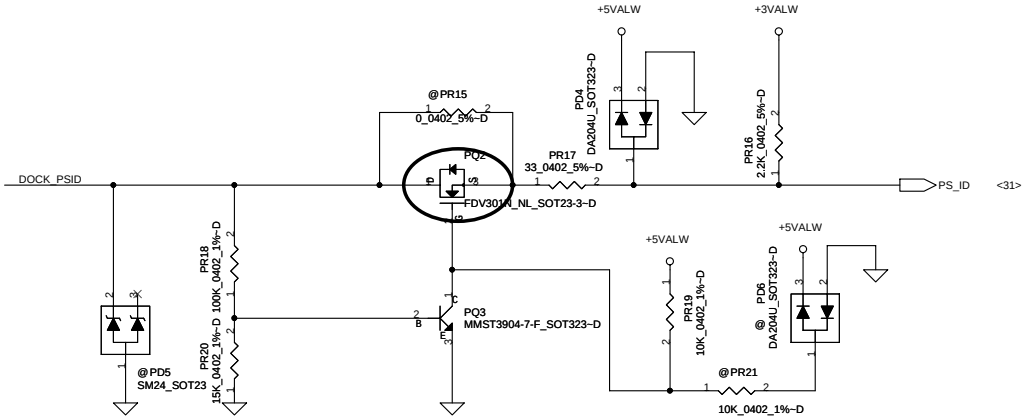

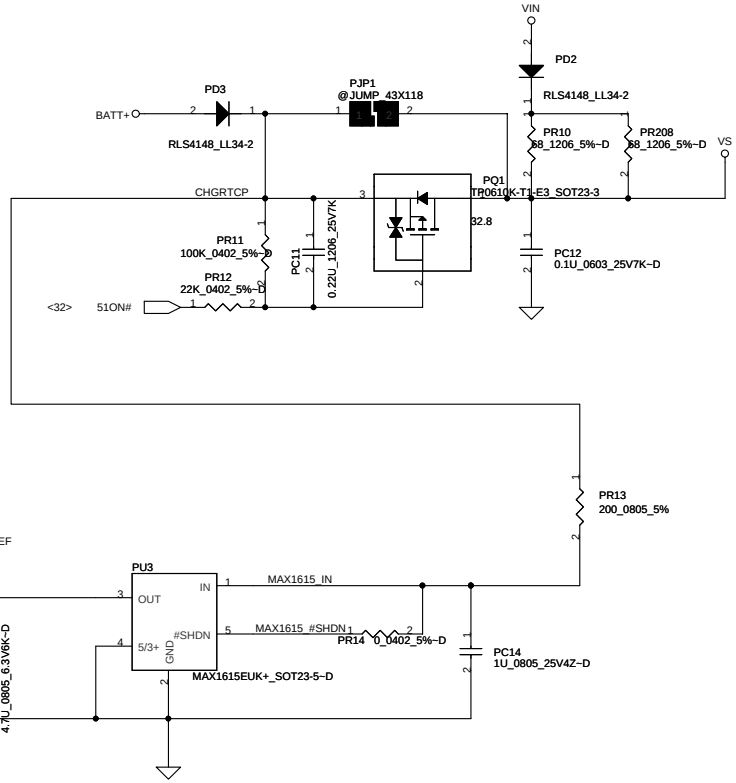

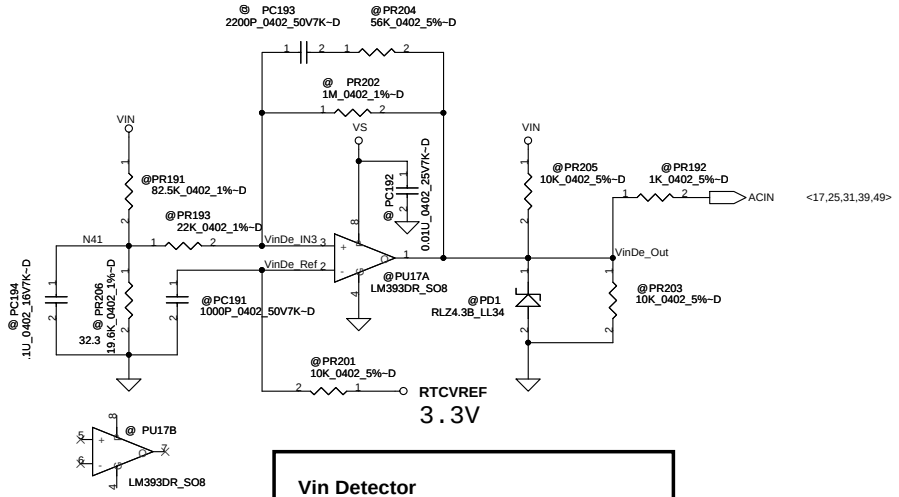

Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

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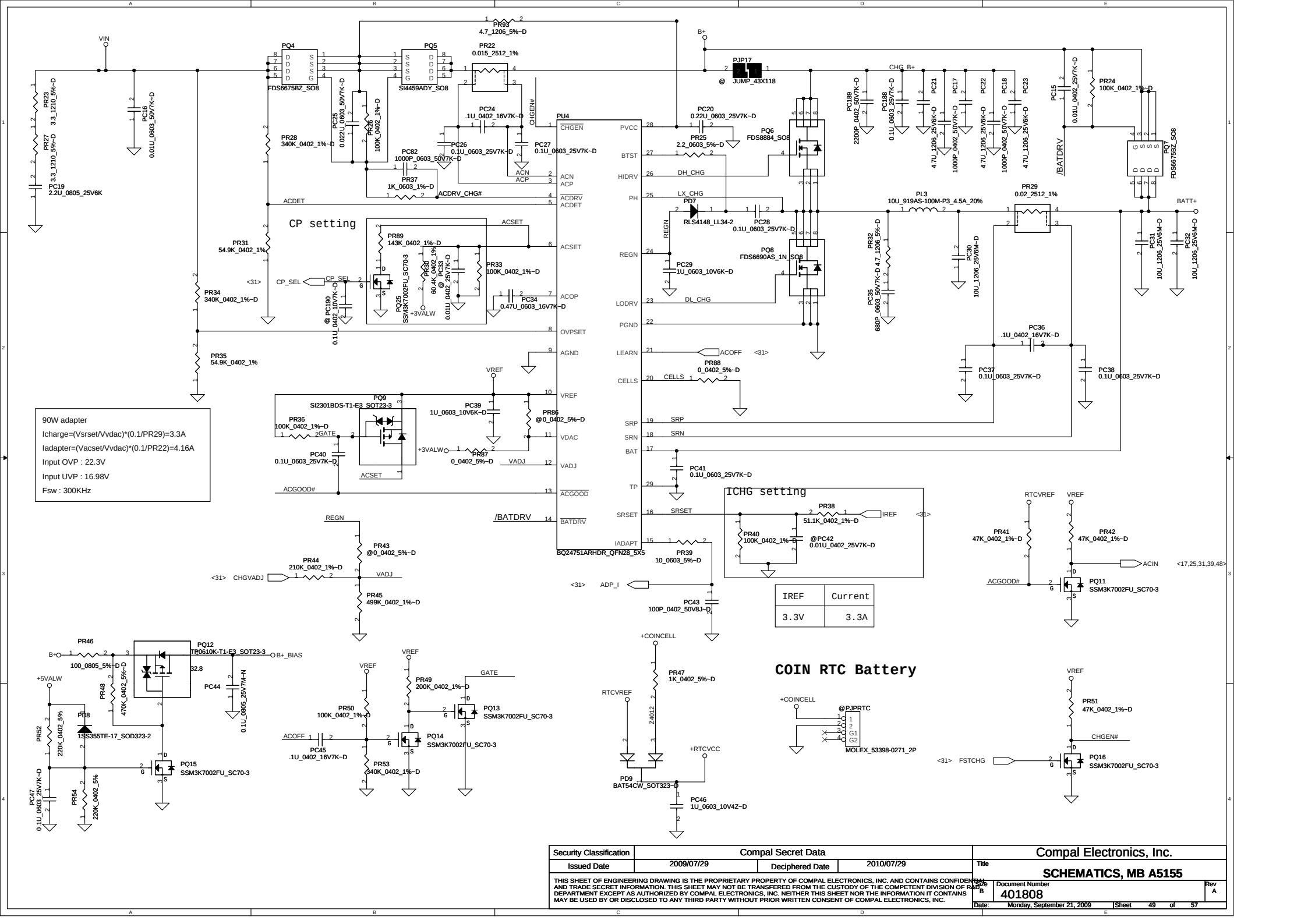
90W adapter
Icharge=(Vsrset/Vvdac)*(0.1/PR29)=3.3A
Iadapter=(Vacset/Vvdac)*(0.1/PR22)=4.16A
Input OVP : 22.3V
Input UVP : 16.98V
Fsw : 300KHz
CP setting
ICHG setting
COIN RTC Battery
BQ24751ARHDR_QFN28_5X5
IREF | Current
3.3V | 3.3A
Security Classification | Compal Secret Data
Issued Date | 2009/07/29 | Deciphered Date | 2010/07/29
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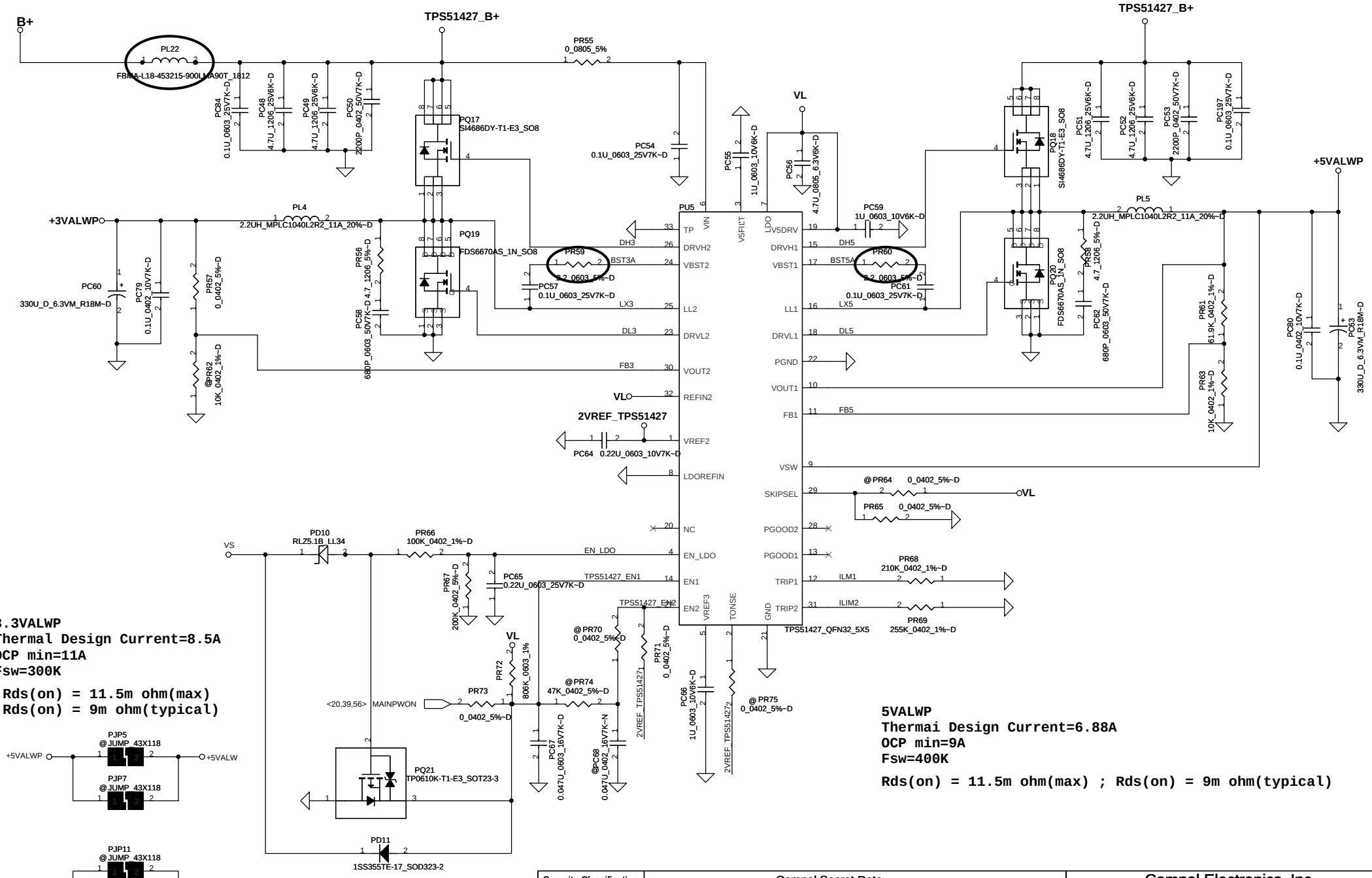

3.3VALWP
Thermal Design Current=8.5A
OCP min=11A
Fsw=300K

Rds(on) = 11.5m ohm(max)
Rds(on) = 9m ohm(typical)

5VALWP
Thermai Design Current=6.88A
OCP min=9A
Fsw=400K

Rds(on) = 11.5m ohm(max) ; Rds(on) = 9m ohm(typical)

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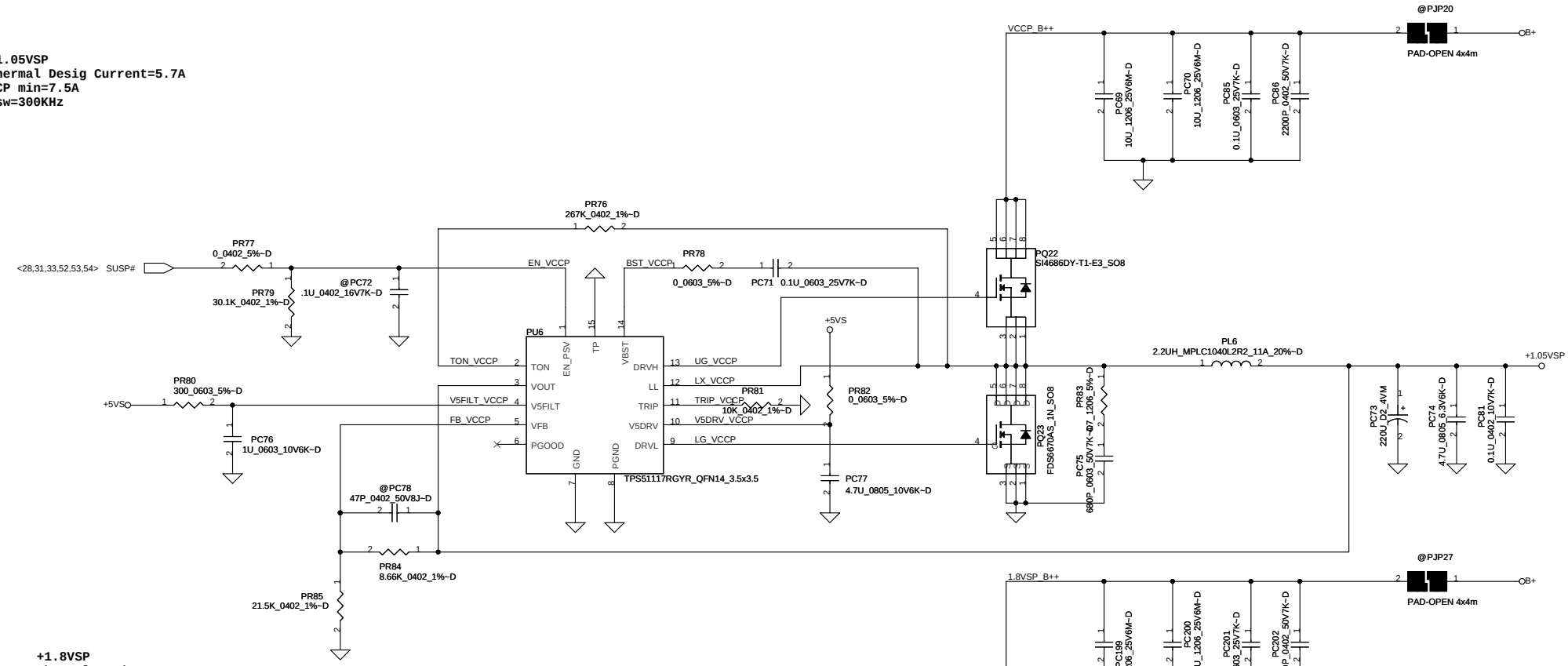
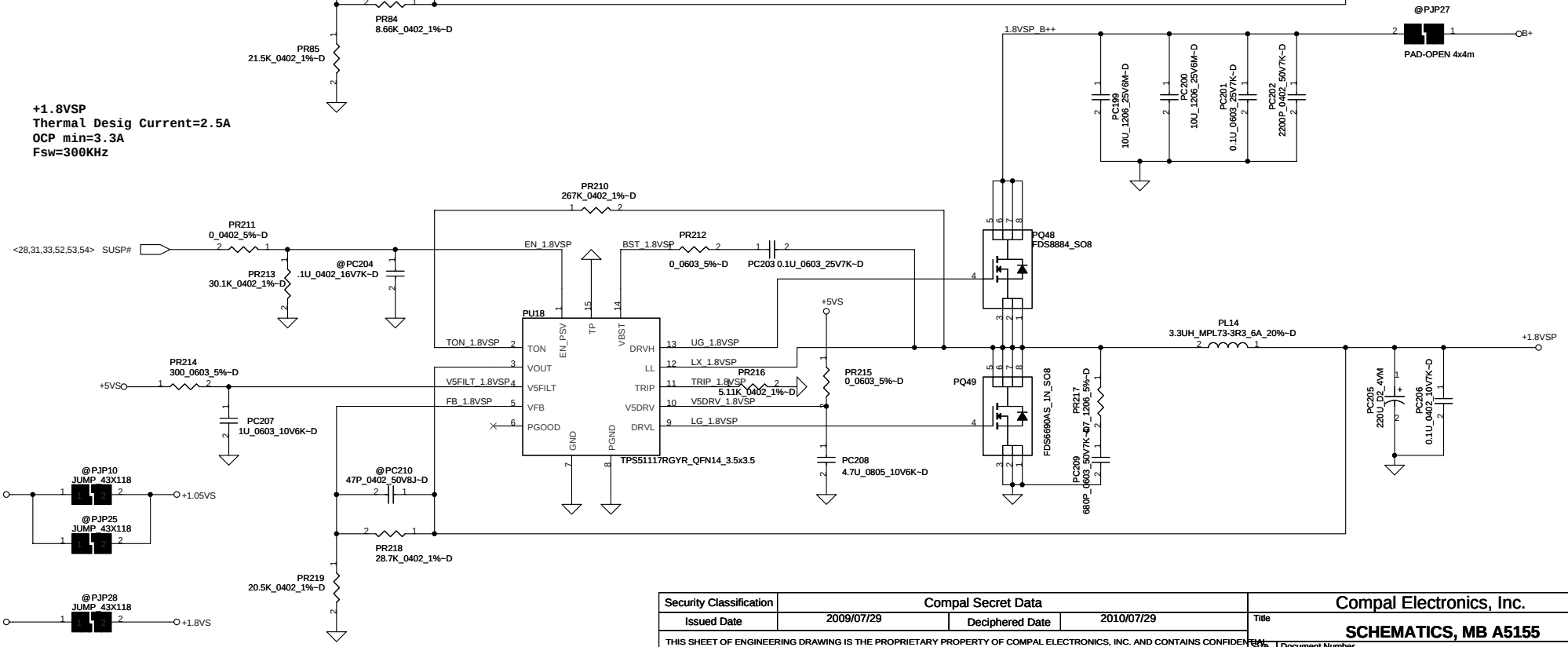
+1.05VSP
Thermal Desig Current=5.7A
OCP min=7.5A
Fsw=300KHz



+1.8VSP
Thermal Desig Current=2.5A
OCP min=3.3A
Fsw=300KHz



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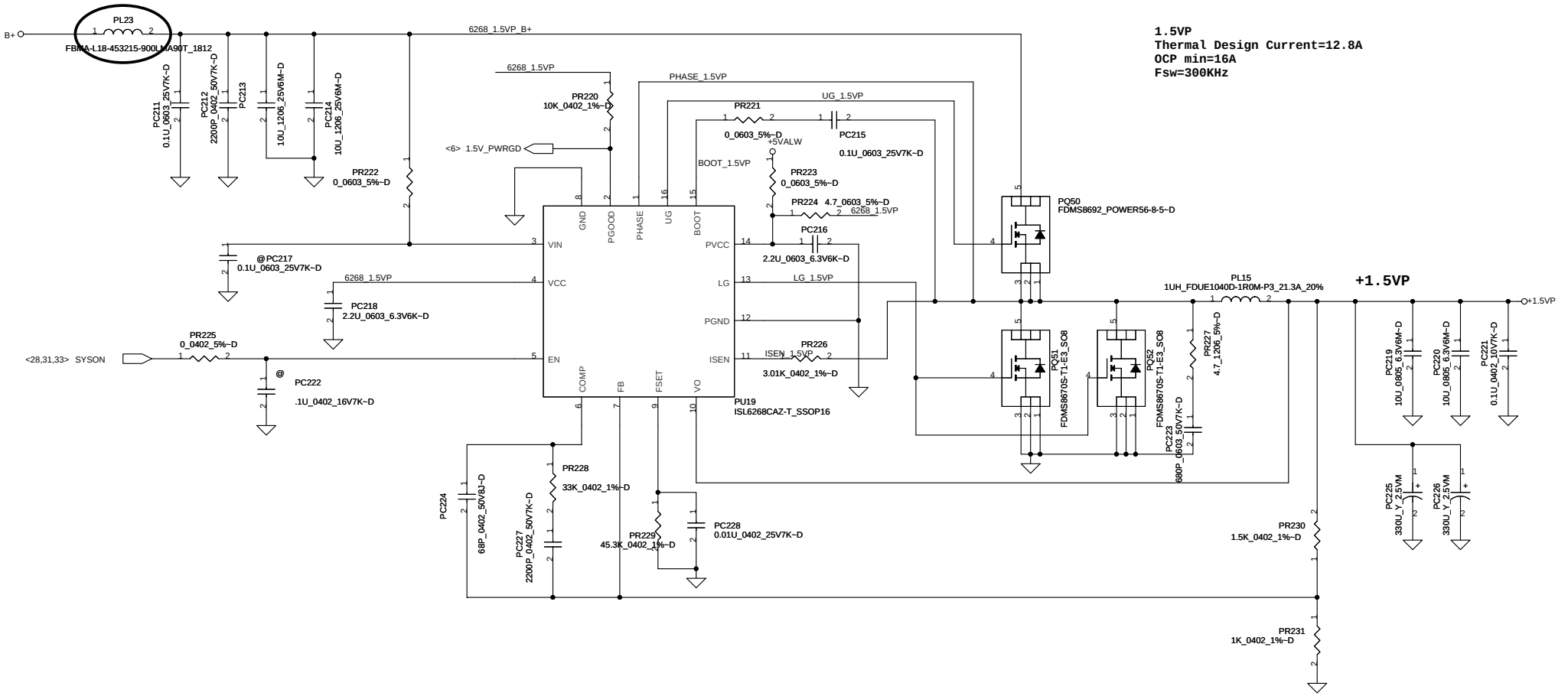

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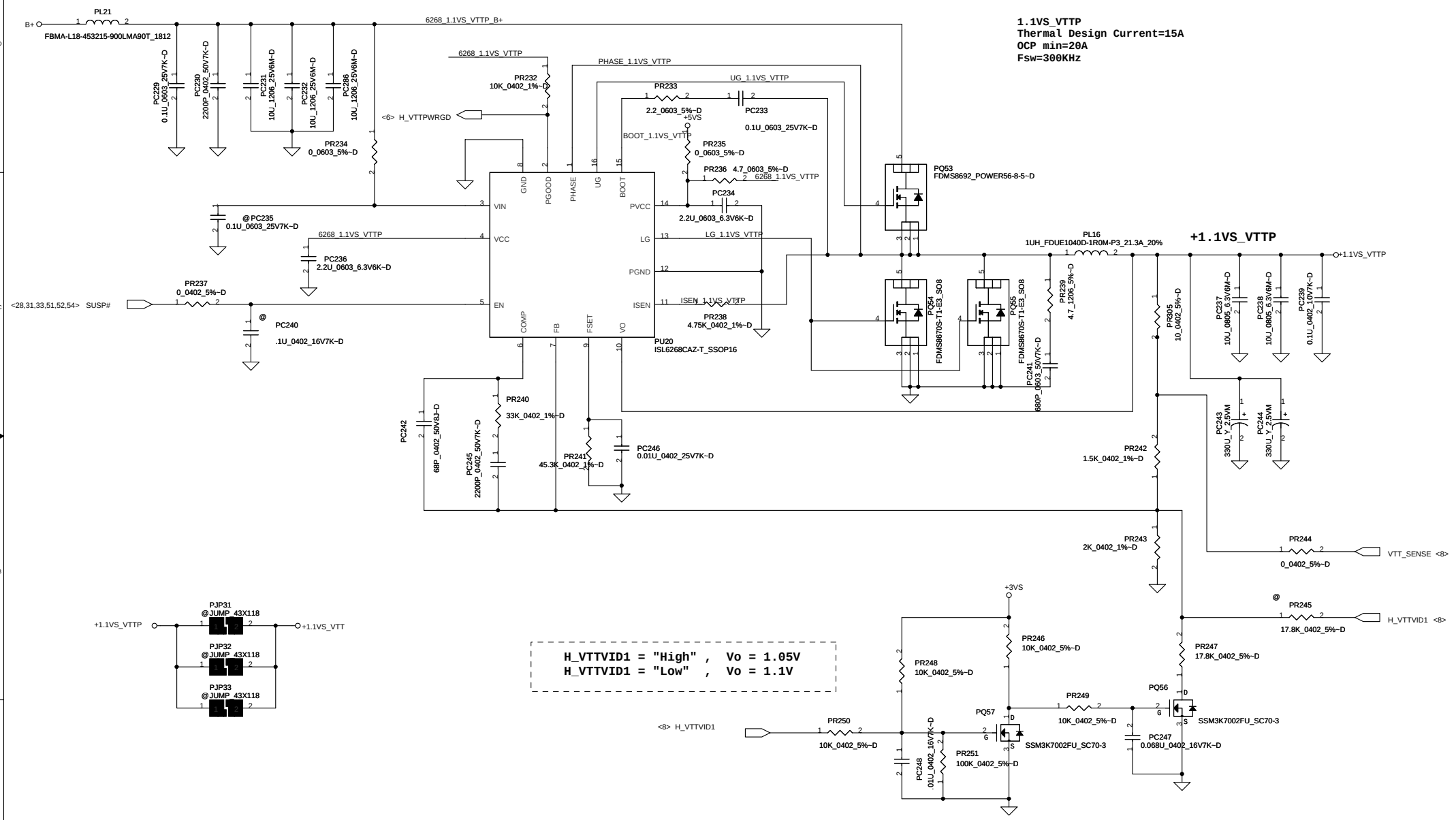

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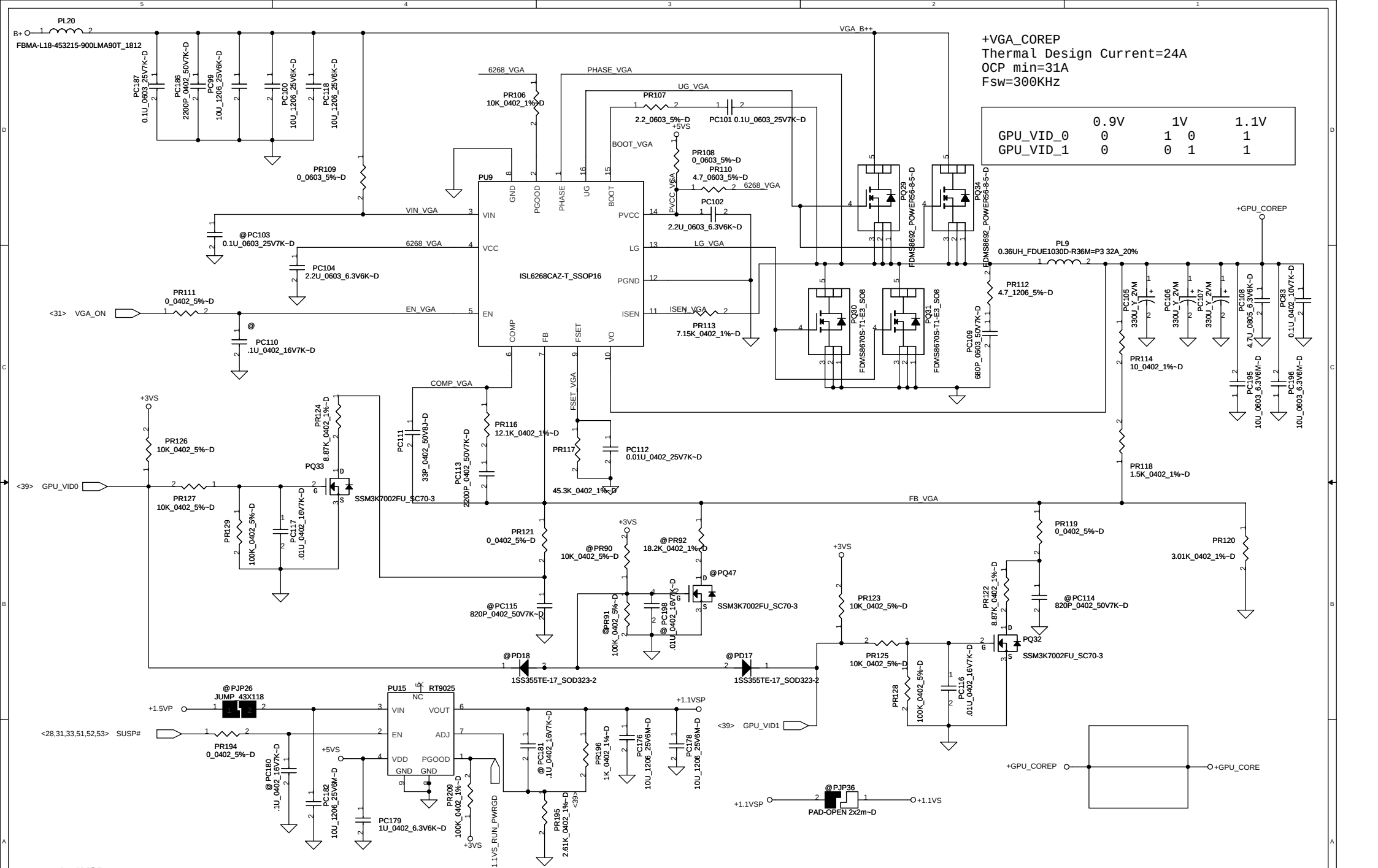

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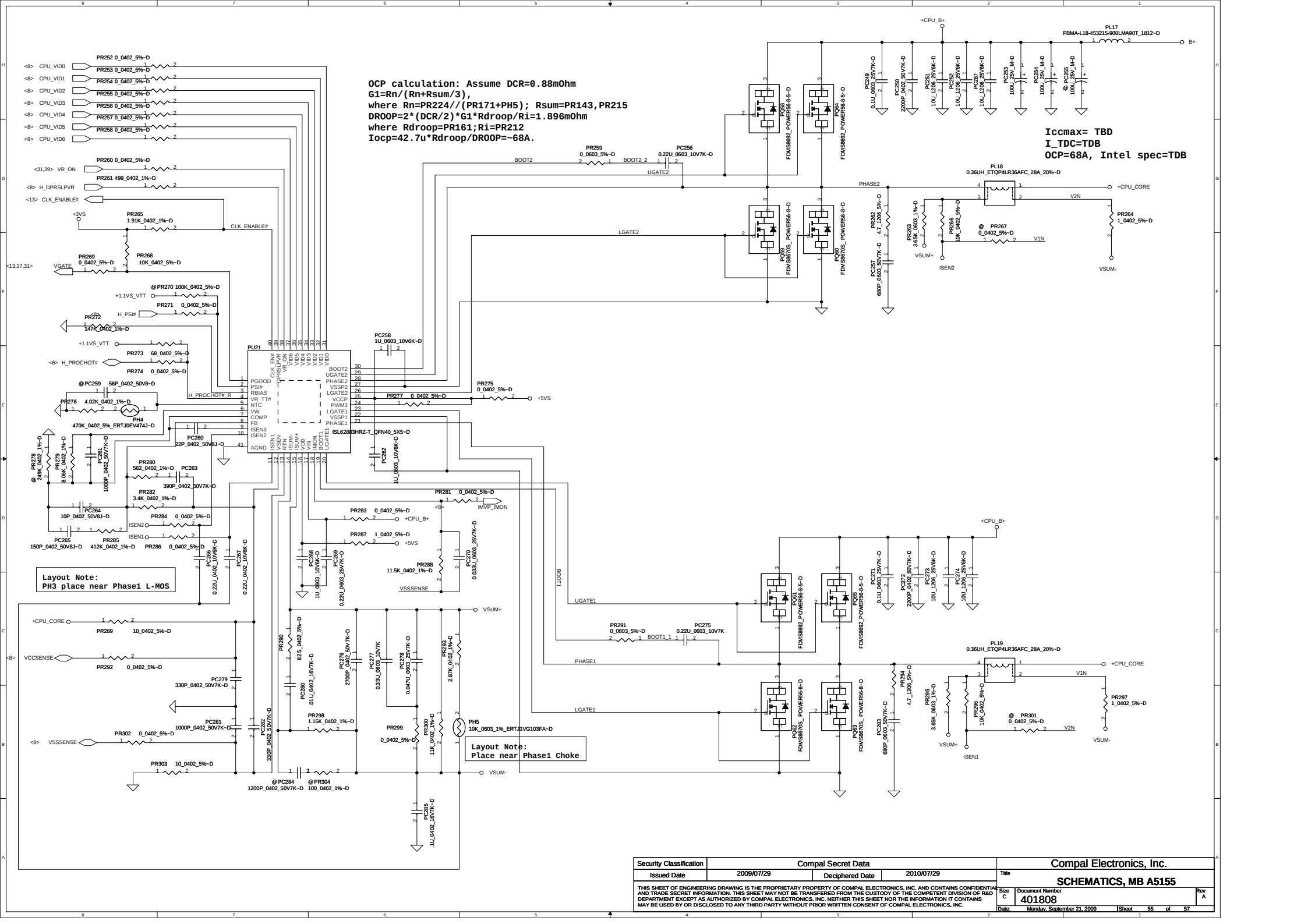

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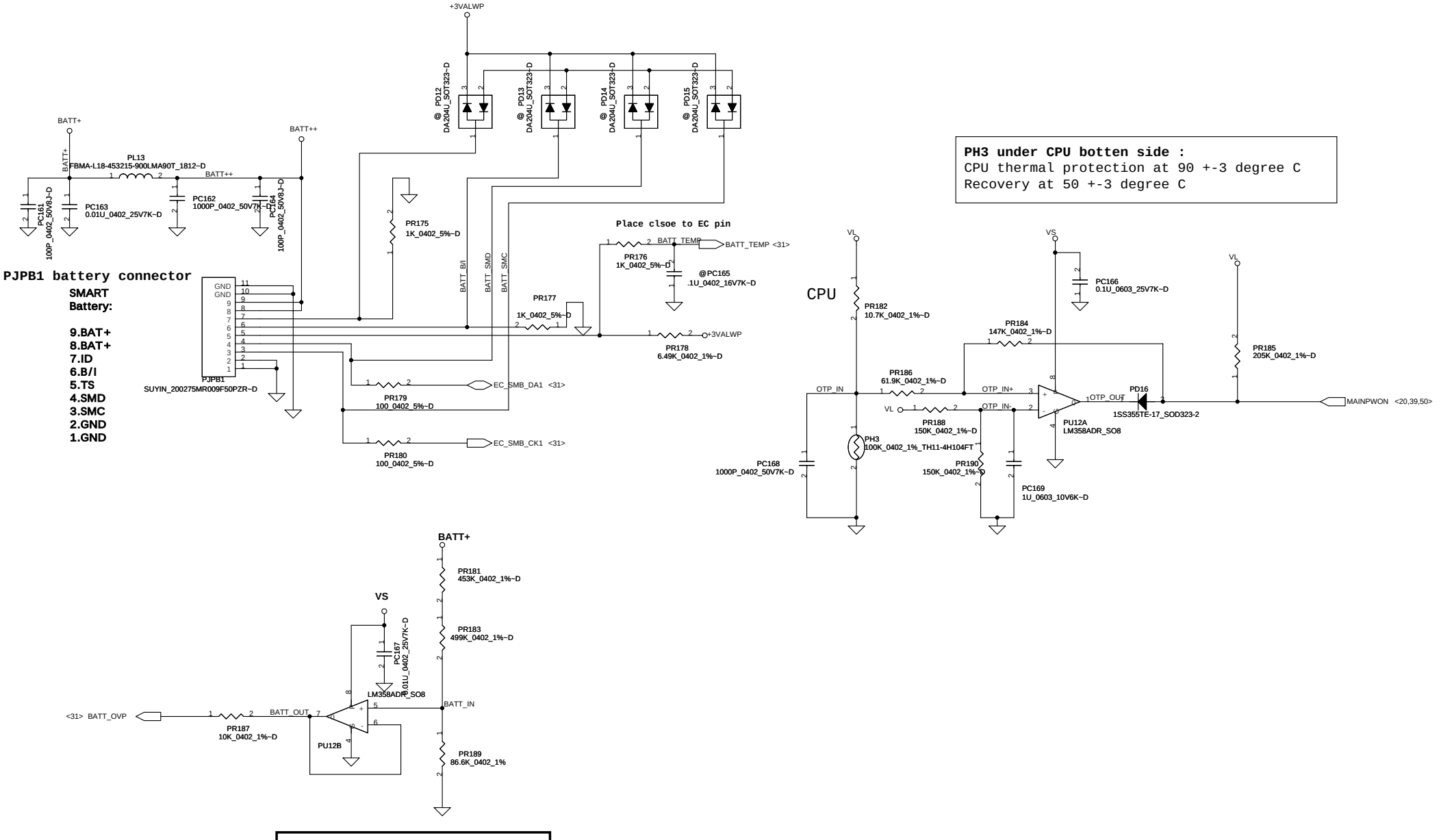
Battery Connect/OTP



LI-3S :13.5V----BATT_OVP=1.126V
BATT_OVP=0.08338*BATT+

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