

Compal Confidential

NDWGO Schematics Document

AMD S1g3/ RS880M/ SB710

2009 / 09 / 22

LA-5991P

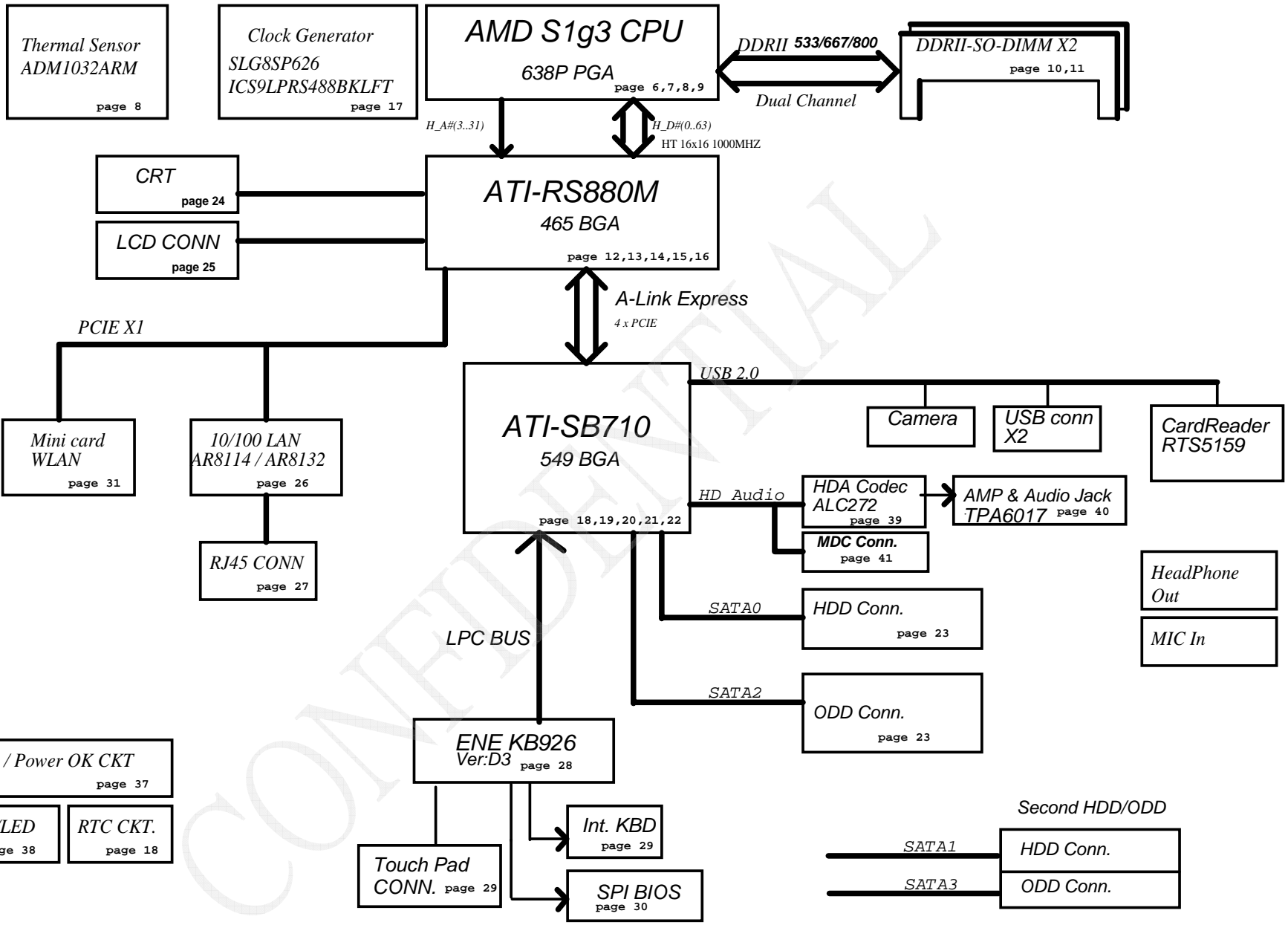
Rev:0.1

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				Custom	401830	A
				Date:	Tuesday, October 13, 2009	Sheet 1 of 47

Compal confidential

Project Code: NDWG0/H0

File Name : LA-5991P



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				401830	401830
				Date:	Tuesday, October 13, 2009
				Sheet	2 of 47

Voltage Rails

VIN	Adapter power supply (19V)			
B+	AC or battery power rail for power circuit.			
+CPU_CORE	Core voltage for CPU			
+0.9V	0.9V switched power rail for DDR terminator			
+1.2V_HT	1.2V switched power rail	ON	OFF	
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON		ON*
+1.8VS	1.8V switched power rail		OFF	
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

EC SM Bus2 address

SB600 SM Bus 1 address

Device	Address	Device	Address
Clock Generator	1101 001Xb	New Card	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Wireless Lan			

SB600 SM Bus 2 address

BOARD ID Table

Board ID	PCB Revision
0	No Support VaryBright
1	
2	
3	Support VaryBright
4	
5	
6	
7	

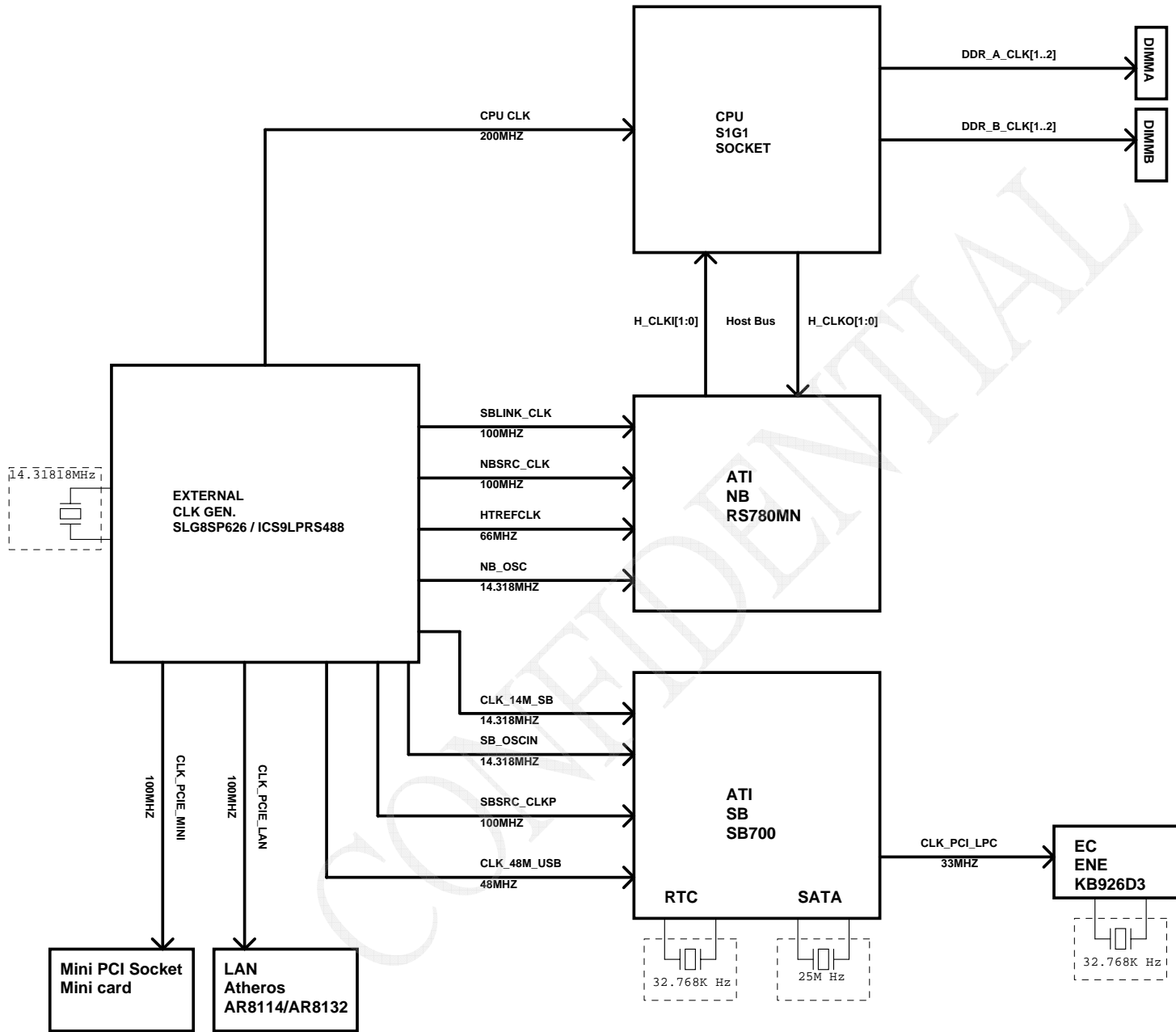
BTO Option Table

BTO Item	BOM Structure
10/100 Lan	8114@
GIGA Lan	8132@
17" ID	17@
15" ID	15@
Support VaryBright	VARY@

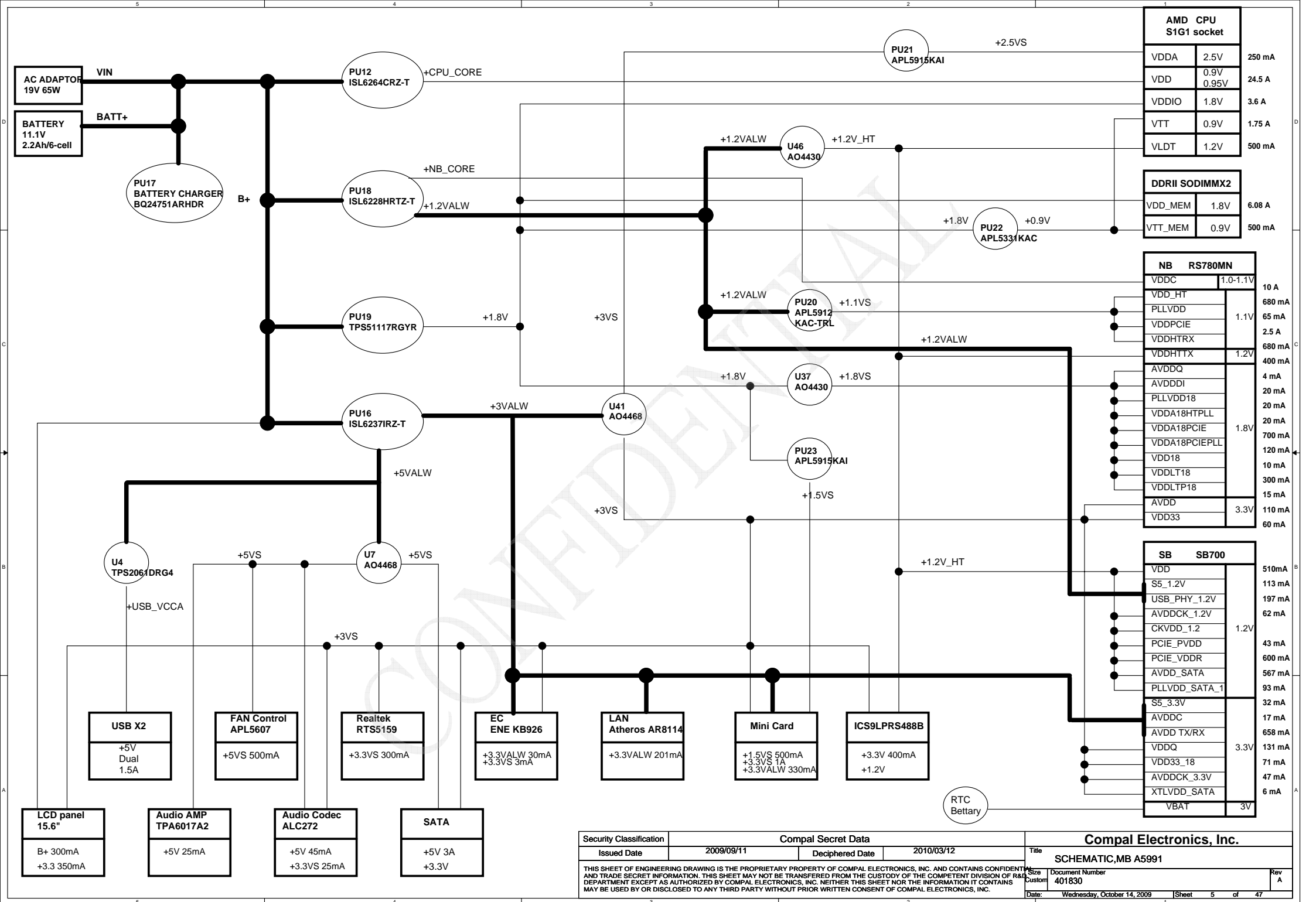
PROJECT ID Table

SKU ID	SKU
0	NCWGO
1	
2	
3	NAL00
4	
5	
6	
7	NCWHO

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								Custom	401830	A	
								Date:	Tuesday, October 13, 2009	Sheet	3 of 47



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				Customer	401830
				Date:	Wednesday, October 14, 2009
				Sheet	4 of 47
				Rev	A



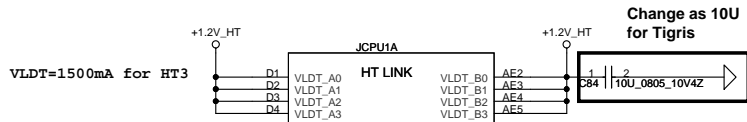
AMD CPU S1G1 socket		
VDDA	2.5V	250 mA
VDD	0.9V / 0.95V	24.5 A
VDDIO	1.8V	3.6 A
VTT	0.9V	1.75 A
VLDT	1.2V	500 mA

DDRII SODIMMx2		
VDD_MEM	1.8V	6.08 A
VTT_MEM	0.9V	500 mA

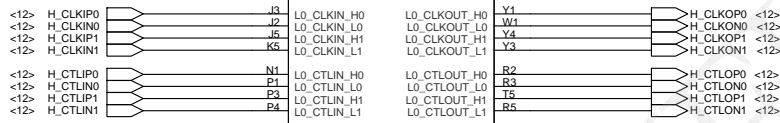
NB RS780MN		
VDDC	1.0-1.1V	10 A
VDD_HT		680 mA
PLLVDD	1.1V	65 mA
VDDPCIE		2.5 A
VDDHTRX		680 mA
VDDHTTX	1.2V	400 mA
AVDDQ		4 mA
AVDDDI		20 mA
PLLVDD18		20 mA
VDDA18HTPLL	1.8V	20 mA
VDDA18PCIE		700 mA
VDDA18PCIEPLL		120 mA
VDD18		10 mA
VDDLTP18		300 mA
AVDD		15 mA
VDD33	3.3V	110 mA

SB SB700		
VDD		510mA
S5_1.2V		113 mA
USB_PHY_1.2V		197 mA
AVDDCK_1.2V	1.2V	62 mA
CKVDD_1.2		43 mA
PCIE_PVDD		600 mA
PCIE_VDDR		567 mA
AVDD_SATA		93 mA
PLLVDD_SATA_1		32 mA
S5_3.3V		17 mA
AVDDC		658 mA
AVDD TX/RX	3.3V	131 mA
VDDQ		71 mA
VDD33_18		47 mA
AVDDCK_3.3V		6 mA
XTLVDD_SATA		
VBAT	3V	

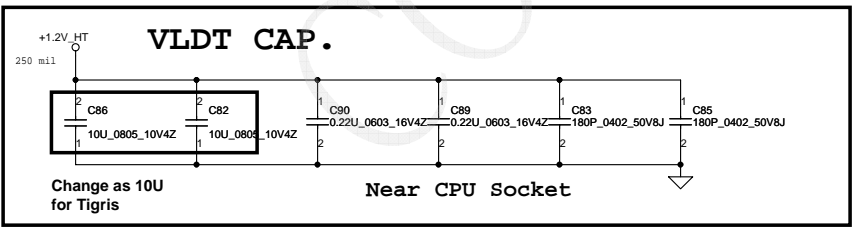
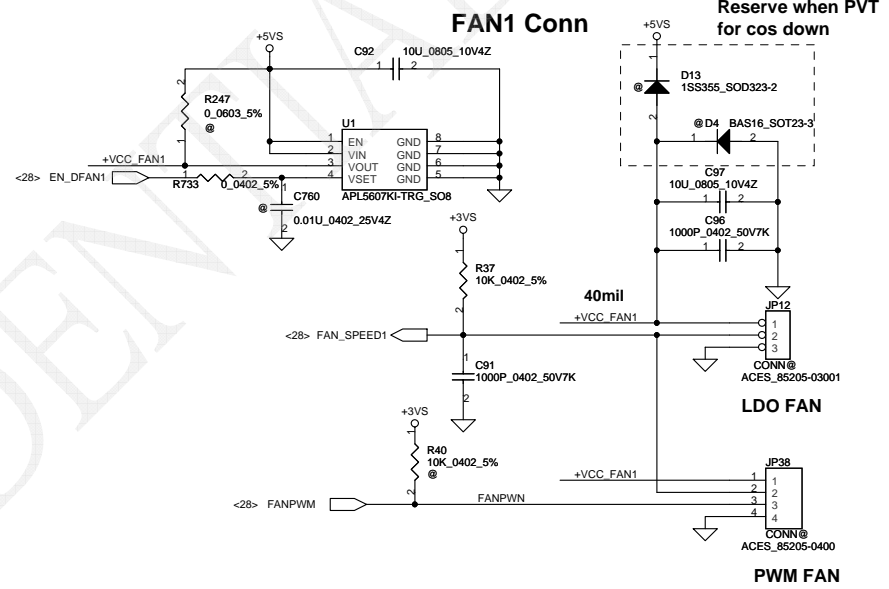
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Size	Document Number	Rev	Date: Wednesday, October 14, 2009 Sheet 5 of 47		
Customer	401830	A			



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H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
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H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
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H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F3	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
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H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

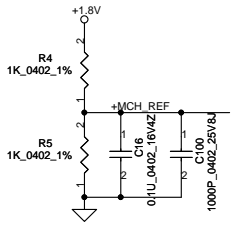
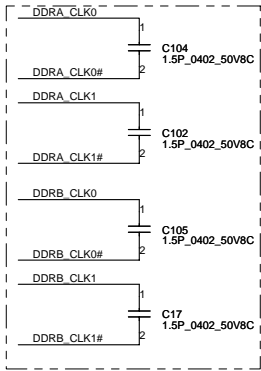


6090022100G_B
Athlon 64 S1
Processor Socket

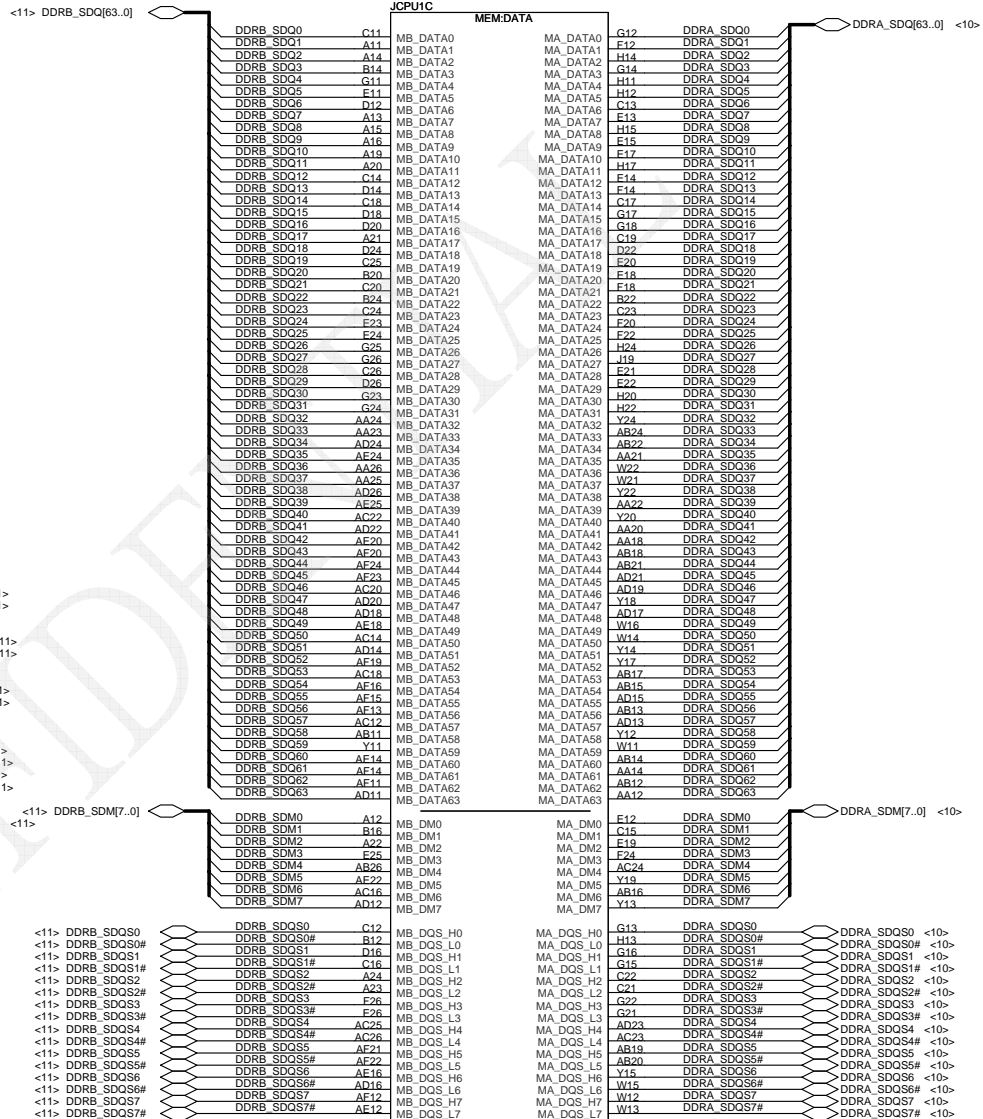
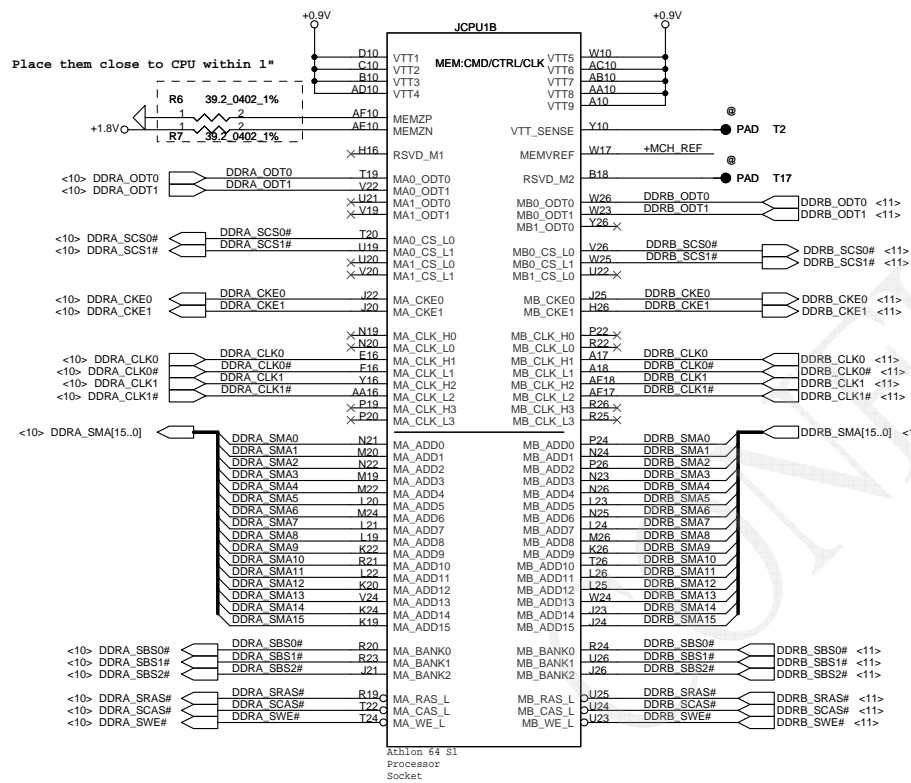


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				Rev A		

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

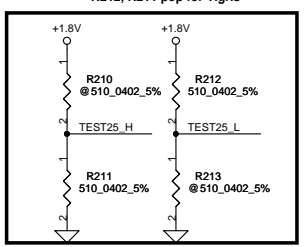
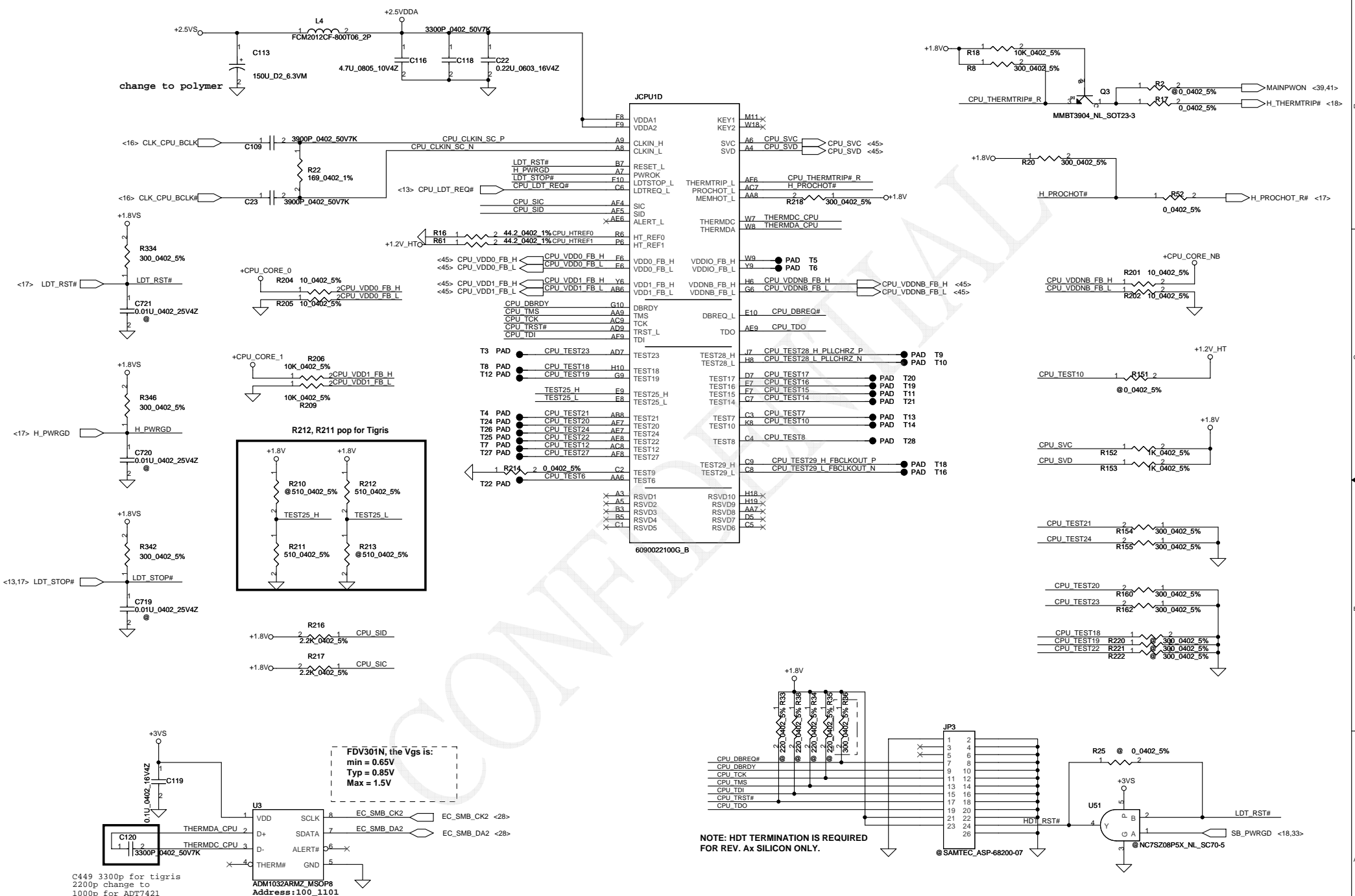


Processor DDR2 Memory Interface



6909022100G_B
Athlon 64 S1
Processor Socket

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Document Number	401830				Rev	A
Date:	Tuesday, October 13, 2009				Sheet	7 of 47



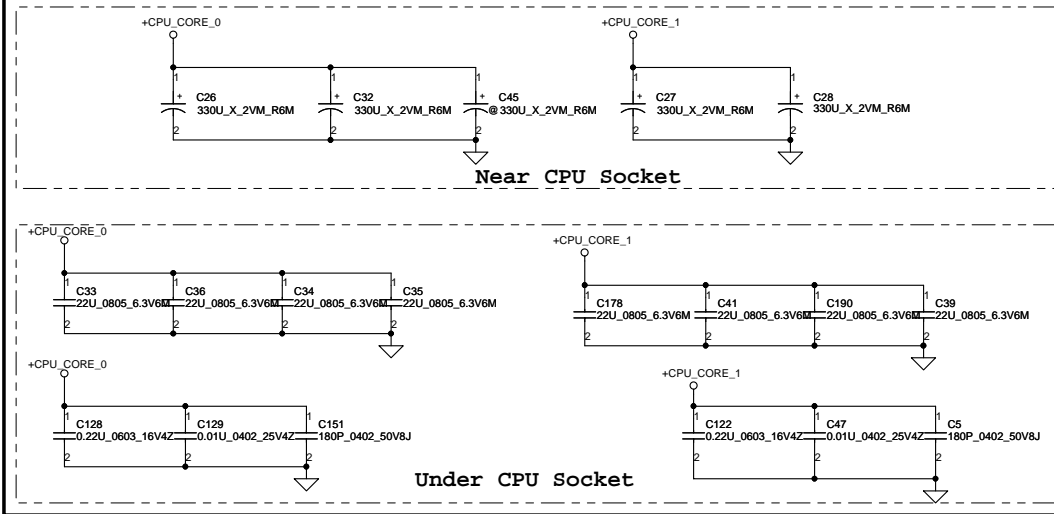
FDV301N, the Vgs is:
 min = 0.65V
 Typ = 0.85V
 Max = 1.5V

C449 3300p for tigris
 2200p change to
 1000p for ADT7421

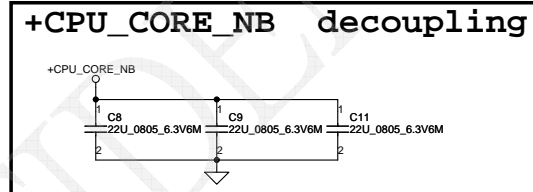
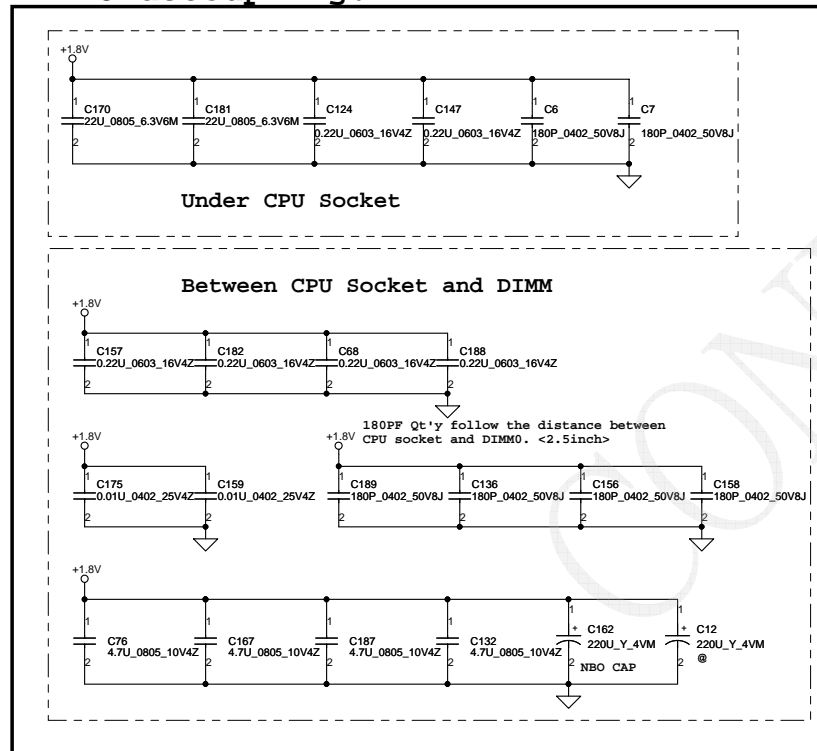
NOTE: HDT TERMINATION IS REQUIRED
 FOR REV. A.x SILICON ONLY.

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Date:	Tuesday, October 13, 2009	Sheet	8	of	47

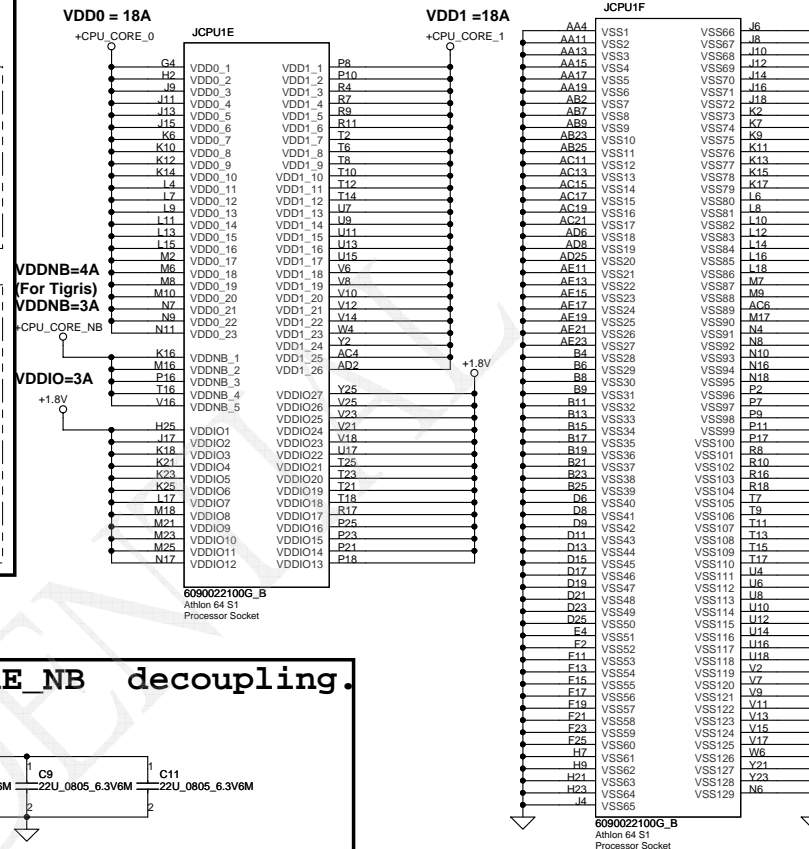
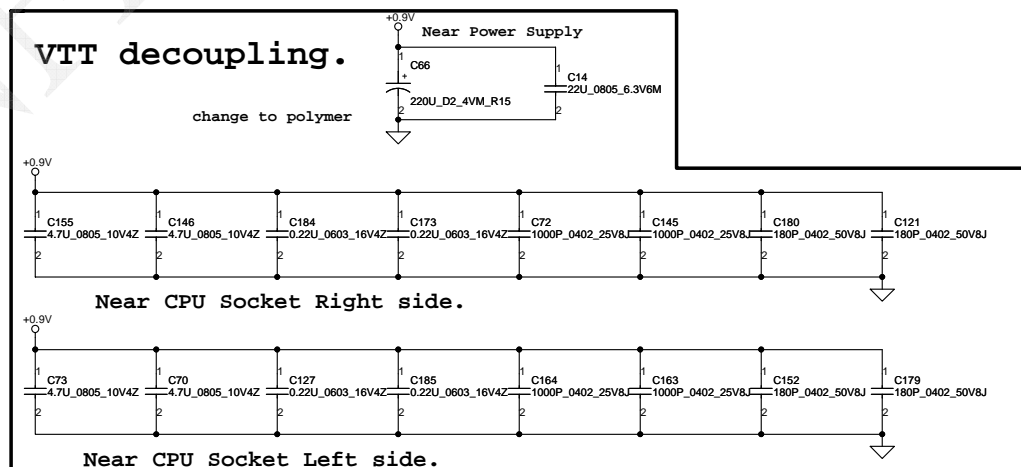
VDD(+CPU_CORE) decoupling.



VDDIO decoupling.

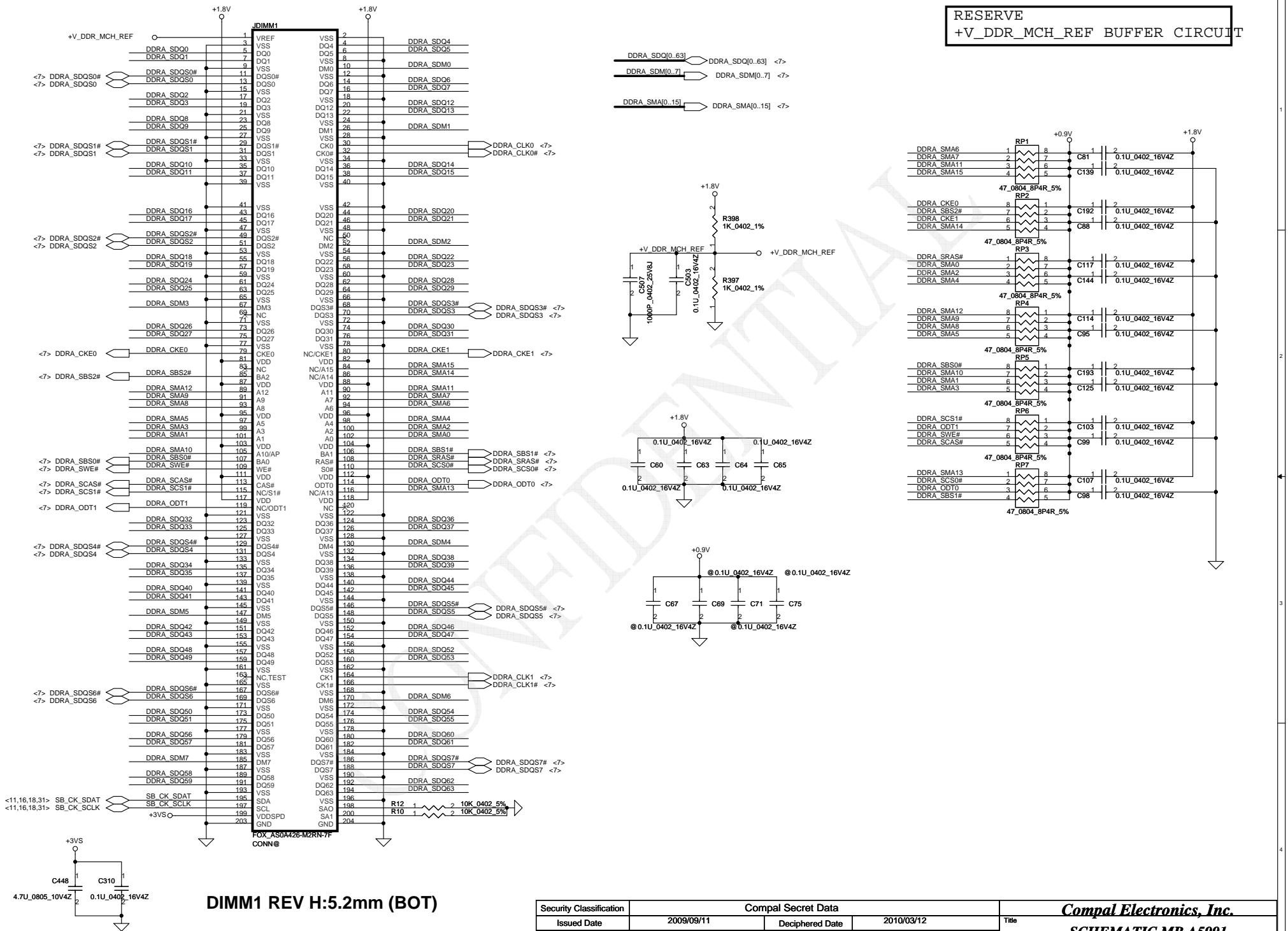


VTT decoupling.



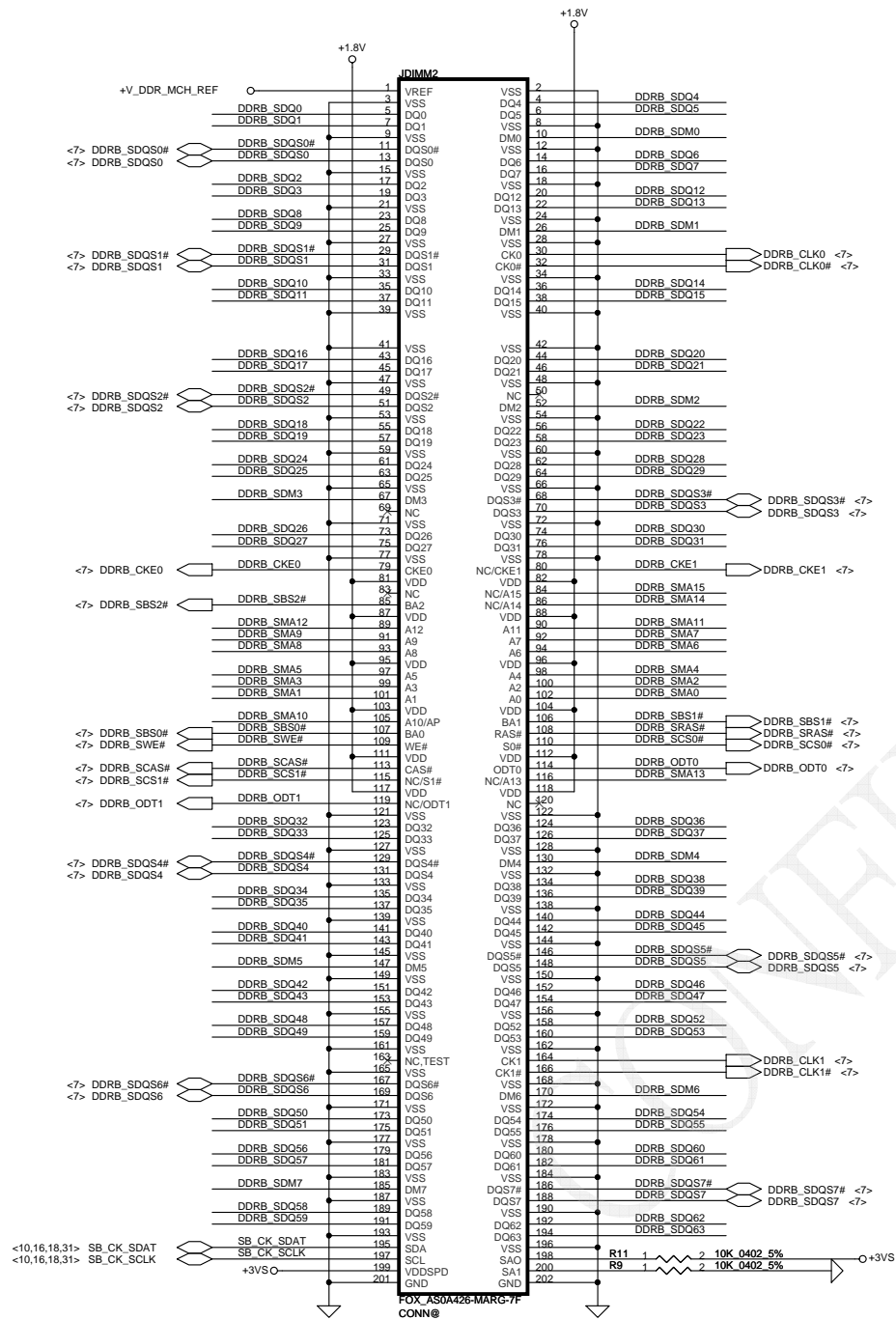
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Date:	Tuesday, October 13, 2009	Sheet	9	of	47	

RESERVE
+V_DDR_MCH_REF BUFFER CIRCUIT

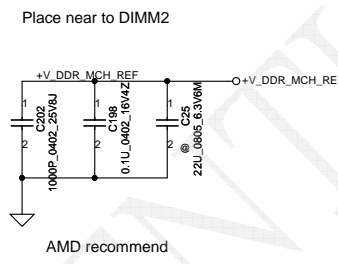
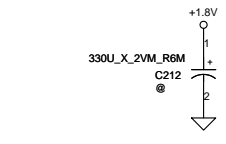
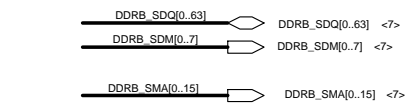


DIMM1 REV H:5.2mm (BOT)

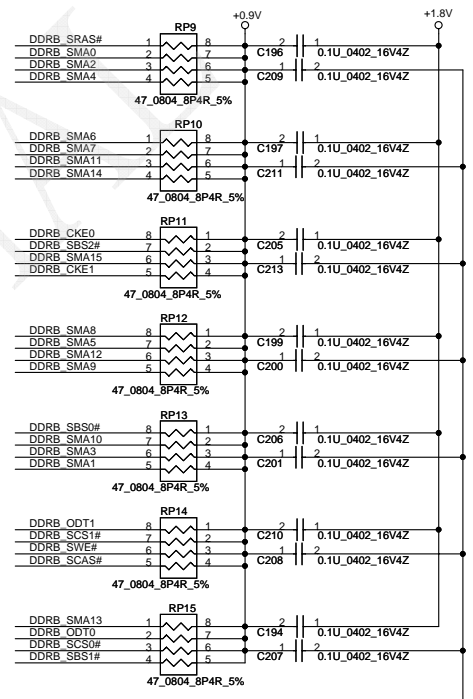
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Document Number	401830			Rev A
Date:	Tuesday, October 13, 2009	Sheet	10	of 47



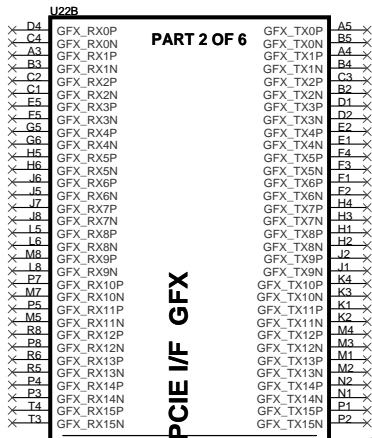
DIMM1 REV H:9.2mm (BOT)



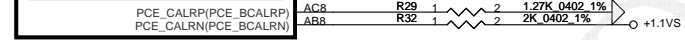
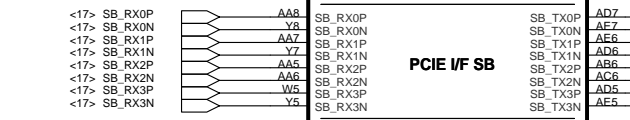
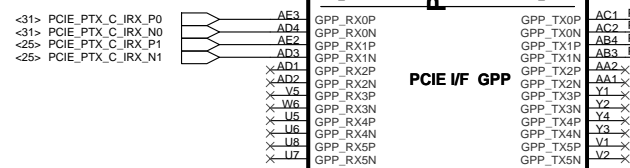
AMD recommend



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				401830	A
Date:				Tuesday, October 13, 2009	Sheet 11 of 47



Check SW Routing
 AN_RS780MN1. Only suggest pair0-3 can use for power save.

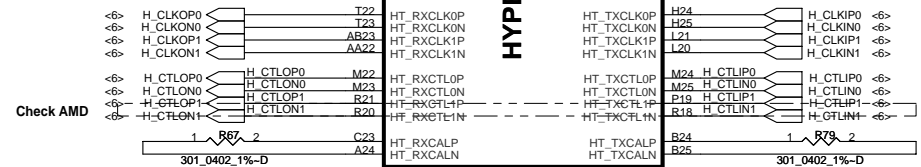
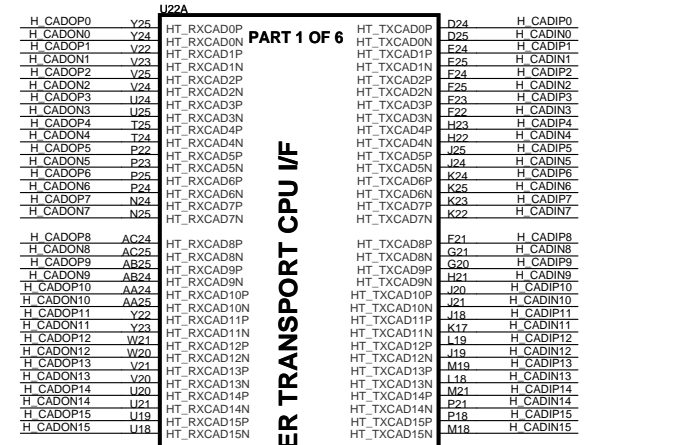
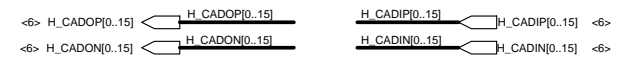


RS780M_FCBGA528
 RS780MN-SA00002DR30 Ver:A13

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

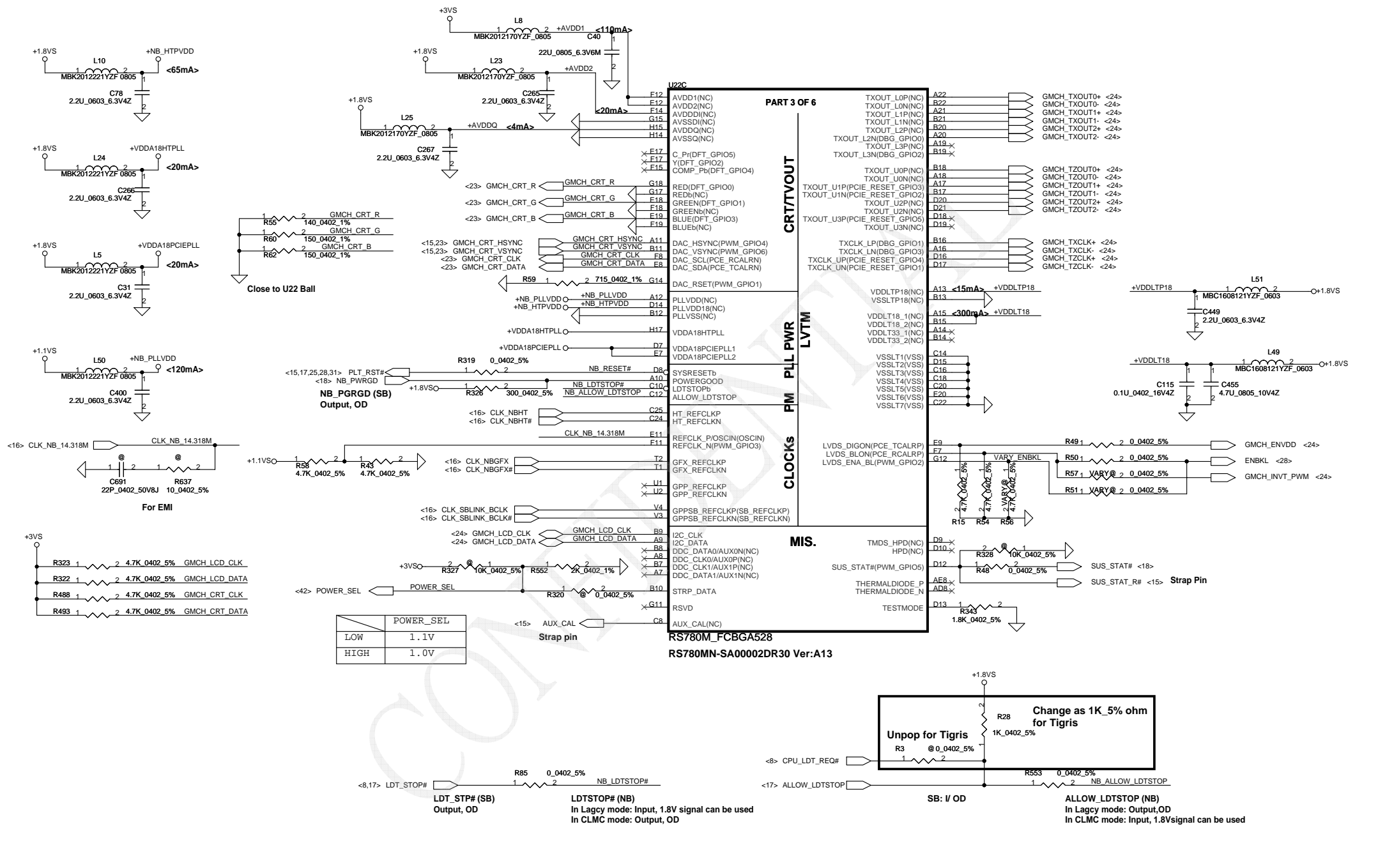
HT Link
 When tune trace length, must keep 1:4 on self-trace



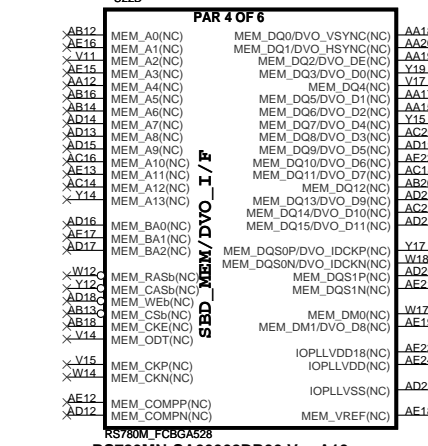
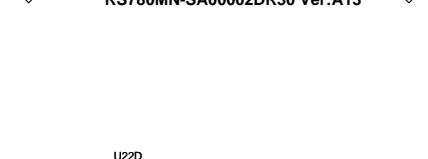
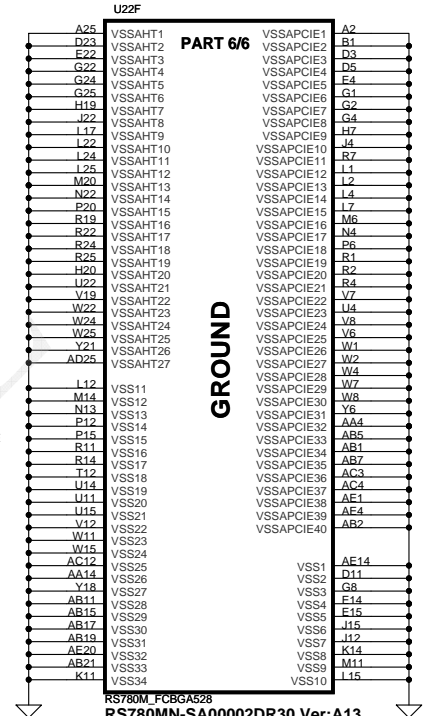
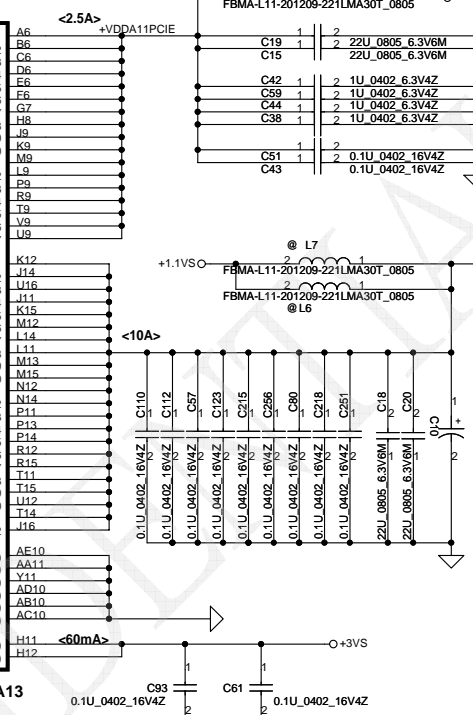
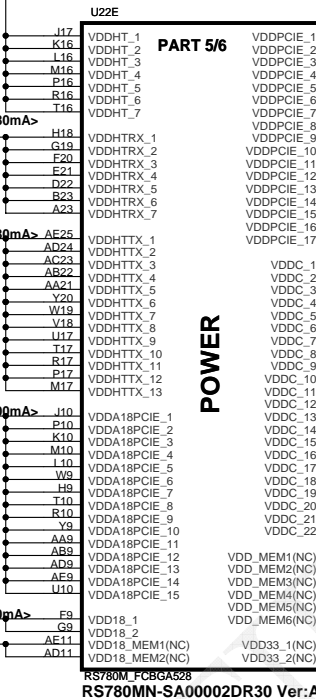
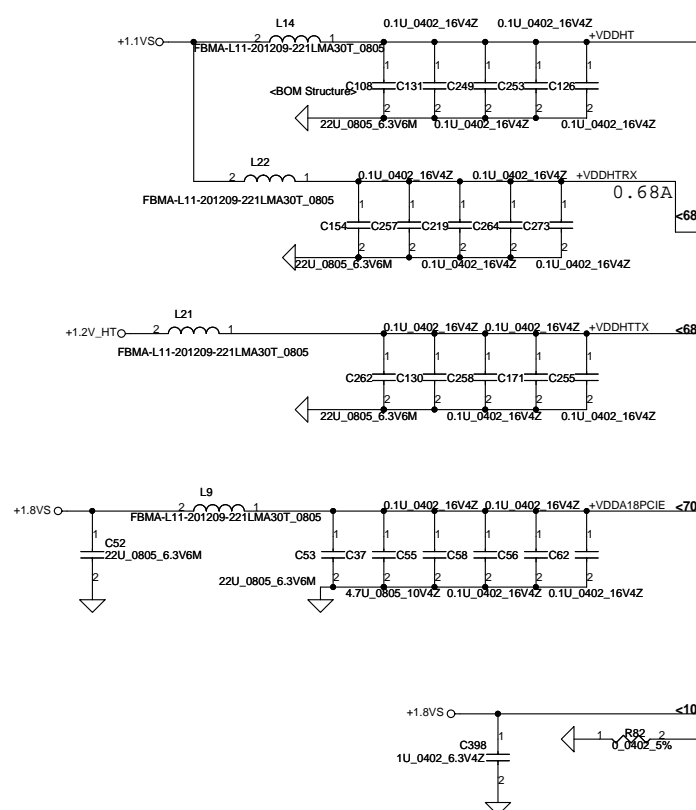
Place within 1" layout 4/8

Place within 1" layout 4/8

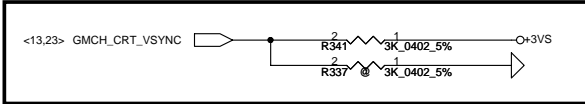
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Size	Document Number		Rev			
401830			A			
Date:	Wednesday, October 14, 2009		Sheet	12 of 47		



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Size	Custom	Document Number	401830	Rev A
Date:	Wednesday, October 14, 2009	Sheet	13	of 47

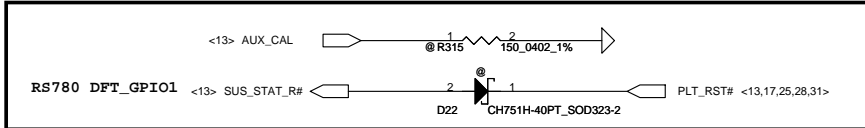


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Size	Customer	401830	Rev	A	
Date:	Wednesday, October 14, 2009	Sheet	14	of 47	



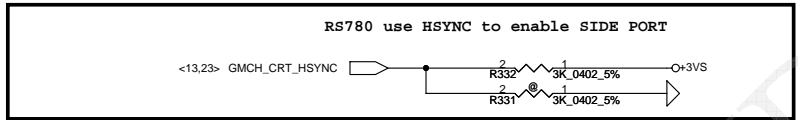
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS780)
 0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

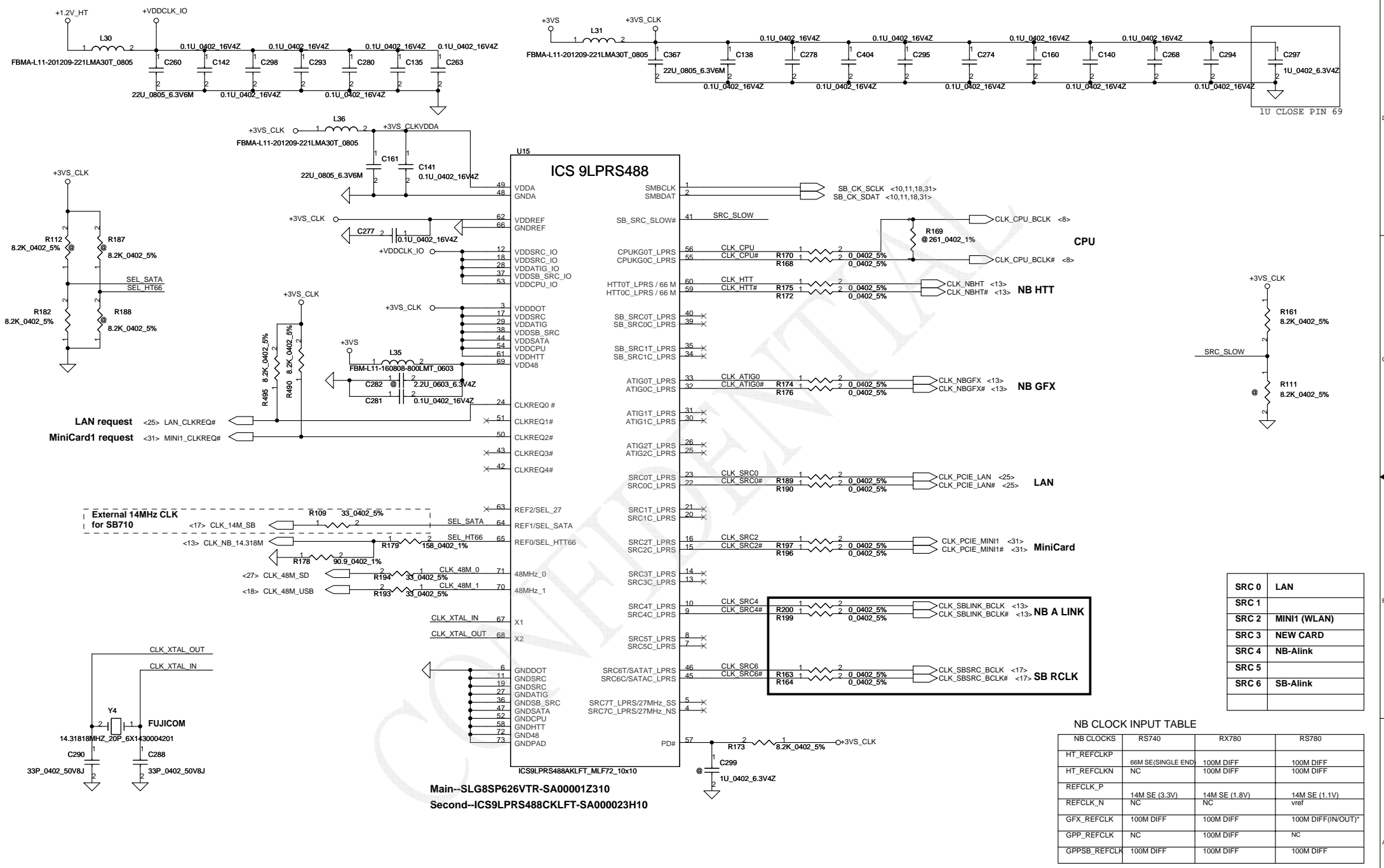


RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0 : Enable (RS780)
 1 : Disable(RS780)

CONFIDENTIAL

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				Custom	401830
				Date:	Wednesday, October 14, 2009
				Sheet	15 of 47
				Rev	A



Main-SLG8SP626VTR-SA00001Z310
 Second-ICS9LPRS488CLKLFT-SA000023H10

SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	NEW CARD
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

NB CLOCK INPUT TABLE

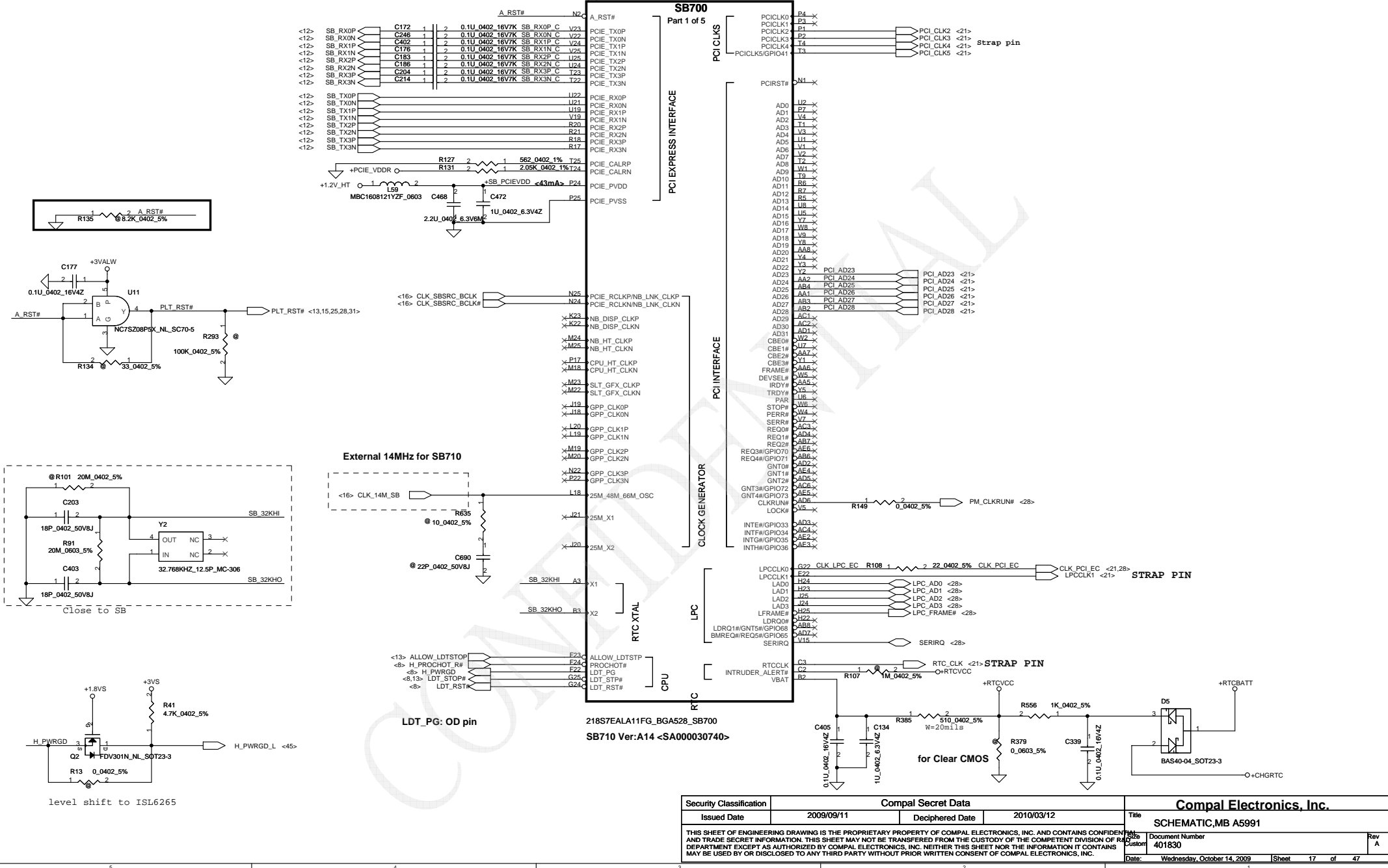
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	NC	NC	vref
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

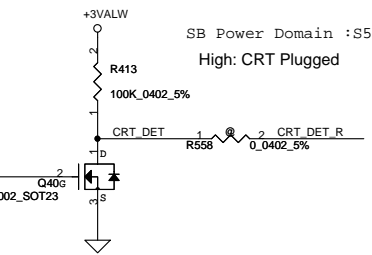
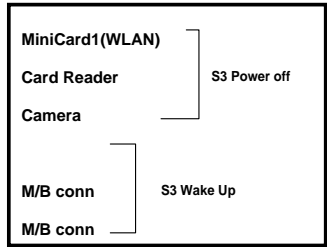
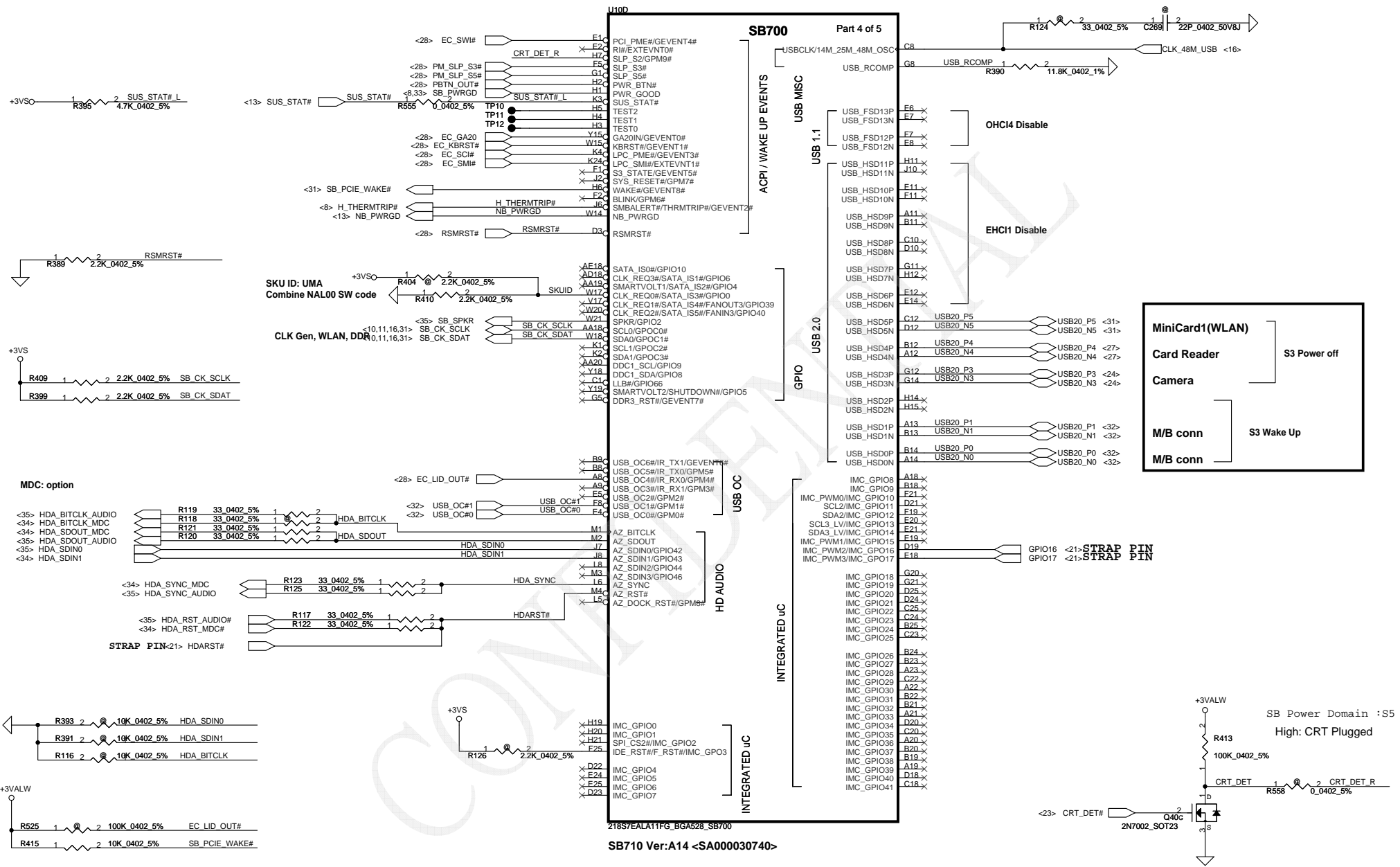
SEL_27M	1	configure as 27M and 27M_SS output
No used	0	configure as SRC_7 output

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Size	Custom
Document Number	401830
Rev	A
Date:	Wednesday, October 14, 2009
Sheet	16 of 47



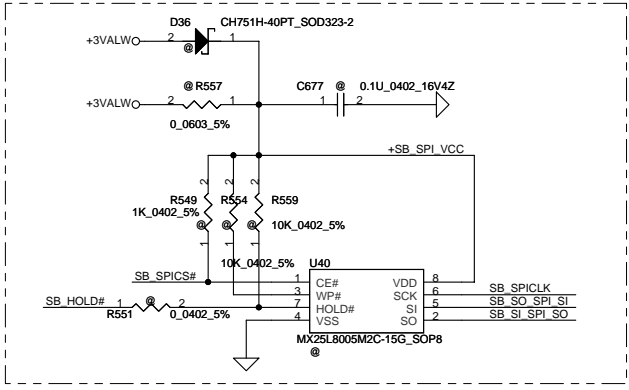
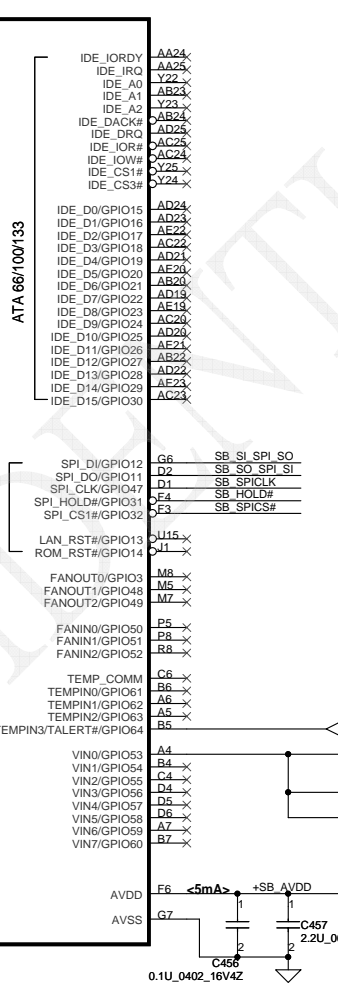
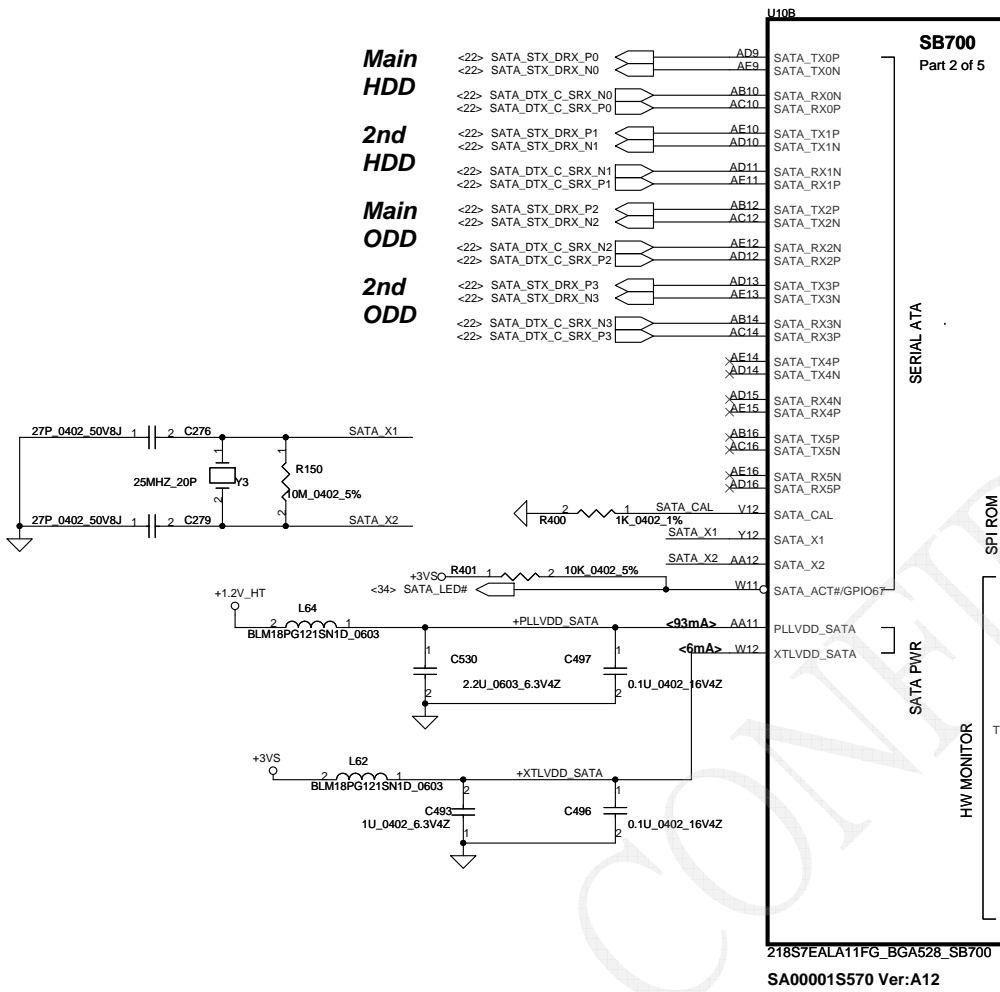
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				Rev A
				Sheet 17 of 47



SB710 Ver:A14 <SA000030740>

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401830	401830	A			
Date:	Wednesday, October 14, 2009	Sheet	18	of	47

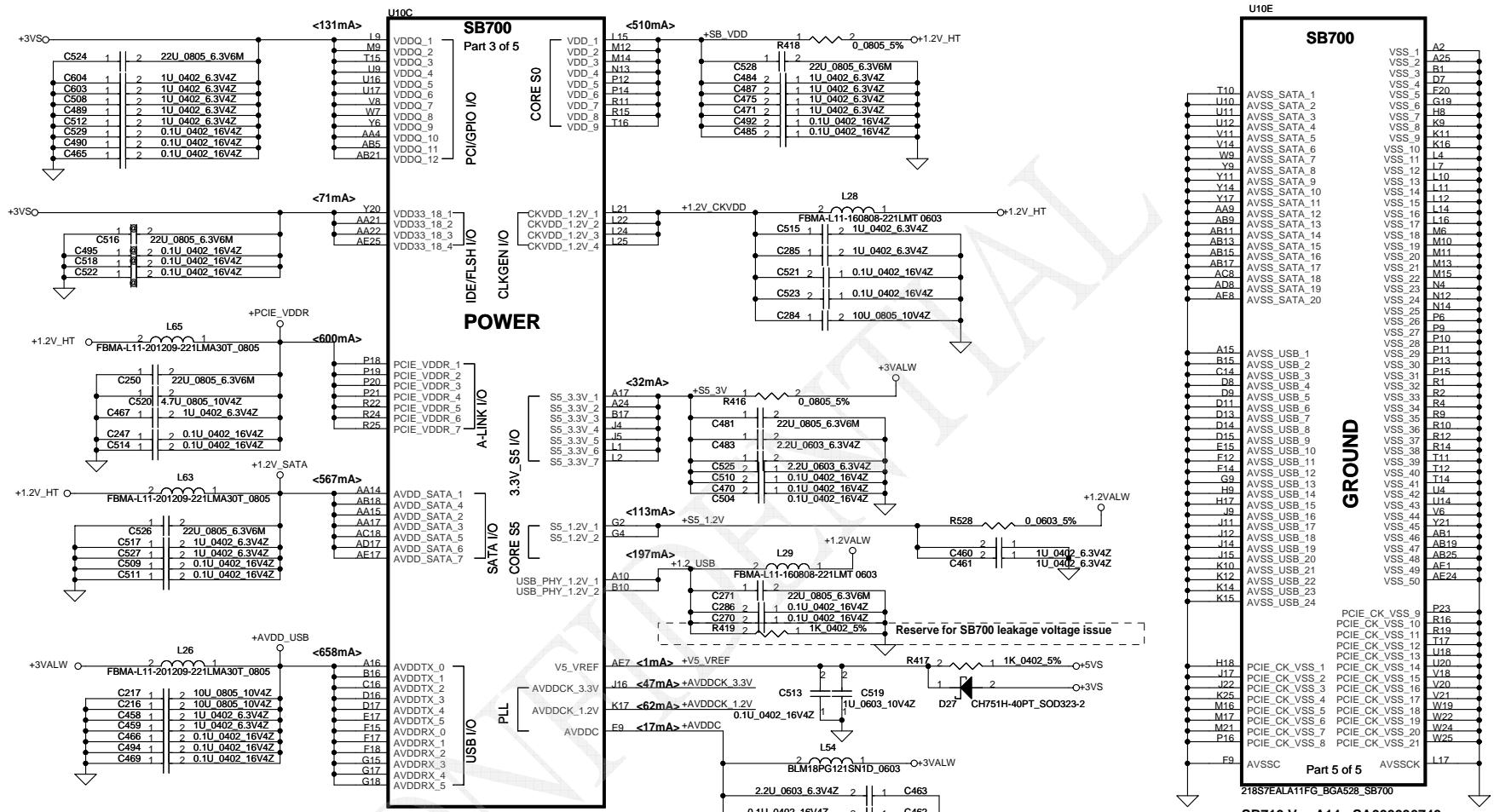
Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller



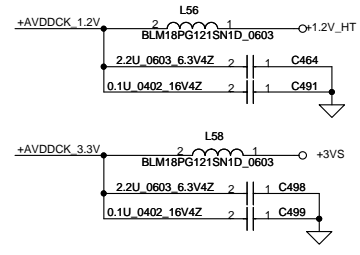
Reserve For Debug

for ACIN level issue

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Date:	Wednesday, October 14, 2009	Sheet	19	of	47



218S7EAL11FG_BGA528_SB700
SB710 Ver:A14 <SA000030740>

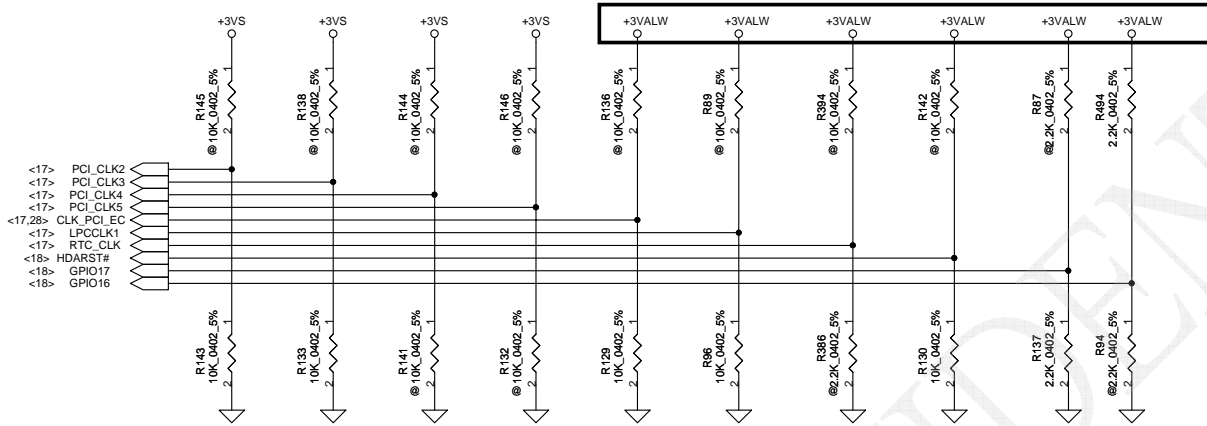


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				401830		A
Date:	Thursday, October 15, 2009	Sheet	20	of 47		

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	

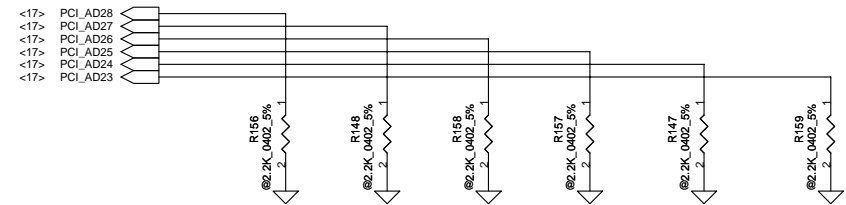


DEBUG STRAPS

DEBUG STRAPS

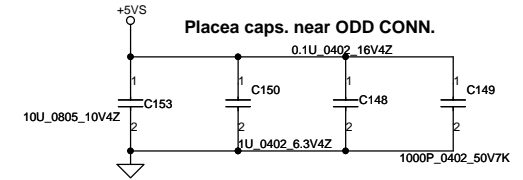
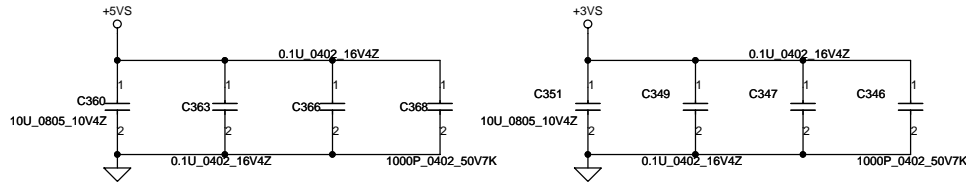
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



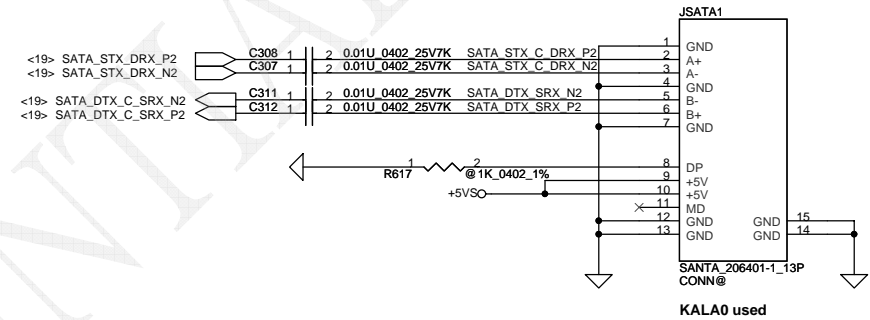
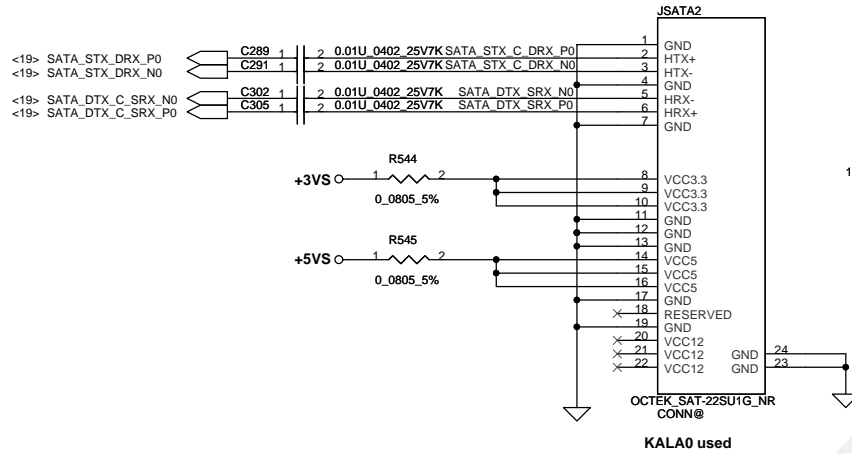
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Date:	Thursday, October 15, 2009	Sheet	21	of	47

Rev A



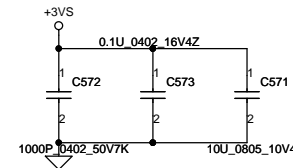
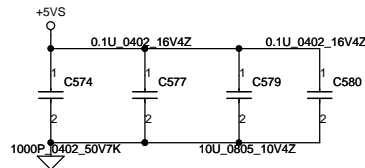
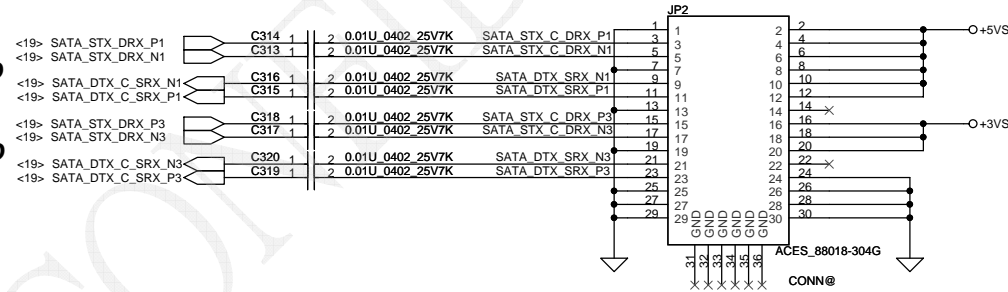
SATA HDD CONN

SATA ODD CONN



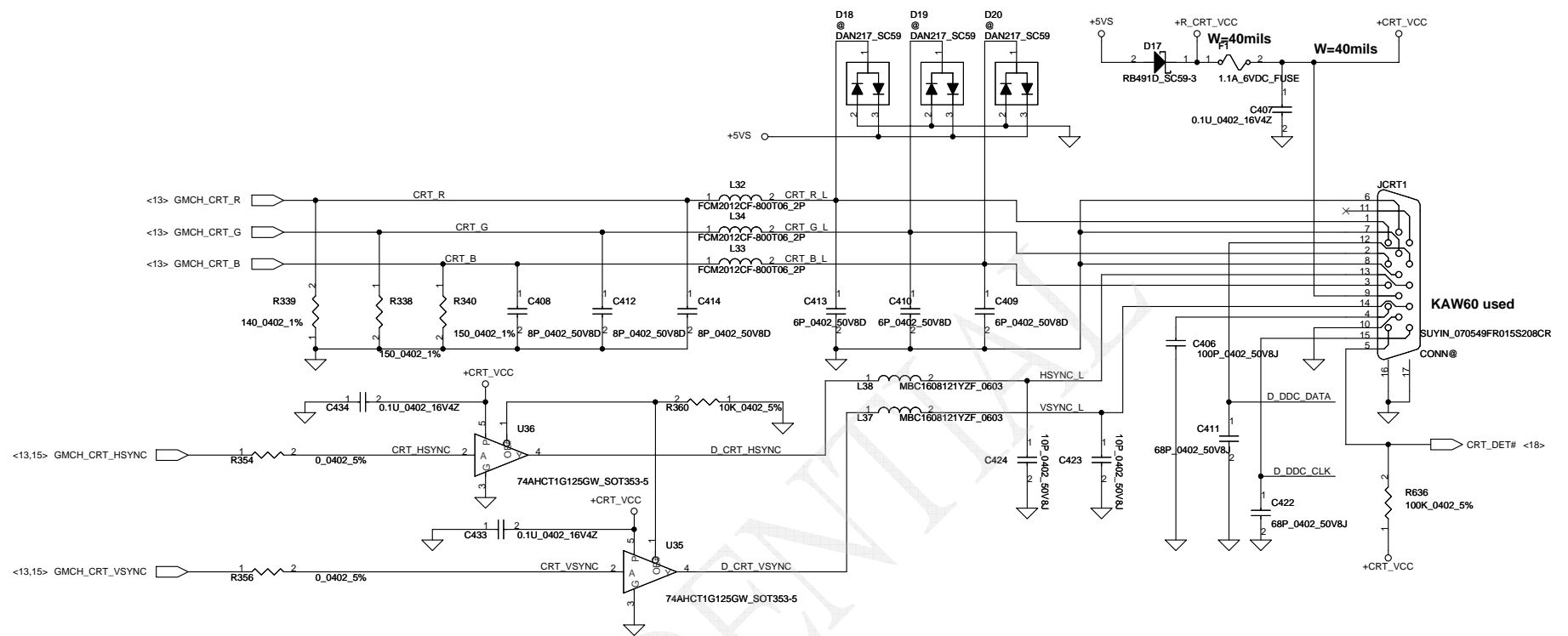
Second HDD

Second ODD

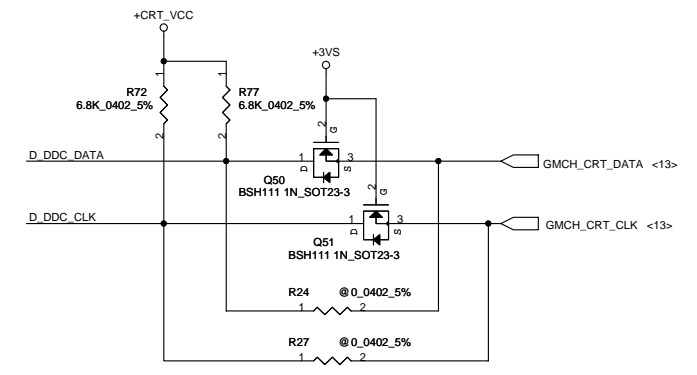


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Size	Document Number	Date	Thursday, October 15, 2009	Sheet	22 of 47
B	401830	Rev	A		

CRT Connector

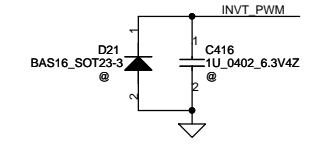
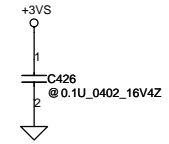
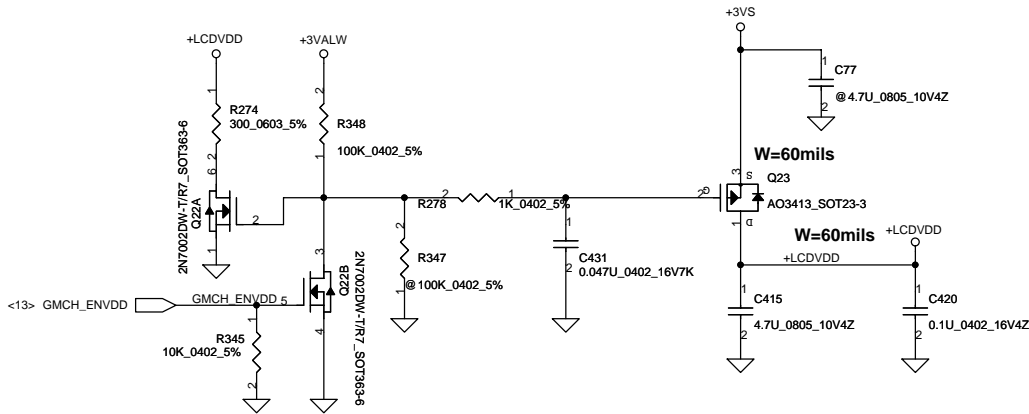


Close to Conn side

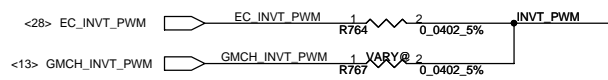
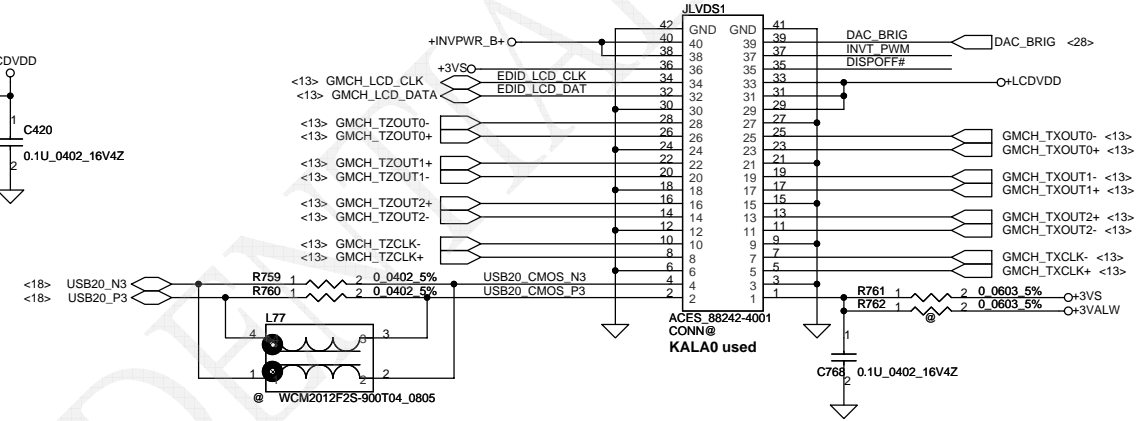


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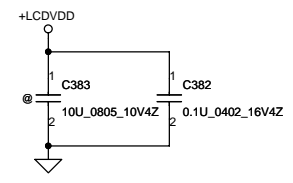
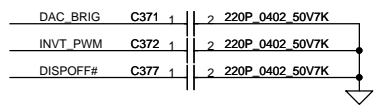
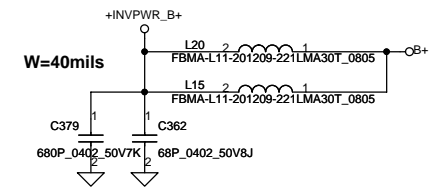
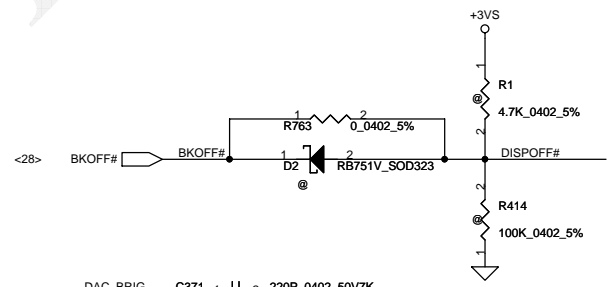
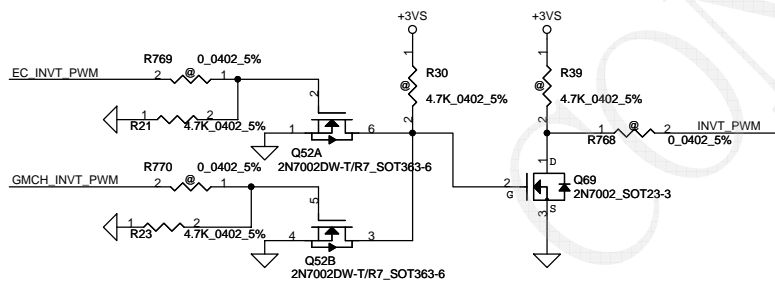
LCD POWER CIRCUIT



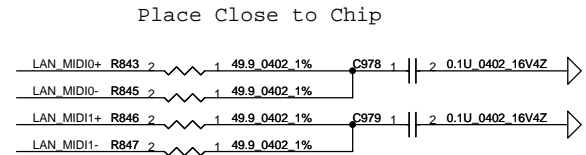
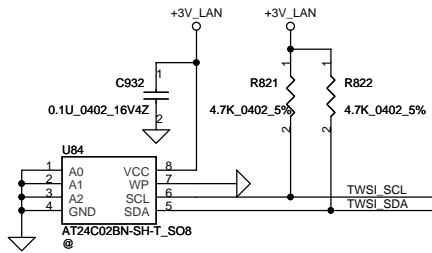
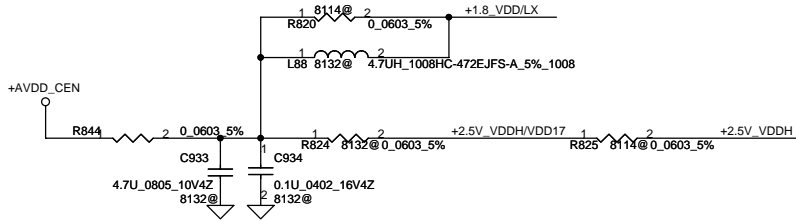
LCD/PANEL CONN.



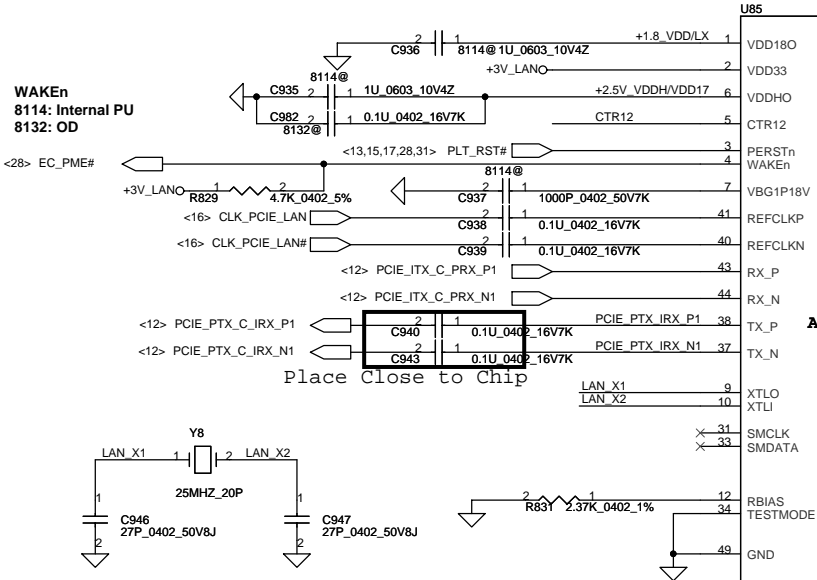
VARYBRIGHT FUNCTION



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				Document Number	A
				401830	
				Date:	Thursday, October 15, 2009
				Sheet	24 of 47



WAKEn
8114: Internal PU
8132: OD

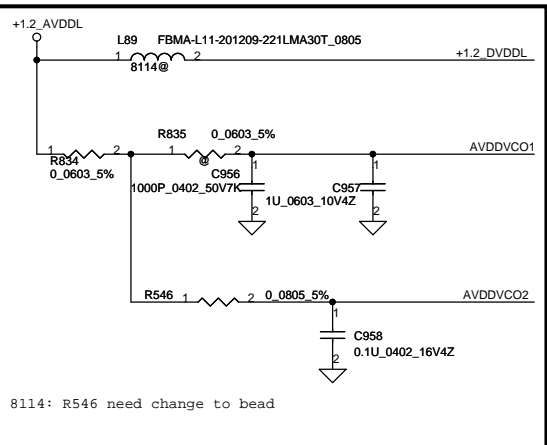
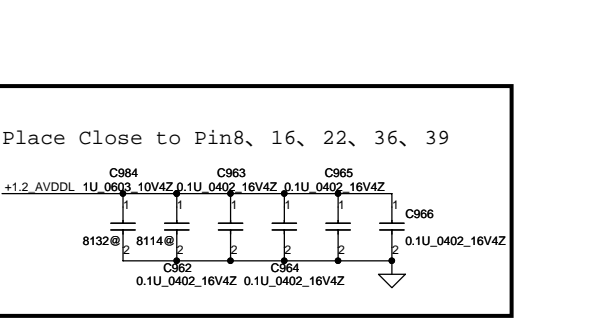
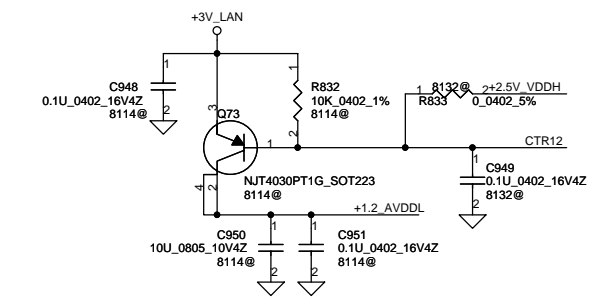
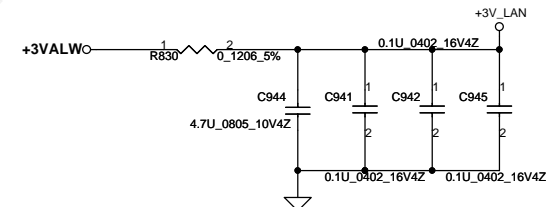


Atheros
AR8114A 10/100 LAN

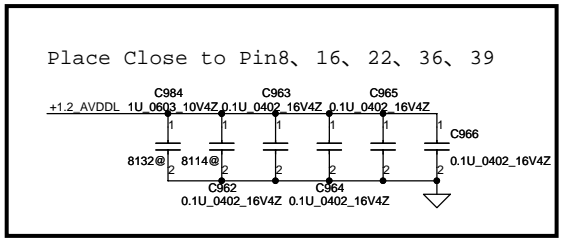
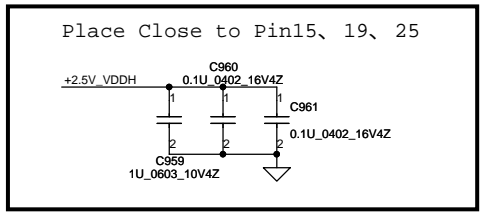
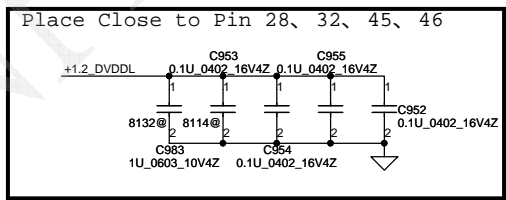
change to AR8132L-AL1E

Place Close to Chip

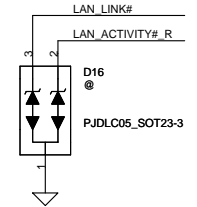
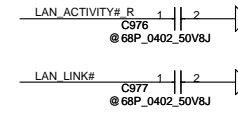
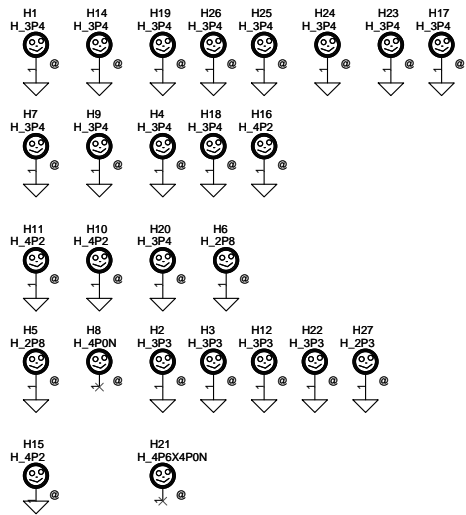
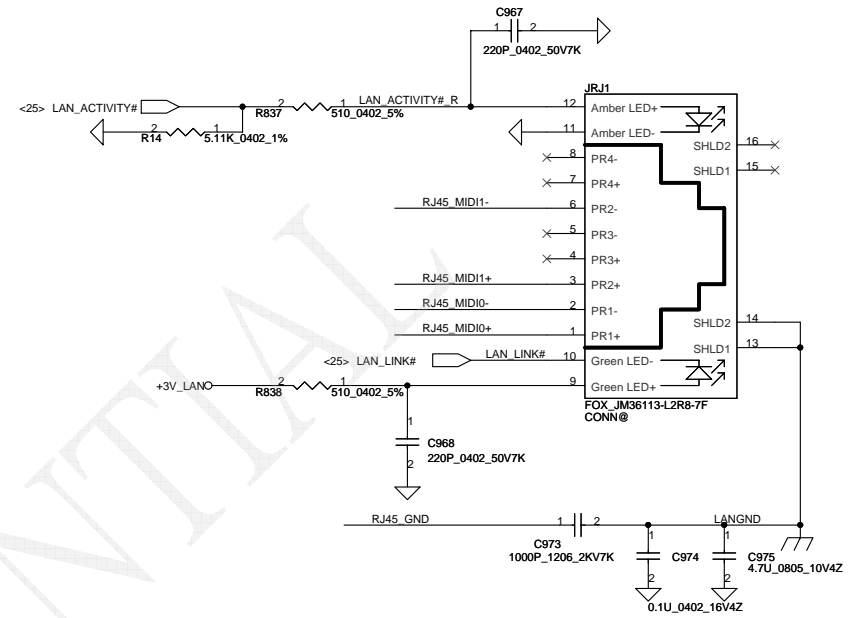
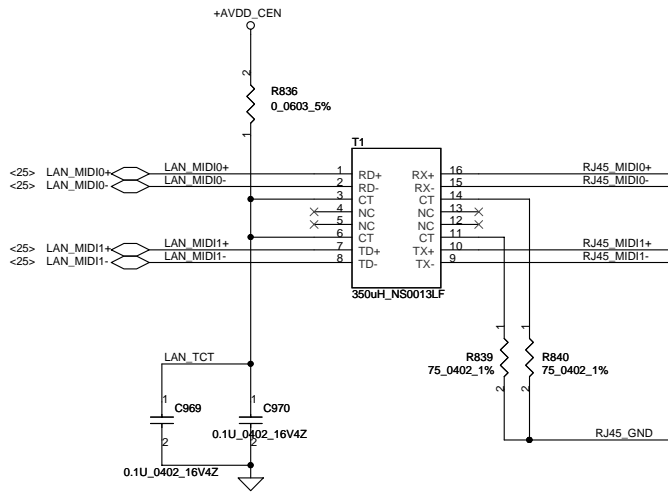
Layout Notice : Close to chip



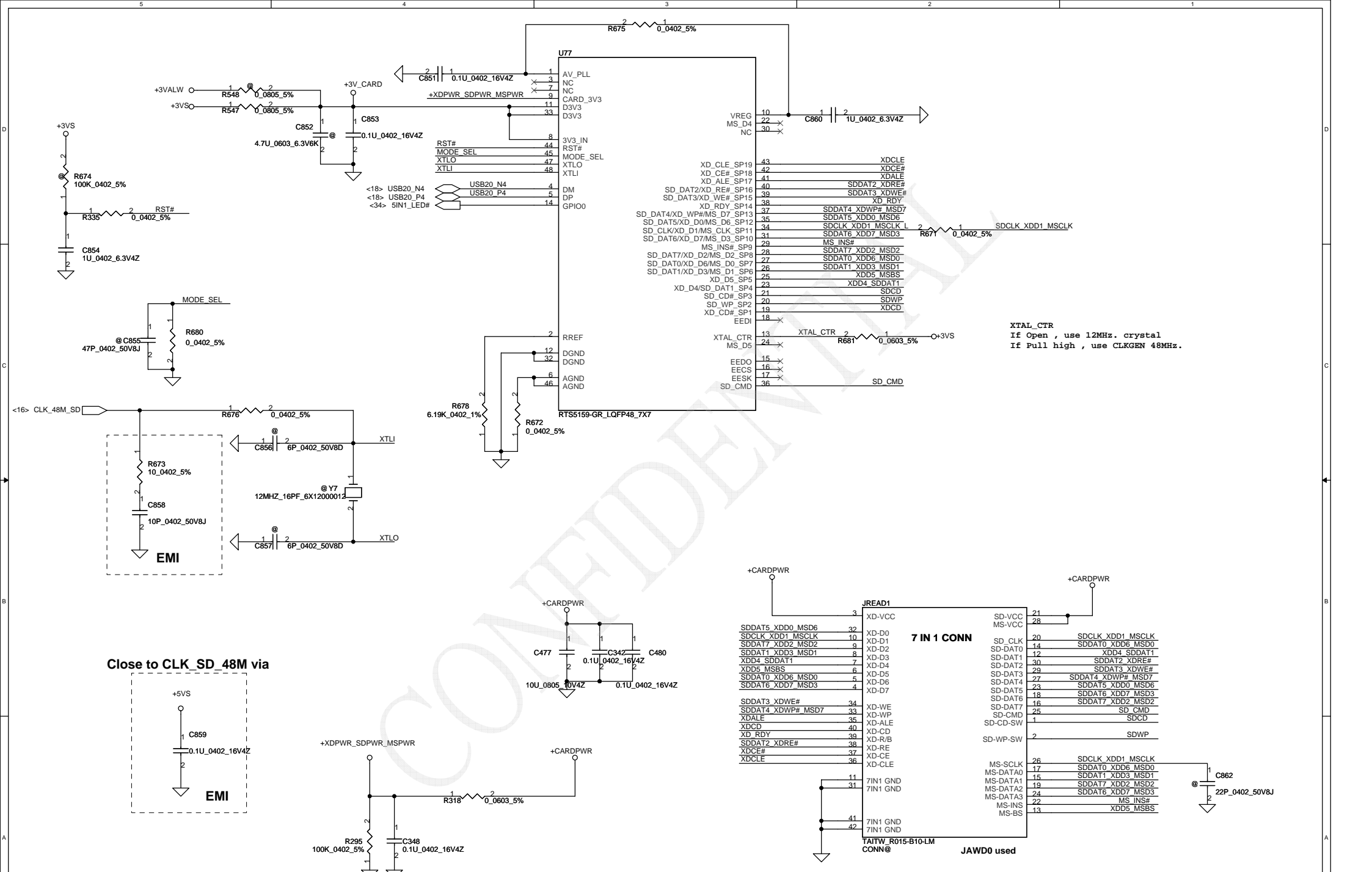
8114: R546 need change to bead



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				401830	A
Date: Thursday, October 15, 2009				Sheet	25 of 47



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Date:	Thursday, October 15, 2009	Sheet	26	of	47



XTAL_CTR
 If Open , use 12MHz. crystal
 If Pull high , use CLKGEN 48MHz.

Close to CLK_SD 48M via

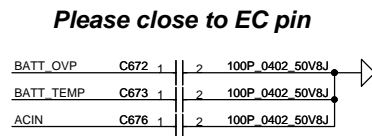
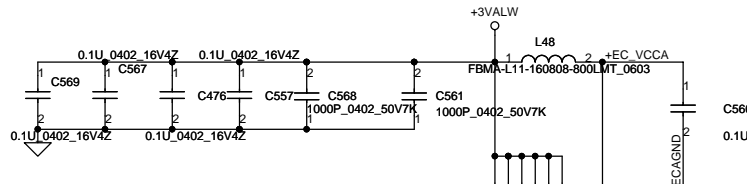
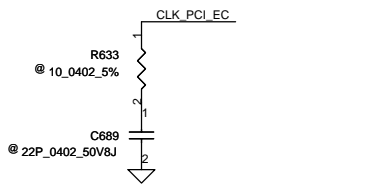
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Size	Document Number	Date:	Thursday, October 15, 2009	Sheet	27 of 47
B	401830				

Compal Electronics, Inc.

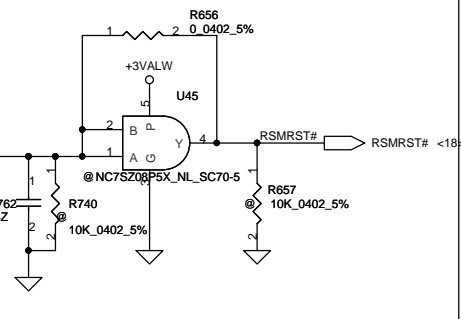
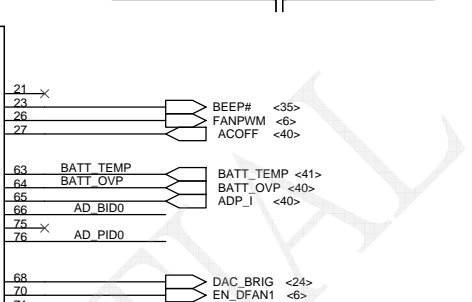
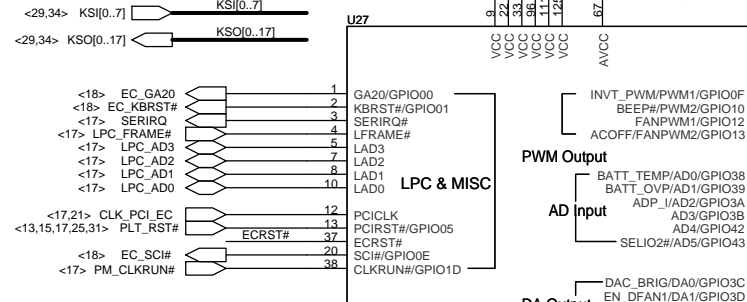
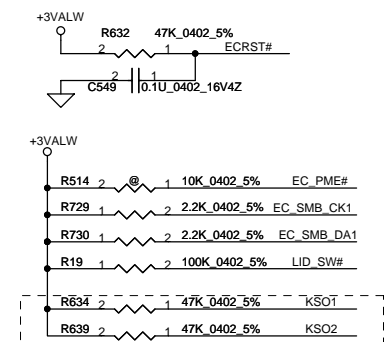
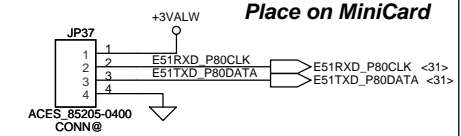
SCHEMATIC,MB A5991

401830

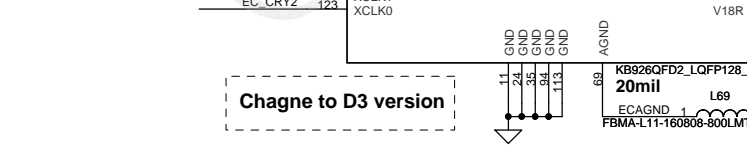
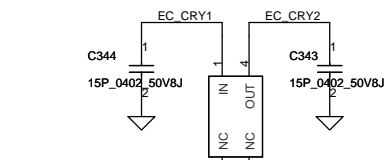
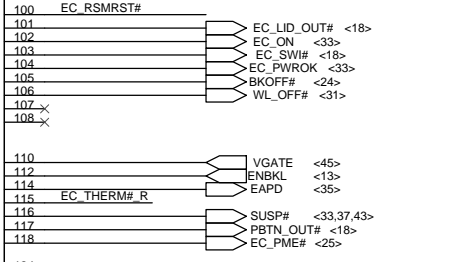
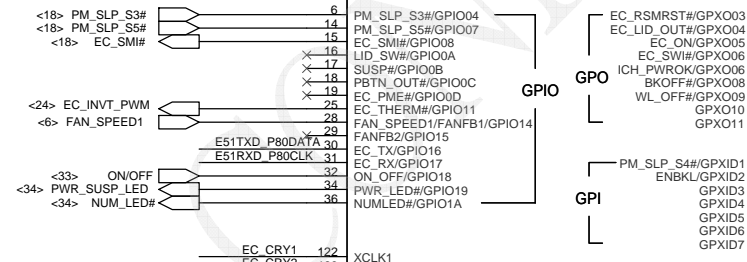
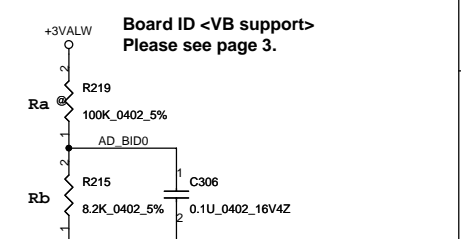
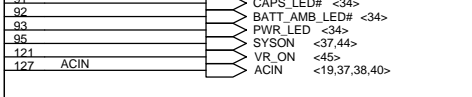
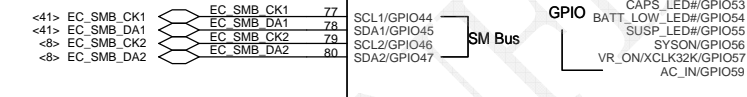
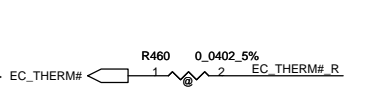
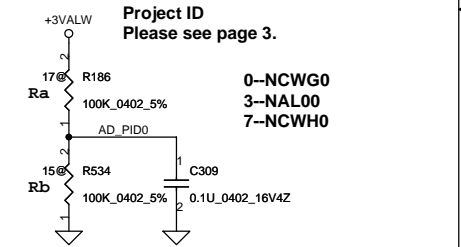
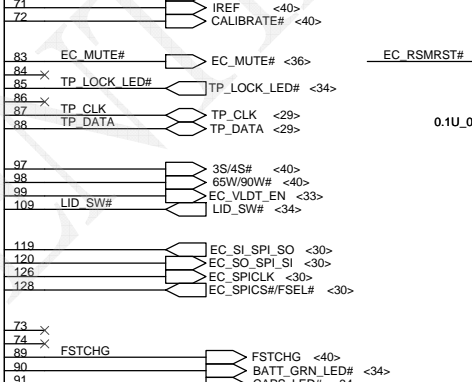
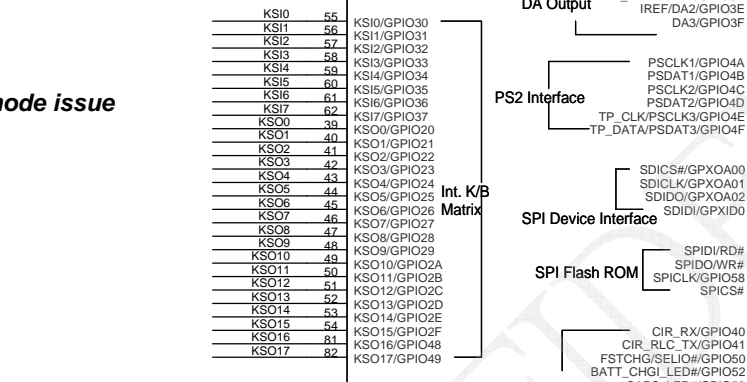
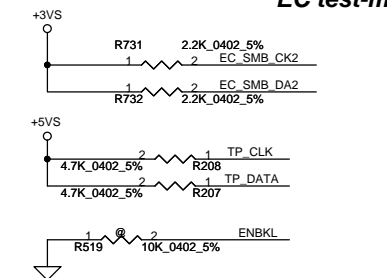
Thursday, October 15, 2009 Sheet 27 of 47



For EC Tools



EC test-mode issue

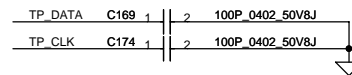
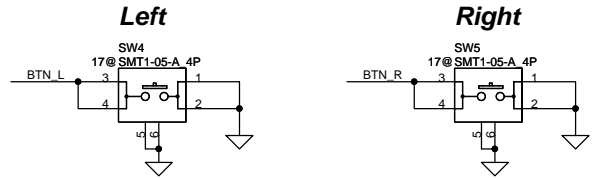


Chagne to D3 version

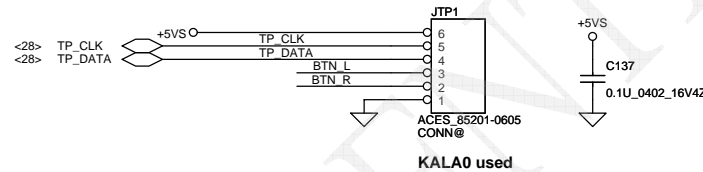
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				401830	A
Date: Thursday, October 15, 2009				Sheet	28 of 47

32.768KHZ_12.5P_MC-306

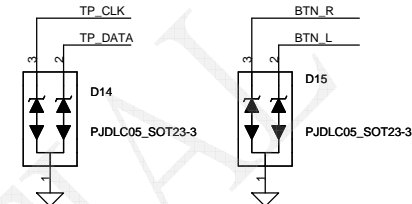
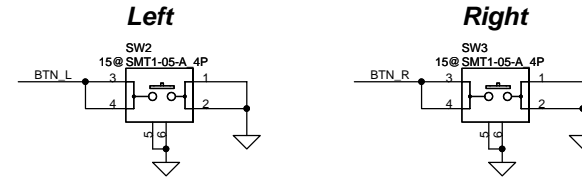
For 17"



To TP/B Conn.

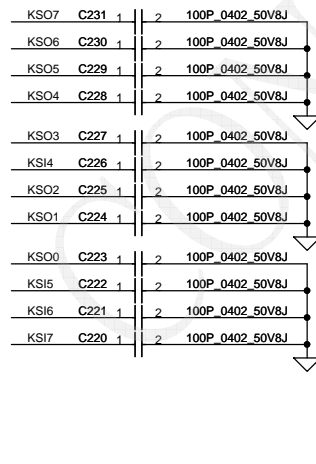
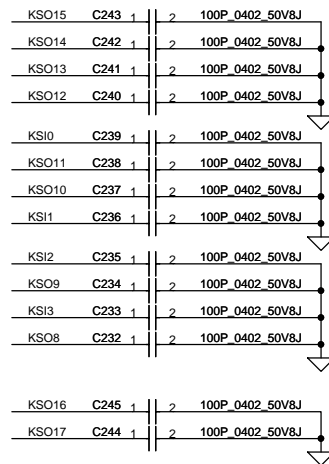


For 15"

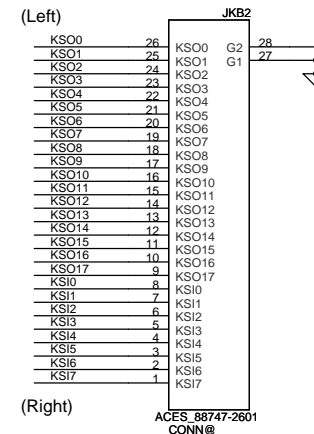
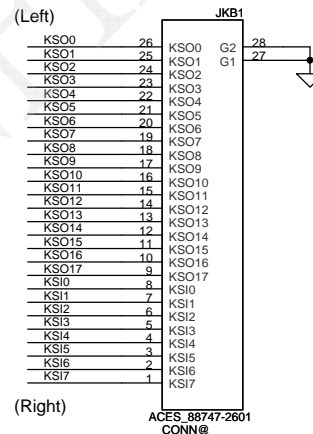


Change to SCA00000200

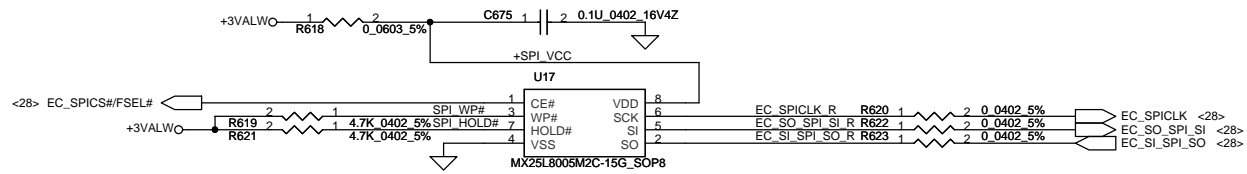
INT_KBD Conn.



KB1 for 15"
KB2 for 17"

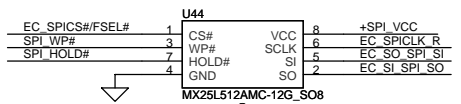
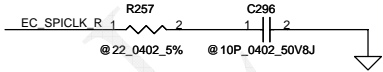


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Date: Thursday, October 15, 2009			Sheet 29 of 47	Rev A



SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

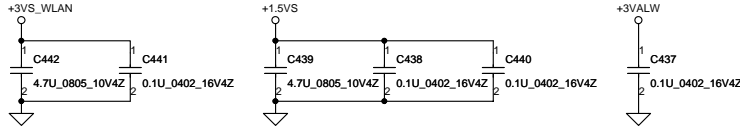
ONLY MXIC used in this project (66MHz)



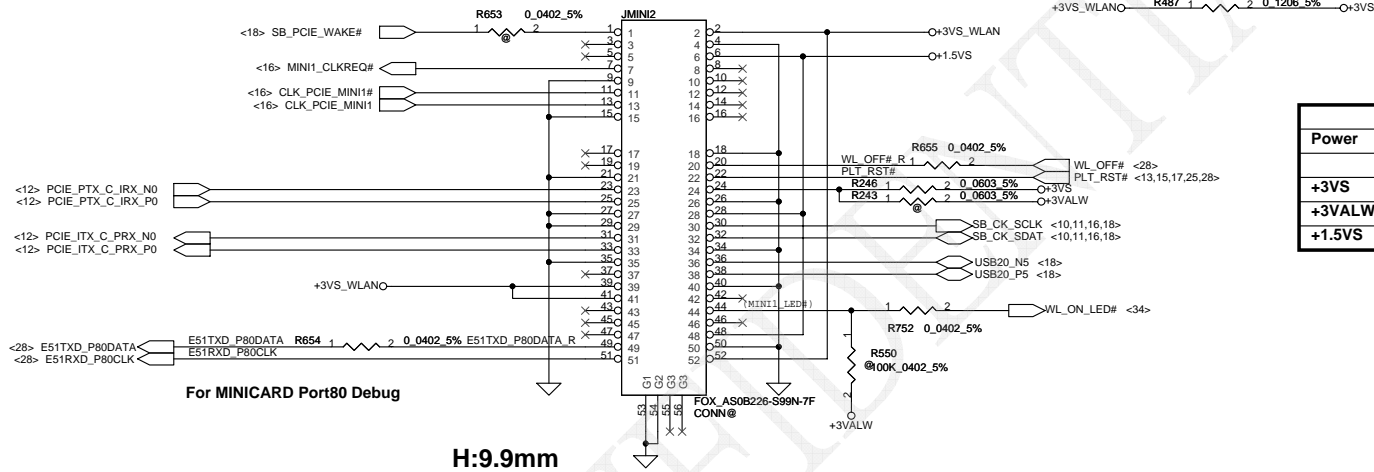
Reserved for BIOS simulator.
 Footprint S08
 SPI ROM Footprint 150mil

CONFIDENTIAL

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				401830
				Rev A
Date:		Monday, October 19, 2009	Sheet	30 of 47

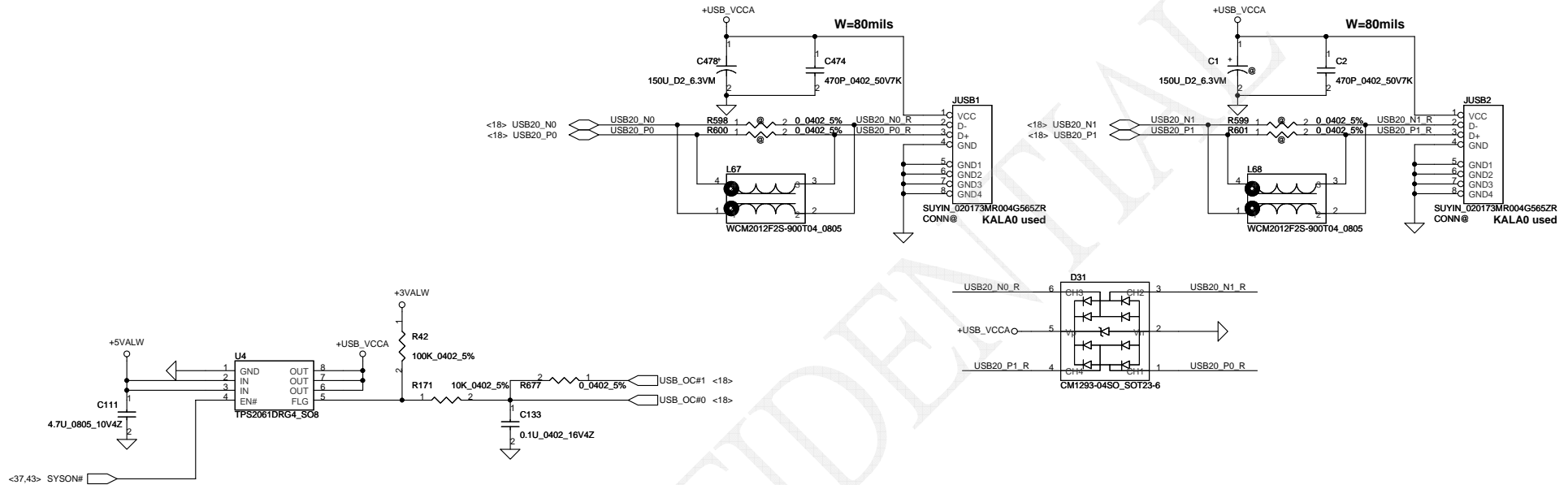


For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

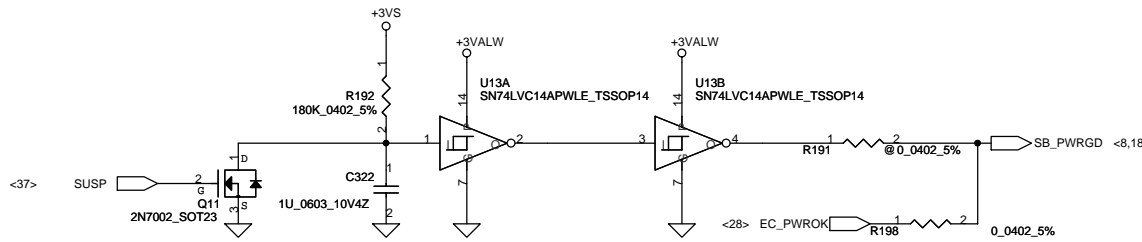
USB CONN. 1 & 2



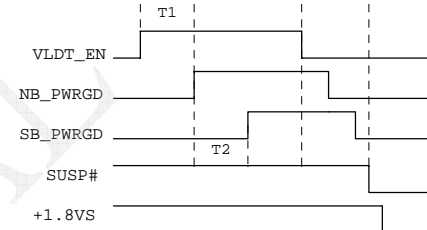
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				401830	A
Date:				Thursday, October 15, 2009	Sheet 32 of 47

Power ON Circuit

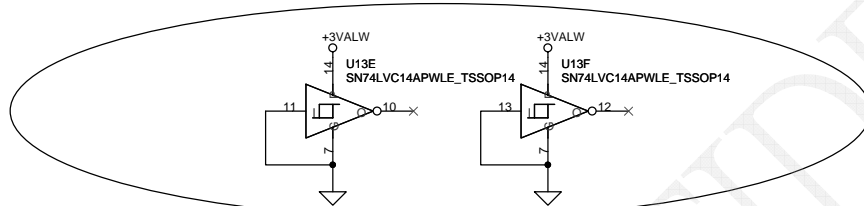
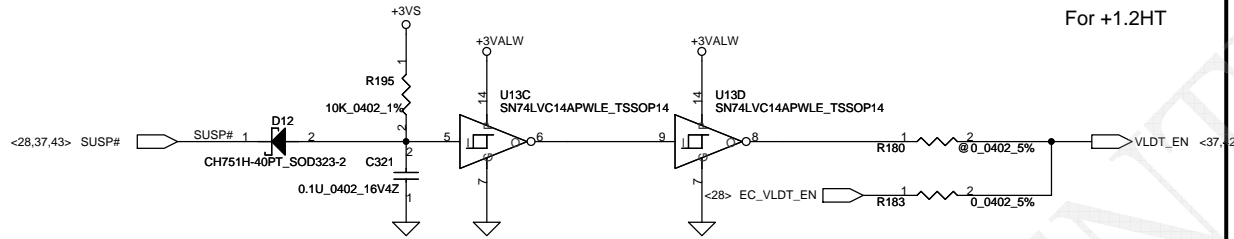
For South Bridge



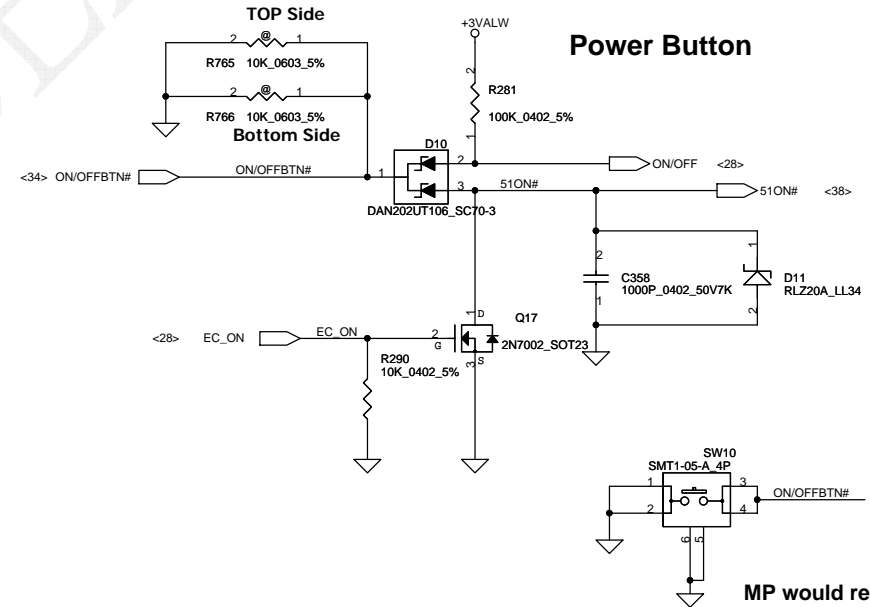
note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



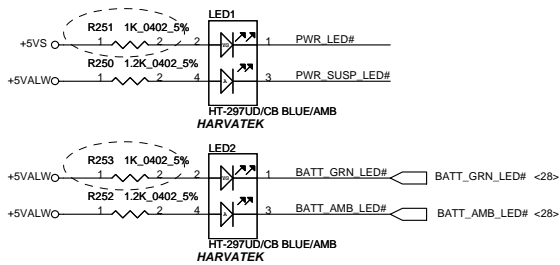
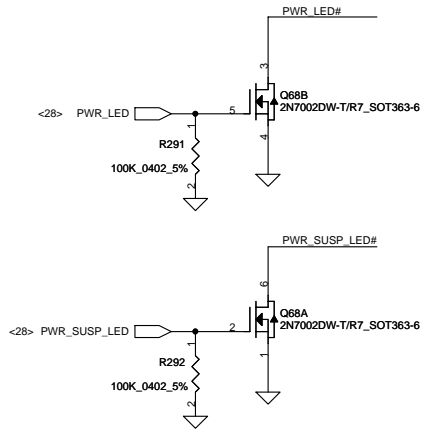
For +1.2HT



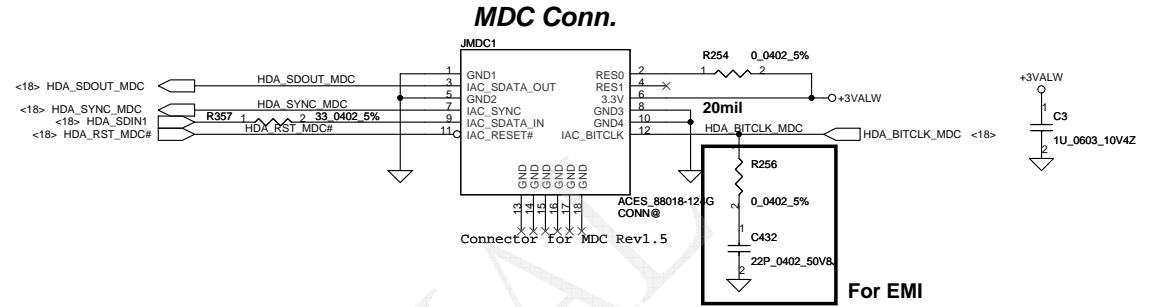
Power Button



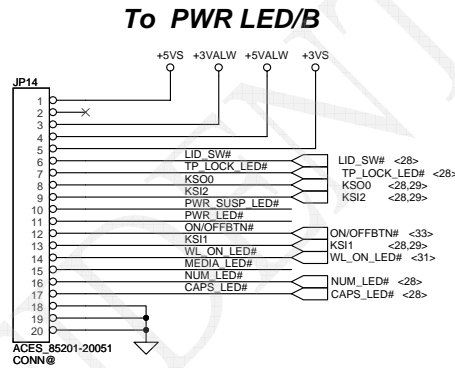
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Size	B	Document Number	401830	Rev	A
Date:	Monday, October 19, 2009	Sheet	33	of	47



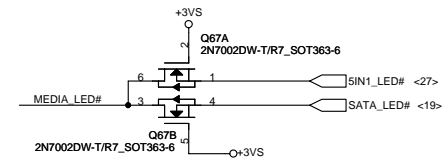
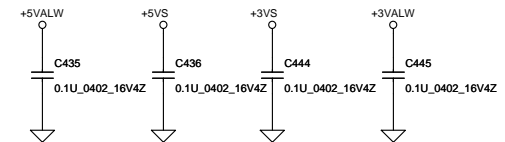
BLUE/AMB LED



For EMI

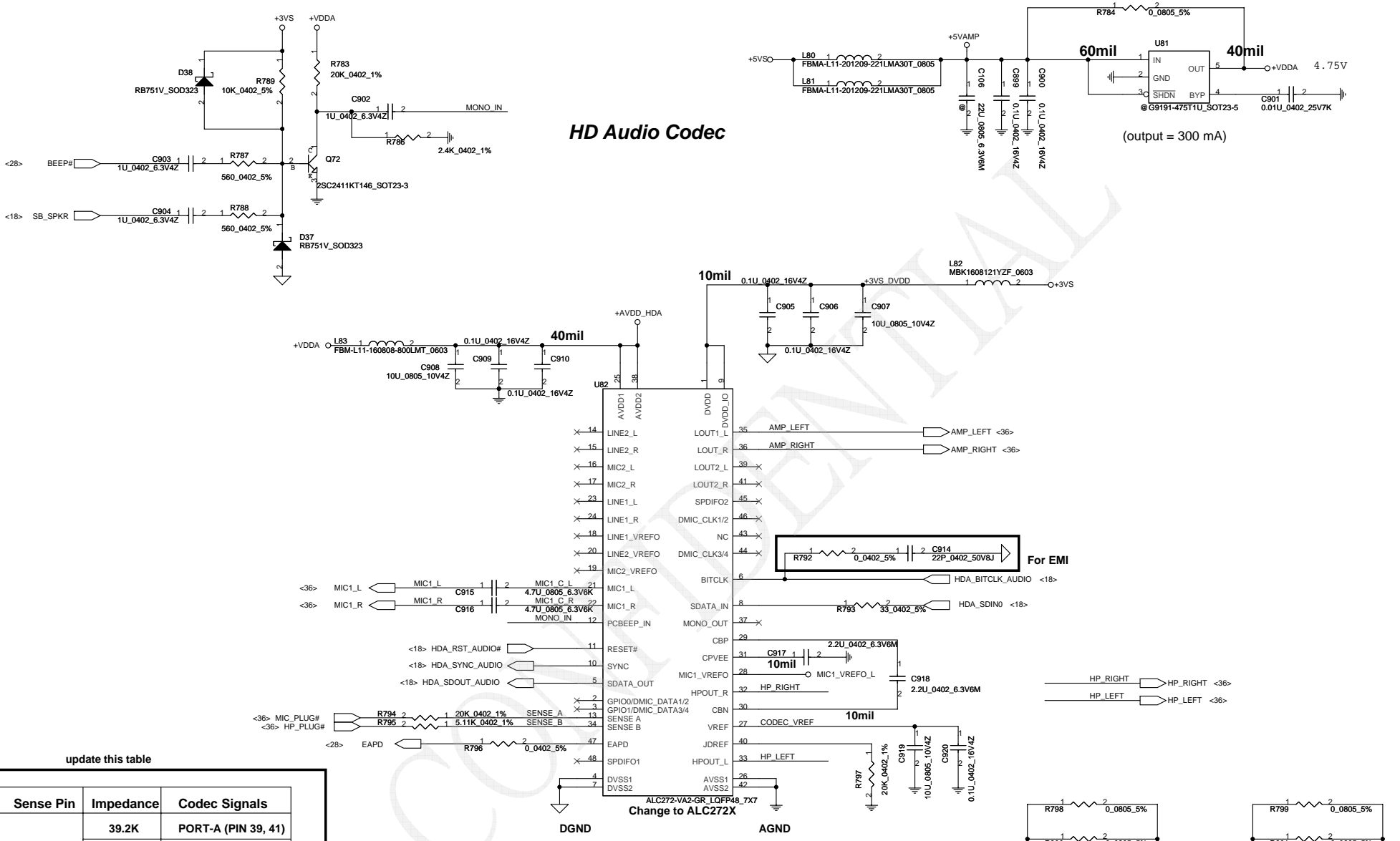


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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				401830
Date: Thursday, October 15, 2009				Sheet 34 of 47

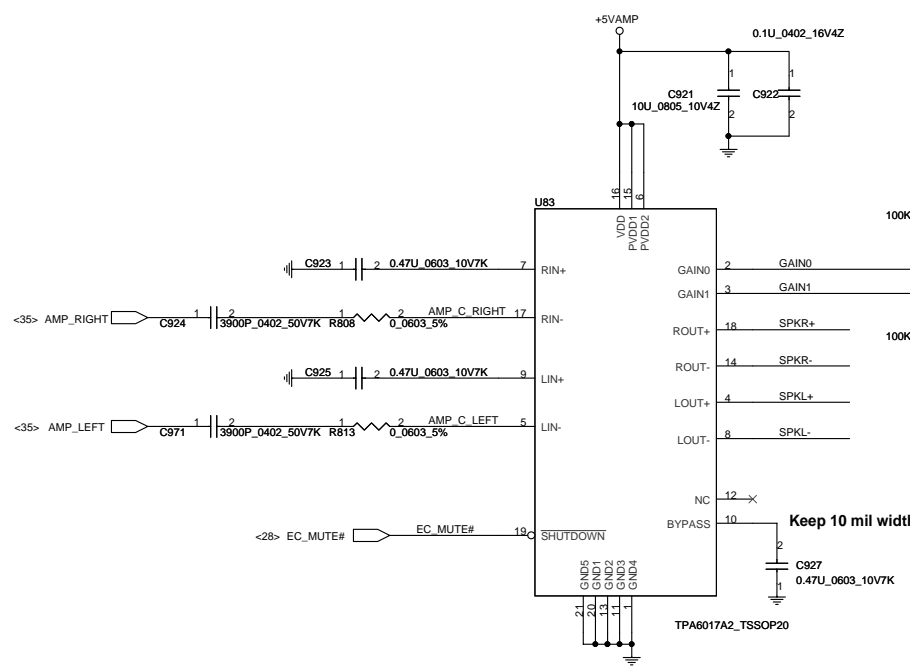
HD Audio Codec



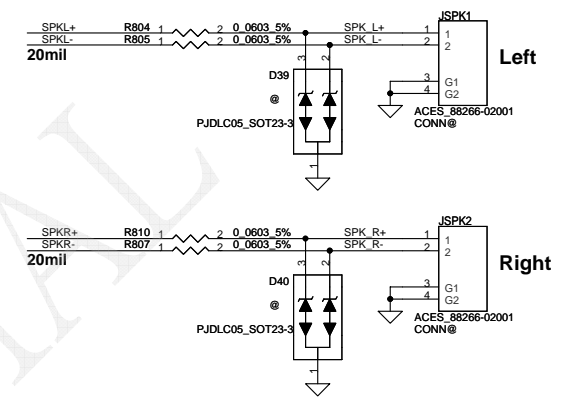
update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

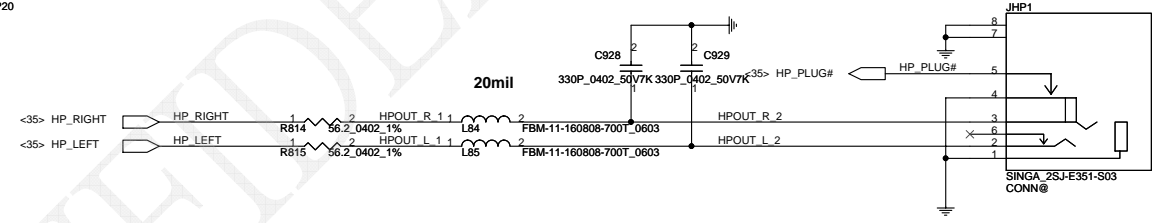
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				Document Number	401830
				Date:	Thursday, October 15, 2009
				Sheet	35 of 47



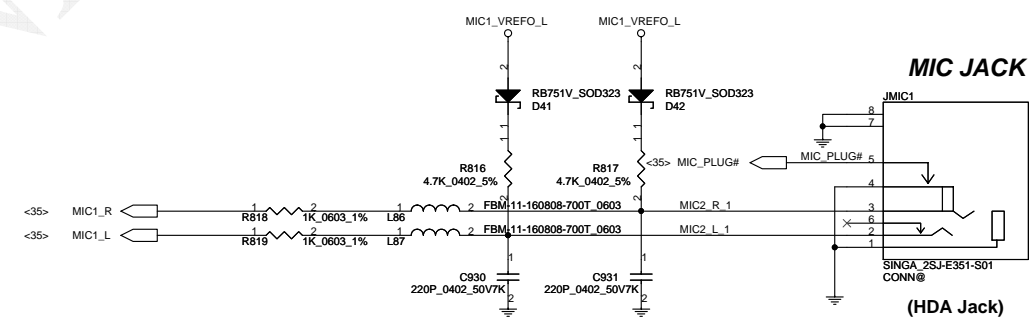
Int. Speaker Conn.



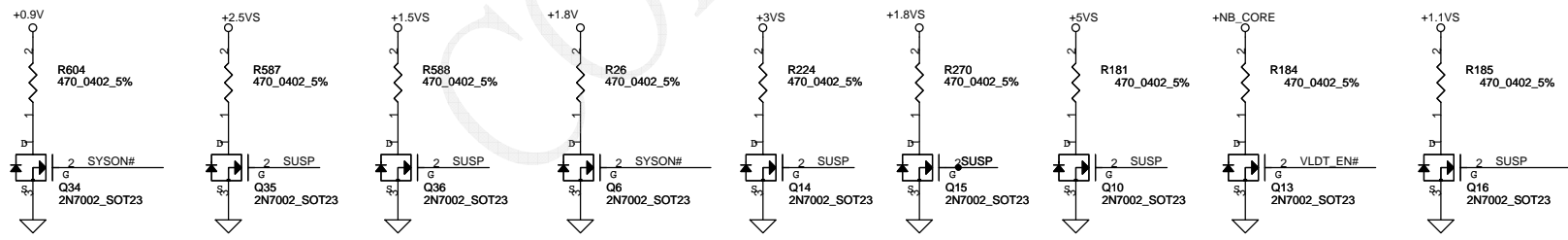
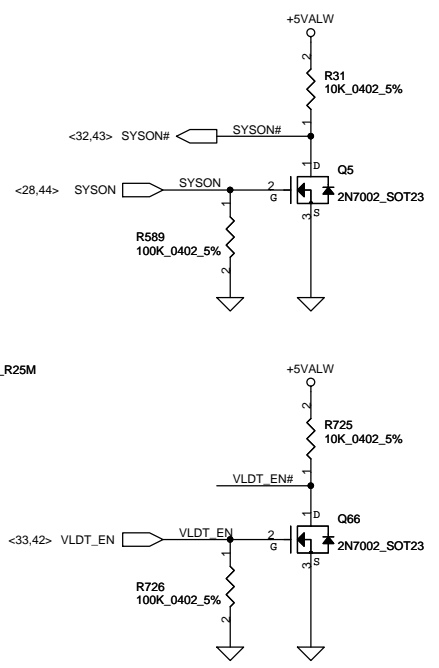
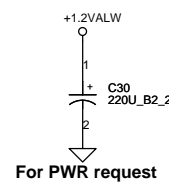
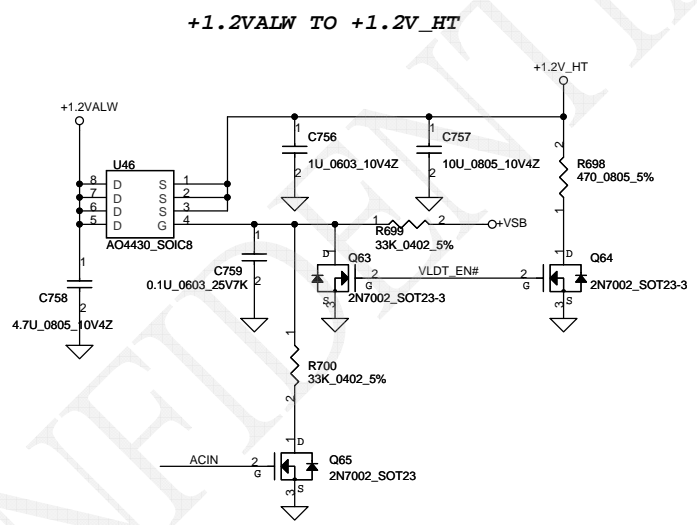
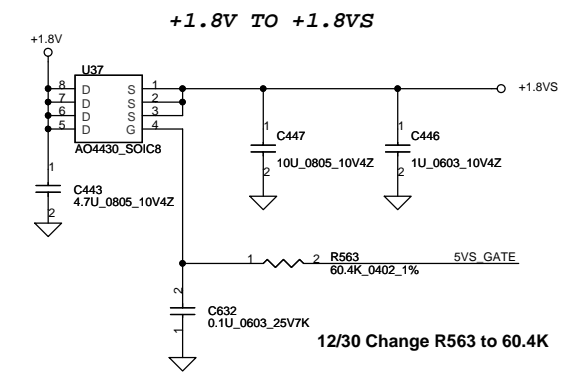
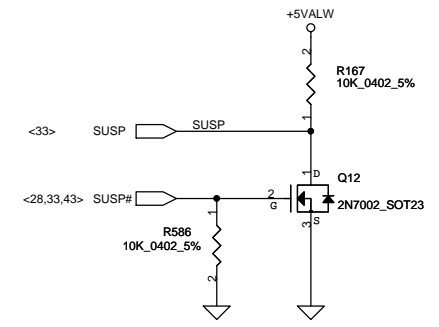
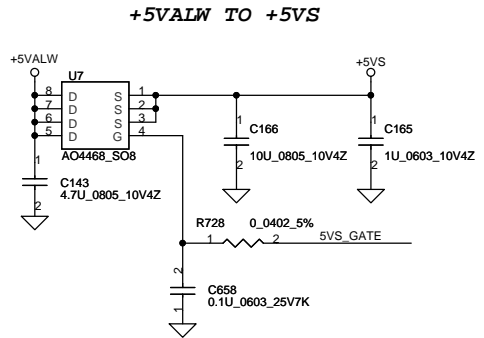
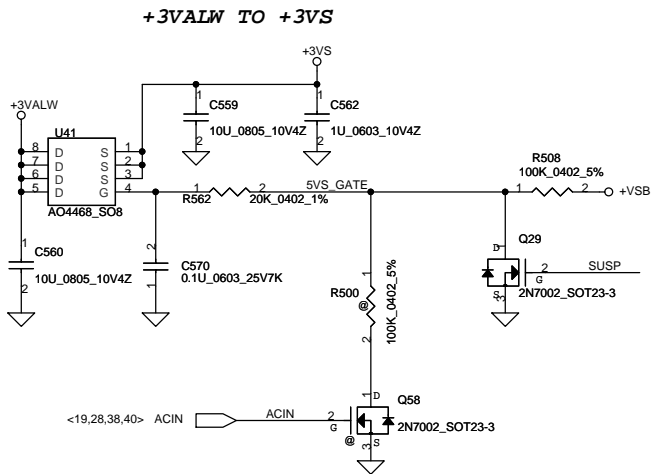
LINE Out/Headphone Out



MIC JACK

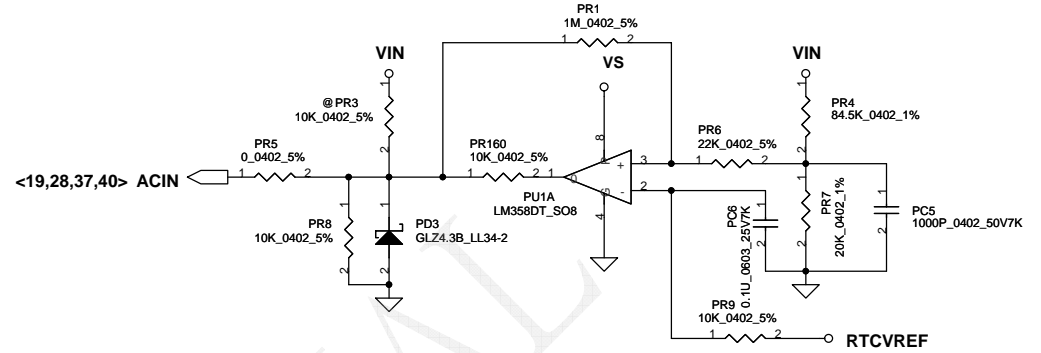
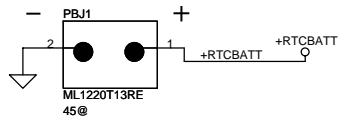
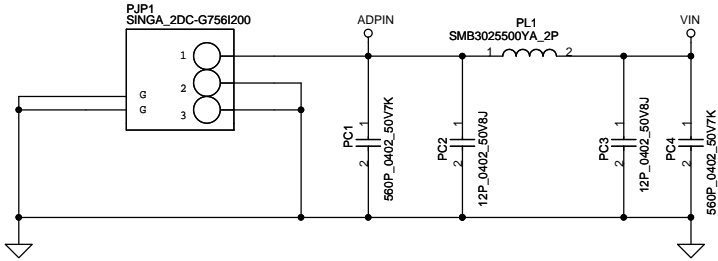


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				401830	A
				Date:	Thursday, October 15, 2009
				Sheet	36 of 47

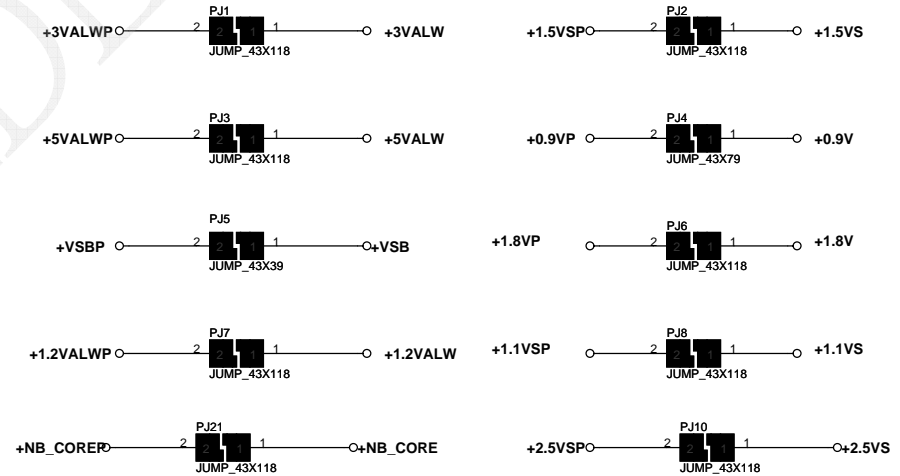
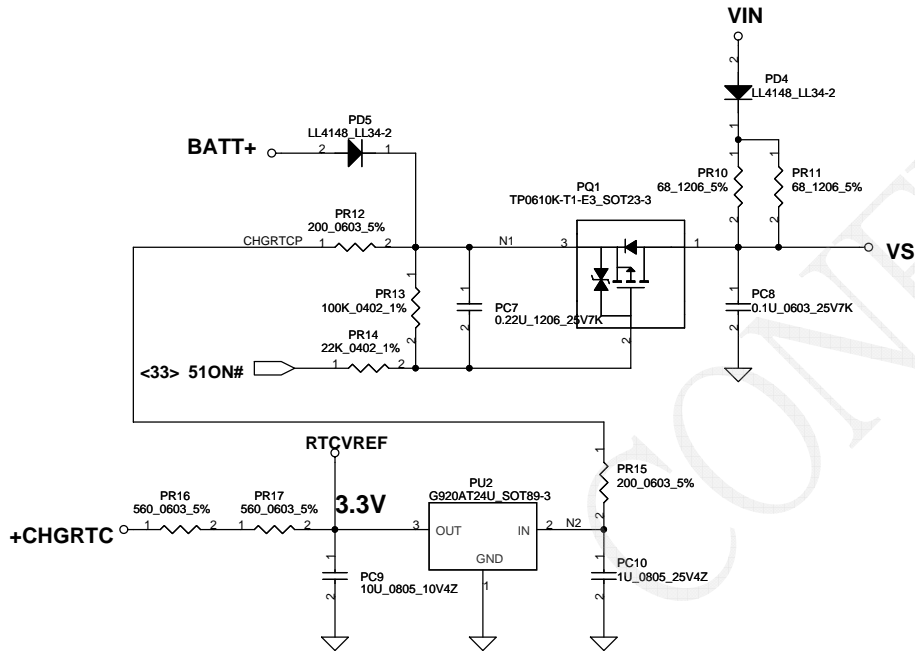


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Date:	Monday, October 19, 2009	Sheet	37	of	47

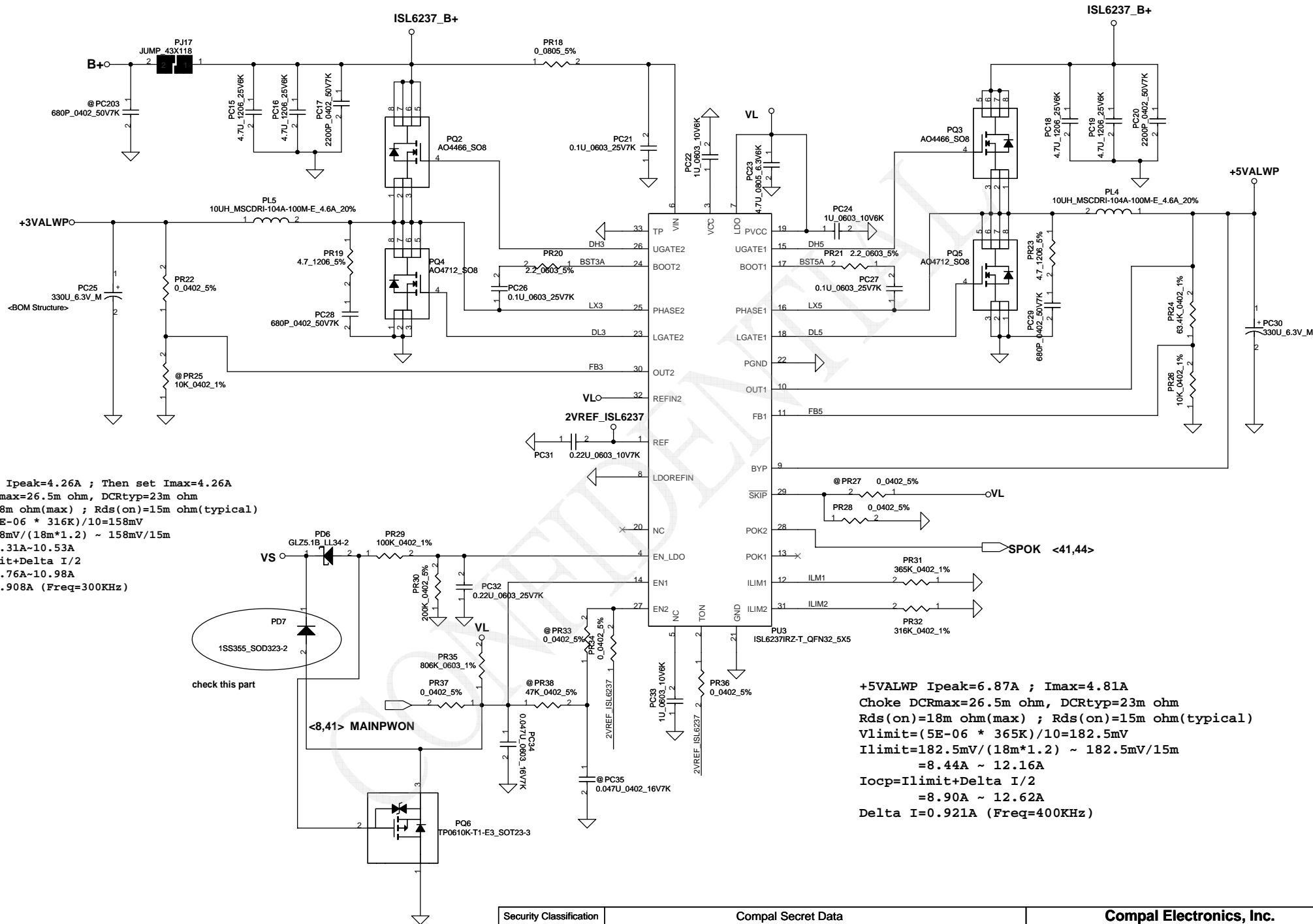
DC231000500



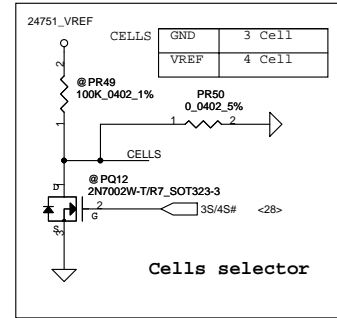
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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Date:	Monday, October 19, 2009	Sheet	38	of	47



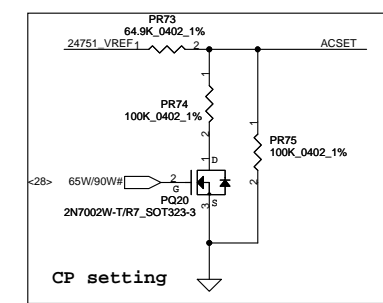
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				401830
				Rev A
Date: Monday, October 19, 2008				Sheet 39 of 47



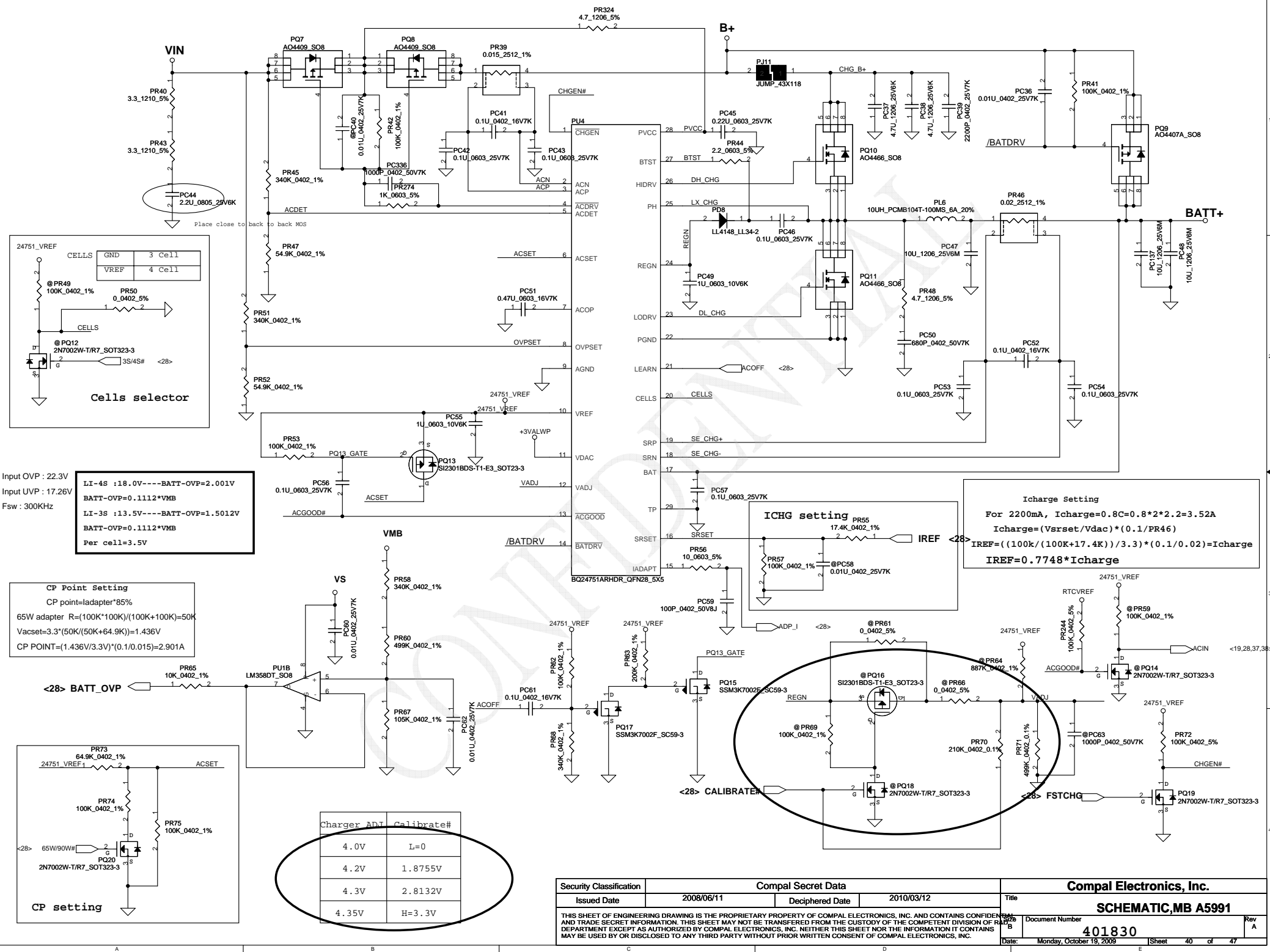
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

LI-4S :18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

CP Point Setting
CP point=ladapter*85%
65W adapter R=(100K*100K)/(100K+100K)=50K
Vacset=3.3*(50K/(50K+64.9K))=1.436V
CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A



Charger ADI	Calibrate#
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

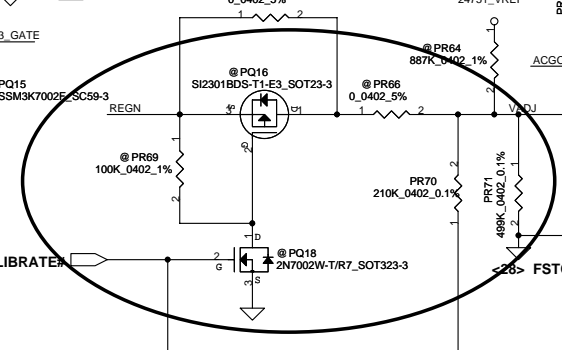


ICHG setting

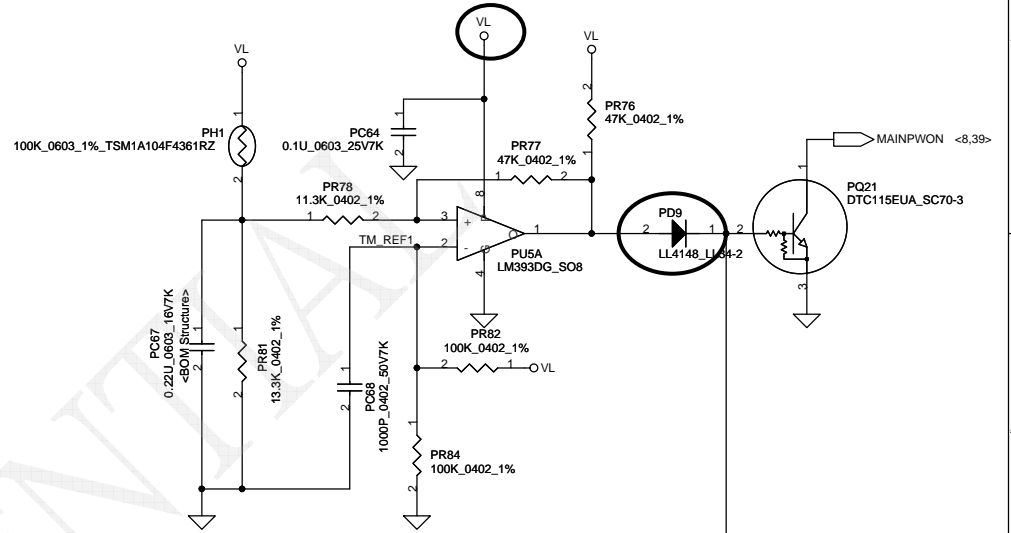
PR55 17.4K_0402_1%
PR57 100K_0402_1%
@PC58 0.01U_0402_25V7K

IREF <28>

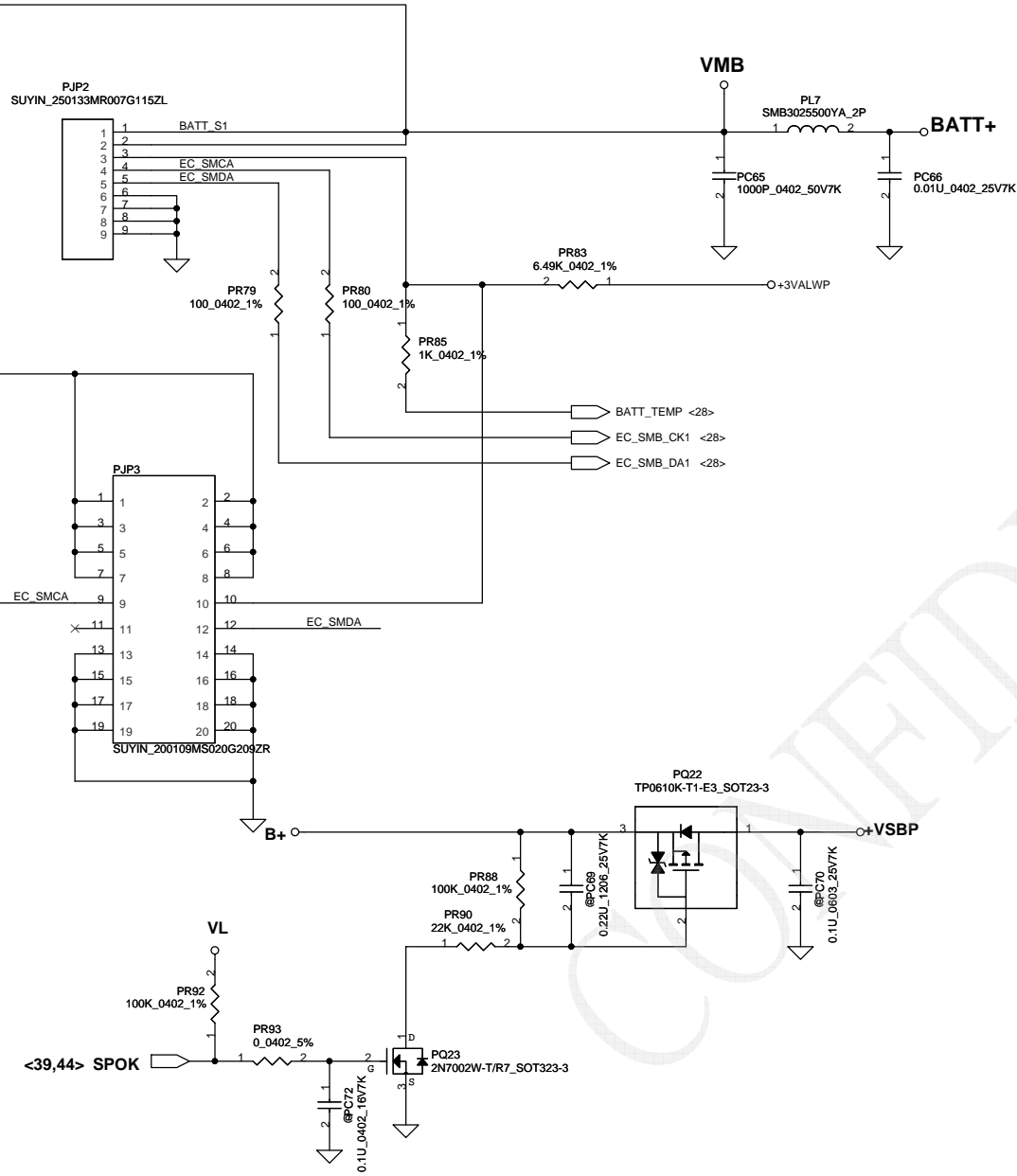
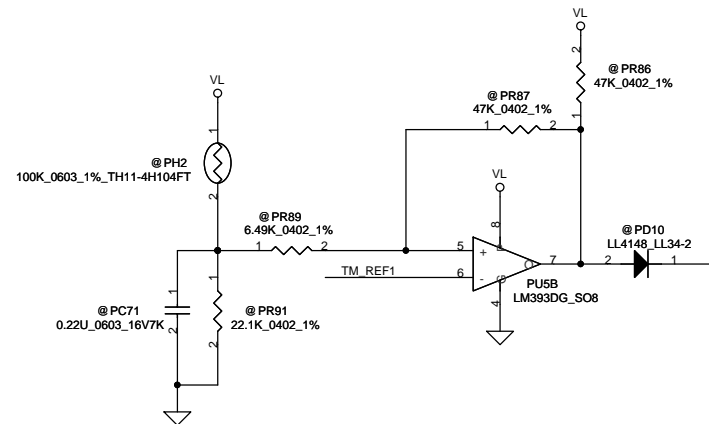
Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
Icharge=(Vsrset/Vdac)*(0.1/PR46)
IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
IREF=0.7748*Icharge



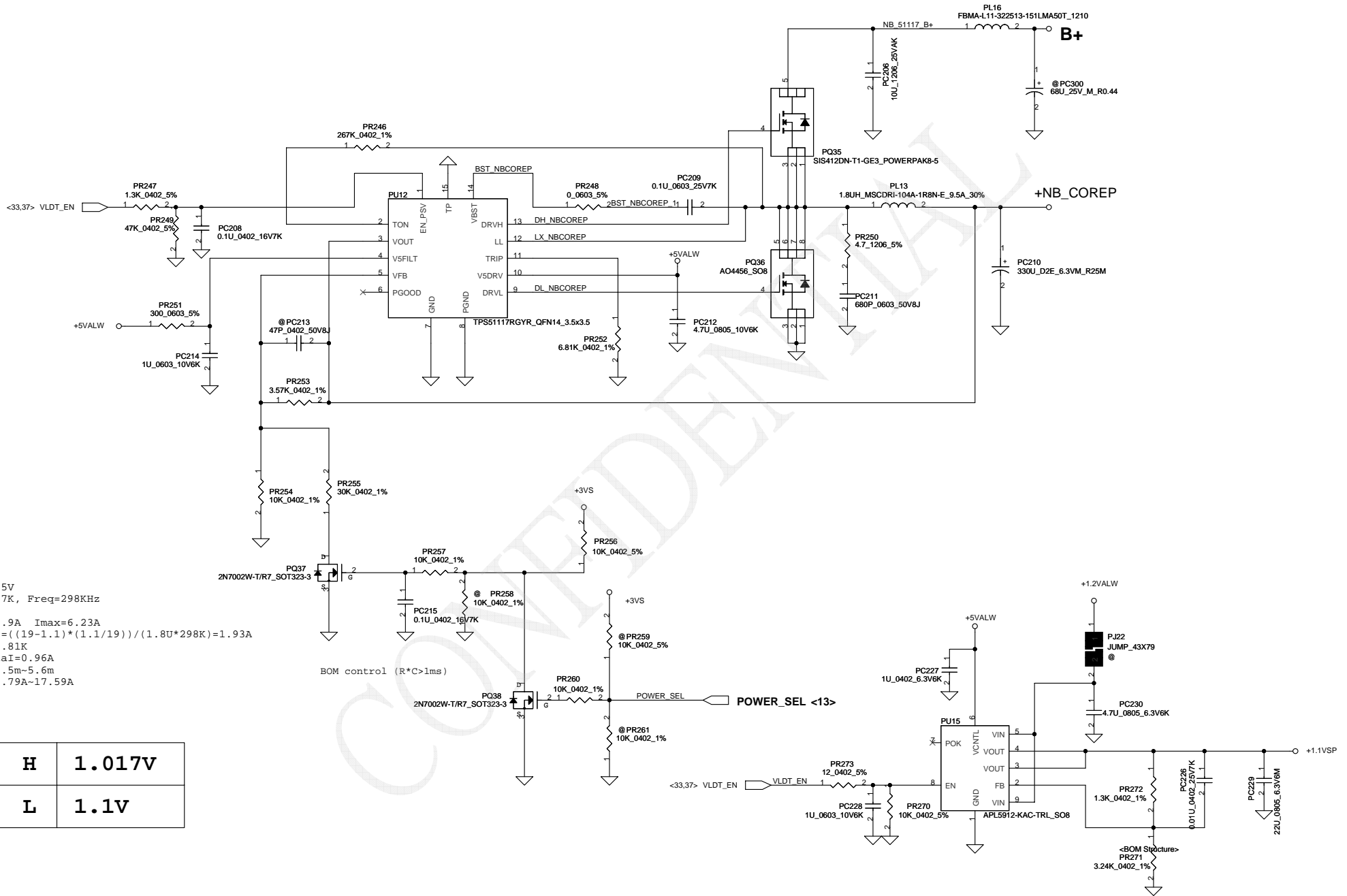
PH1 under CPU bottom side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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Date:	Monday, October 19, 2009	Sheet	41	of	47

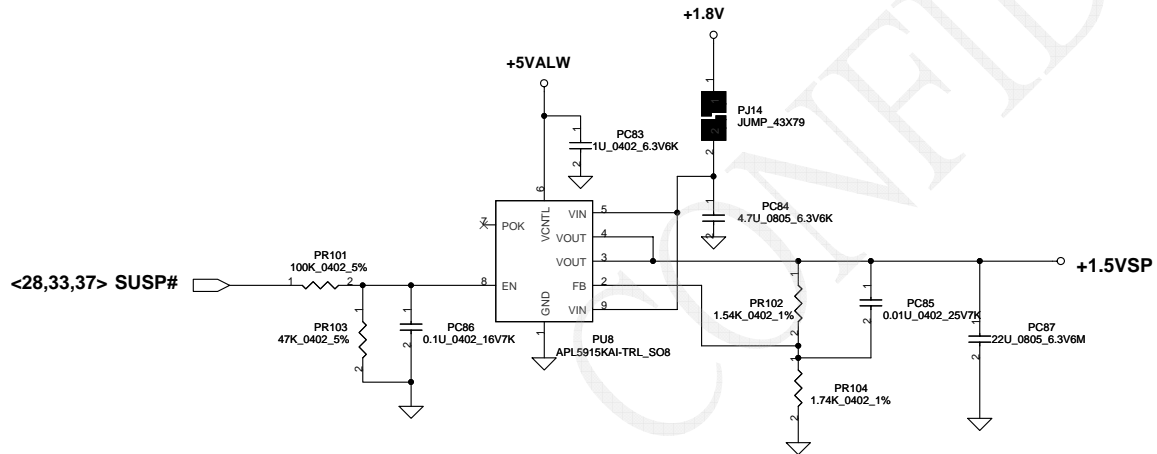
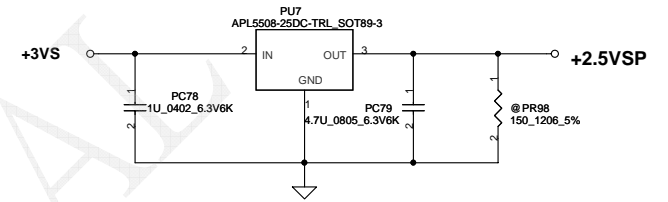
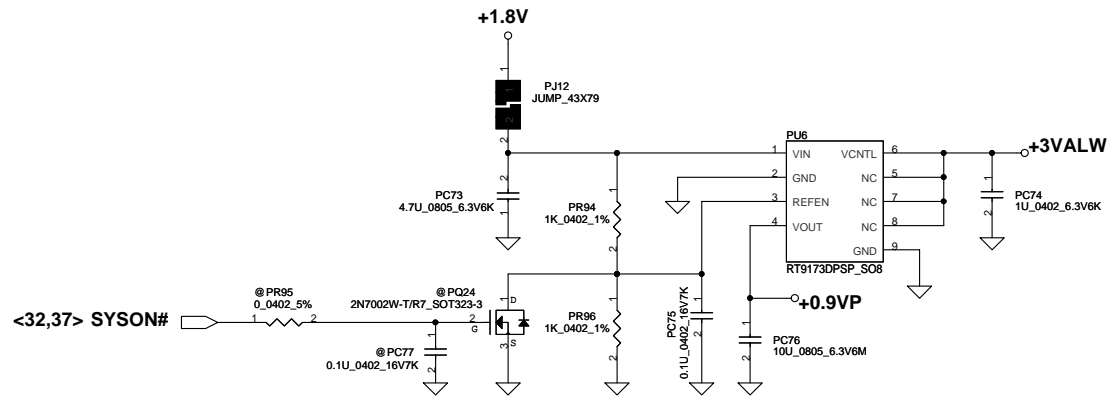


VFB=0.75V
 Rton=267K, Freq=298KHz
 Ipeak=8.9A Imax=6.23A
 $\Delta I = ((19-1.1) * (1.1/19)) / (1.8U * 298K) = 1.93A$
 Rtrip=6.81K
 $1/2\Delta I = 0.96A$
 Rdson=4.5m~5.6m
 Iocp=10.79A~17.59A

BOM control (R*C>1ms)

H	1.017V
L	1.1V

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401830	Document Number	401830		Date: Monday, October 19, 2009
Sheet	42	of	47	

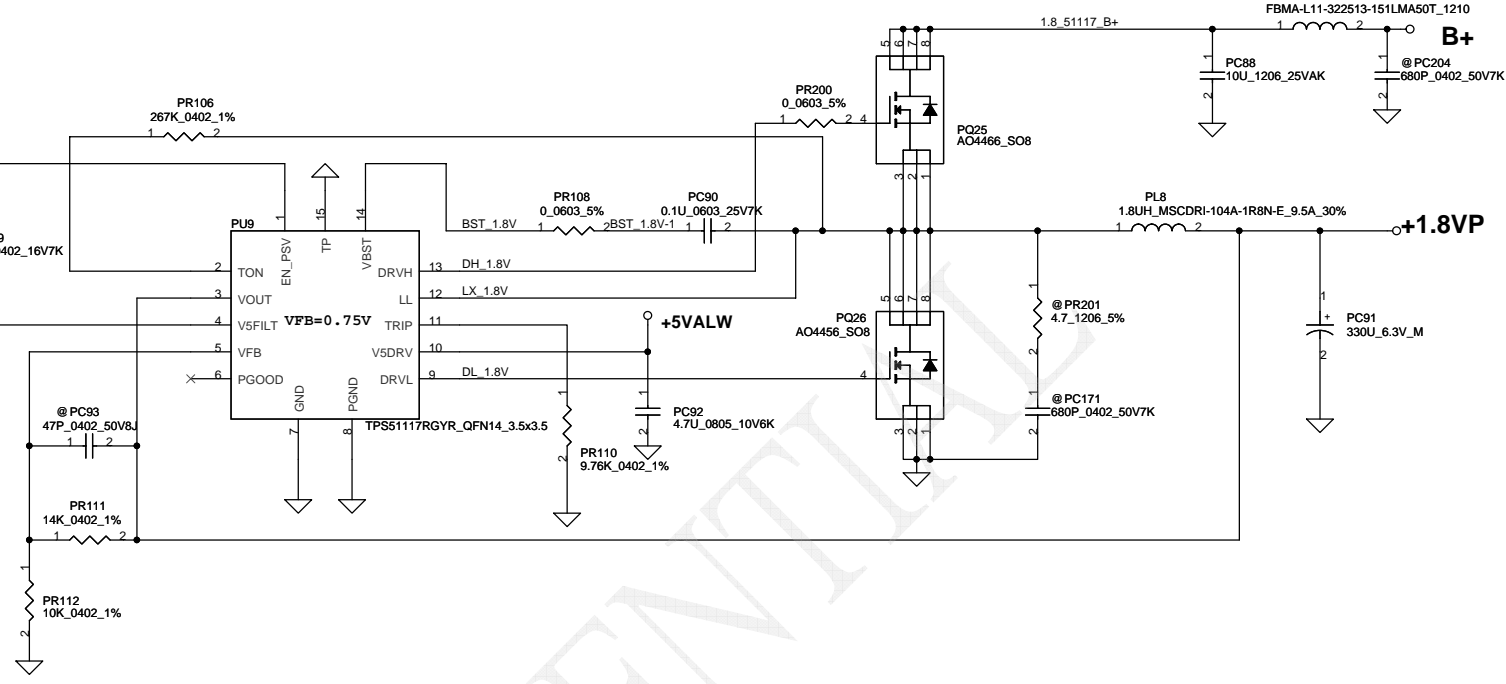


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Date	Monday, October 19, 2009	Sheet	43	Rev	A
Document Number	401830				

<28,37> SYSON

VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

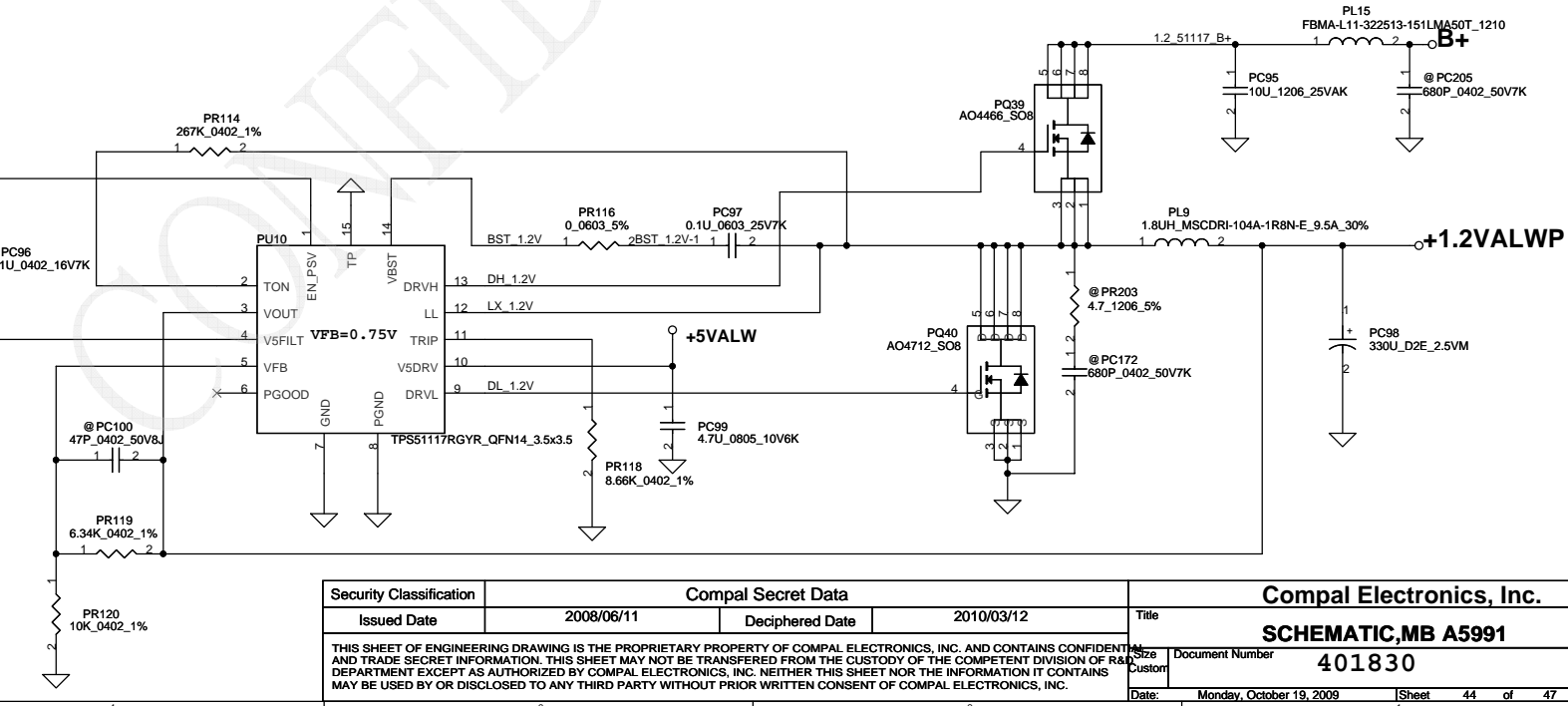
$C_{out} ESR = 15m\ \Omega$
 $I_{peak} = 11.96A, I_{max} = 8.372A$
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (L * F_{sw})$
 $((19 - 1.8) * (1.8 / 19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$
 $R_{trip} = 9.76K$
 $I_{ocp} = 15.20A - 24.71A$



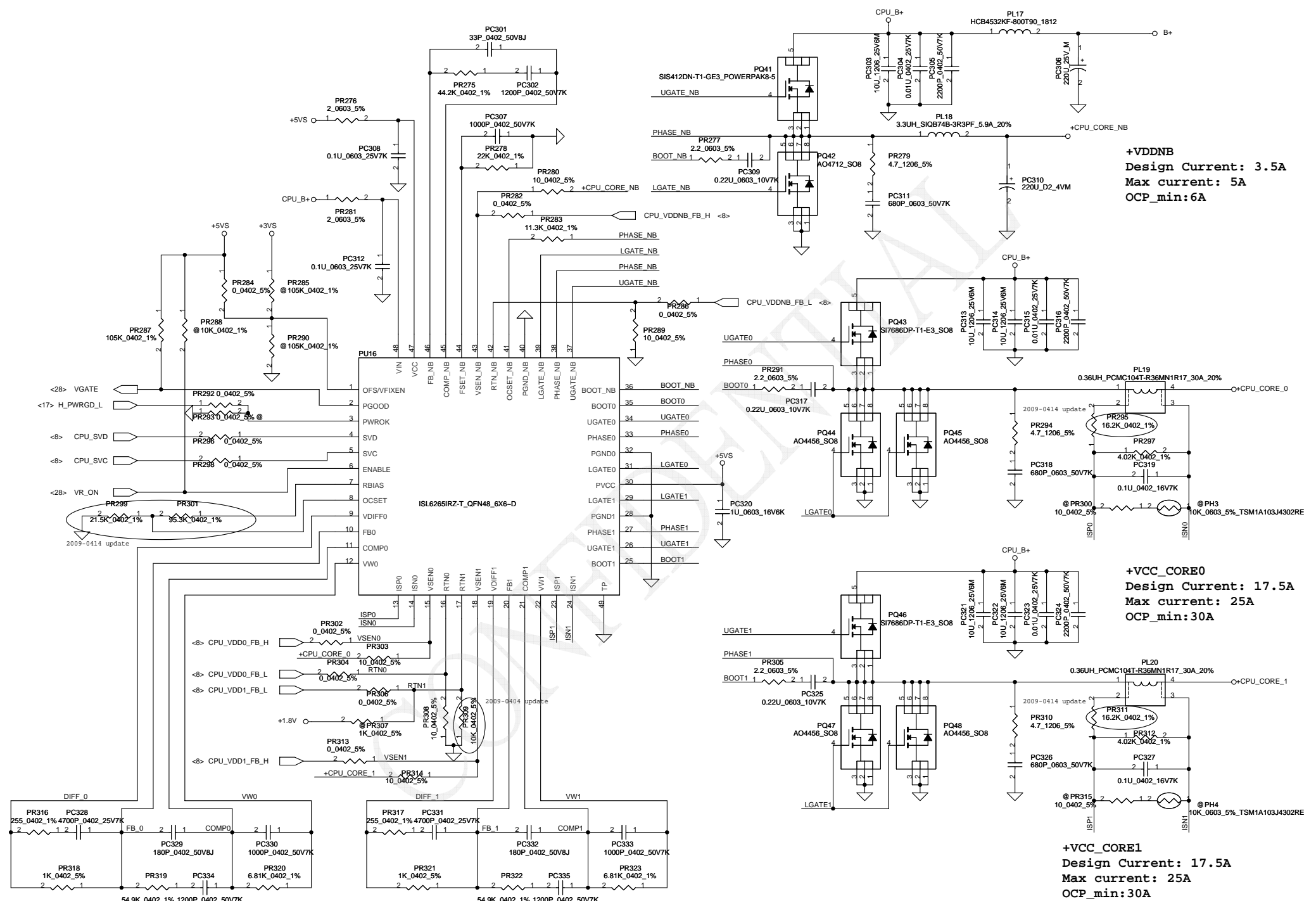
<39,41> SPOK

VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP $I_{peak} = 7.4A ; I_{max} = 5.180A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw})$
 $((19 - 1.2) * (1.2 / 19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$
 $R_{dson} = 15m / 18m\ \Omega$
 $set\ R_{trip} = 8.66K$
 $I_{ocp_min} = 4.77A$
 $I_{ocp_max} = 7.74A$



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Size	Custom	Document Number	401830		Rev A
Date	Monday, October 19, 2009	Sheet	44	of	47



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Issued Date	2008/11/03	Deciphered Date	2009/11/03	SCHEMATIC, MB A5991	
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				401830	A
				Date: Monday, October 19, 2009	Sheet 45 of 47

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
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14							
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17							
18							

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Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1					26				
2					27				
3					28				
4					29				
5					30				
6					31				
7					32				
8					33				
9									
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Date:	Monday, October 19, 2009	Sheet	47	of	47
				Rev	A