

# Compal Confidential

## NAV51 Schematics Document

### Intel Pineview Processor with Tigerpoint + DDRII

2010-03-31

REV: 1.0

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				Size B	Document Number	Rev
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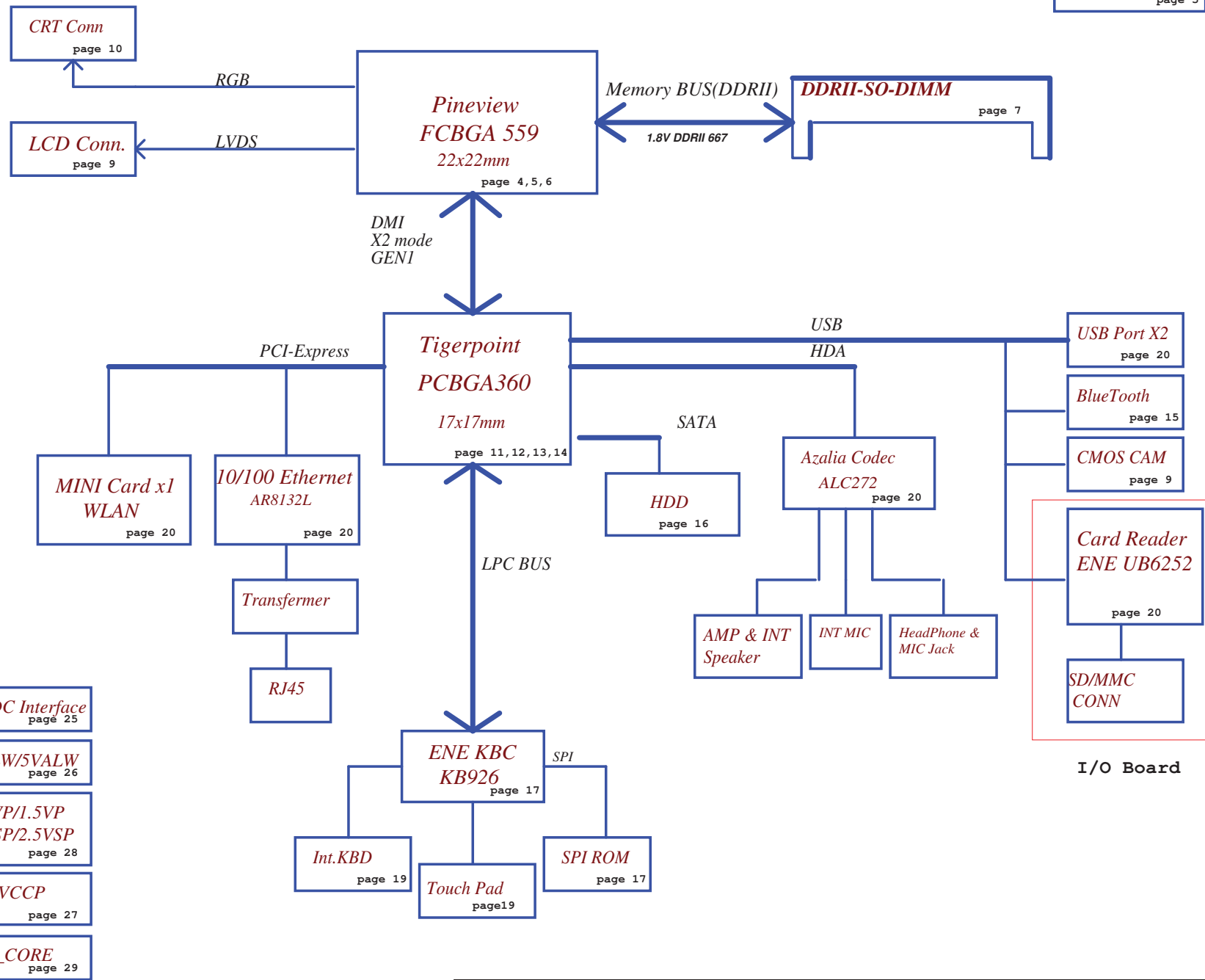
# Compal Confidential

Model Name : NAV51  
File Name : LA-6311P



Clock Generator  
CK505  
page 8

Thermal Sensor  
EMC1402  
page 5



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- CHARGER** page 25
- CPU\_CORE** page 29
- DC/DC Interface** page 25
- 3VALW/5VALW** page 26
- 0.89VP/1.5VP**  
**0.9VSP/2.5VSP** page 28
- 1.8V/VCCP** page 27

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOARD ID Table(Page 17)

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0 (EVT)	0	0 V	0 V	0 V
1 (DVT)	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2 (PVT)	18K +/- 5%	0.436 V	0.503 V	0.538 V
3 (MP)	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

## No PCI Device

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

## Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

## USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
		Port1	MB USB Conn2.
	UHCI2	Port2	
	UHCI3	Port3	CMOS
		Port4	Card Reader
		Port5	
EHCI2	UHCI4	Port6	BT
		Port7	WLAN
	UHCI5	Port8	
		Port9	
		Port10	
	UHCI6	Port11	

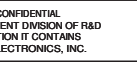
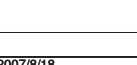
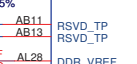
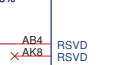
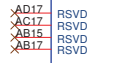
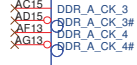
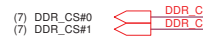
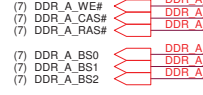
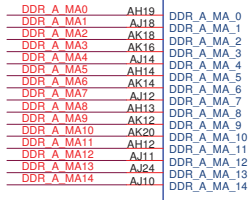
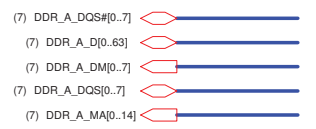
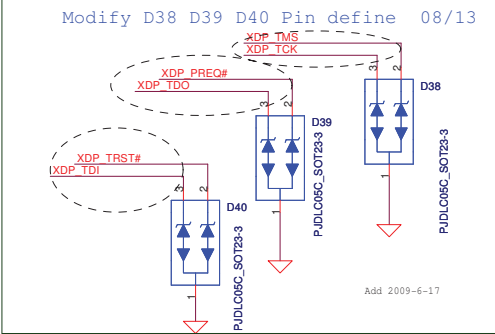
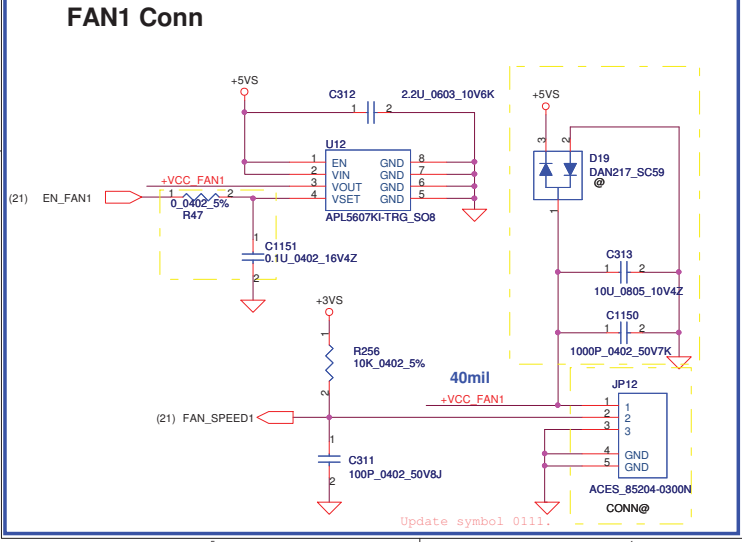
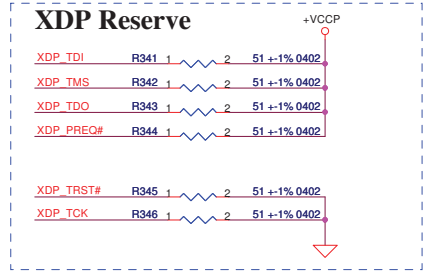
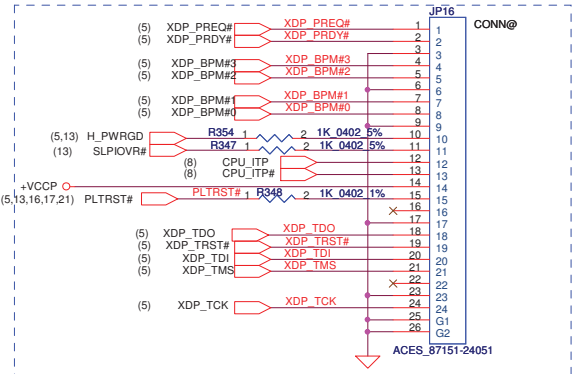
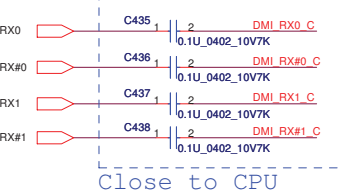
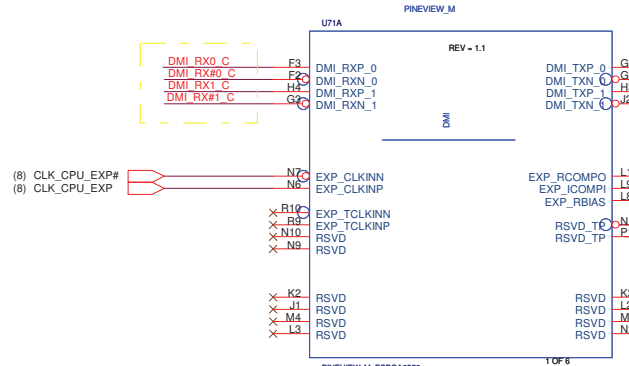
## PCIE table

PCIE port1	LAN
PCIE port2	Wireless Card
PCIE port3	
PCIE port4	
PCIE port5	
PCIE port6	

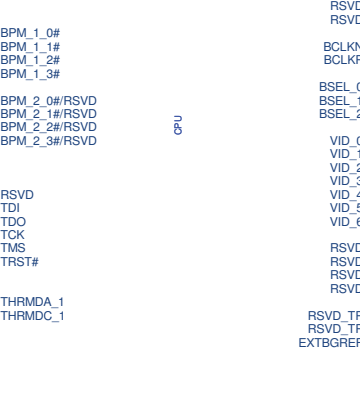
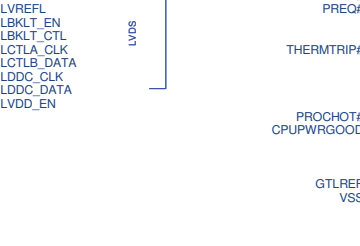
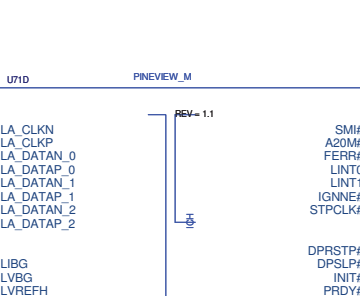
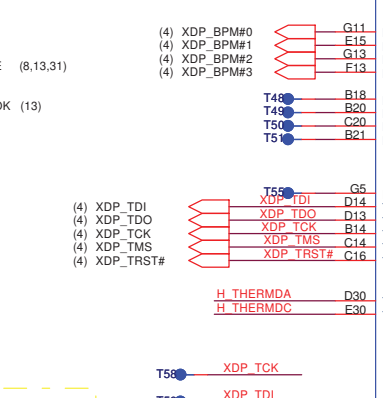
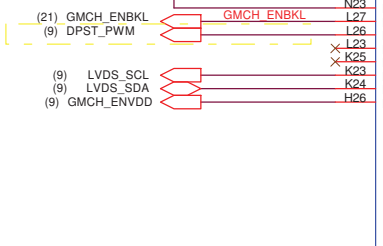
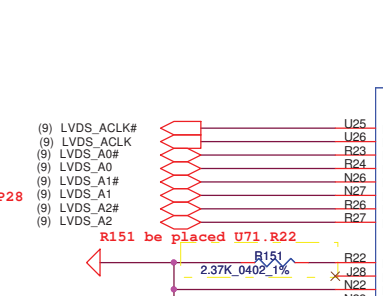
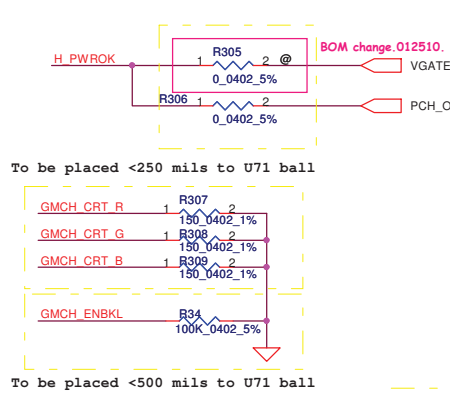
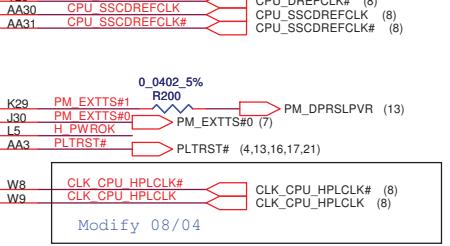
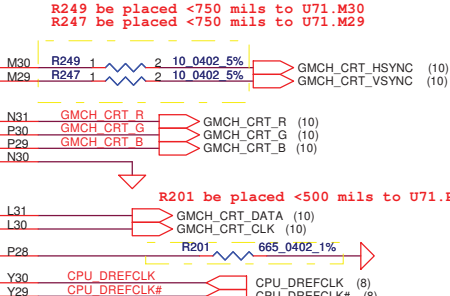
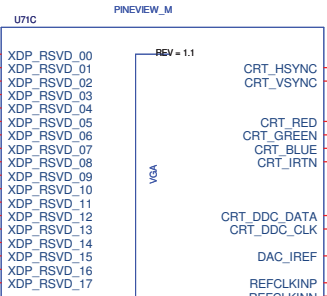
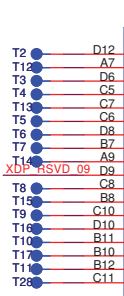
## SATA table

SATA port0	HDD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	

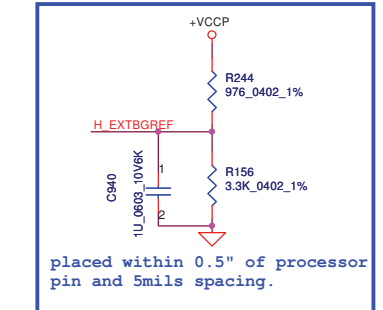
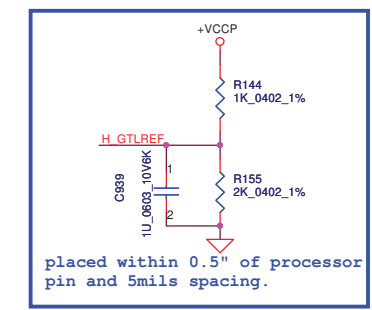
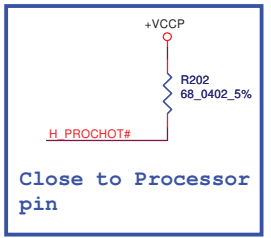
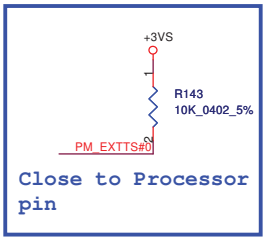
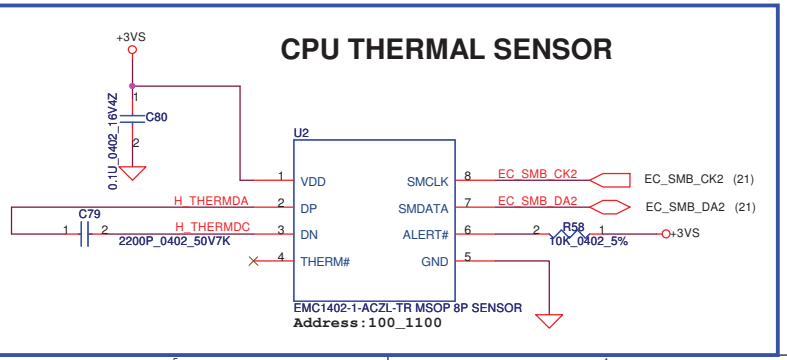
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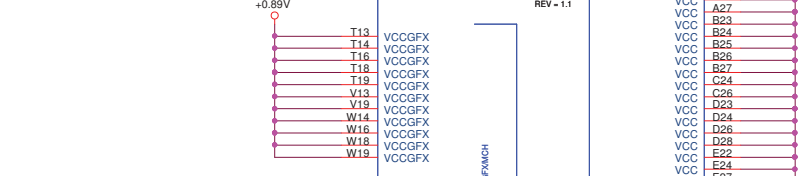
H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil



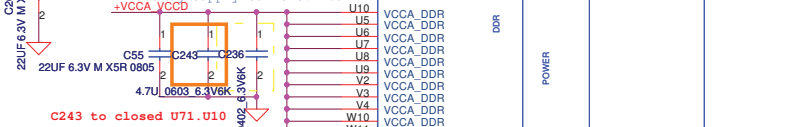
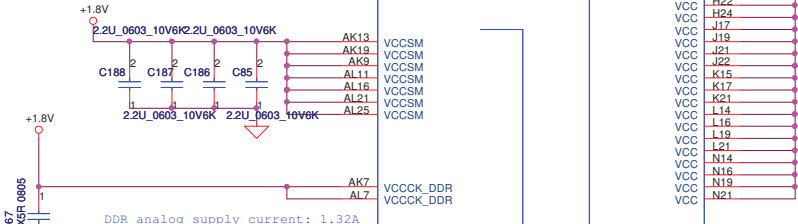
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Title Pineview(2/3)			
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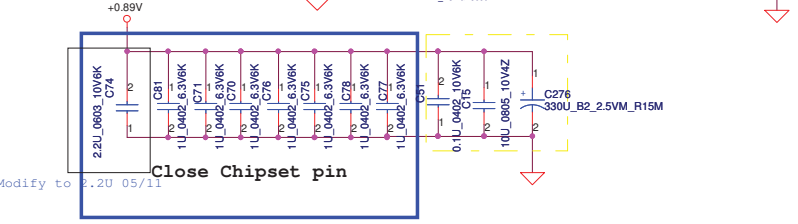
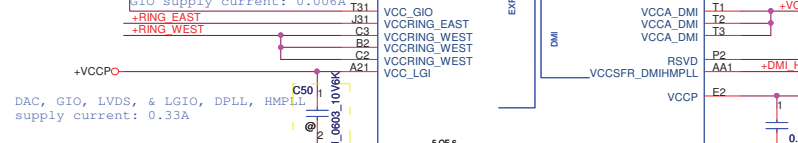
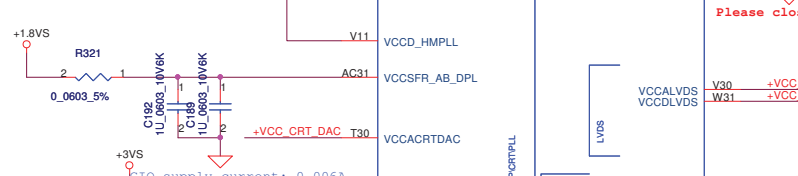
GFX supply current: 1.38A  
Sustained GFX supply current: 1.05A



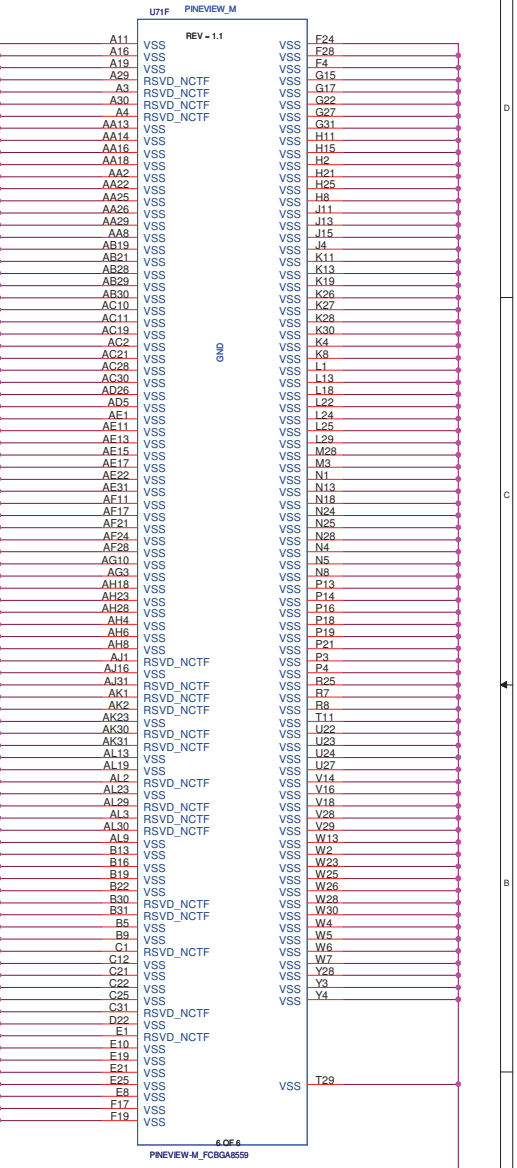
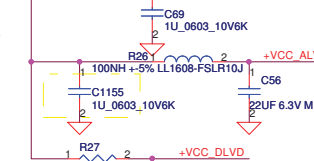
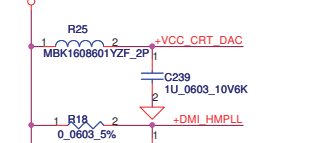
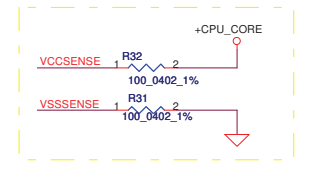
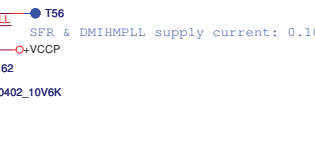
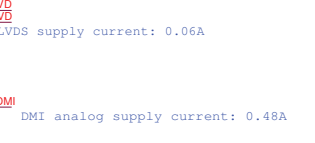
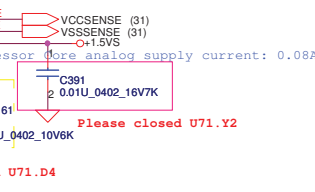
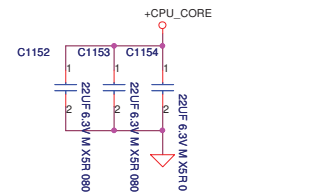
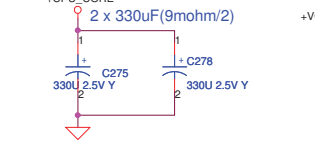
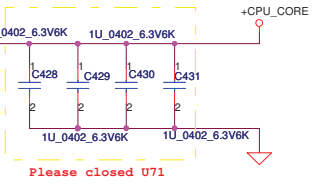
DDR supply current 2.27A



Display PLL SFR and CRT DAC supply current: 0.154A



Close Chipset pin  
Modify to 2.2U 05/11

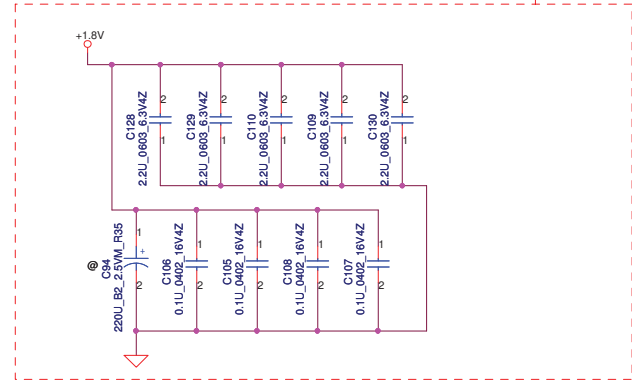


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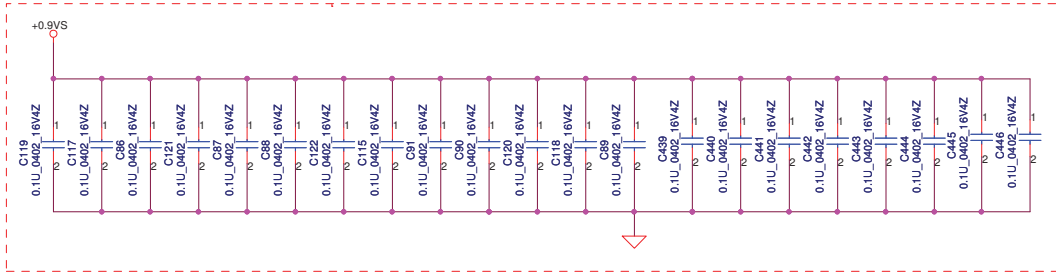
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- (4) DDR\_A\_DOS#[0..7]
- (4) DDR\_A\_D[0..63]
- (4) DDR\_A\_DM[0..7]
- (4) DDR\_A\_DOS[0..7]
- (4) DDR\_A\_MA[0..14]

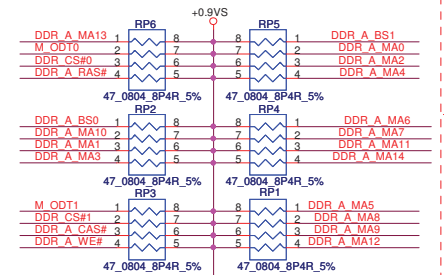
**Layout Note:**  
Place near JDIM1



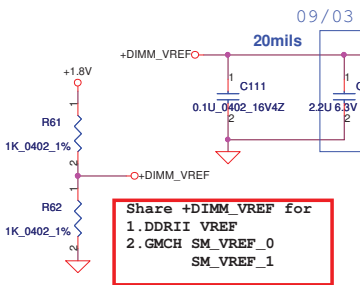
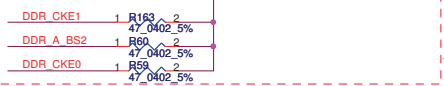
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



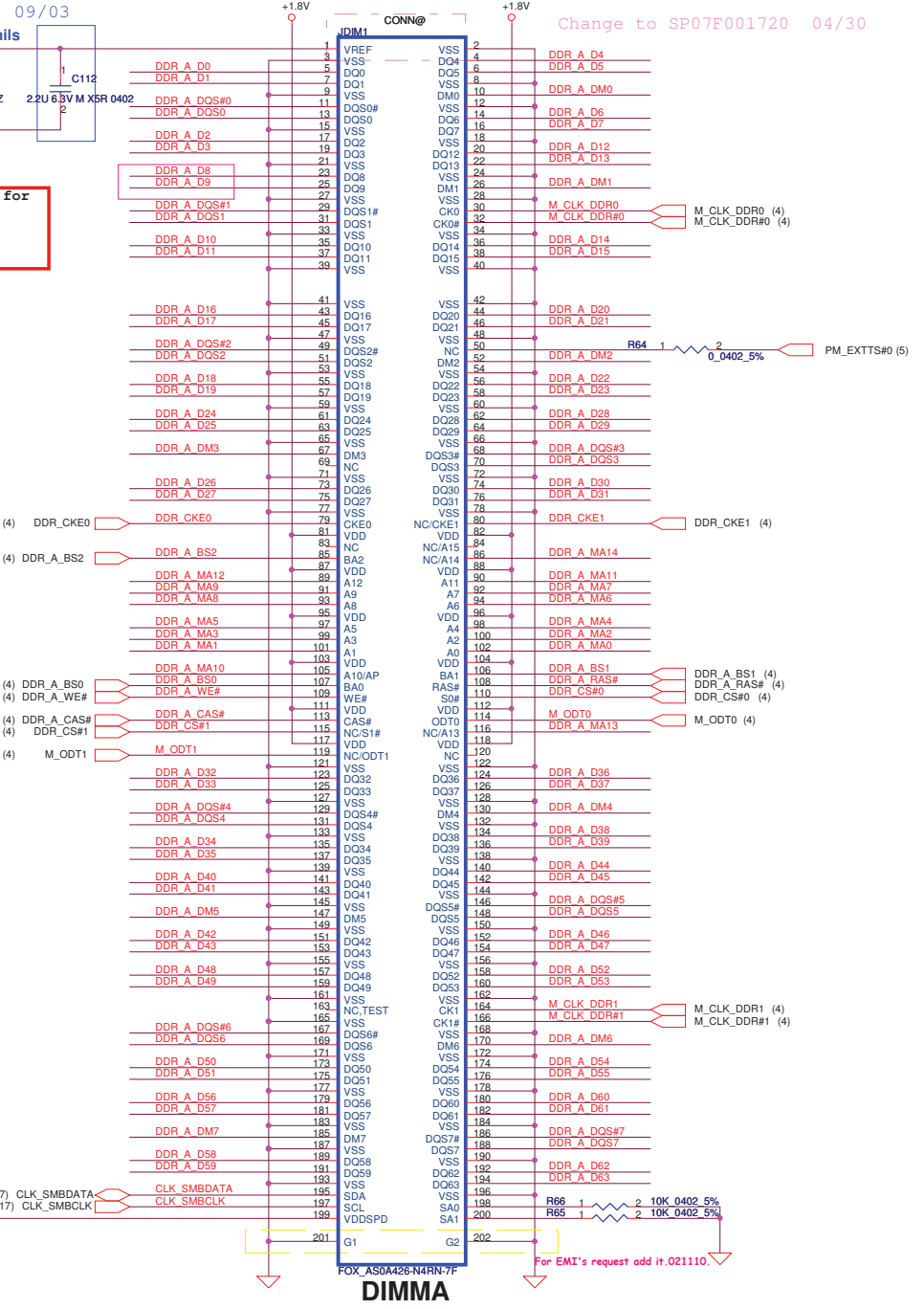
**Layout Note:**  
Place these resistor closely DIMMA, all trace length < 1000 mil



**Layout Note:**  
Place these resistor closely DIMMA, all trace length Max=1000 mil



**Share +DIMM\_VREF for**  
1. DDRII VREF  
2. GMCH SM\_VREF\_0  
SM\_VREF\_1



Change to SP07F001720 04/30

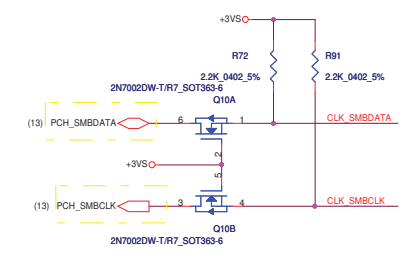
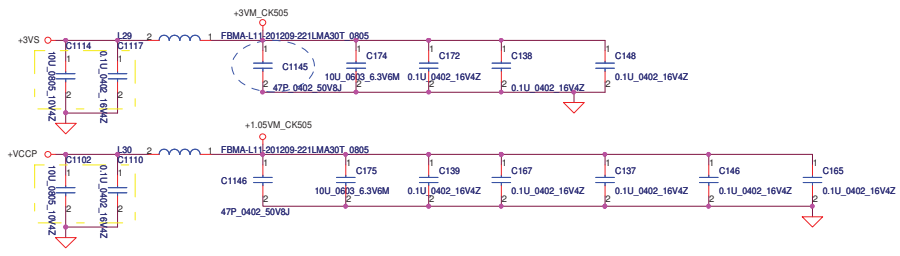
**DIMMA**

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				DDRII-SODIMMA		
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				Date: Tuesday, April 13, 2010	Sheet 7 of 33	

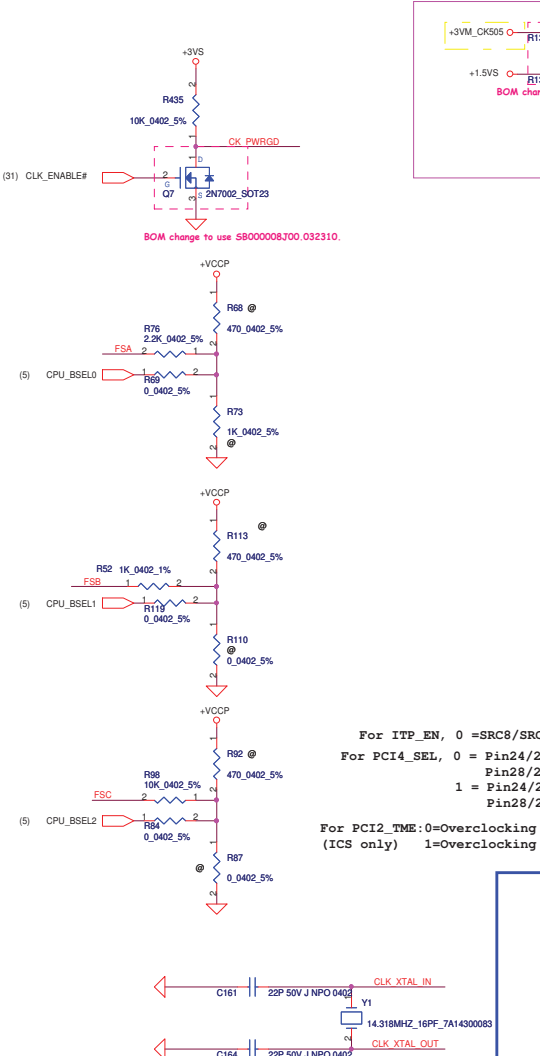
NAV51 LA-6311P

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

Reserved

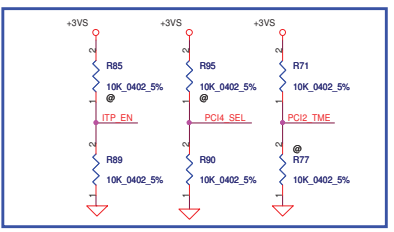


SA00003H730 (Realtek :RTM890N-397-VC-GRT)



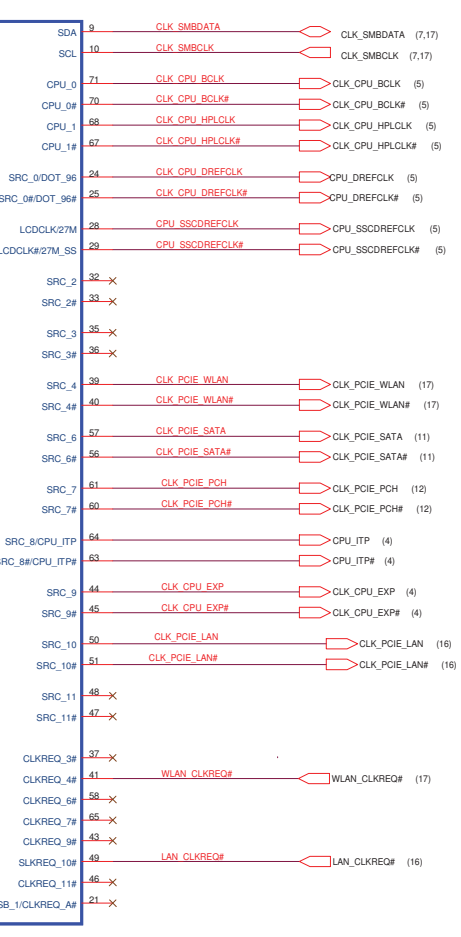
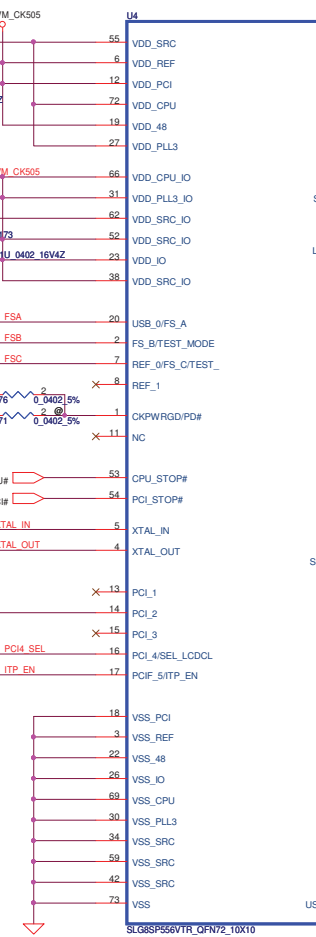
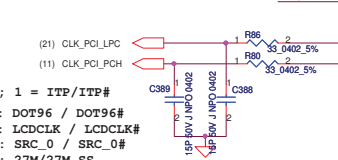
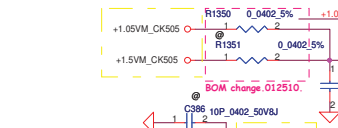
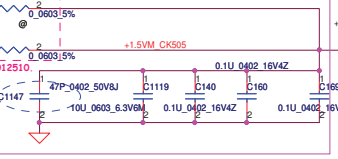
For ITP\_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#  
 For PC14\_SEL, 0 = Pin24/25 : DOT96 / DOT96#  
 Pin28/29 : LCDCLK / LCDCLK#  
 1 = Pin24/25 : SRC\_0 / SRC\_0#  
 Pin28/29 : 27M/27M\_SS

For PCI2\_TME: 0=Overclocking of CPU and SRC allowed (ICS only) 1=Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil

Change co-layer net name to +1.5VM\_CK505 07/03



SRC PORT LIST

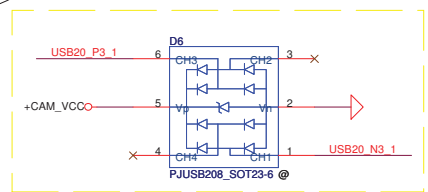
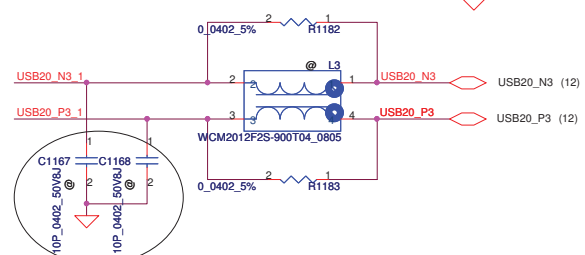
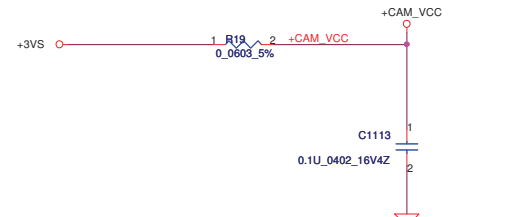
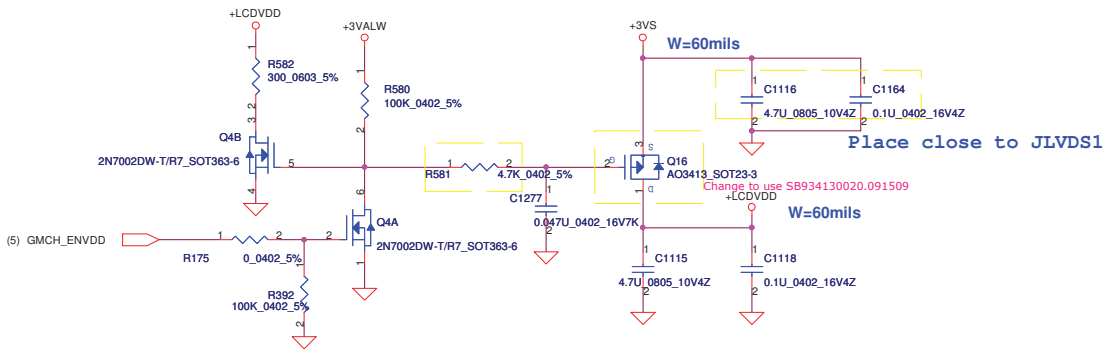
PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	
REQ_A#	

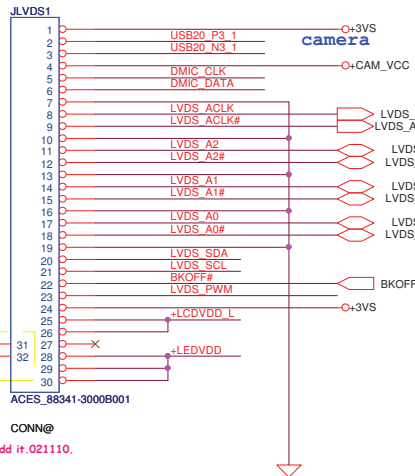
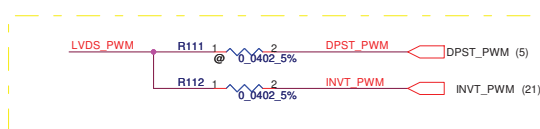
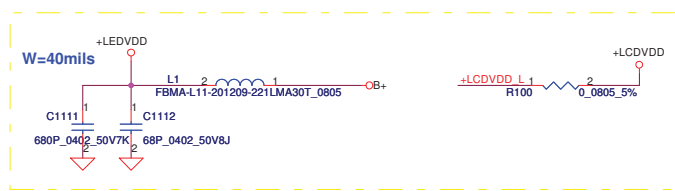


# LCD POWER CIRCUIT

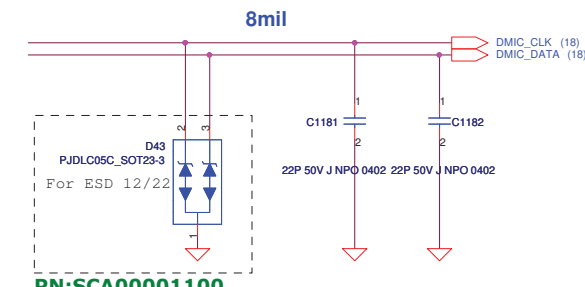
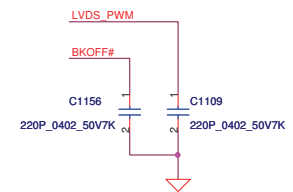
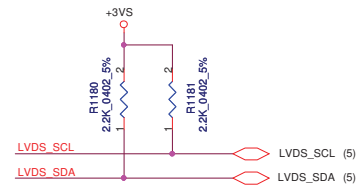


Reserve D6 for ESD\_011310.  
Swap D6 .011510.

# CMOS & LCD/PANEL BD. Conn.

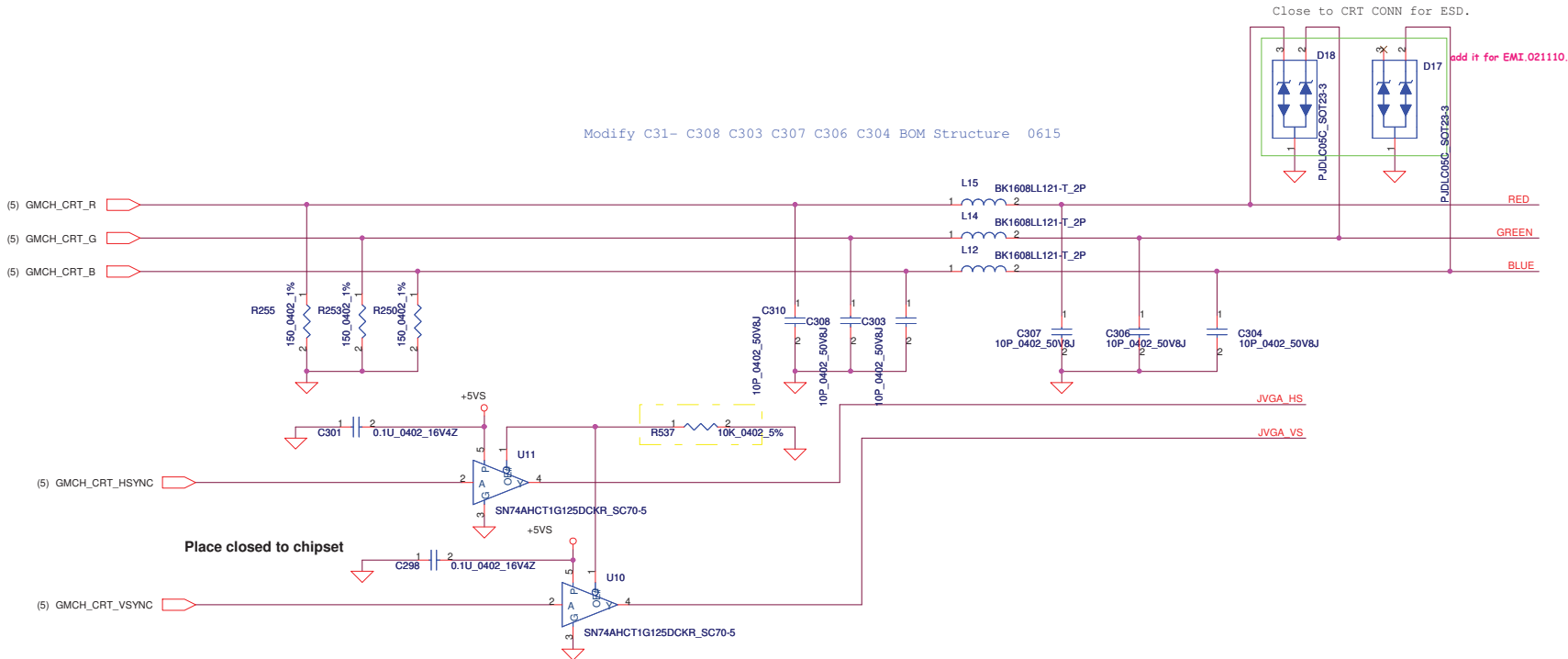


For EMI's request add it.021110.

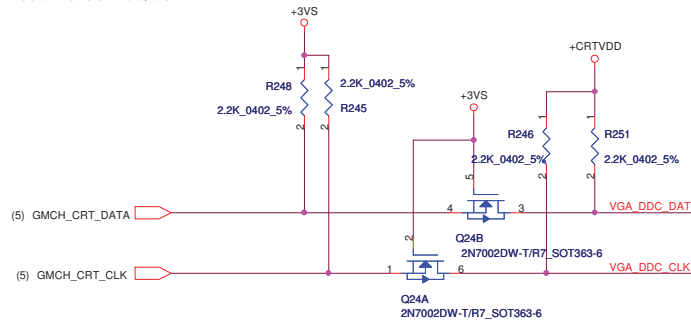


PN:SCA00001100

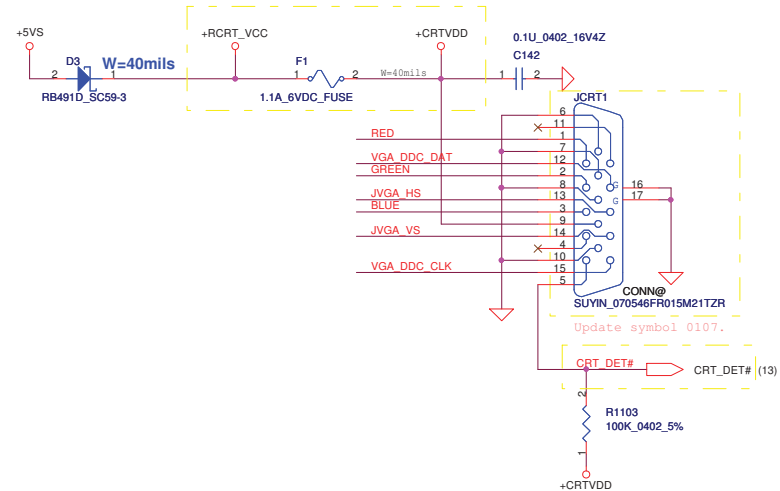
Security Classification	Compal Secret Data			Title		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	LVDS /INVERTER		
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				Date:	Tuesday, April 13, 2010	Sheet 9 of 33



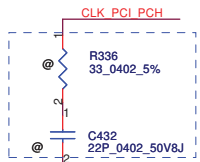
Add R1283 R1284  
Change R247 R249 to 10 ohm  
Add @ on U10 U11 C301 C298 06/08



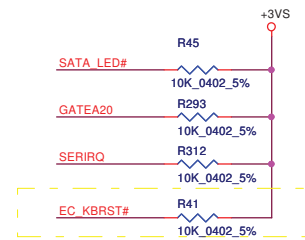
### CRT PORT



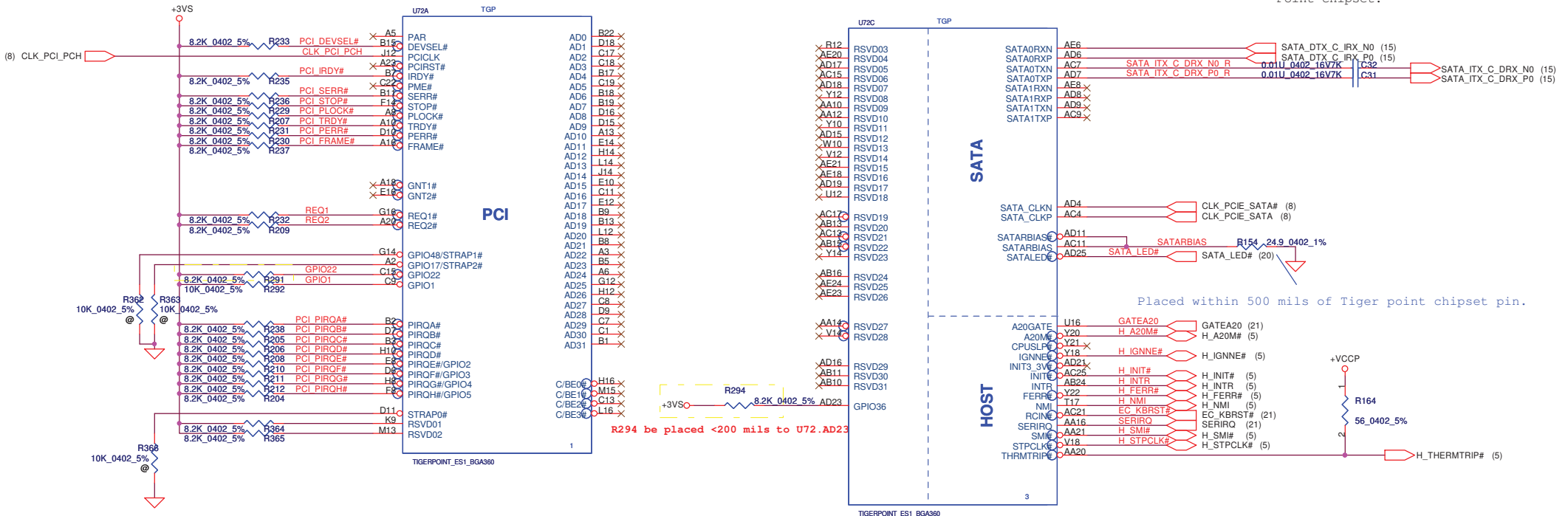
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
				CRT PORT	
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				Rev	0.2



For EMI, close to TigerPoint



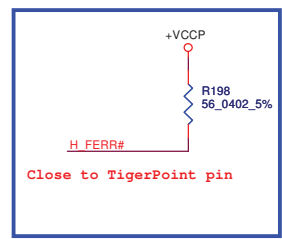
56 ohm±5% pull-up resistor has to be within 1" from the Tiger Point chipset.



Placed within 500 mils of Tiger point chipset pin.

R294 be placed <200 mils to U72.AD23

STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

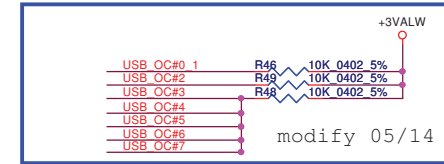
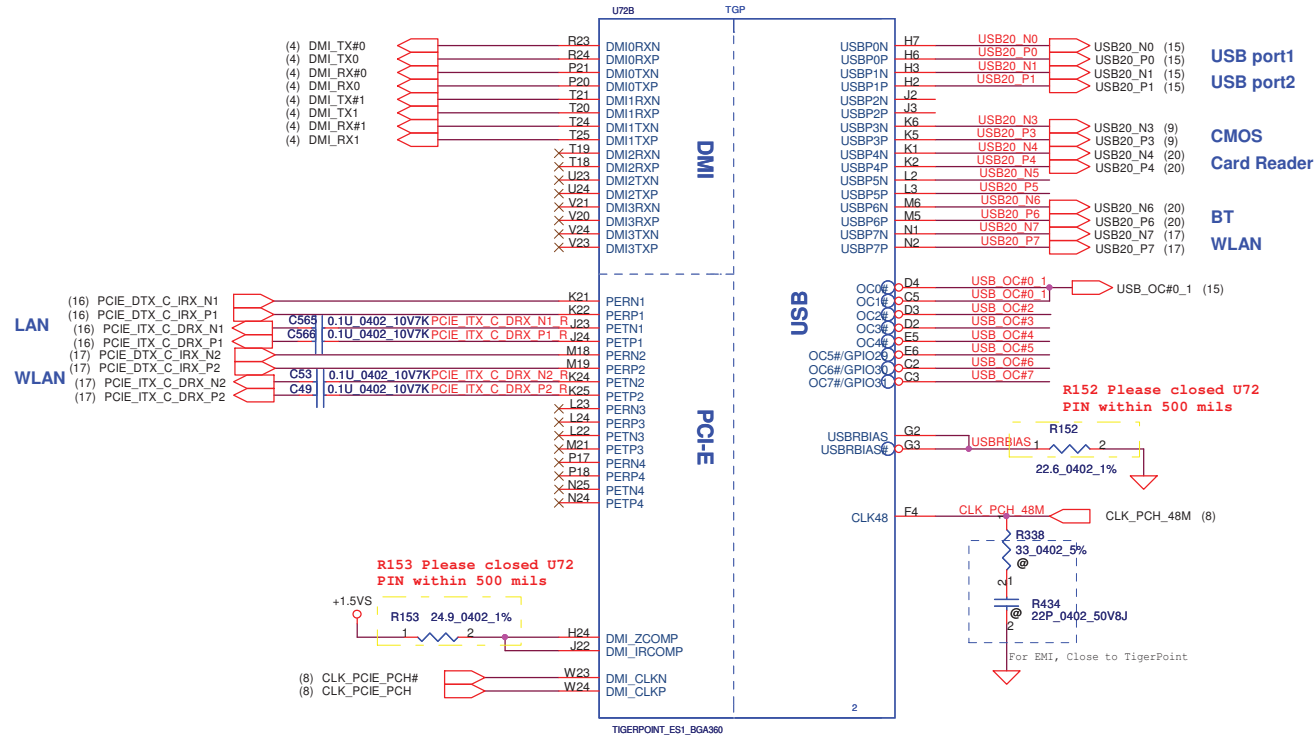


**ESD request**

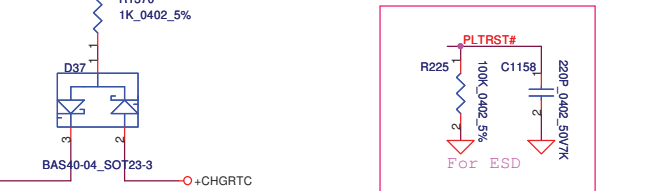
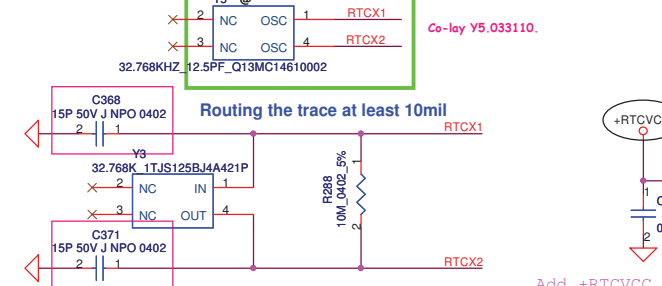
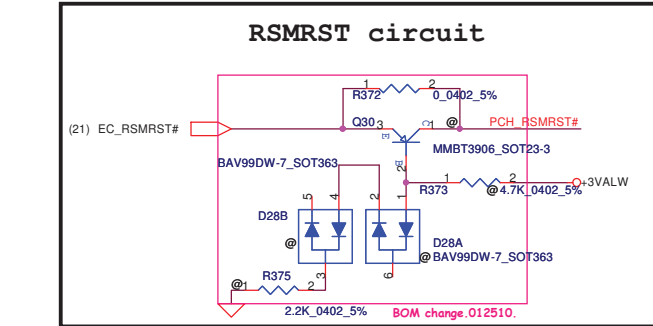
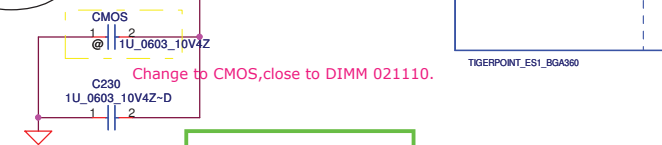
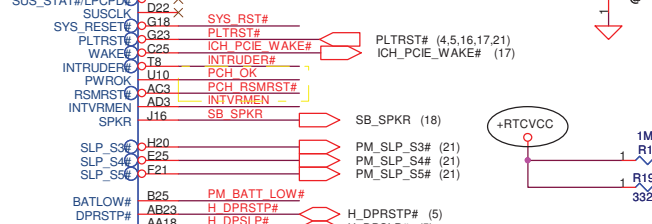
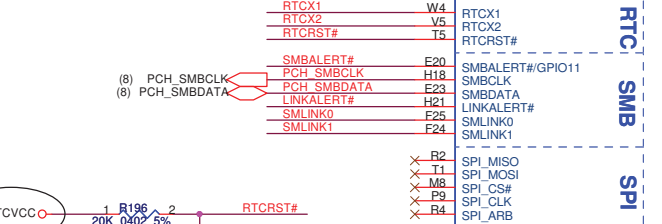
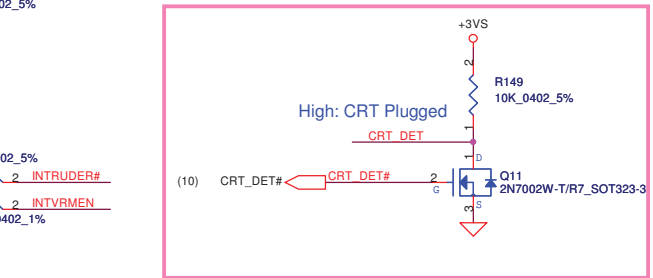
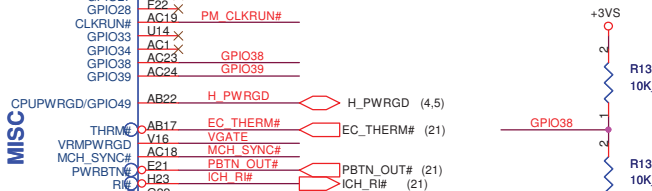
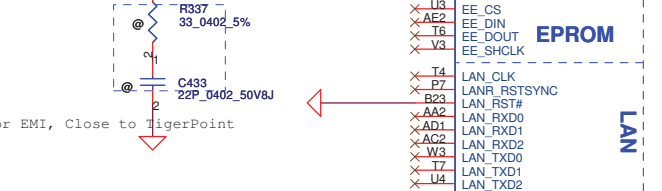
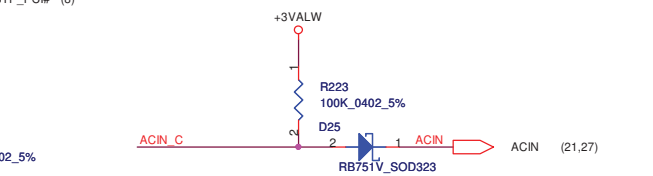
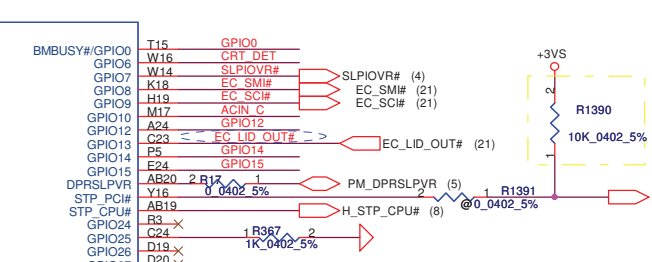
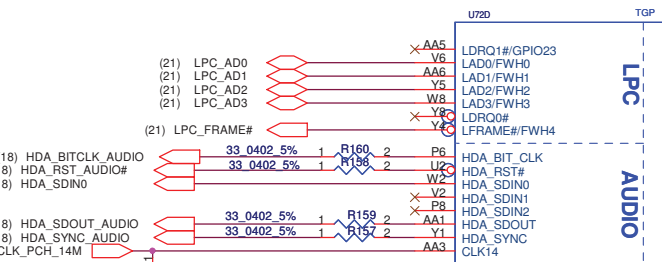
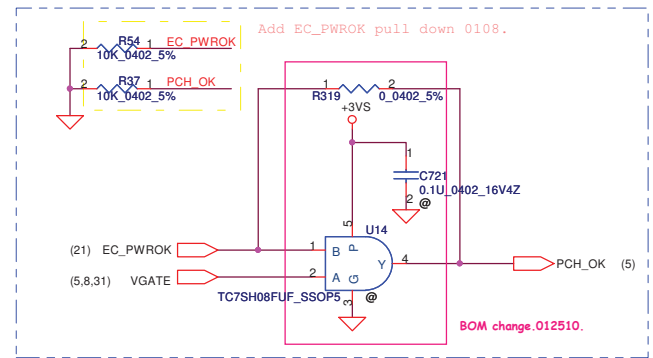
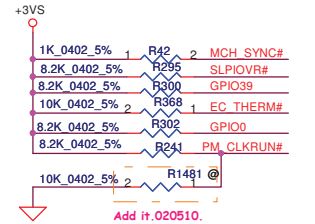
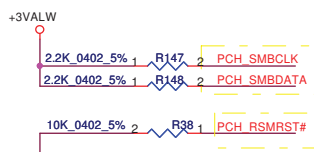
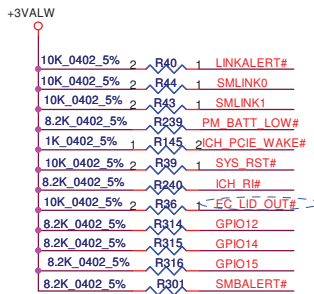
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H_IGNNE#	C451@	2	100P_0402_50V8J
H_INIT#	C452@	2	100P_0402_50V8J
H_INTR#	C453@	2	100P_0402_50V8J
H_FERR#	C454@	2	100P_0402_50V8J
H_NMI#	C455@	2	100P_0402_50V8J
H_SMI#	C456@	2	100P_0402_50V8J
H_STPCLK#	C457@	2	100P_0402_50V8J

PCIe Port List	
1	LAN
2	WLAN
3	
4	

USB Port List	
0	USB Left1
1	USB Left2
2	
3	CMOS
4	CardReader
5	
6	BT
7	WLAN



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Date:	Tuesday, April 13, 2010	Sheet	12	of	33

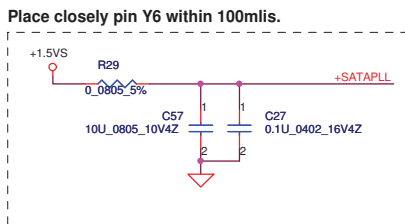
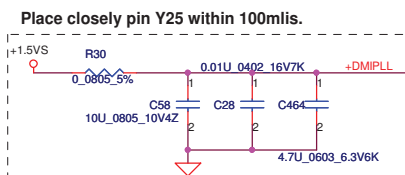
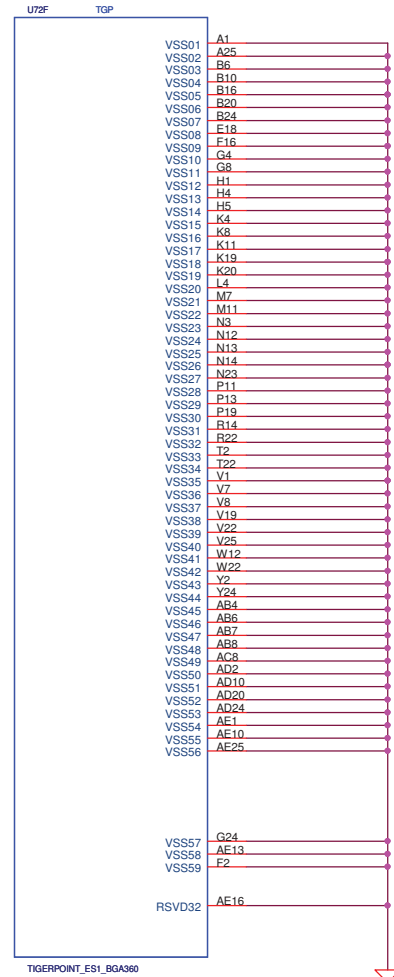
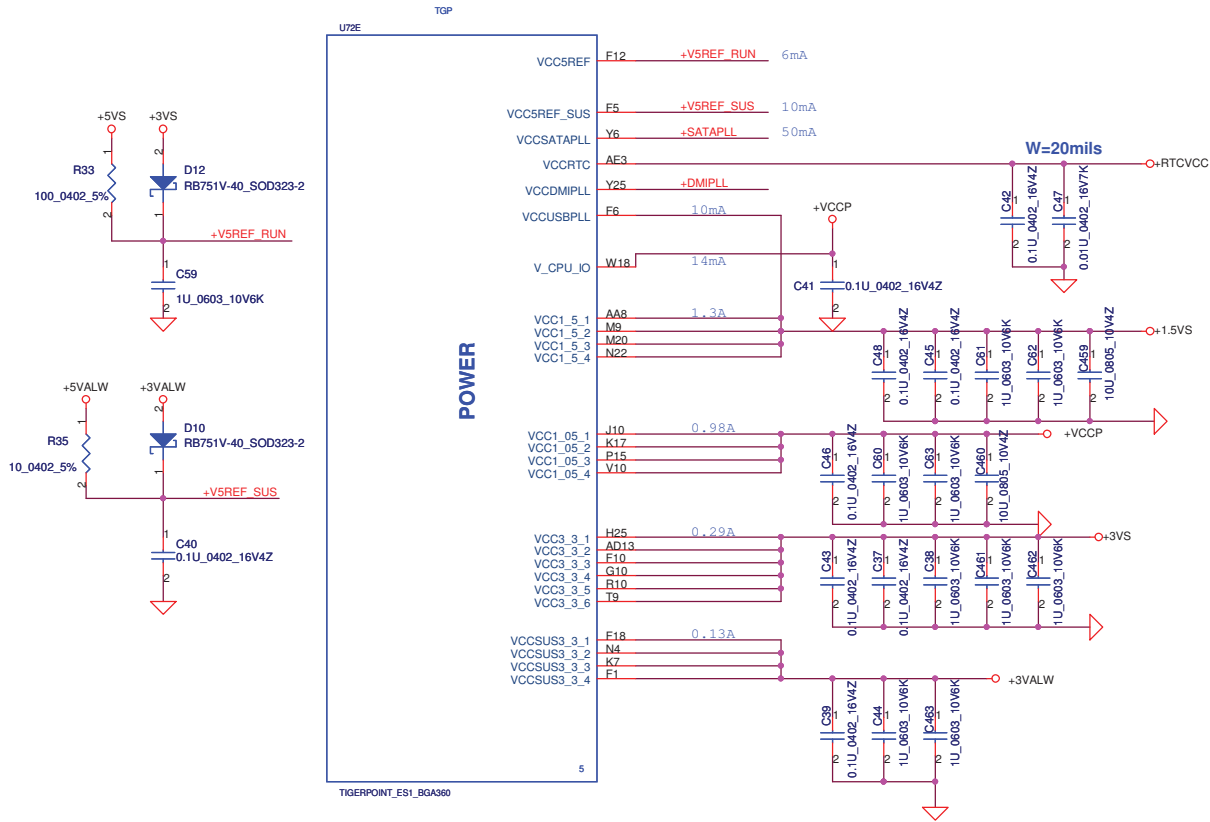


Change C368/C371 from 12pf to 15pf.022510.

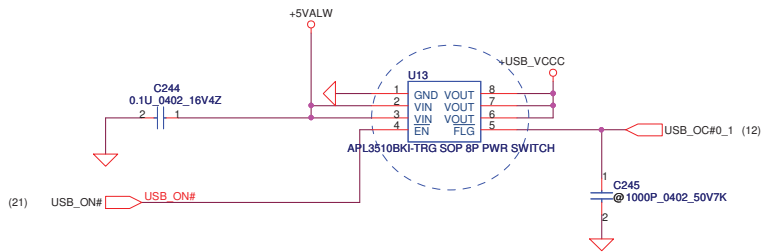
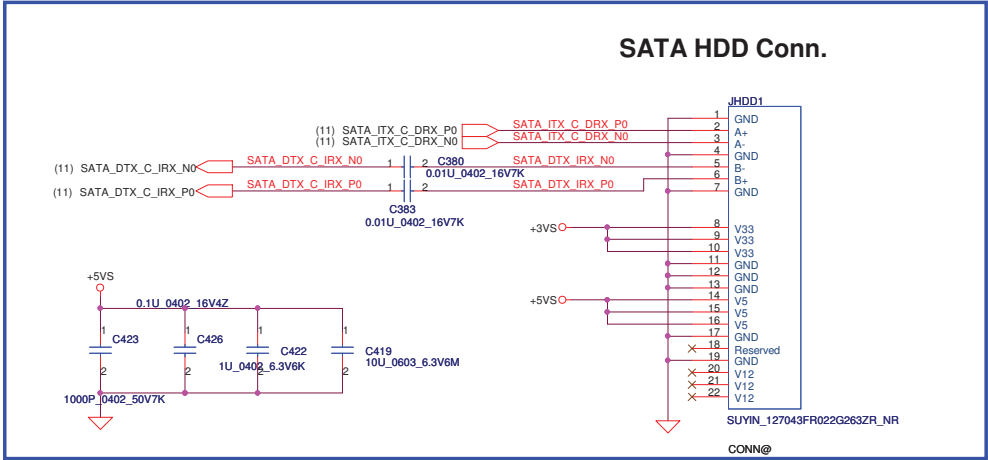
Change C368/C371 from 12pf to 15pf.022510.

Add +RTCVCC circuit 06/12

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Size	Document Number	NAV51 LA-6311P		Rev	1.0
Custom	Date:	Tuesday, April 13, 2010	Sheet	13	of 33



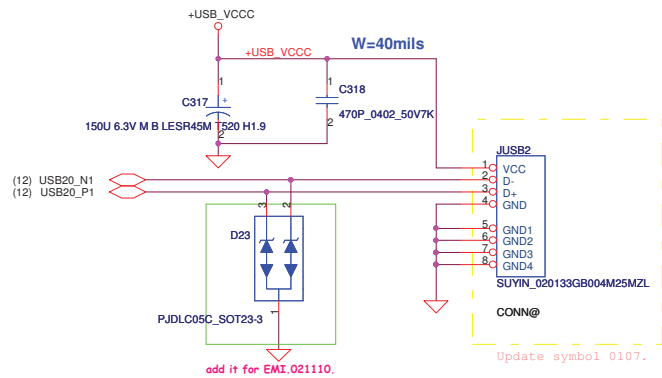
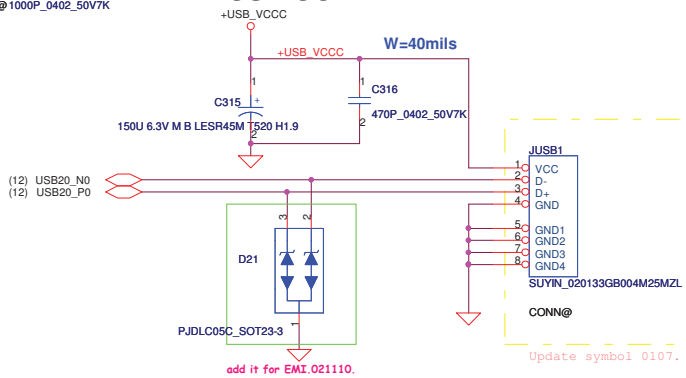
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				Document Number	NAV51 LA-6311P
				Date:	Tuesday, April 13, 2010
				Sheet	14 of 33



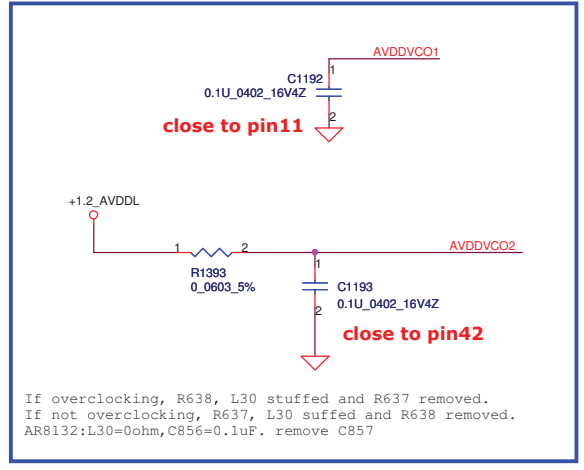
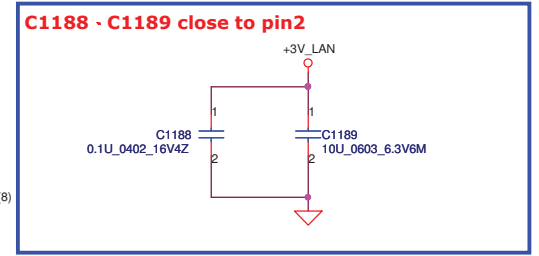
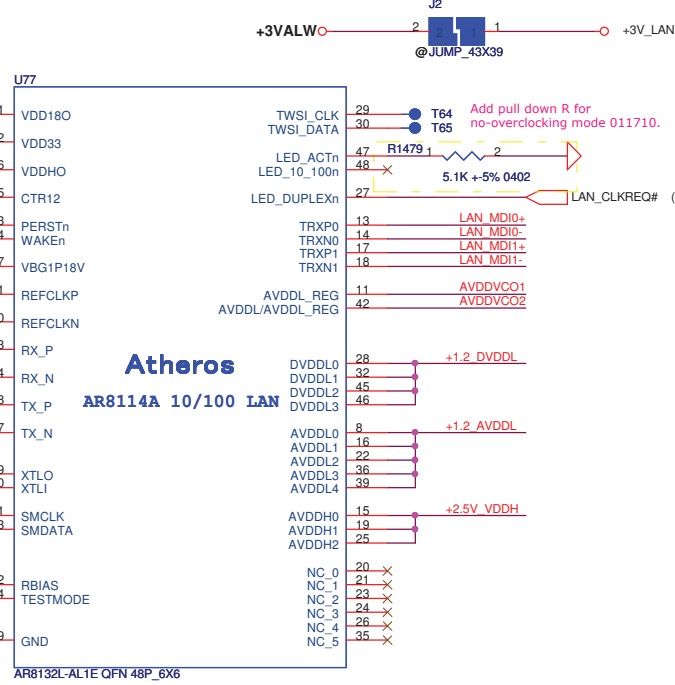
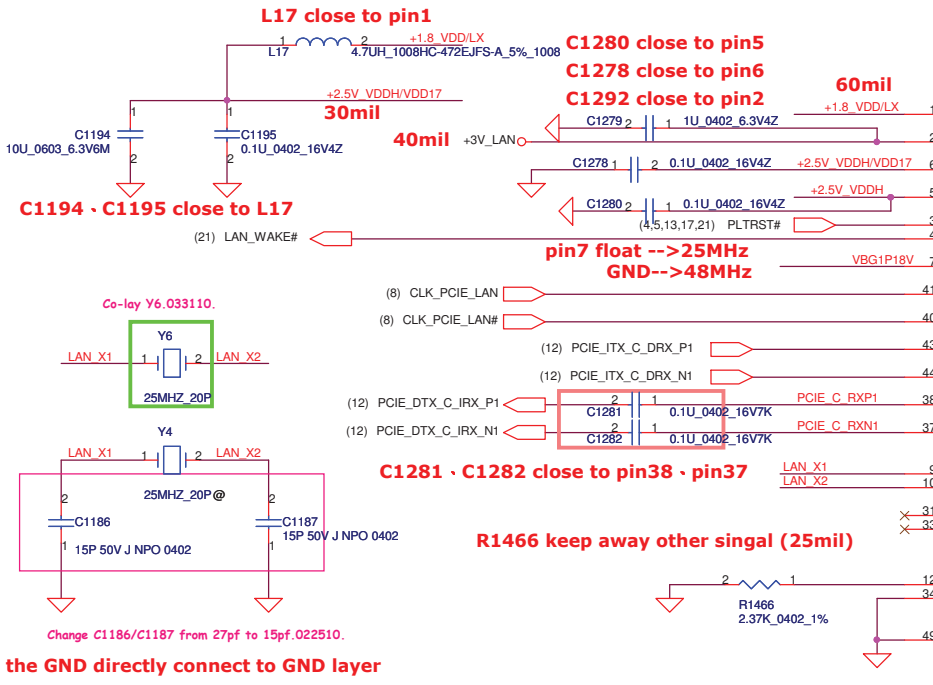
### USB CONN.1

Change JUSB1 JUSB2 to NEW P/N SP010906181 06/23

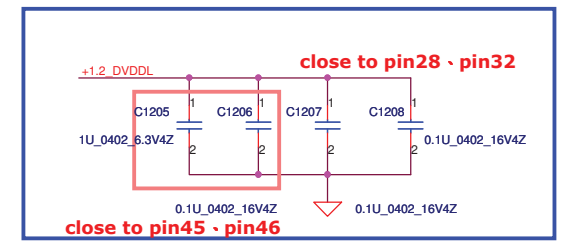
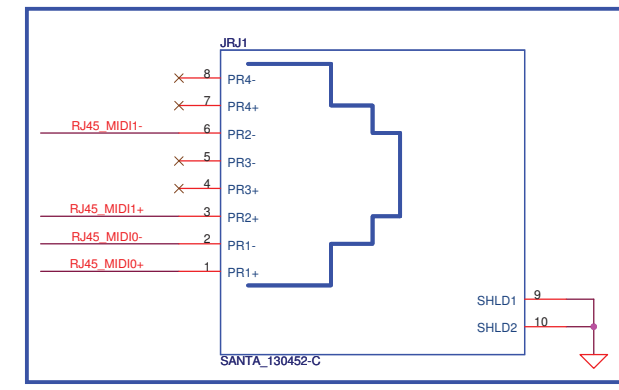
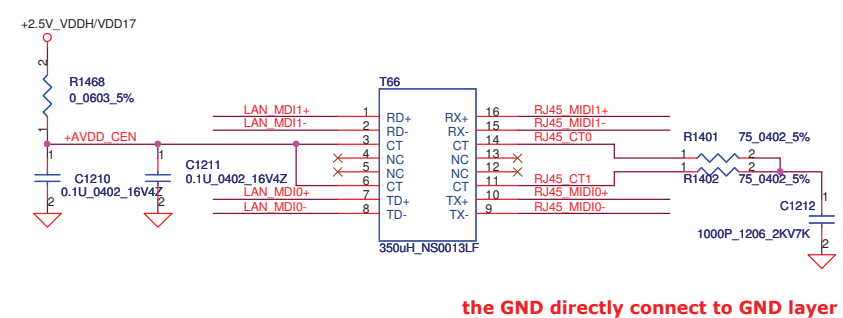
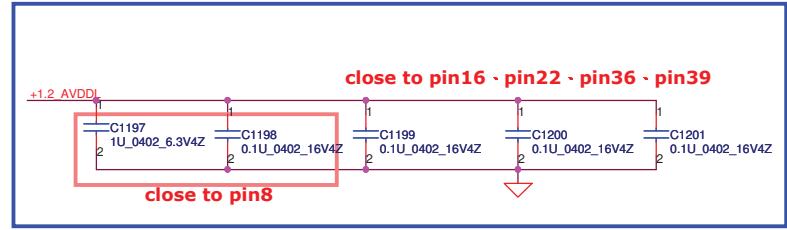
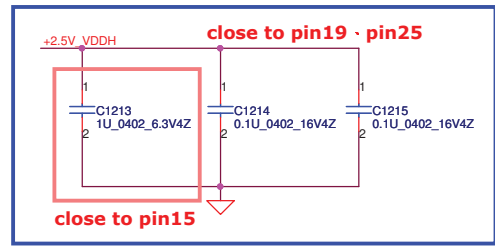
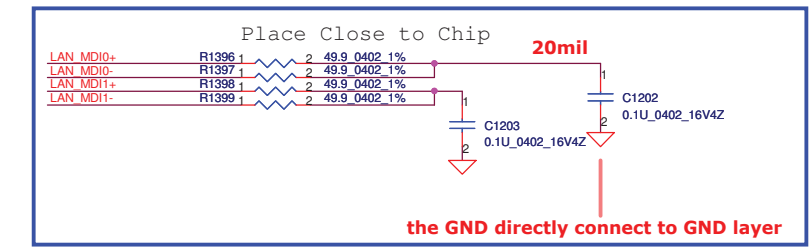
### USB CONN.2



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title <b>SATA,CONN. / USB CONN.</b>	
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				Date: Tuesday, April 13, 2010	Rev 0.2
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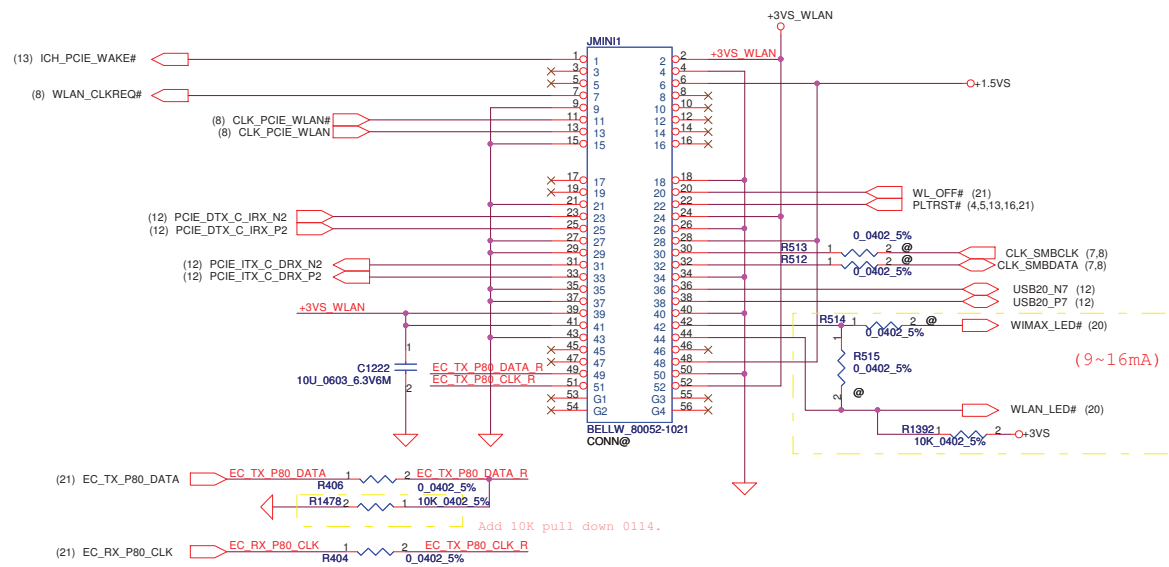
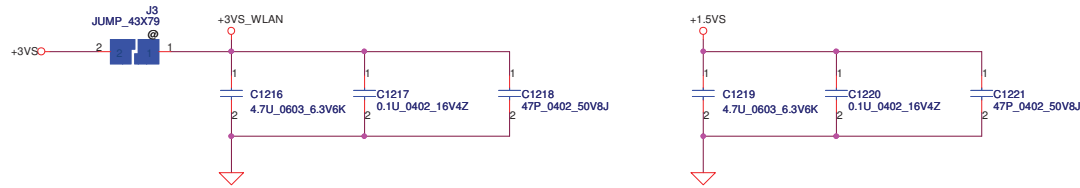
Change C1186/C1187 from 27pf to 15pf.022510.  
the GND directly connect to GND layer

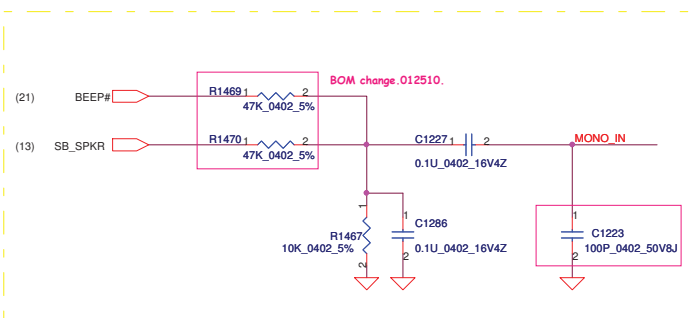


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Size	Custom	Document Number	NAV51 LA-6311P		Rev
Date:	Tuesday, April 13, 2010	Sheet	16	of	33

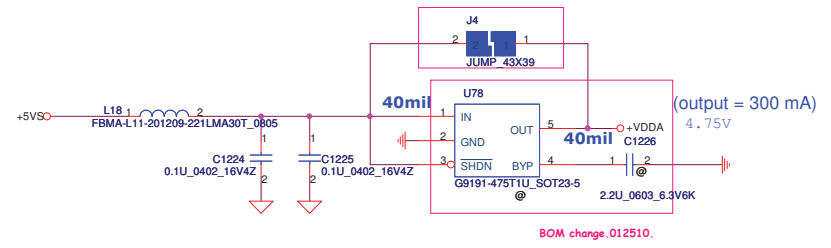


# Mini-Express Card for WLAN

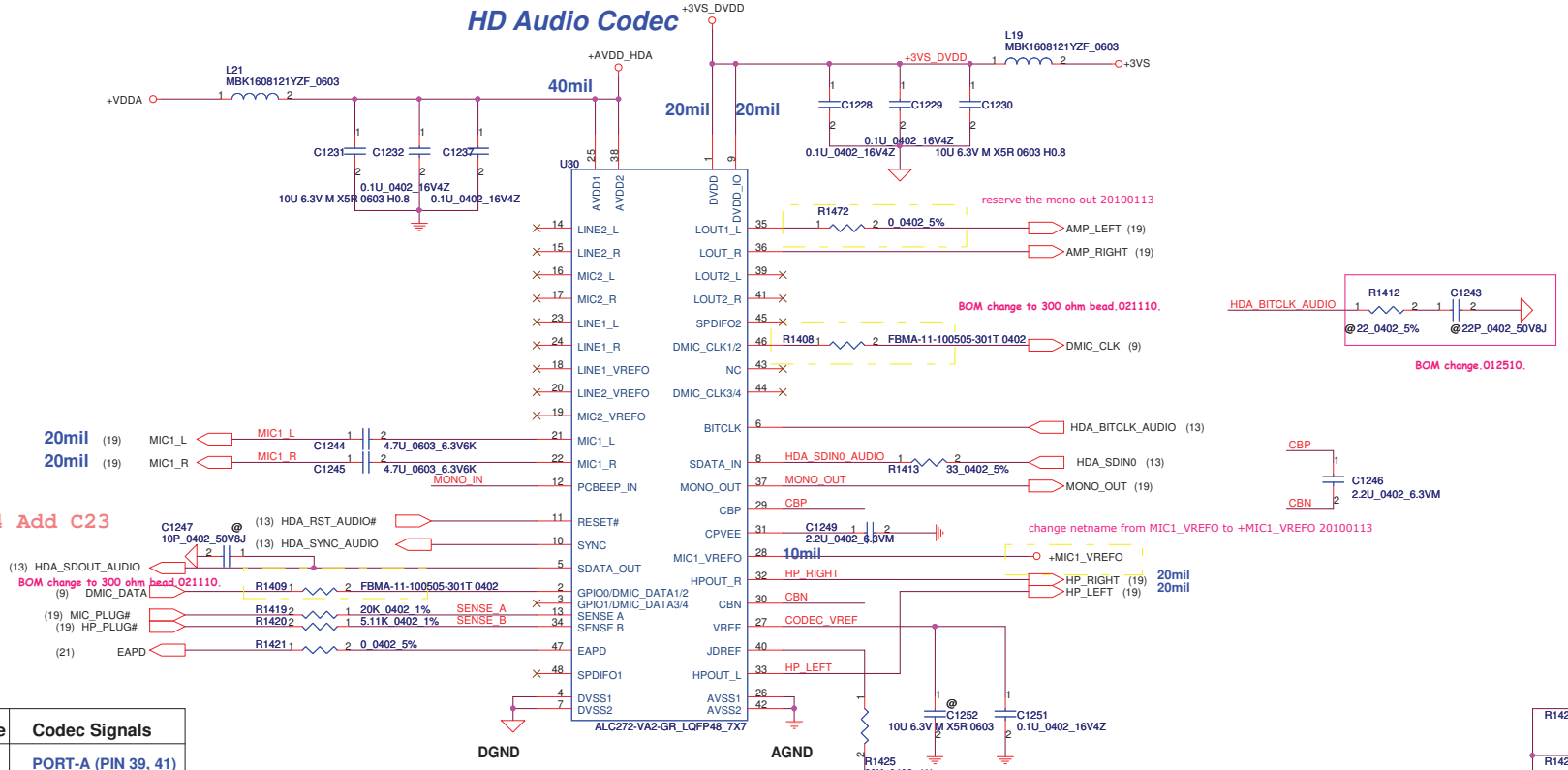




simplify the pcbecp circuit 011410.



### HD Audio Codec



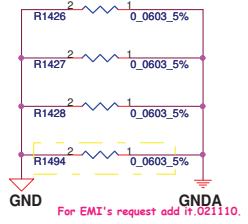
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Change to SA00002CI20 ALC272-VA2-GR

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Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Compal Electronics, Inc.			
Title: HD Audio Codec ALC272			
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change C1255 - C1256 - C1257 - C1258 - C1283 from 0.47uF to 0.1uF 20100113

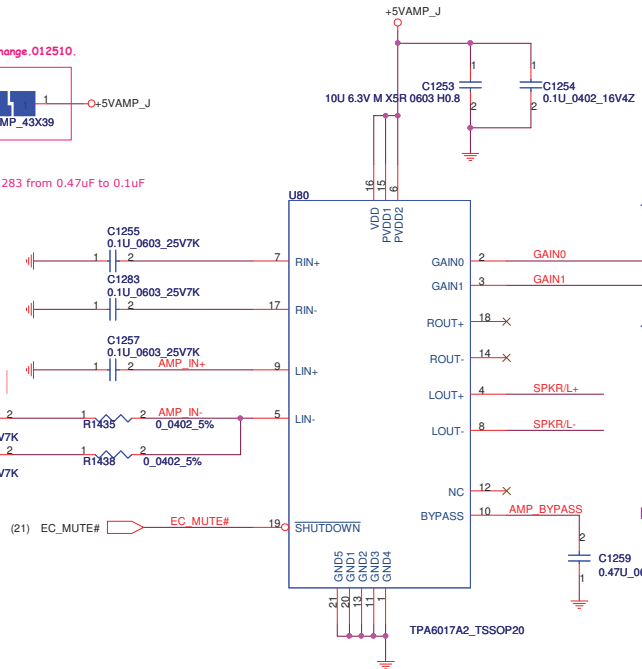
reserve the mono out 20100113

(18) MONO\_OUT → R1473 @ 0.402\_5%

(18) AMP\_LEFT → C1256 0.1U\_0603\_25V7K

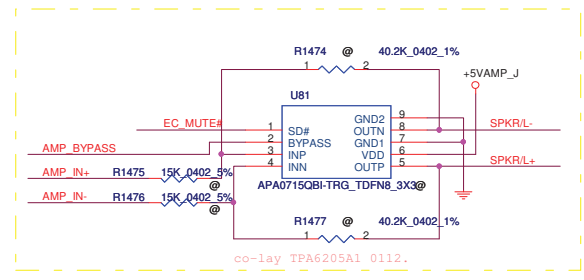
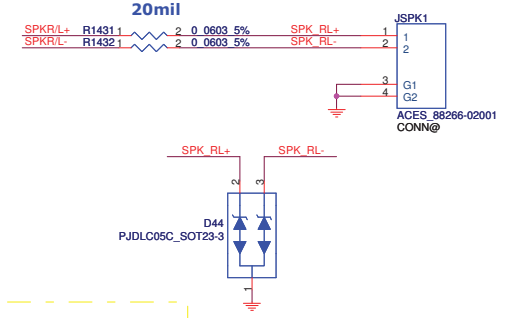
(18) AMP\_RIGHT → C1258 0.1U\_0603\_25V7K

(21) EC\_MUTE# → EC\_MUTE#

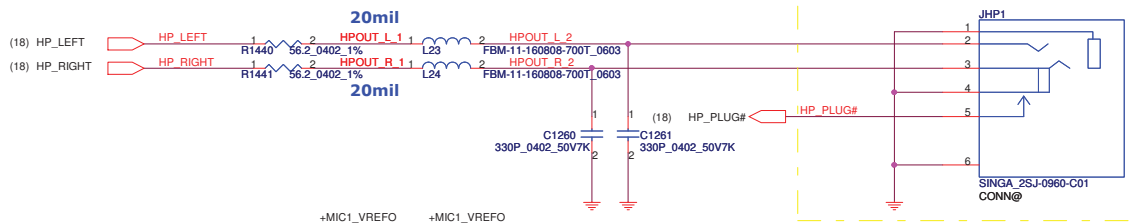


Keep 10 mil width

**Int. Speaker Conn.**

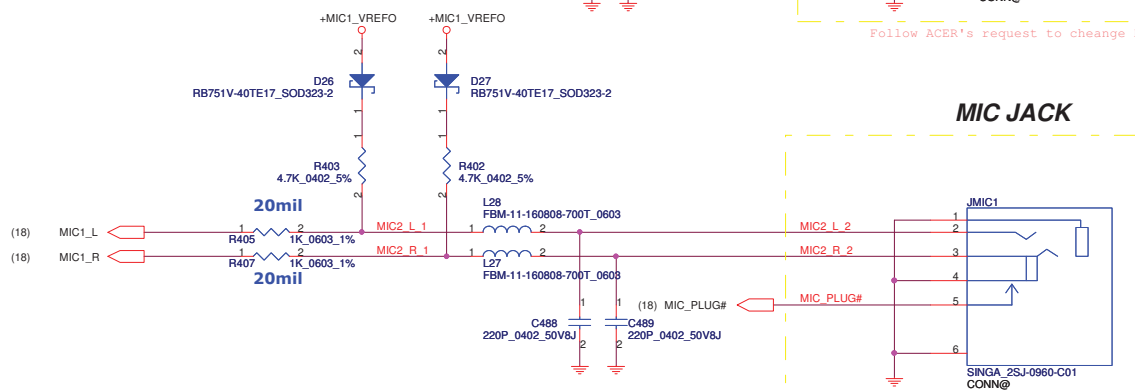


**(Use NAL00 PCB Footprint)  
Headphone Out**



Follow ACER's request to change HP CONN P/N.011410.

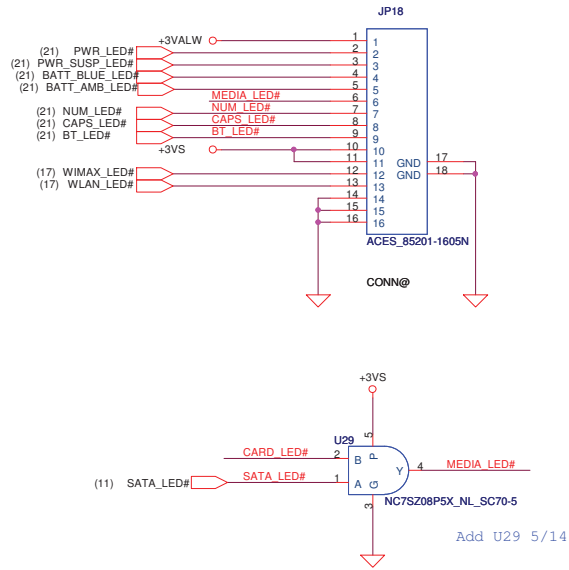
**MIC JACK**



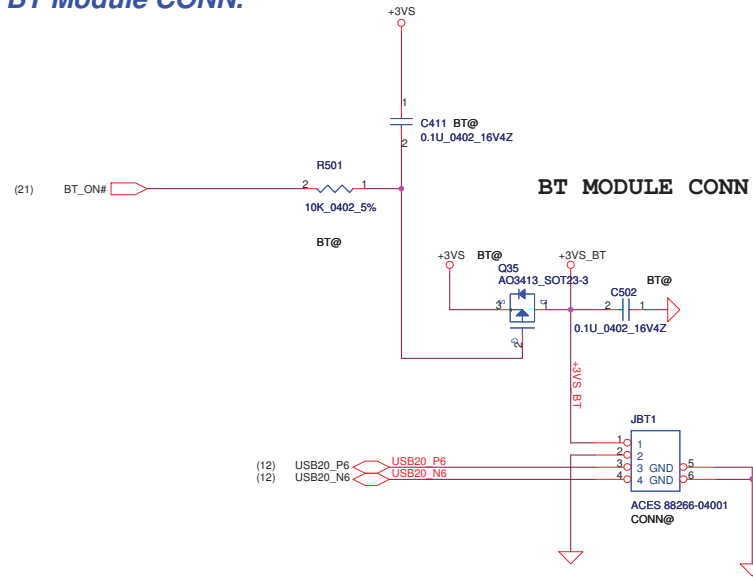
Follow ACER's request to change MIC CONN P/N.011410.

<b>Compal Electronics, Inc.</b>		
Title	<Title> <b>Amplifier &amp; Audio Jack</b>	Rev
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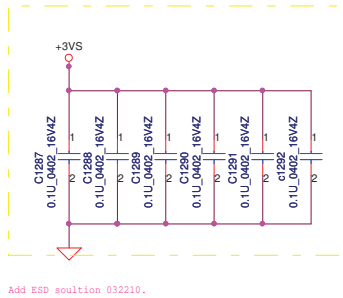
### LED PCB CONN.



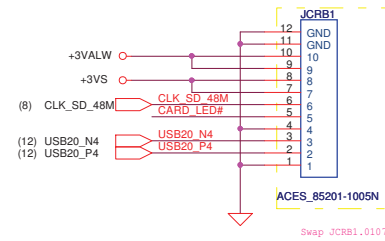
### BT Module CONN.



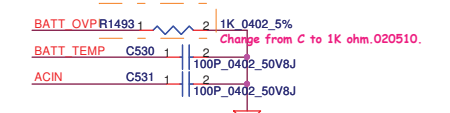
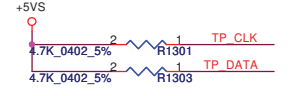
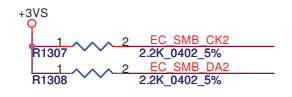
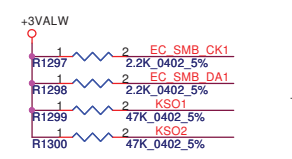
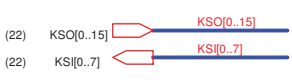
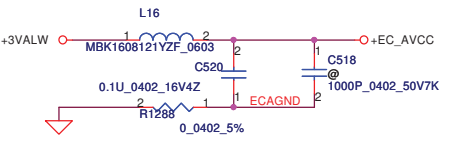
### ESD



### Card Reader CONN.



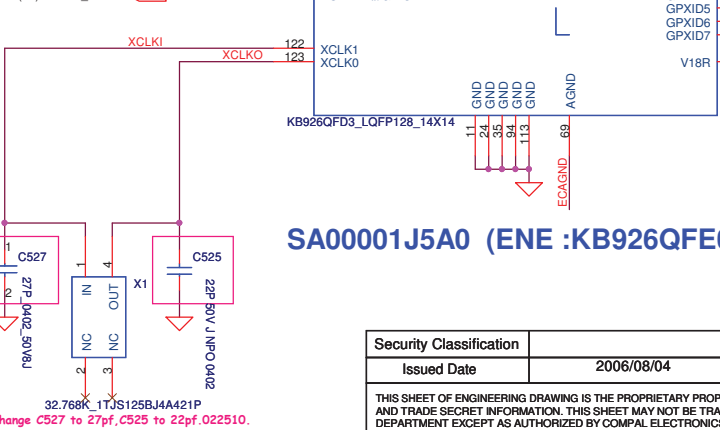
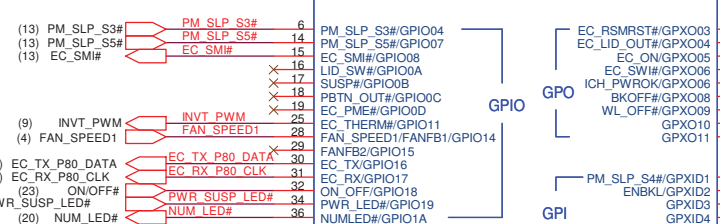
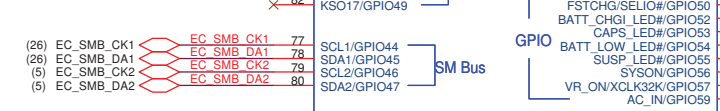
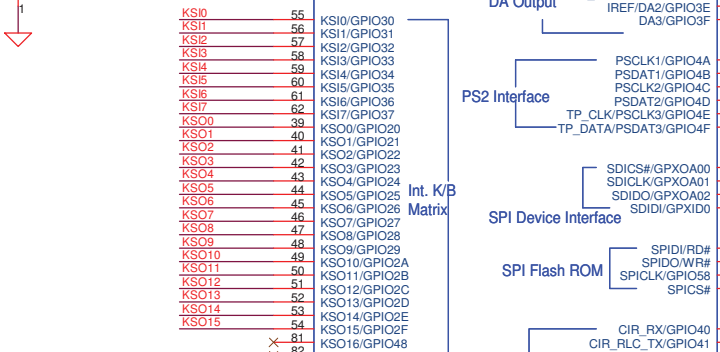
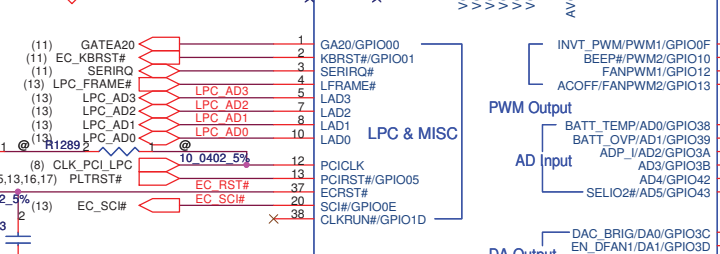
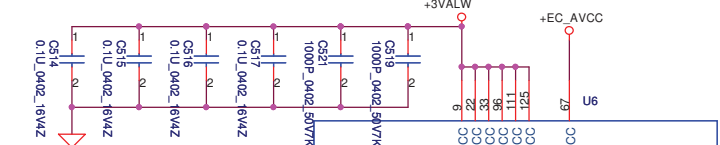
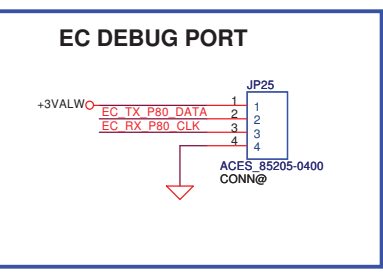
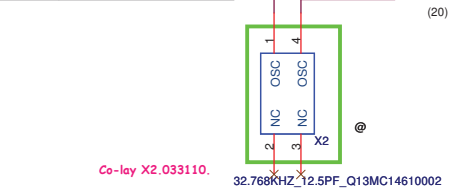
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				Card reader		
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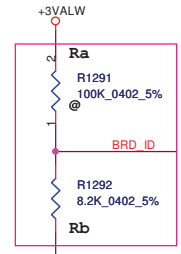
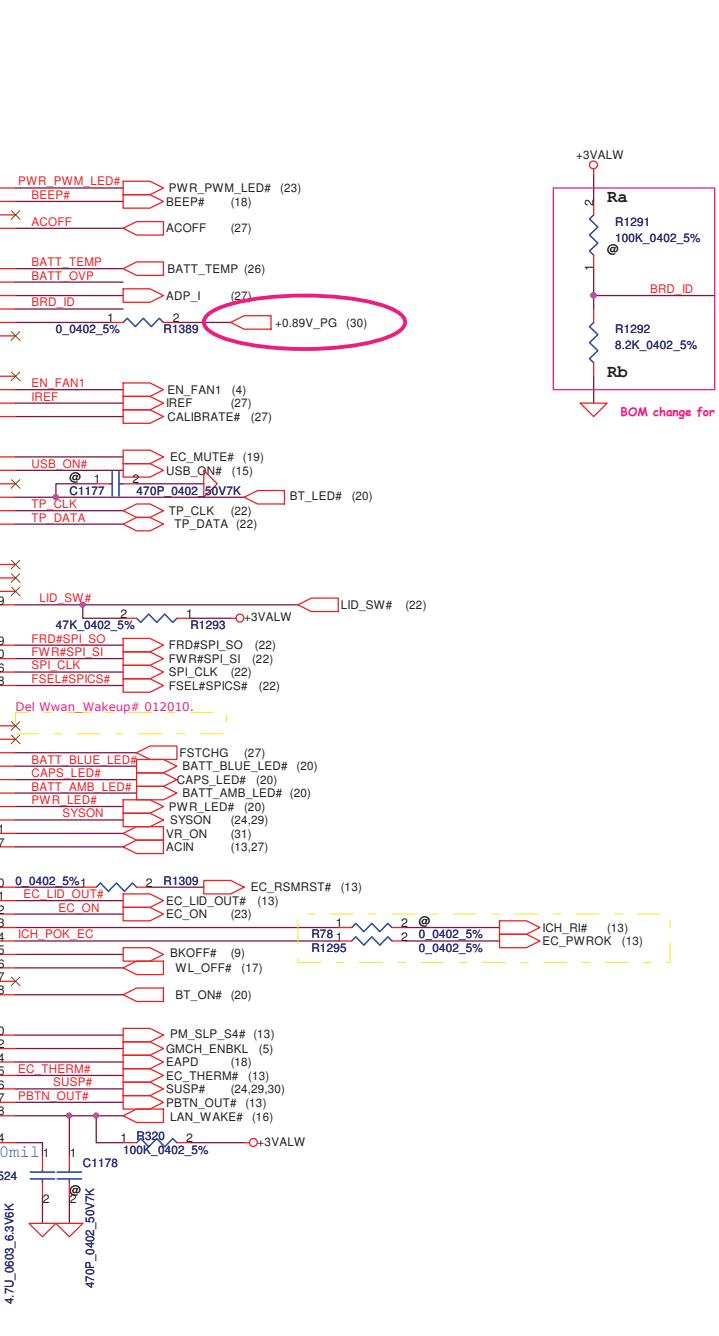
	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF#	v	v		Low

Swap to WLAN

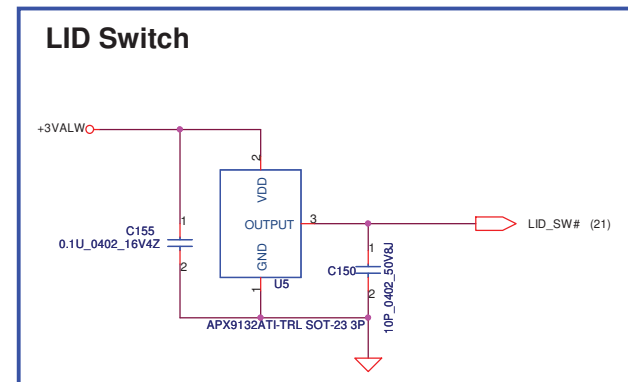
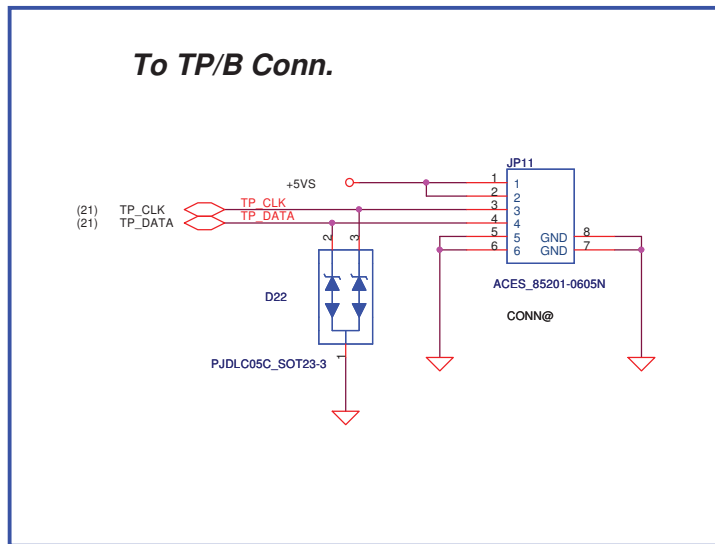
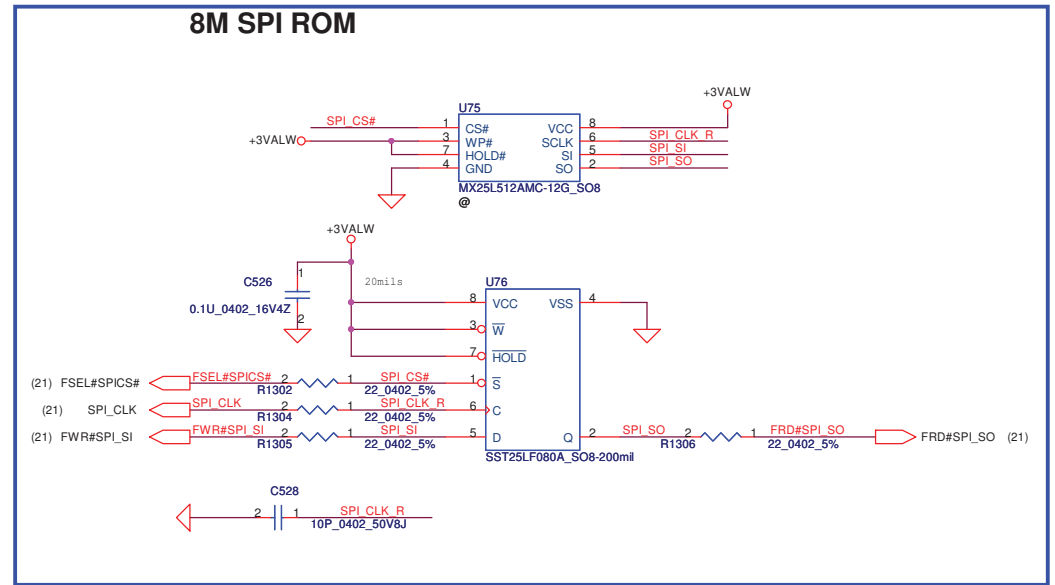
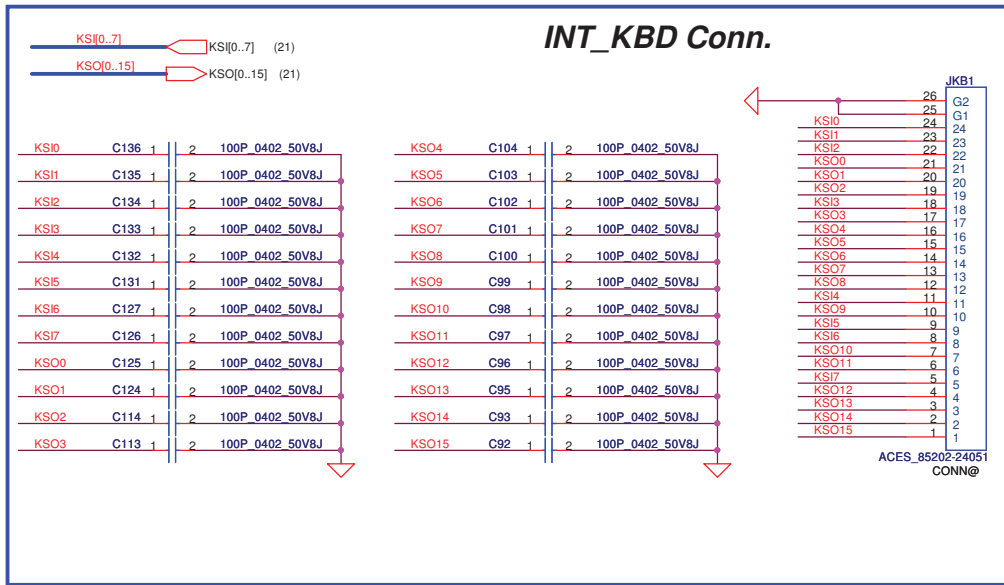
	KSO1
KSI1	WL_BTN#
KSI5	



### SA00001J5A0 (ENE :KB926QFE0)



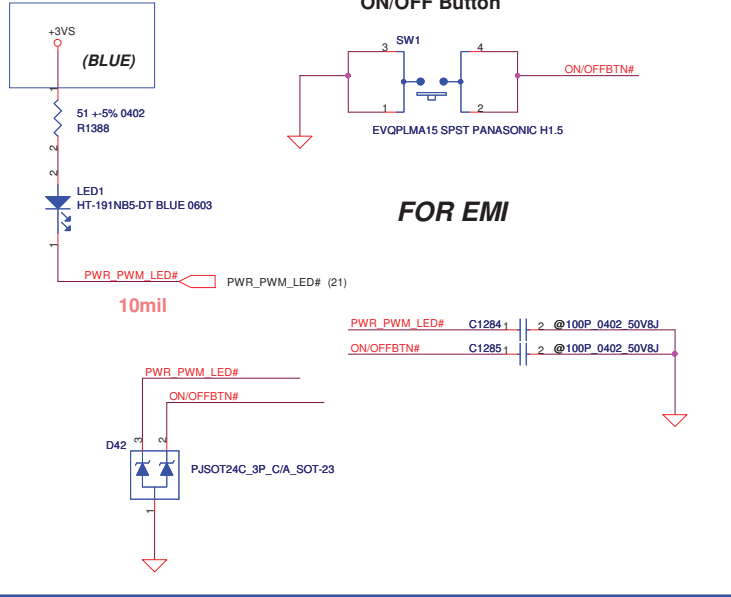
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Add For NAV50 07/06  
09/03 Change +5VS to +3VS

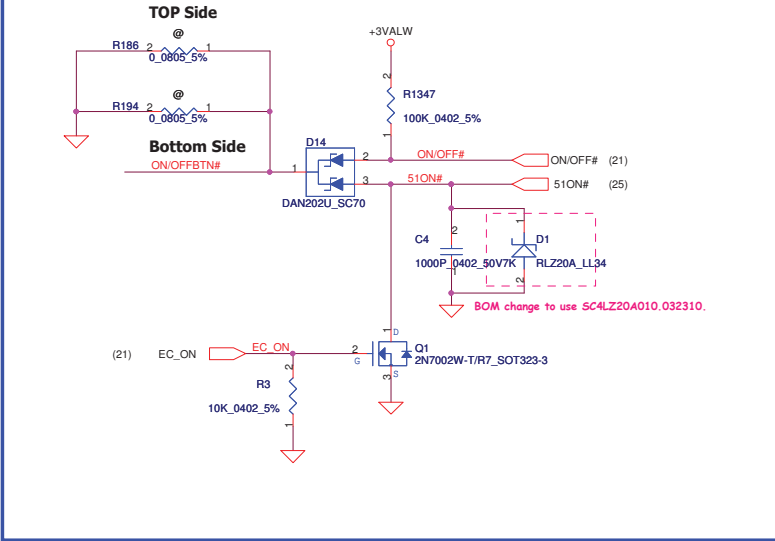
**ON/OFF Button**



**FOR EMI**

PWR\_PWM\_LED# C1284 1 2 @100P\_0402\_50V8J  
ON/OFFBTN# C1285 1 2 @100P\_0402\_50V8J

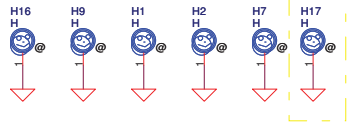
**Power Button Logic**



H\_3P2X3P7N



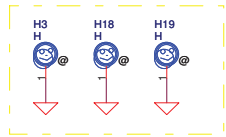
H\_2P6



H\_3P0



H\_3P3



H\_3P3N

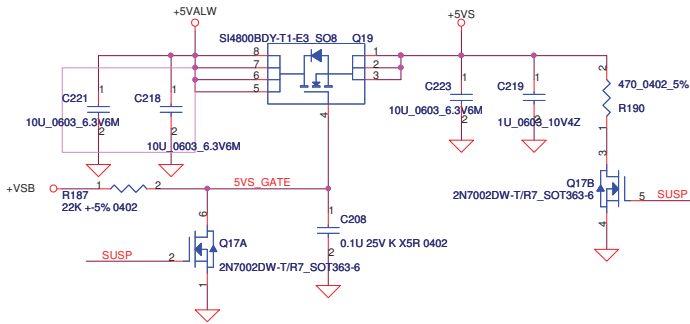


H\_3P4X3P2N

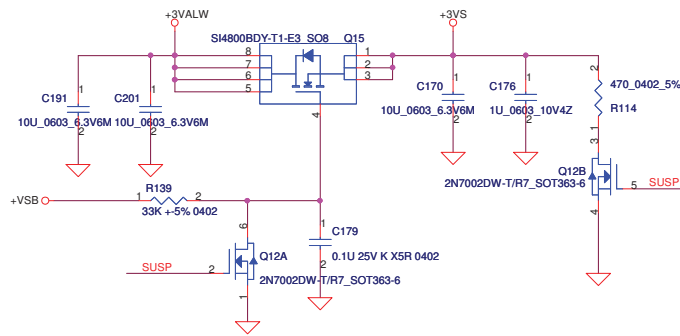


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Date: Tuesday, April 13, 2010			Sheet: 23 of 33	Document Number NAV51 LA-6311P Rev 0.2

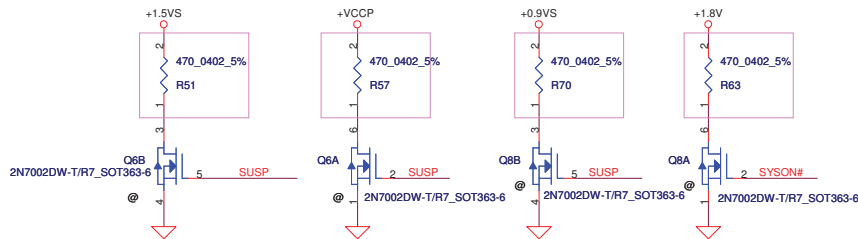
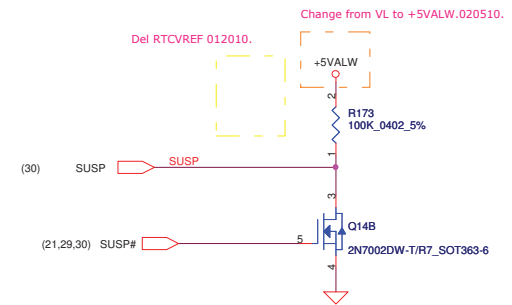
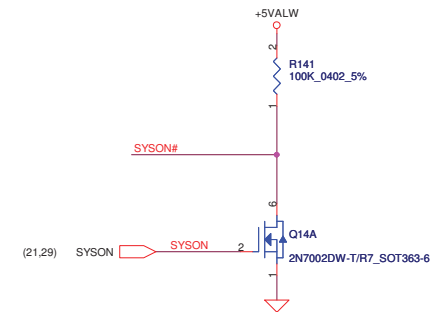
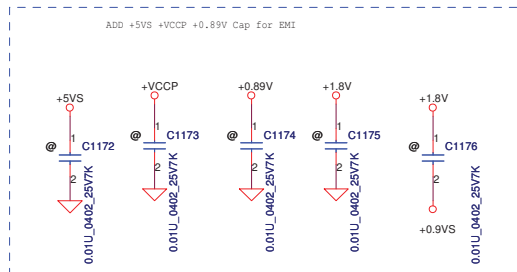
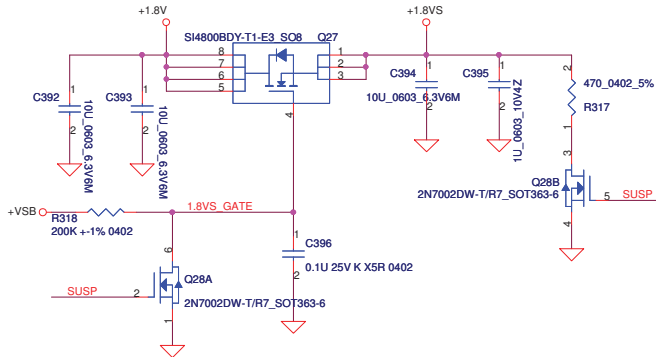
**+5VALW TO +5VS**



**+3VALW TO +3VS**

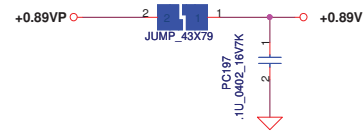
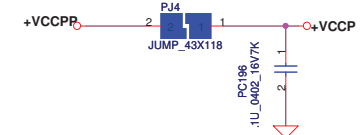
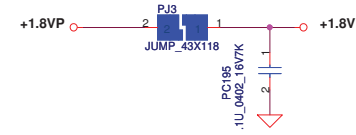
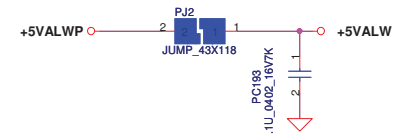
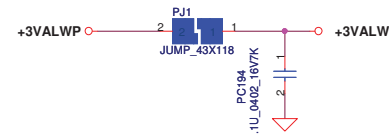
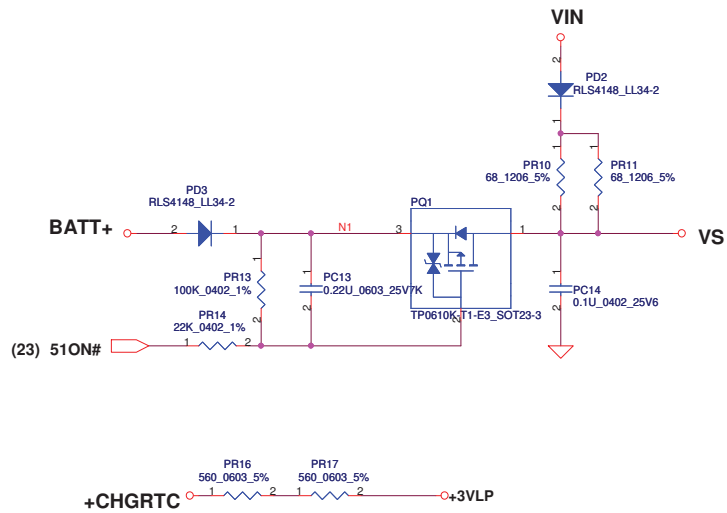
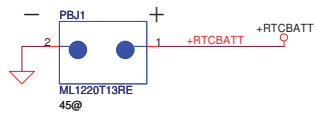
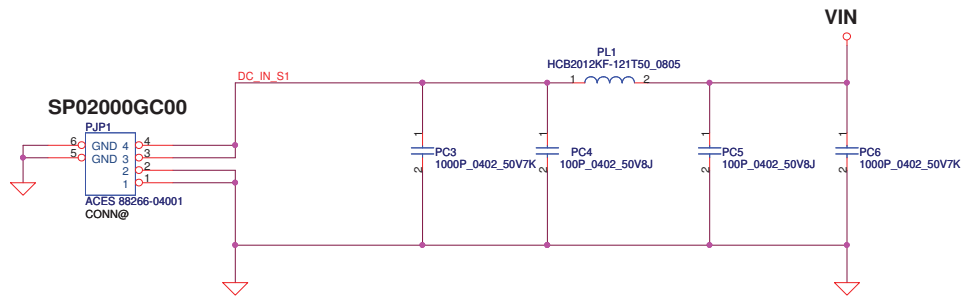


**+1.8V to +1.8VS**



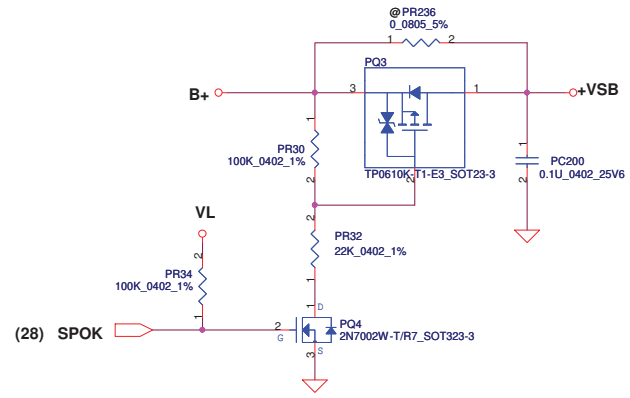
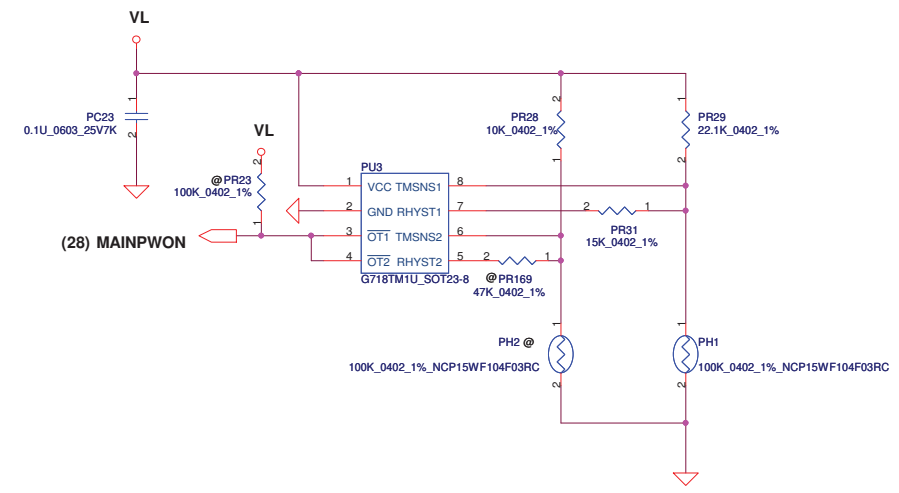
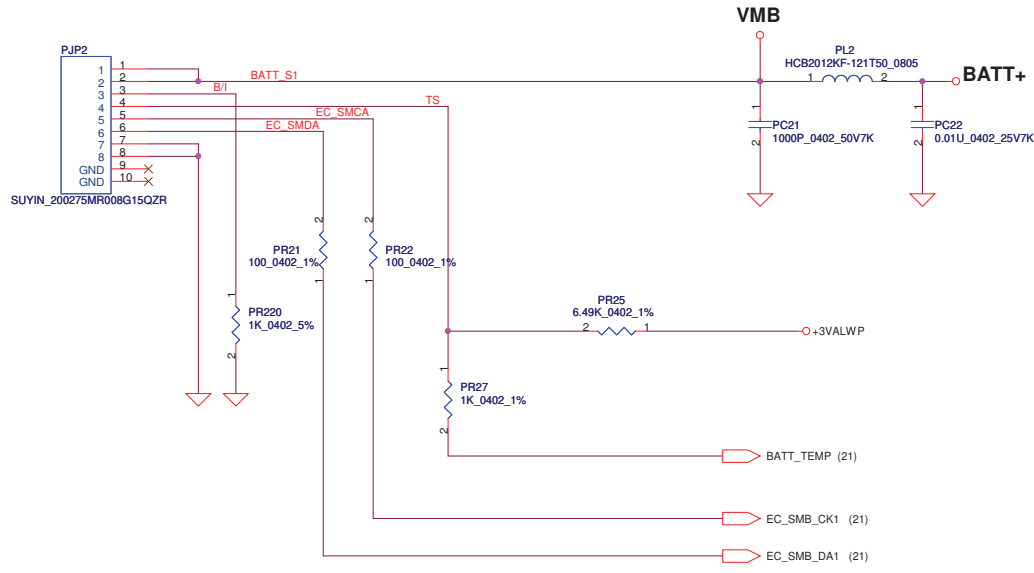
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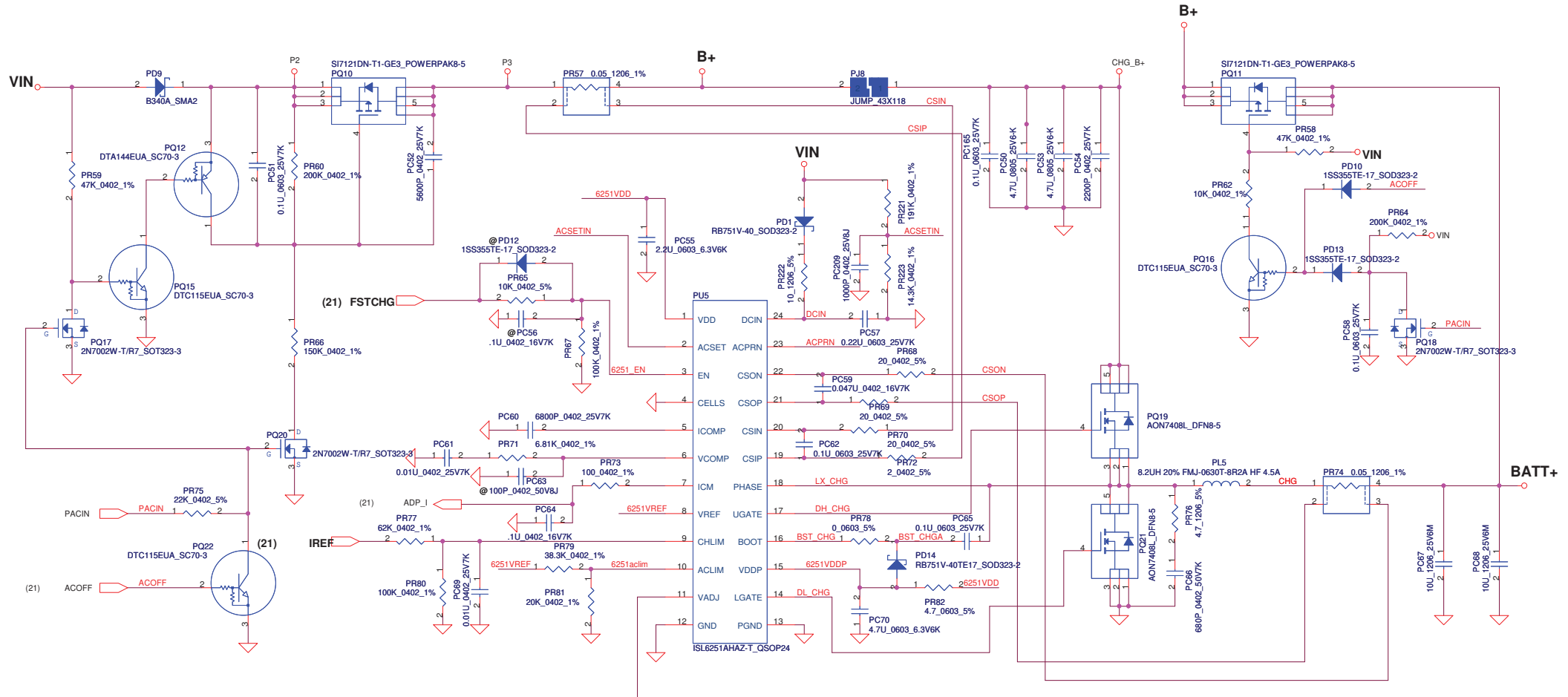


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Size	Document Number	Rev		0.1	
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PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C  
 Recovery at 72 degree C



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Size	Custom	Document Number	NAV51 LA-6311P	Rev	0.1
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Iada=0~1.58A(30W) CP = 85%\*Iada ; CP = 1.343A

CP mode  
 $V_{acLim} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$   
 $I_{input} = (1 / 0.05) * ((0.05 * V_{acLim}) / (2.39 + 0.05))$   
 where  $V_{acLim} = 0.8199V$ ,  $I_{input} = 1.343A$

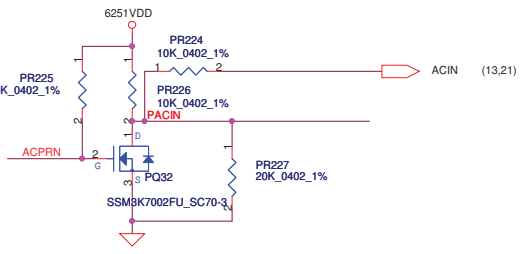
CC=0.3~1.76A  
 $I_{REF} = 1.62 * I_{charge}$   
 $I_{REF} = 0.486V \sim 2.85V$   
 $3.24V \implies 2A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

VADJ-->VREF-->4.41V  
 VADJ-->Ground-->3.59V  
 $V_{cell} = (0.175 * VADJ + 3.99)$

(21) CALIBRATE#  
 PR83 15.4K\_0402\_1%  
 PR85 31.6K\_0402\_1%

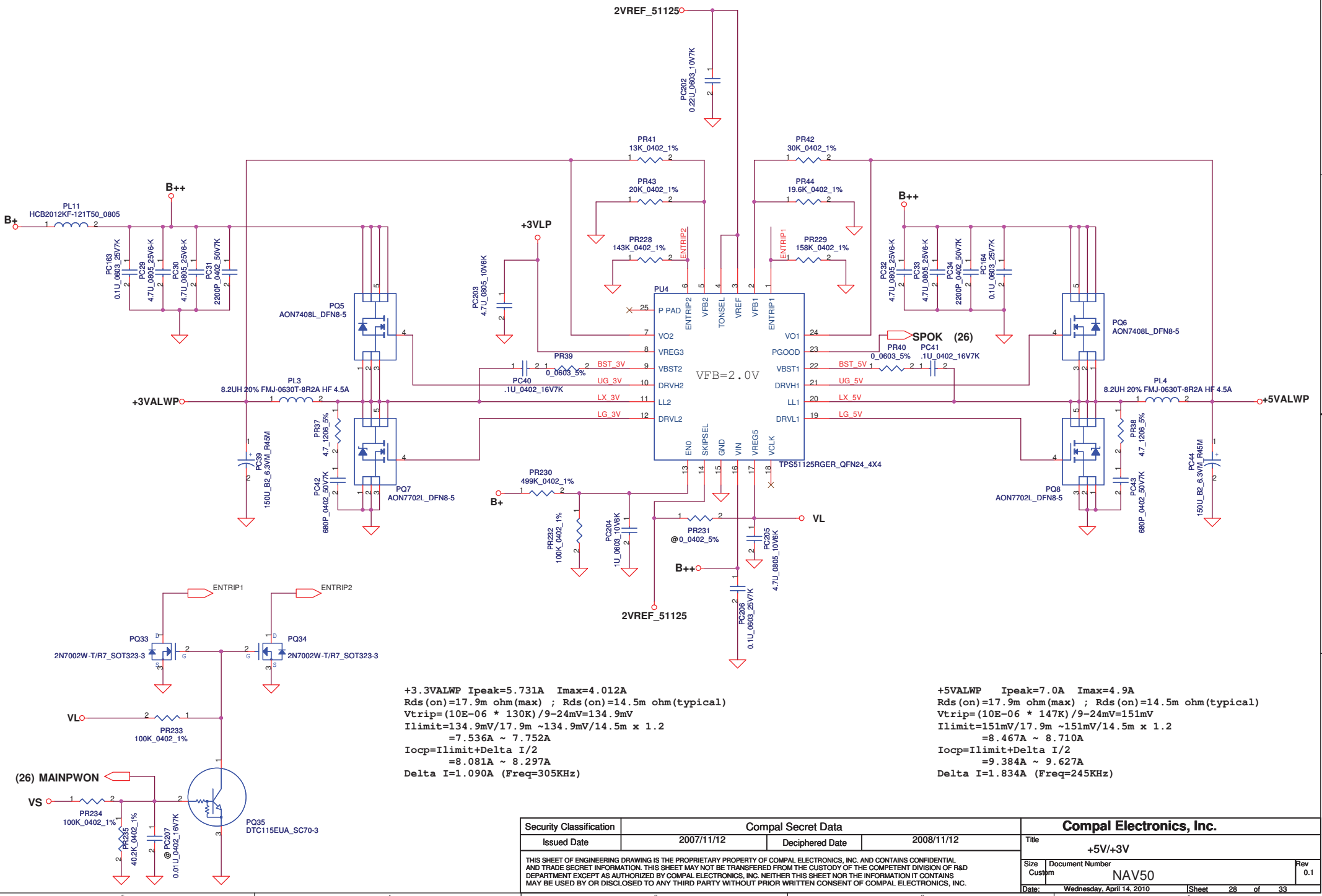
$V_{th, rise (typical)} = ((191K / 14.3K) + 1) * 1.26$   
 $= 18.89V$   
 $V_{th, fall (typical)} = ((191K / 14.3K) + 1) * 1.26 - 3.4\mu A * 191K$   
 $= 17.43V$



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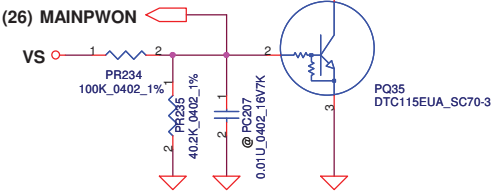
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<b>CHARGER</b>			
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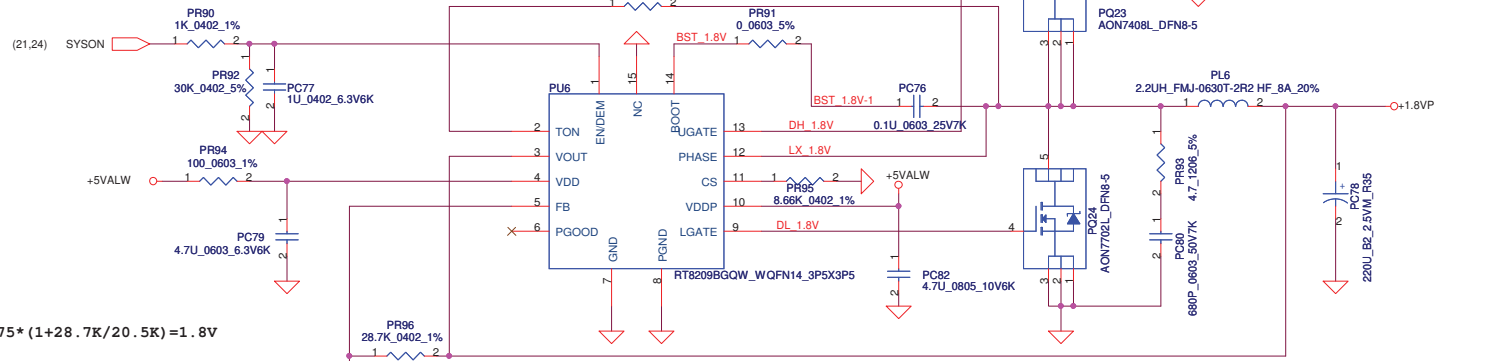


+3.3VALWP Ipeak=5.731A Imax=4.012A  
 Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)  
 Vtrip=(10E-06 \* 130K)/9-24mV=134.9mV  
 Ilimit=134.9mV/17.9m ~134.9mV/14.5m x 1.2  
 =7.536A ~ 7.752A  
 Iocp=Ilimit+Delta I/2  
 =8.081A ~ 8.297A  
 Delta I=1.090A (Freq=305KHz)

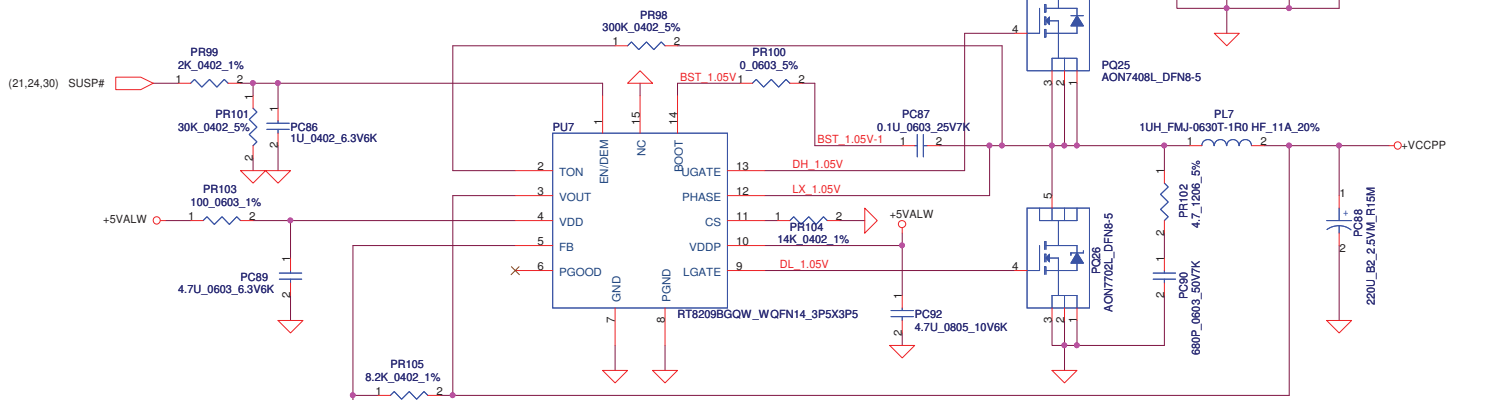
+5VALWP Ipeak=7.0A Imax=4.9A  
 Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)  
 Vtrip=(10E-06 \* 147K)/9-24mV=151mV  
 Ilimit=151mV/17.9m ~151mV/14.5m x 1.2  
 =8.467A ~ 8.710A  
 Iocp=Ilimit+Delta I/2  
 =9.384A ~ 9.627A  
 Delta I=1.834A (Freq=245KHz)



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				+5V/+3V	
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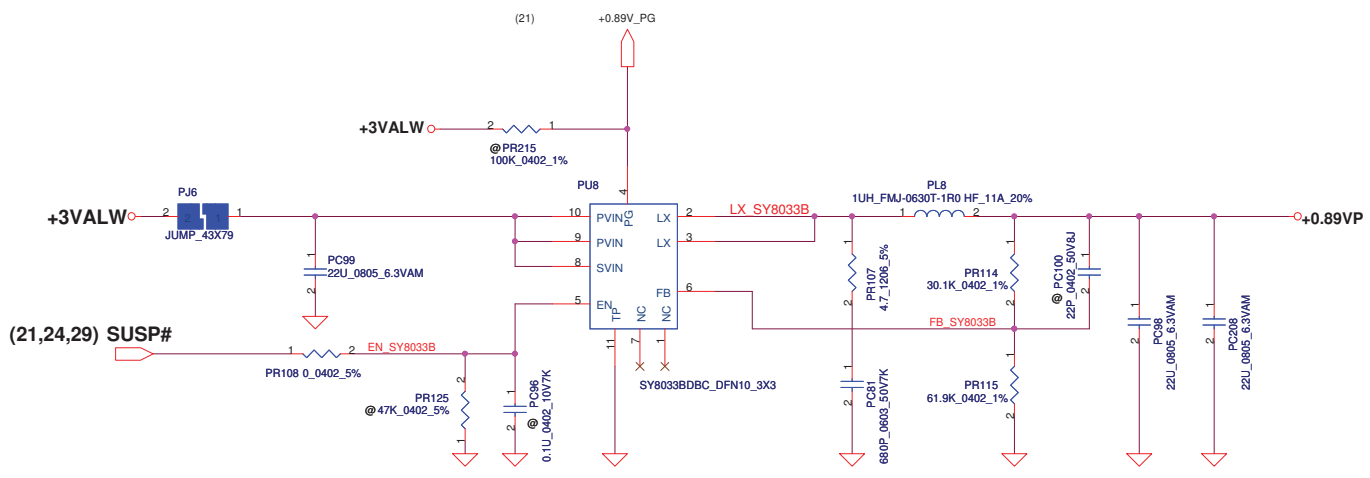


$V_o = 1.8V$      $V_{FB} = 0.75V$   
 $V_o = V_{FB} * (1 + PR96/PR97) = 0.75 * (1 + 28.7K/20.5K) = 1.8V$   
 $f_{sw} = 328KHz$   
 $C_{out} ESR = 15m\ \Omega$      $R_{dson(max)} = 17.9m\ \Omega$      $R_{dson(typical)} = 14.5m\ \Omega$   
 $I_{peak} = 4.97A$ ,  $I_{max} = 3.479A$ ,  $I_{ocp} = 5.964A$   
 $\Delta I = ((19 - 1.8) * (1.8/19)) / (2.2u * 328K) = 2.259A$   
 $\Rightarrow 1/2 \Delta I = 1.129A$   
 $V_{trip} = R_{trip} * I_{0uA} = 8.66K * 10uA = 0.0866V$   
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.129$   
 $= 0.0866 / (0.0179) + 1.129 = 5.967A$   
 $I_{ocpmax} = (0.0866 / (0.0145 * 1.2)) + 1.129A = 6.106A$   
 $I_{ocp} = 5.967A \sim 6.106A$

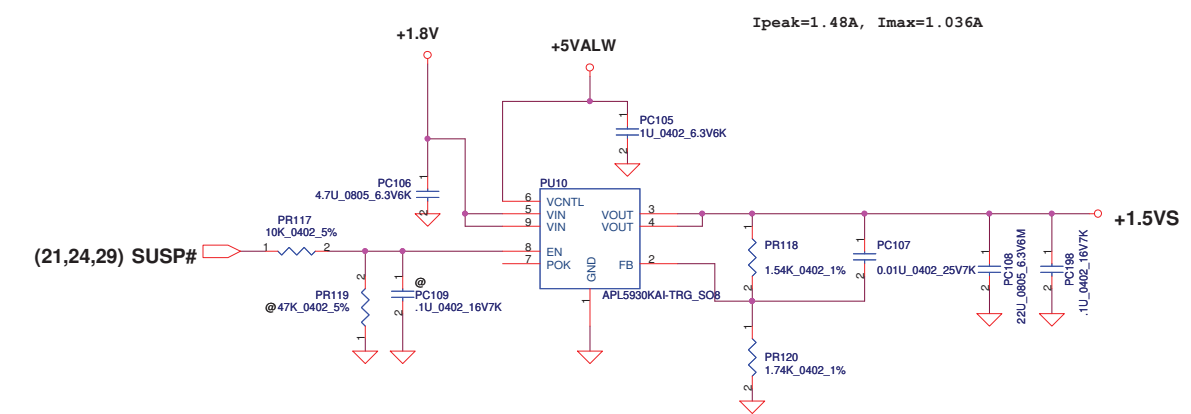


$V_o = 1.05V$      $V_{FB} = 0.75V$   
 $V_o = V_{FB} * (1 + PR105/PR106) = 0.75 * (1 + 8.2K/20.5K) = 1.05V$   
 $f_{sw} = 280KHz$   
 $C_{out} ESR = 15m\ \Omega$      $R_{dson(max)} = 17.9m\ \Omega$      $R_{dson(typical)} = 14.5m\ \Omega$   
 $I_{peak} = 3.124A$ ,  $I_{max} = 2.187A$ ,  $I_{ocp} = 3.749A$   
 $\Delta I = ((19 - 1.05) * (1.05/19)) / (1.5u * 280K) = 3.549A$   
 $\Rightarrow 1/2 \Delta I = 1.774A$   
 $V_{trip} = R_{trip} * I_{0uA} = 14K * 10uA = 0.14V$   
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.774$   
 $= 0.14 / (0.0179) + 1.774 = 9.596A$   
 $I_{ocpmax} = (0.14 / (0.0145 * 1.2)) + 1.774A = 9.820A$   
 $I_{ocp} = 9.596A \sim 9.820A$

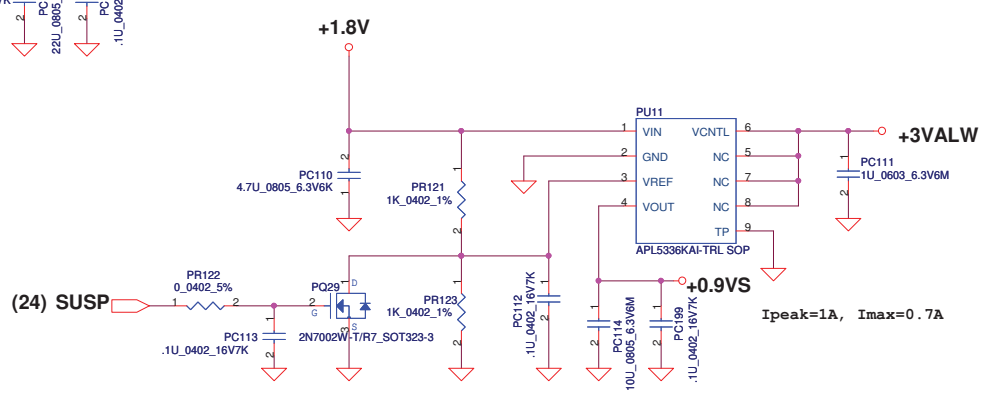
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<Vo=0.89V> VFB=0.6V  
 $V_o = V_{FB} * (1 + PR_{114} / PR_{115}) = 0.6 * (1 + 30.1K / 61.9) = 0.89V$   
 $I_{peak} = 2.64A, I_{max} = 1.848A$

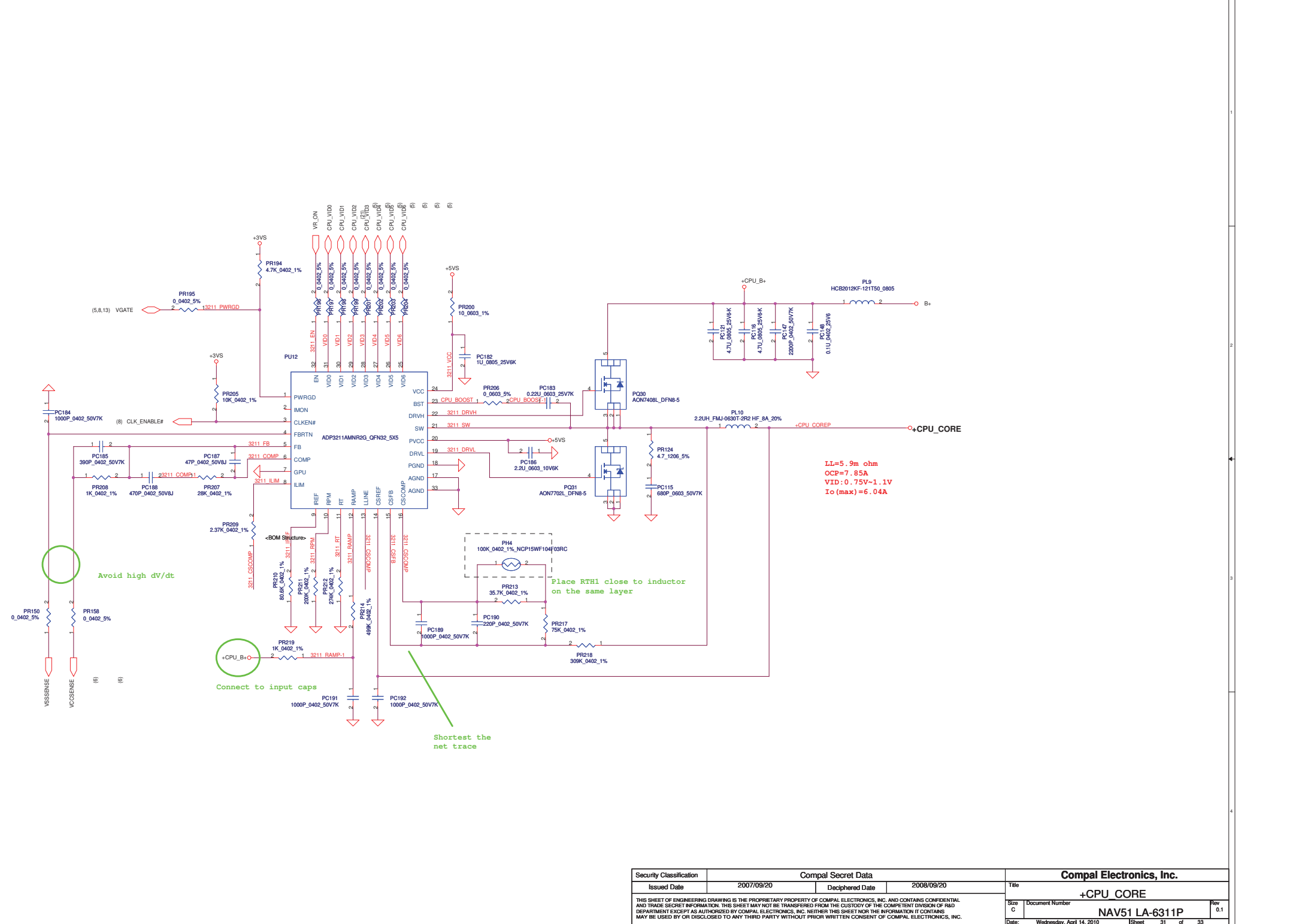


$I_{peak} = 1.48A, I_{max} = 1.036A$



$I_{peak} = 1A, I_{max} = 0.7A$

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LL=5.9m ohm  
 OCP=7.85A  
 VID:0.75V-1.1V  
 Io(max)=6.04A

Avoid high dV/dt

Connect to input caps

Shortest the net trace

Place RTH1 close to inductor on the same layer

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						2010.1.8	EVT
2						2010.1.11	EVT
3							
4							
5							
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	PU8 Vin change to +3VALW	modify for HW layout request	0.1	30		2010.1.8	EVT
2	PU4 Pin25 change to no connect	modify for 3/5V load balance(TI FAE request)	0.1	28		2010.1.11	EVT
3							
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