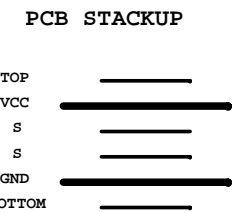
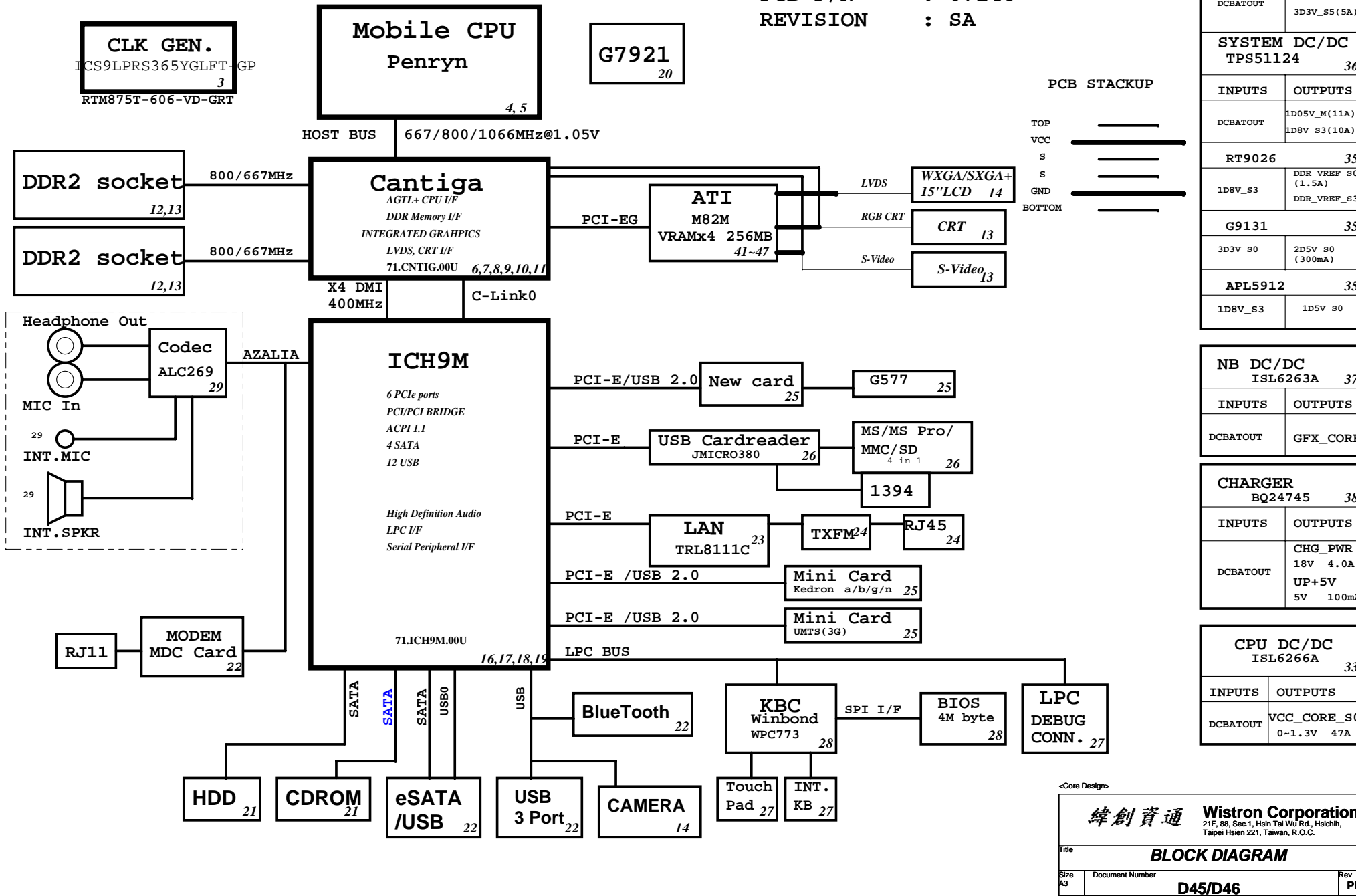


# D45/D46 Block Diagram

Project code: 91.4J001.001--D45  
 91.4K001.001--D46  
 PCB P/N : 07248  
 REVISION : SA



| SYSTEM DC/DC TPS51125 34 |                          |
|--------------------------|--------------------------|
| INPUTS                   | OUTPUTS                  |
| DCBATOUT                 | 5V_S5(5A)<br>3D3V_S5(5A) |

| SYSTEM DC/DC TPS51124 36 |                                  |
|--------------------------|----------------------------------|
| INPUTS                   | OUTPUTS                          |
| DCBATOUT                 | 1D05V_M(11A)<br>1D8V_S3(10A)     |
| RT9026 35                |                                  |
| 1D8V_S3                  | DDR_VREF_S0(1.5A)<br>DDR_VREF_S3 |
| G9131 35                 |                                  |
| 3D3V_S0                  | 2D5V_S0(300mA)                   |
| APL5912 35               |                                  |
| 1D8V_S3                  | 1D5V_S0                          |

| NB DC/DC ISL6263A 37 |          |
|----------------------|----------|
| INPUTS               | OUTPUTS  |
| DCBATOUT             | GFX_CORE |

| CHARGER BQ24745 38 |  |
|--------------------|--|
| INPUTS             | OUTPUTS                                  |
| DCBATOUT           | CHG_PWR<br>18V 4.0A<br>UP+5V<br>5V 100mA |

| CPU DC/DC ISL6266A 33 |                           |
|-----------------------|---------------------------|
| INPUTS                | OUTPUTS                   |
| DCBATOUT              | VCC_CORE_S0<br>0~1.3V 47A |

<Core Design>

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Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **D45/D46** Rev: **PD**

Date: Friday, March 14, 2008 Sheet 1 of 47

# ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

| Signal                        | Usage/When Sampled   | Comment   |
|-------------------------------|--|---|
| HDA_SDOUT                     | XOR Chain Entrance/<br>PCIE Port Config1 bit1,<br>Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down        |
| HDA_SYNC                      | PCIE config1 bit0,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)  |
| GNT2#/GPIO53                  | PCIE config2 bit2,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)  |
| GPIO20                        | Reserved   | This signal should not be pulled high.  |
| GNT1#/GPIO51                  | ESI Strap (Server Only)<br>Rising Edge of PWROK                        | ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.  |
| GNT3#/GPIO55                  | Top-Block Swap Override.<br>Rising Edge of PWROK.                      | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting PWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#:<br>SPI_CS1#/<br>GPIO58 | Boot BIOS Destination Selection 0:1.<br>Rising Edge of PWROK.          | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h;bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.   |
| SPI_MOSI                      | Integrated TPM Enable,<br>Rising Edge of CLPWROK                       | Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.                                    |
| GPIO49                        | DMI Termination Voltage,<br>Rising Edge of PWROK.                      | The signal is required to be low for desktop applications and required to be high for mobile applications.  |
| SATALED#                      | PCI Express Lane Reversal. Rising Edge of PWROK.                       | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)   |
| SPKR                          | No Reboot.<br>Rising Edge of PWROK.                                    | If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO timer system reboot feature). The status is readable via the NO REBOOT bit.   |
| TP3                           | XOR Chain Entrance.<br>Rising Edge of PWROK.                           | This signal should not be pull low unless using XOR Chain testing.  |
| GPIO33/<br>HDA_DOCK_EN#       | Flash Descriptor Security Override Strap<br>Rising Edge of PWROK       | Sampled low:the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor. |

# ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

| SIGNAL                   | Resistor Type/Value   |
|--------------------------|---|
| CL_CLK[1:0]              | PULL-UP 20K   |
| CL_DATA[1:0]             | PULL-UP 20K   |
| CL_RST0#                 | PULL-UP 20K   |
| DPRSLPVR/GPIO16          | PULL-DOWN 20K   |
| ENERGY_DETECT            | PULL-UP 20K   |
| HDA_BIT_CLK              | PULL-DOWN 20K   |
| HDA_DOCK_EN#/GPIO33      | PULL-UP 20K   |
| HDA_RST#                 | PULL-DOWN 20K   |
| HDA_SDIN[3:0]            | PULL-DOWN 20K   |
| HDA_SDOUT                | PULL-DOWN 20K   |
| HDA_SYNC                 | PULL-DOWN 20K   |
| GLAN_DOCK#               | The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55,53,51] | PULL-UP 20K   |
| GPIO[20]                 | PULL-DOWN 20K   |
| GPIO[49]                 | PULL-UP 20K   |
| LDA[3:0]#/FHW[3:0]#      | PULL-UP 20K   |
| LAN_RXD[2:0]             | PULL-UP 20K   |
| LDRQ[0]                  | PULL-UP 20K   |
| LDRQ[1]/GPIO23           | PULL-UP 20K   |
| PME#                     | PULL-UP 20K   |
| PWRBTN#                  | PULL-UP 20K   |
| SATALED#                 | PULL-UP 15K   |
| SPI_CS1#/GPIO58/CLGPIO6  | PULL-UP 20K   |
| SPI_MOSI                 | PULL-DOWN 20K   |
| SPI_MISO                 | PULL-UP 20K   |
| SPKR                     | PULL-DOWN 20K   |
| TACH_[3:0]               | PULL-UP 20K   |
| TP[3]                    | PULL-UP 20K   |
| USB[11:0][P,N]           | PULL-DOWN 15K   |

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

| Pin Name                                     | Strap Description   | Configuration  |
|--|---|--|
| CFG[2:0]                                     | FSB Frequency Select                                      | 000 = FSB1067<br>011 = FSB667<br>010 = FSB800<br>others = Reserved   |
| CFG[4:3]<br>CFG8<br>CFG[15:14]<br>CFG[18:17] | Reserved  |  |
| CFG5   | DMI x2 Select   | 0 = DMI x2<br>1 = DMI x4 (Default)   |
| CFG6   | iTPM Host Interface                                       | 0= The iTPM Host Interface is enabled(Note2)<br>1=The iTPM Host Interface is disabled(default)   |
| CFG7   | Intel Management engine Crypto strap                      | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality<br>1 = TLS cipher suite with confidentiality (default)                                       |
| CFG9   | PCIe Graphics Lane  | 0 = Reverse Lanes,15->0,14->1 ect..<br>1= Normal operation(Default):Lane Numbered in order   |
| CFG10  | PCIe Loopback enable                                      | 0 = Enable (Note 3)<br>1 = Disabled (default)  |
| CFG[13:12]                                   | XOR/ALL   | 00 = Reserve<br>10 = XOR mode Enabled<br>01 = ALLIZ mode Enabled (Note 3)<br>11 = Disabled (default)   |
| CFG16  | FSB Dynamic ODT   | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)  |
| CFG19  | DMI Lane Reversal   | 0 = Normal operation(Default): Lane Numbered in order<br>1 = Reverse Lanes<br>DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3)<br>DMI x2 mode[MCH -> ICH]:(3->0,2->1) |
| CFG20  | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe | 0 = Only Digital Display Port or PCIe is operational (Default)<br>1 = Digital display Port and PCIe are operating simulataneously via the PEG port                   |
| SDVO_CTRLDATA                                | SDVO Present  | 0 =No SDVO Card Present (Default)<br>1 = SDVO Card Present   |
| LDDC_DATA                                    | Local Flat Panel (LFP) Present                            | 0 = LFP Disabled (Default)<br>1= LFP Card Present; PCIe disabled   |

**NOTE:**  
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

## PCI Routing

page 17

|        | IDSEL | INT   | REQ | GNT |
|--------|-------|---|-----|-----|
| II7412 | AD22  | G:CARDBUS<br>B:1394<br>F:Flash Media<br>G:SD Host | 0   | 0   |

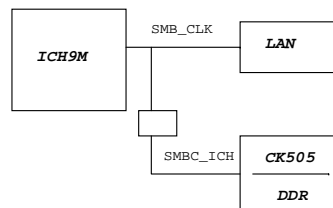
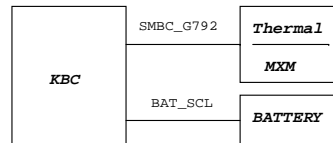
## PCIE Routing

|       |               |
|-------|---------------|
| LANE2 | MiniCard WLAN |
| LANE3 | NewCard WLAN  |

## USB Table

| USB  |                   |
|------|-------------------|
| Pair | Device            |
| 0    | Combo (ESATA/USB) |
| 1    | NC                |
| 2    | USB2              |
| 3    | USB4              |
| 4    | USB3              |
| 5    | BLUETOOTH         |
| 6    | WEBCAM            |
| 7    | FT                |
| 8    | MINICARD          |
| 9    | NEW1              |

## SMBus



UMA

|  |               |
|--|---------------|
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| <b>Reference</b>   |               |
| <b>D45/D46</b>   |               |
| Date: Friday, March 14, 2008   | Sheet 2 of 47 |

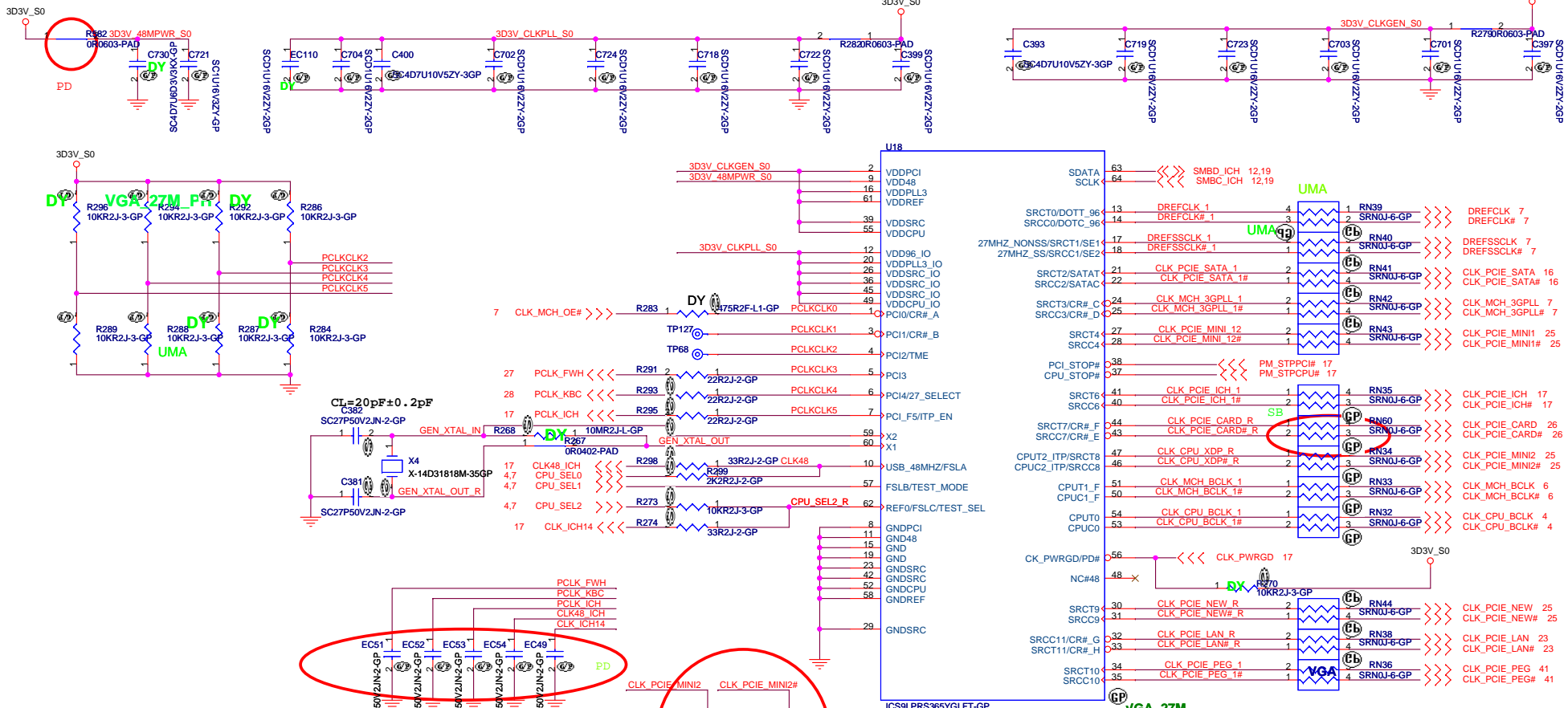
A

B

C

D

E



ICS9LPRS365YGLFT setting table

| PIN NAME      | DESCRIPTION   |
|---------------|---|
| PCI0/CR#_A    | Byte 5, bit 7<br>0 = PCIO enabled (default)<br>1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair<br>Byte 5, bit 6<br>0 = CR#_A controls SRC0 pair (default),<br>1 = CR#_A controls SRC2 pair |
| PCI1/CR#_B    | Byte 5, bit 5<br>0 = PCI1 enabled (default)<br>1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair<br>Byte 5, bit 4<br>0 = CR#_B controls SRC1 pair (default)<br>1 = CR#_B controls SRC4 pair  |
| PCI2/TME      | 0 = Overclocking of CPU and SRC Allowed<br>1 = Overclocking of CPU and SRC NOT allowed  |
| PCI3          |   |
| PCI4/27M_SEL  | 0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT9#<br>1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#  |
| PCI_F5/ITP_EN | 0 =SRCC/SRCC#<br>1 = ITP/ITP#   |
| SRCT3/CR#_C   | Byte 5, bit 3<br>0 = SRC3 enabled (default)<br>1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair<br>Byte 5, bit 2<br>0 = CR#_C controls SRC0 pair (default),<br>1 = CR#_C controls SRC2 pair |

| PIN NAME     | DESCRIPTION  |
|--------------|--|
| SRCC3/CR#_D  | Byte 5, bit 1<br>0 = SRC3 enabled (default)<br>1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair<br>Byte 5, bit 0<br>0 = CR#_D controls SRC1 pair (default)<br>1 = CR#_D controls SRC4 pair |
| SRCC7/CR#_E  | Byte 6, bit 7<br>0 = SRC7# enabled (default)<br>1 = CR#_F controls SRC6  |
| SRCT7/CR#_F  | Byte 6, bit 6<br>0 = SRC7 enabled (default)<br>1 = CR#_F controls SRC8   |
| SRCC11/CR#_G | Byte 6, bit 5<br>0 = SRC11# enabled (default)<br>1 = CR#_G controls SRC9   |
| SRCT11/CR#_H | Byte 6, bit 4<br>0 = SRC11 enabled (default)<br>1 = CR#_H controls SRC10   |

| SEL2 | SEL1 | SEL0 | CPU  | FSB   |
|------|------|------|------|-------|
| FSC  | FSB  | FSA  |      |       |
| 1    | 0    | 1    | 100M | X     |
| 0    | 0    | 1    | 133M | 533M  |
| 0    | 1    | 1    | 166M | 667M  |
| 0    | 1    | 0    | 200M | 800M  |
| 0    | 0    | 0    | 266M | 1067M |

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**Clock Generator**

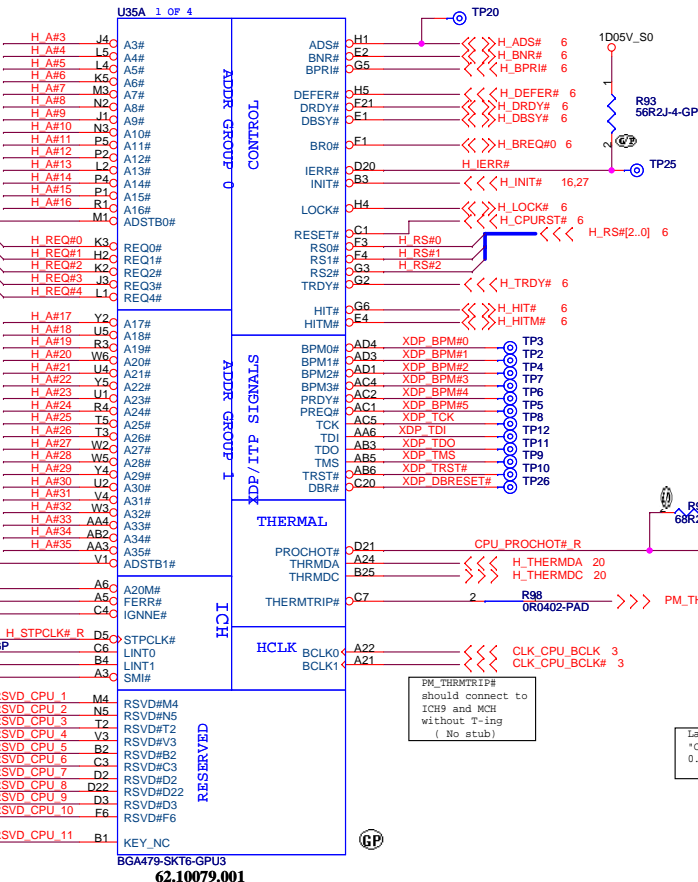
Title

Size Document Number **D45/D46** Rev **PD**

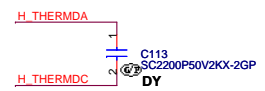
Date: Tuesday, March 18, 2008 Sheet 3 of 47

6 H\_A#[35..3] <<>> H\_A#[35..3]

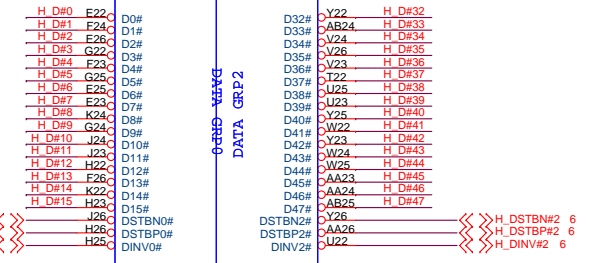
H\_DINV#[3..0] <<>> H\_DINV#[3..0] 6  
H\_DSTBN#[3..0] <<>> H\_DSTBN#[3..0] 6  
H\_DSTBP#[3..0] <<>> H\_DSTBP#[3..0] 6  
H\_D#[63..0] <<>> H\_D#[63..0] 6



Place testpoint on H\_IERR# with a GND 0.1" away



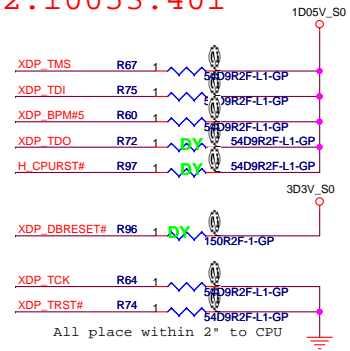
6 H\_DSTBN#0  
6 H\_DSTBP#0  
6 H\_DINV#0



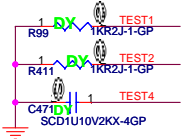
Layout Note: "CPU\_GTLREF0" 0.5" max length.

PM\_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)

SB use 62.10053.401



All place within 2" to CPU



Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

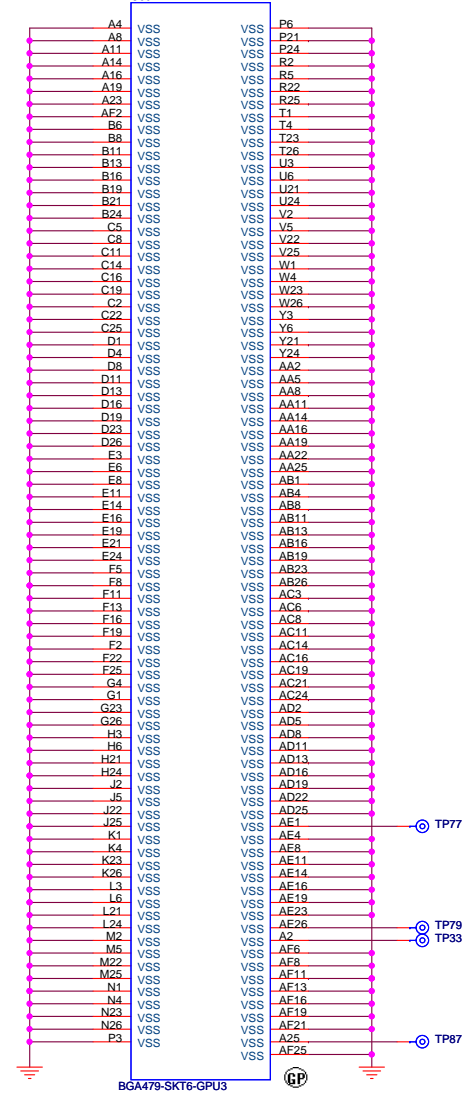
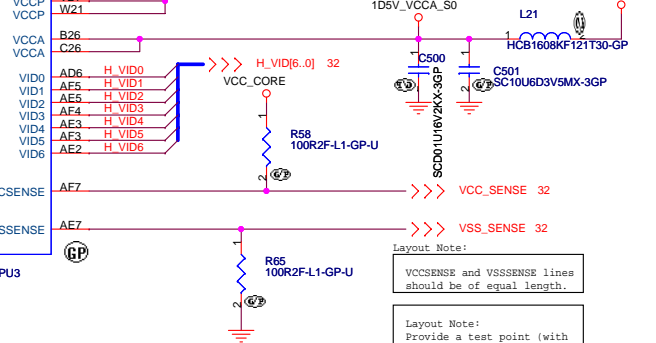
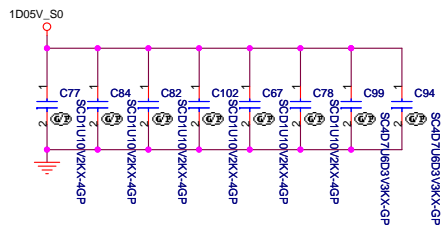
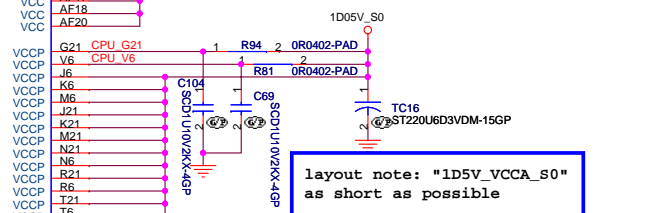
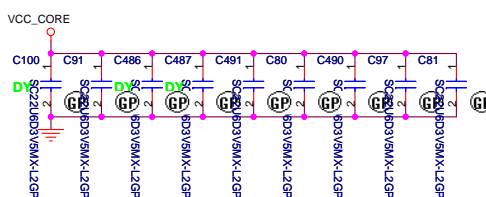
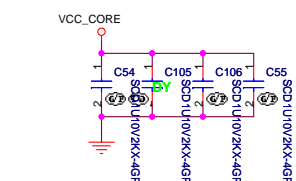
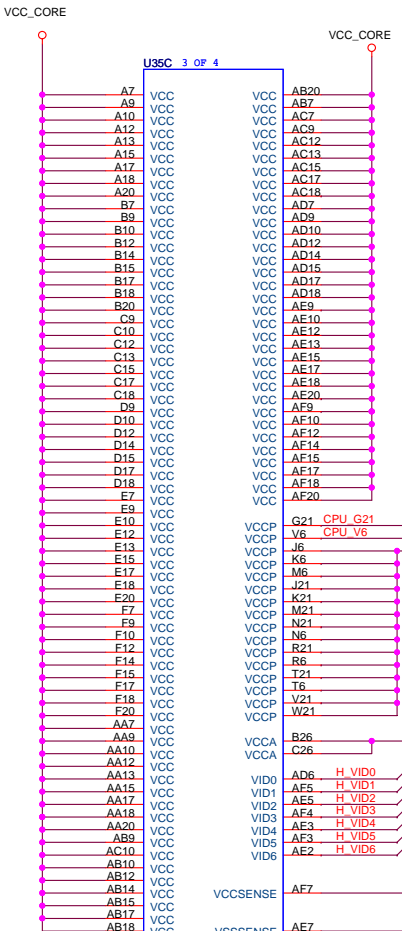
ZZZZ

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Title: **CPU (1 of 2)**

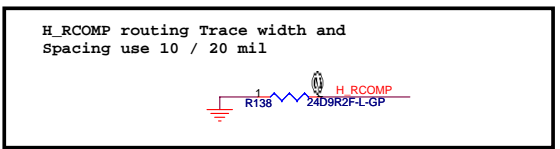
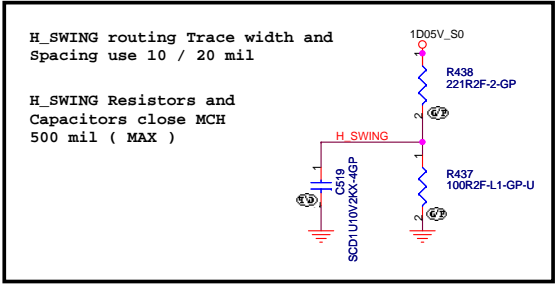
Size: Document Number **D45/D46** Rev PD

Date: Friday, March 14, 2008 Sheet 4 of 47

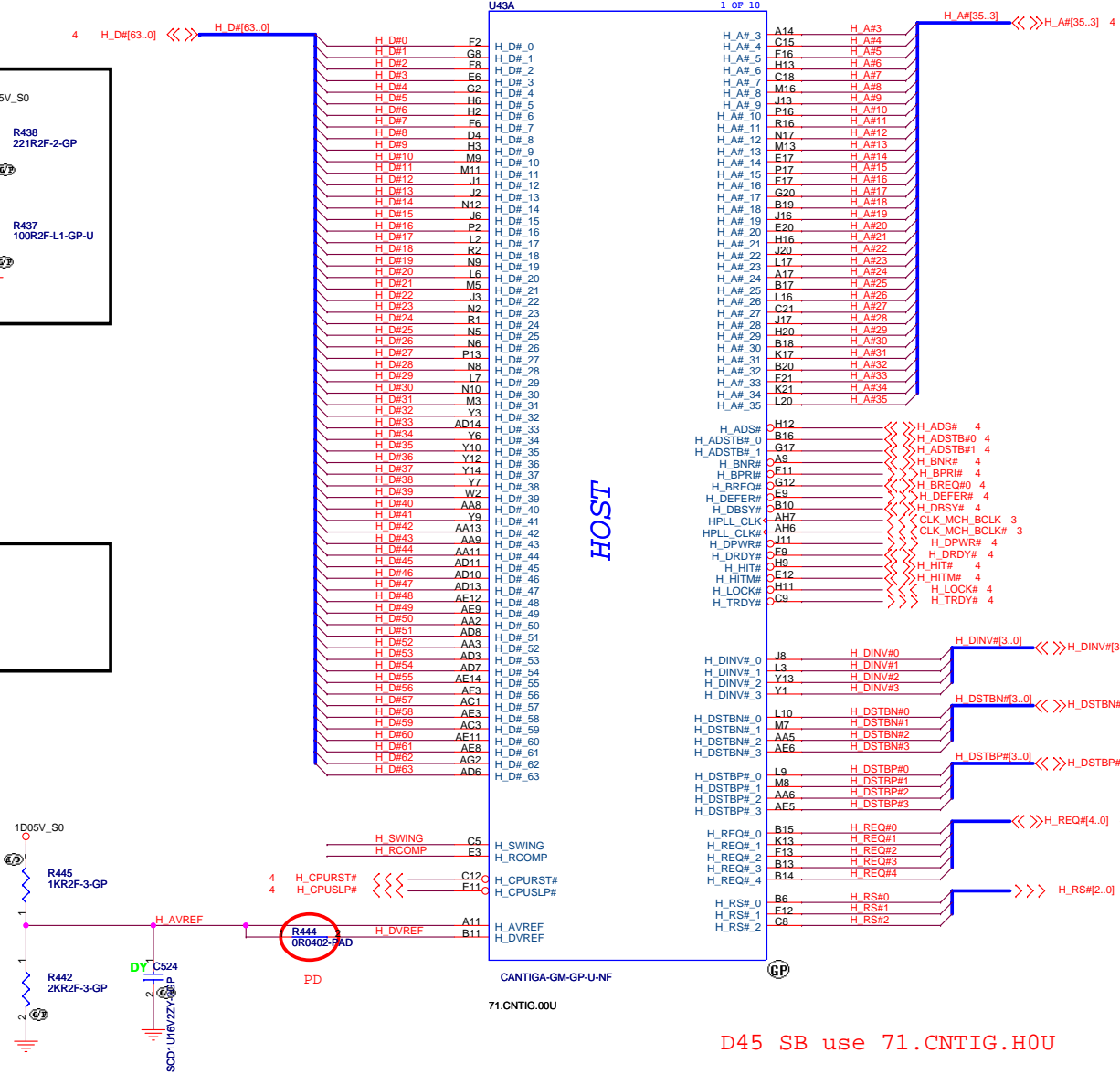


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Place them near to the chip ( < 0.5" )



D45 SB use 71.CNTIG.H0U

D46 SB use 71.CNTIG.G0U

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Title: **Cantiga (1 of 6)**

Size: Document Number: **D45/D46** Rev: **PD**

Date: Friday, March 14, 2008 Sheet 6 of 47





12 M\_A\_DQ[63..0] <<< M\_A\_DQ[63..0]

|          |      |          |
|----------|------|----------|
| M_A_DQ0  | AJ38 | SA_DQ_0  |
| M_A_DQ1  | AJ41 | SA_DQ_1  |
| M_A_DQ2  | AN38 | SA_DQ_2  |
| M_A_DQ3  | AM38 | SA_DQ_3  |
| M_A_DQ4  | AJ36 | SA_DQ_4  |
| M_A_DQ5  | AJ40 | SA_DQ_5  |
| M_A_DQ6  | AM44 | SA_DQ_6  |
| M_A_DQ7  | AM42 | SA_DQ_7  |
| M_A_DQ8  | AN43 | SA_DQ_8  |
| M_A_DQ9  | AN44 | SA_DQ_9  |
| M_A_DQ10 | AL40 | SA_DQ_10 |
| M_A_DQ11 | AT38 | SA_DQ_11 |
| M_A_DQ12 | AN41 | SA_DQ_12 |
| M_A_DQ13 | AN39 | SA_DQ_13 |
| M_A_DQ14 | AJ44 | SA_DQ_14 |
| M_A_DQ15 | AJ42 | SA_DQ_15 |
| M_A_DQ16 | AV39 | SA_DQ_16 |
| M_A_DQ17 | AY44 | SA_DQ_17 |
| M_A_DQ18 | BA40 | SA_DQ_18 |
| M_A_DQ19 | BD43 | SA_DQ_19 |
| M_A_DQ20 | AV41 | SA_DQ_20 |
| M_A_DQ21 | AY43 | SA_DQ_21 |
| M_A_DQ22 | BB41 | SA_DQ_22 |
| M_A_DQ23 | BC40 | SA_DQ_23 |
| M_A_DQ24 | BD38 | SA_DQ_24 |
| M_A_DQ25 | AV37 | SA_DQ_25 |
| M_A_DQ26 | BD36 | SA_DQ_26 |
| M_A_DQ27 | AT36 | SA_DQ_27 |
| M_A_DQ28 | AY38 | SA_DQ_28 |
| M_A_DQ29 | BB38 | SA_DQ_29 |
| M_A_DQ30 | AV36 | SA_DQ_30 |
| M_A_DQ31 | AW36 | SA_DQ_31 |
| M_A_DQ32 | BD13 | SA_DQ_32 |
| M_A_DQ33 | AU11 | SA_DQ_33 |
| M_A_DQ34 | BC11 | SA_DQ_34 |
| M_A_DQ35 | BA12 | SA_DQ_35 |
| M_A_DQ36 | AU13 | SA_DQ_36 |
| M_A_DQ37 | AV13 | SA_DQ_37 |
| M_A_DQ38 | BD12 | SA_DQ_38 |
| M_A_DQ39 | BC12 | SA_DQ_39 |
| M_A_DQ40 | BB9  | SA_DQ_40 |
| M_A_DQ41 | BA9  | SA_DQ_41 |
| M_A_DQ42 | AU10 | SA_DQ_42 |
| M_A_DQ43 | AV9  | SA_DQ_43 |
| M_A_DQ44 | BA11 | SA_DQ_44 |
| M_A_DQ45 | BD9  | SA_DQ_45 |
| M_A_DQ46 | AY8  | SA_DQ_46 |
| M_A_DQ47 | BA6  | SA_DQ_47 |
| M_A_DQ48 | AV5  | SA_DQ_48 |
| M_A_DQ49 | AV7  | SA_DQ_49 |
| M_A_DQ50 | AT9  | SA_DQ_50 |
| M_A_DQ51 | AN8  | SA_DQ_51 |
| M_A_DQ52 | AU5  | SA_DQ_52 |
| M_A_DQ53 | AU6  | SA_DQ_53 |
| M_A_DQ54 | AT5  | SA_DQ_54 |
| M_A_DQ55 | AN10 | SA_DQ_55 |
| M_A_DQ56 | AM11 | SA_DQ_56 |
| M_A_DQ57 | AM5  | SA_DQ_57 |
| M_A_DQ58 | AJ9  | SA_DQ_58 |
| M_A_DQ59 | AJ8  | SA_DQ_59 |
| M_A_DQ60 | AN12 | SA_DQ_60 |
| M_A_DQ61 | AM13 | SA_DQ_61 |
| M_A_DQ62 | AJ11 | SA_DQ_62 |
| M_A_DQ63 | AJ12 | SA_DQ_63 |

**DDR SYSTEM MEMORY A**

4 OF 10

|           |      |                    |
|-----------|------|--------------------|
| SA_BS_0   | BD21 | M_A_BS#0 12,13     |
| SA_BS_1   | BG18 | M_A_BS#1 12,13     |
| SA_BS_2   | AT25 | M_A_BS#2 12,13     |
| SA_RAS#   | BB20 | M_A_RAS# 12,13     |
| SA_CAS#   | BB20 | M_A_CAS# 12,13     |
| SA_WE#    | AY20 | M_A_WE# 12,13      |
| SA_DM_0   | AM37 | M_A_DM[7..0] 12    |
| SA_DM_1   | AT41 | M_A_DM1            |
| SA_DM_2   | AY41 | M_A_DM2            |
| SA_DM_3   | BB12 | M_A_DM3            |
| SA_DM_4   | AY6  | M_A_DM4            |
| SA_DM_5   | AT7  | M_A_DM5            |
| SA_DM_6   | AT7  | M_A_DM6            |
| SA_DM_7   | AJ5  | M_A_DM7            |
| SA_DQS_0  | AJ44 | M_A_DQS[7..0] 12   |
| SA_DQS_1  | AT44 | M_A_DQS1           |
| SA_DQS_2  | BA43 | M_A_DQS2           |
| SA_DQS_3  | BC37 | M_A_DQS3           |
| SA_DQS_4  | AW12 | M_A_DQS4           |
| SA_DQS_5  | AUR  | M_A_DQS5           |
| SA_DQS_6  | AM7  | M_A_DQS6           |
| SA_DQS_7  | AJ43 | M_A_DQS#0          |
| SA_DQS#_0 | AT43 | M_A_DQS#1          |
| SA_DQS#_1 | BA44 | M_A_DQS#2          |
| SA_DQS#_2 | BD37 | M_A_DQS#3          |
| SA_DQS#_3 | AY12 | M_A_DQS#4          |
| SA_DQS#_4 | BD8  | M_A_DQS#5          |
| SA_DQS#_5 | AU9  | M_A_DQS#6          |
| SA_DQS#_6 | AM8  | M_A_DQS#7          |
| SA_DQS#_7 | BA21 | M_A_A[14..0] 12,13 |
| SA_MA_0   | BC24 | M_A_A1             |
| SA_MA_1   | BC24 | M_A_A2             |
| SA_MA_2   | BH24 | M_A_A3             |
| SA_MA_3   | BG25 | M_A_A4             |
| SA_MA_4   | BA24 | M_A_A5             |
| SA_MA_5   | BD24 | M_A_A6             |
| SA_MA_6   | BG27 | M_A_A7             |
| SA_MA_7   | BF25 | M_A_A8             |
| SA_MA_8   | AW24 | M_A_A9             |
| SA_MA_9   | BC21 | M_A_A10            |
| SA_MA_10  | BG28 | M_A_A11            |
| SA_MA_11  | BH26 | M_A_A12            |
| SA_MA_12  | BH17 | M_A_A13            |
| SA_MA_13  | AY25 | M_A_A14            |
| SA_MA_14  | AY25 | M_A_A14            |

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71.CNTIG.000



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|          |      |               |
|----------|------|---------------|
| M_B_DQ0  | AK47 | M_B_DQ[63..0] |
| M_B_DQ1  | AH46 | M_B_DQ[63..0] |
| M_B_DQ2  | AP47 | M_B_DQ[63..0] |
| M_B_DQ3  | AP46 | M_B_DQ[63..0] |
| M_B_DQ4  | AJ46 | M_B_DQ[63..0] |
| M_B_DQ5  | AM48 | M_B_DQ[63..0] |
| M_B_DQ6  | AM48 | M_B_DQ[63..0] |
| M_B_DQ7  | AP48 | M_B_DQ[63..0] |
| M_B_DQ8  | AU47 | M_B_DQ[63..0] |
| M_B_DQ9  | EA48 | M_B_DQ[63..0] |
| M_B_DQ10 | AU46 | M_B_DQ[63..0] |
| M_B_DQ11 | AY48 | M_B_DQ[63..0] |
| M_B_DQ12 | AT47 | M_B_DQ[63..0] |
| M_B_DQ13 | AR47 | M_B_DQ[63..0] |
| M_B_DQ14 | BA47 | M_B_DQ[63..0] |
| M_B_DQ15 | BC46 | M_B_DQ[63..0] |
| M_B_DQ16 | BC44 | M_B_DQ[63..0] |
| M_B_DQ17 | BC44 | M_B_DQ[63..0] |
| M_B_DQ18 | BG43 | M_B_DQ[63..0] |
| M_B_DQ19 | BF43 | M_B_DQ[63..0] |
| M_B_DQ20 | BE45 | M_B_DQ[63..0] |
| M_B_DQ21 | BC41 | M_B_DQ[63..0] |
| M_B_DQ22 | BF40 | M_B_DQ[63..0] |
| M_B_DQ23 | BF41 | M_B_DQ[63..0] |
| M_B_DQ24 | AV37 | M_B_DQ[63..0] |
| M_B_DQ25 | BF38 | M_B_DQ[63..0] |
| M_B_DQ26 | BH35 | M_B_DQ[63..0] |
| M_B_DQ27 | BG35 | M_B_DQ[63..0] |
| M_B_DQ28 | BH40 | M_B_DQ[63..0] |
| M_B_DQ29 | BG39 | M_B_DQ[63..0] |
| M_B_DQ30 | BG34 | M_B_DQ[63..0] |
| M_B_DQ31 | BH34 | M_B_DQ[63..0] |
| M_B_DQ32 | BH14 | M_B_DQ[63..0] |
| M_B_DQ33 | BG12 | M_B_DQ[63..0] |
| M_B_DQ34 | BH11 | M_B_DQ[63..0] |
| M_B_DQ35 | BG8  | M_B_DQ[63..0] |
| M_B_DQ36 | BH12 | M_B_DQ[63..0] |
| M_B_DQ37 | BF11 | M_B_DQ[63..0] |
| M_B_DQ38 | BF9  | M_B_DQ[63..0] |
| M_B_DQ39 | BG7  | M_B_DQ[63..0] |
| M_B_DQ40 | BC5  | M_B_DQ[63..0] |
| M_B_DQ41 | BC6  | M_B_DQ[63..0] |
| M_B_DQ42 | AY3  | M_B_DQ[63..0] |
| M_B_DQ43 | AV1  | M_B_DQ[63..0] |
| M_B_DQ44 | BF6  | M_B_DQ[63..0] |
| M_B_DQ45 | BF5  | M_B_DQ[63..0] |
| M_B_DQ46 | BA1  | M_B_DQ[63..0] |
| M_B_DQ47 | BD3  | M_B_DQ[63..0] |
| M_B_DQ48 | AV2  | M_B_DQ[63..0] |
| M_B_DQ49 | AU3  | M_B_DQ[63..0] |
| M_B_DQ50 | AR3  | M_B_DQ[63..0] |
| M_B_DQ51 | AN2  | M_B_DQ[63..0] |
| M_B_DQ52 | AY2  | M_B_DQ[63..0] |
| M_B_DQ53 | AV1  | M_B_DQ[63..0] |
| M_B_DQ54 | AP3  | M_B_DQ[63..0] |
| M_B_DQ55 | AR1  | M_B_DQ[63..0] |
| M_B_DQ56 | AL1  | M_B_DQ[63..0] |
| M_B_DQ57 | AL2  | M_B_DQ[63..0] |
| M_B_DQ58 | AJ1  | M_B_DQ[63..0] |
| M_B_DQ59 | AH1  | M_B_DQ[63..0] |
| M_B_DQ60 | AM2  | M_B_DQ[63..0] |
| M_B_DQ61 | AM3  | M_B_DQ[63..0] |
| M_B_DQ62 | AH3  | M_B_DQ[63..0] |
| M_B_DQ63 | AJ3  | M_B_DQ[63..0] |

**DDR SYSTEM MEMORY B**

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|           |      |                    |
|-----------|------|--------------------|
| SB_BS_0   | BC16 | M_B_BS#0 12,13     |
| SB_BS_1   | BB17 | M_B_BS#1 12,13     |
| SB_BS_2   | BB33 | M_B_BS#2 12,13     |
| SB_RAS#   | AU17 | M_B_RAS# 12,13     |
| SB_CAS#   | BG16 | M_B_CAS# 12,13     |
| SB_WE#    | BF14 | M_B_WE# 12,13      |
| SB_DM_0   | AM47 | M_B_DM[7..0] 12    |
| SB_DM_1   | AY47 | M_B_DM1            |
| SB_DM_2   | BD40 | M_B_DM2            |
| SB_DM_3   | BF35 | M_B_DM3            |
| SB_DM_4   | BG11 | M_B_DM4            |
| SB_DM_5   | BA3  | M_B_DM5            |
| SB_DM_6   | AP1  | M_B_DM6            |
| SB_DM_7   | AK2  | M_B_DM7            |
| SB_DQS_0  | AL47 | M_B_DQS[7..0] 12   |
| SB_DQS_1  | AV48 | M_B_DQS1           |
| SB_DQS_2  | BG41 | M_B_DQS2           |
| SB_DQS_3  | BG37 | M_B_DQS3           |
| SB_DQS_4  | BH8  | M_B_DQS4           |
| SB_DQS_5  | BB2  | M_B_DQS5           |
| SB_DQS_6  | AU1  | M_B_DQS6           |
| SB_DQS_7  | AN6  | M_B_DQS7           |
| SB_DQS#_0 | AL46 | M_B_DQS#0          |
| SB_DQS#_1 | AV47 | M_B_DQS#1          |
| SB_DQS#_2 | BH41 | M_B_DQS#2          |
| SB_DQS#_3 | BH37 | M_B_DQS#3          |
| SB_DQS#_4 | BG9  | M_B_DQS#4          |
| SB_DQS#_5 | BC2  | M_B_DQS#5          |
| SB_DQS#_6 | AT2  | M_B_DQS#6          |
| SB_DQS#_7 | AN5  | M_B_DQS#7          |
| SB_MA_0   | AV17 | M_B_A[14..0] 12,13 |
| SB_MA_1   | BA25 | M_B_A1             |
| SB_MA_2   | BC25 | M_B_A2             |
| SB_MA_3   | AU25 | M_B_A3             |
| SB_MA_4   | AV25 | M_B_A4             |
| SB_MA_5   | BB28 | M_B_A5             |
| SB_MA_6   | AU28 | M_B_A6             |
| SB_MA_7   | AV28 | M_B_A7             |
| SB_MA_8   | AT33 | M_B_A8             |
| SB_MA_9   | BD33 | M_B_A9             |
| SB_MA_10  | BB16 | M_B_A10            |
| SB_MA_11  | AV33 | M_B_A11            |
| SB_MA_12  | AY33 | M_B_A12            |
| SB_MA_13  | BH15 | M_B_A13            |
| SB_MA_14  | AU33 | M_B_A14            |

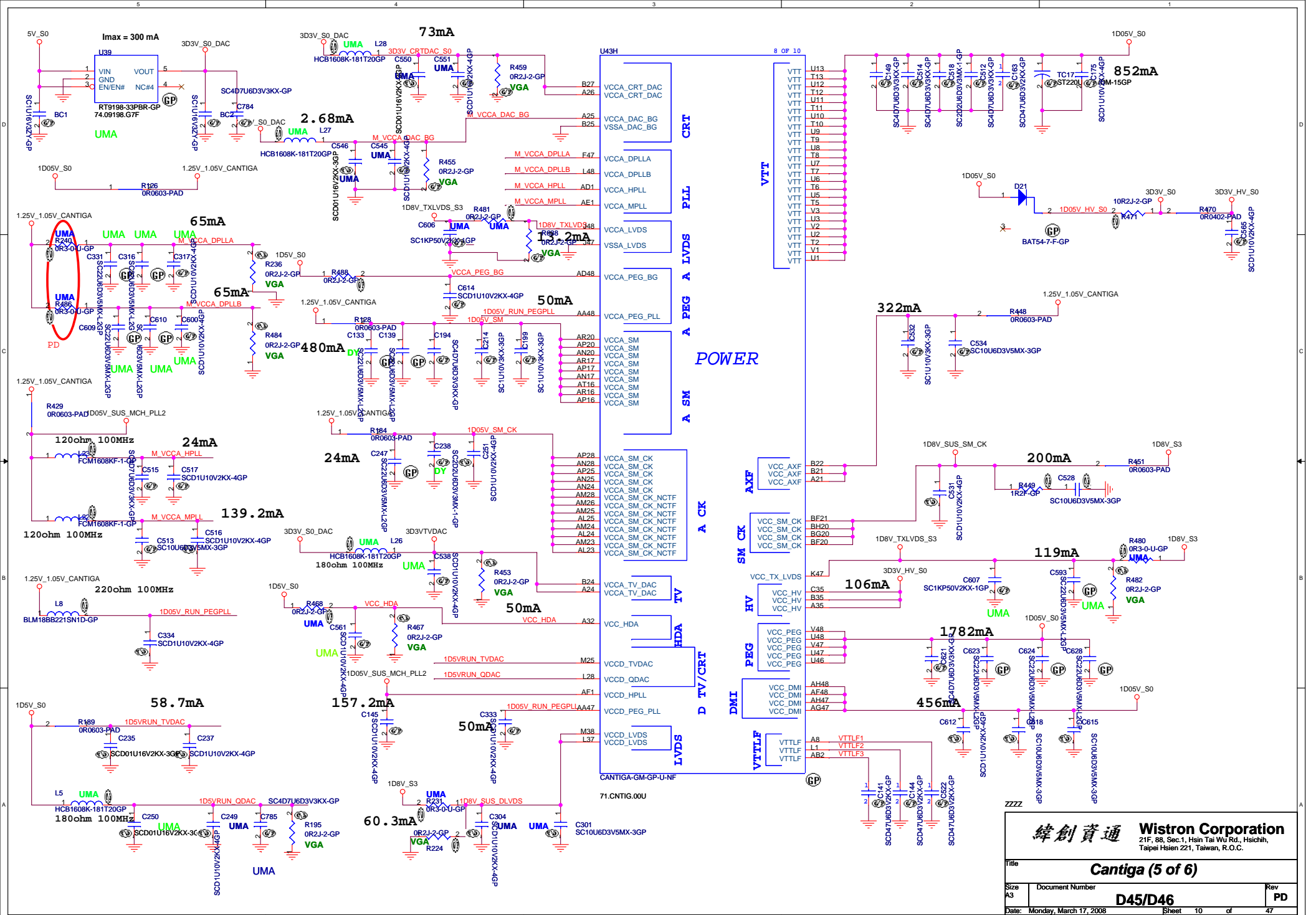
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71.CNTIG.000



|                         |                        |  |         |
|-------------------------|------------------------|--|---------|
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| Title                   |                        |  |         |
| <b>Cantiga (3 of 6)</b> |                        |  |         |
| Size                    | Document Number        | Rev  | PD      |
| <b>D45/D46</b>          |                        |  |         |
| Date:                   | Friday, March 14, 2008 | Sheet  | 8 of 47 |

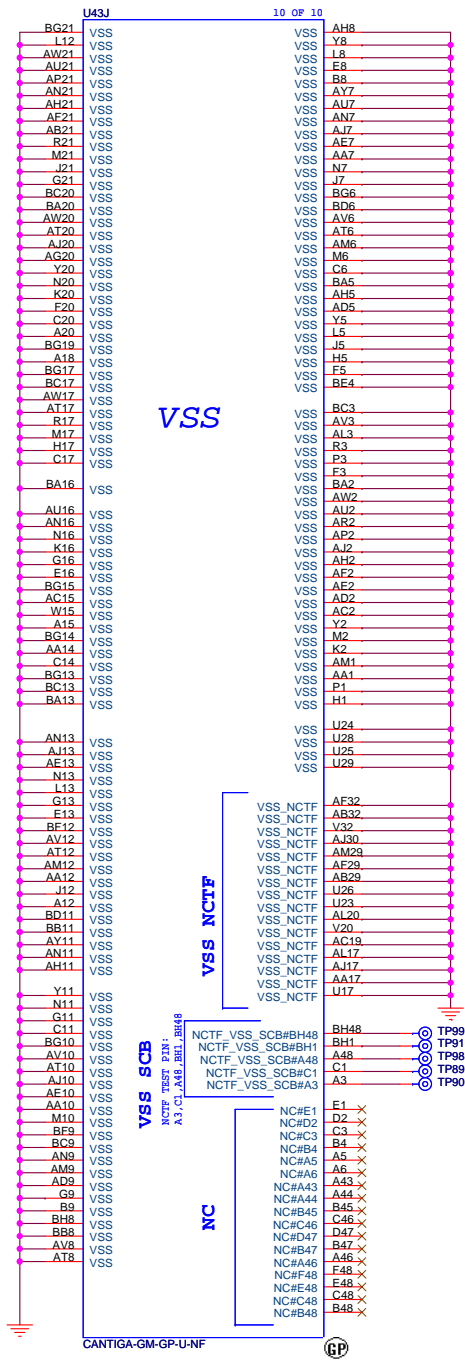
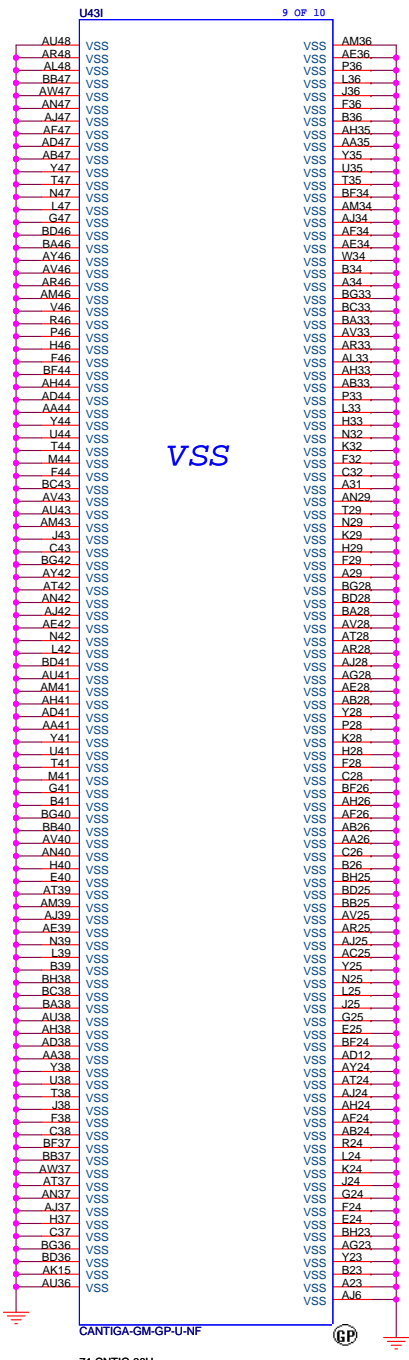






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|       |                        |       |                  |    |     |
|-------|------------------------|-------|------------------|----|-----|
| Title |                        |       | Cantiga (5 of 6) |    |     |
| Size  | Document Number        |       | D45/D46          |    | Rev |
| A3    |                        |       |                  |    | PD  |
| Date: | Monday, March 17, 2008 | Sheet | 10               | of | 47  |



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Title: **Cantiga (6 of 6)**

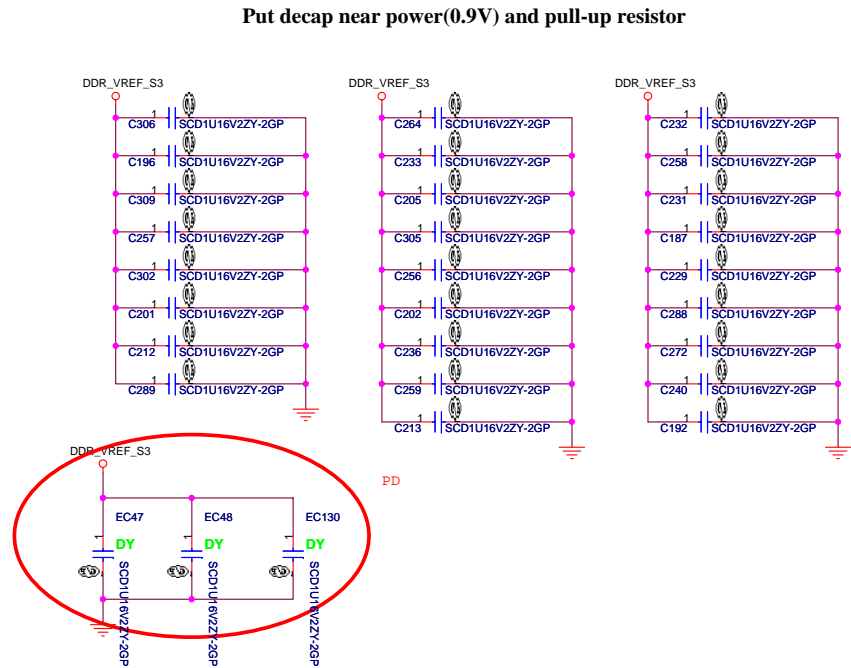
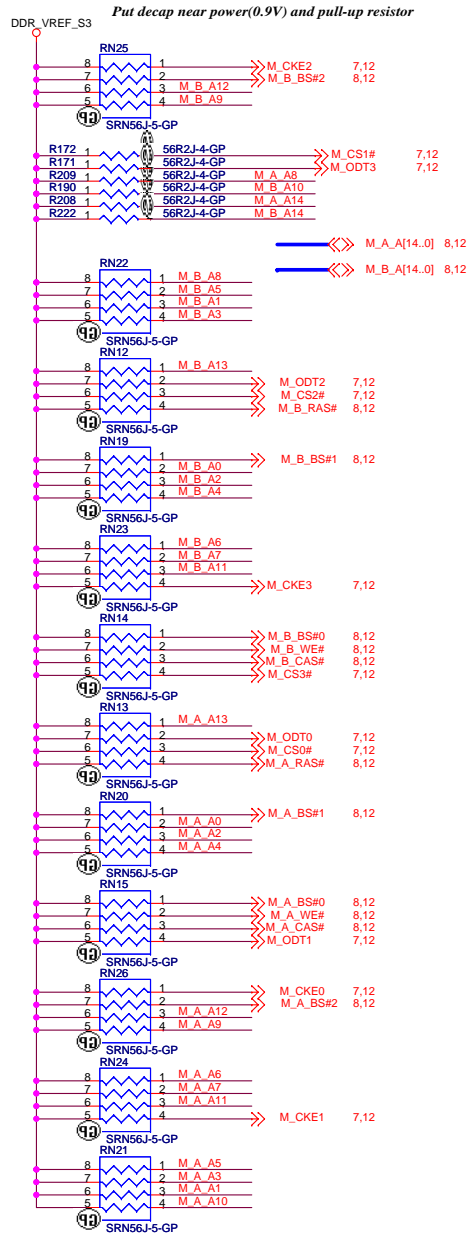
Size: Document Number **D45/D46** Rev: PD

Date: Friday, March 14, 2008 Sheet 11 of 47

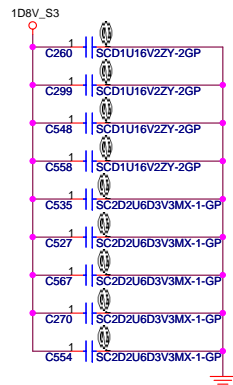


# PARALLEL TERMINATION

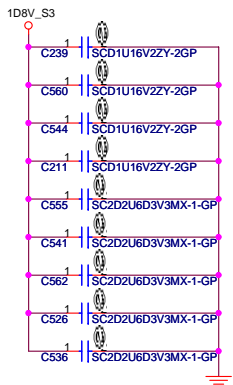
# Decoupling Capacitor



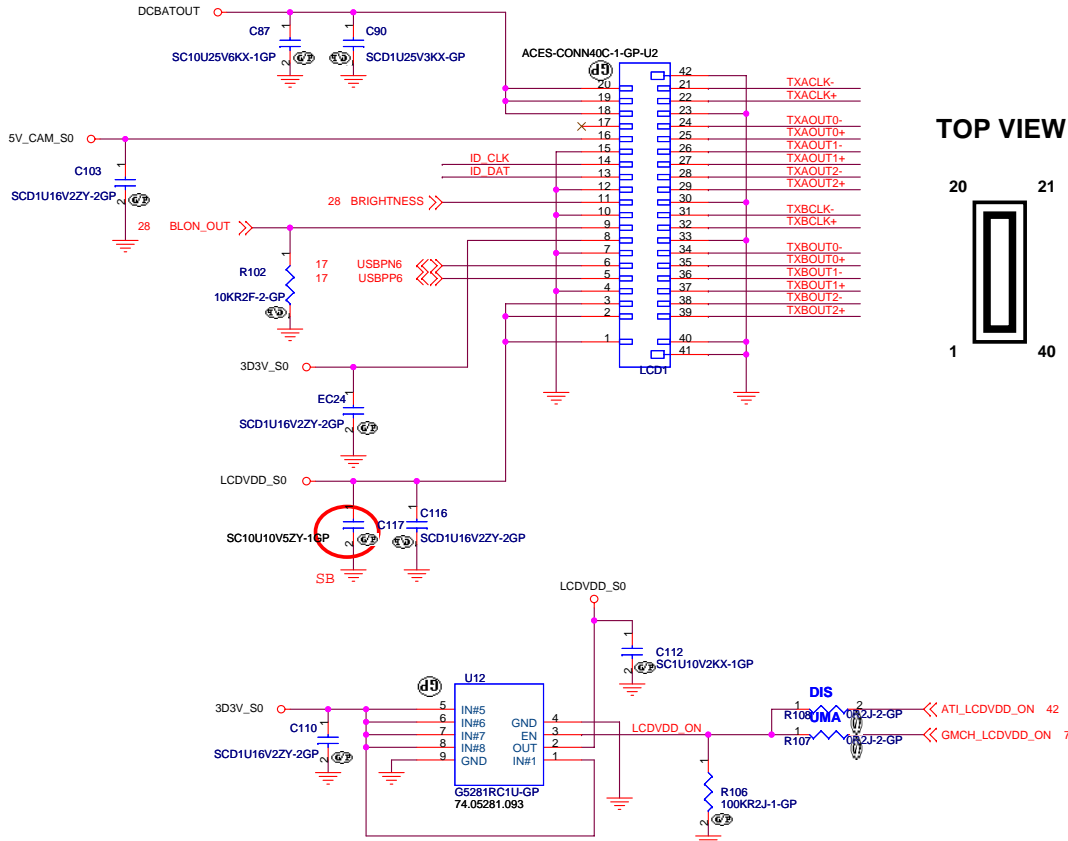
Place these Caps near DM1



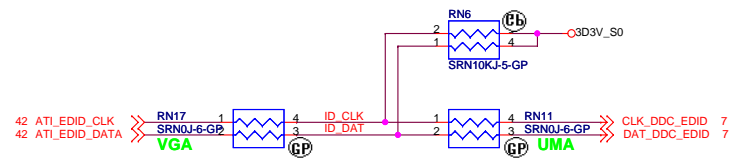
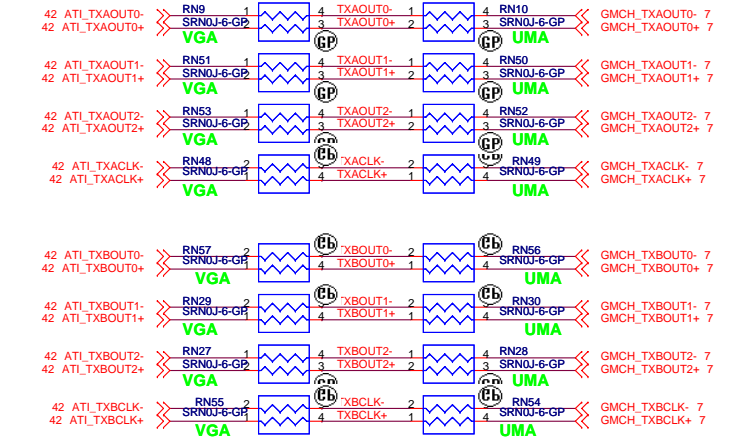
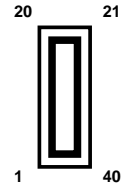
Place these Caps near DM2



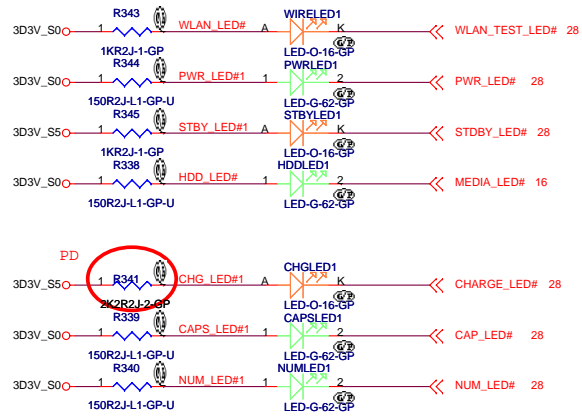
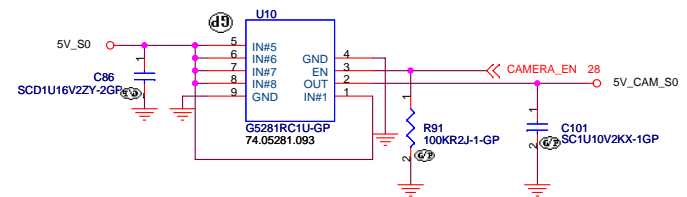
# LCD CONNECTOR



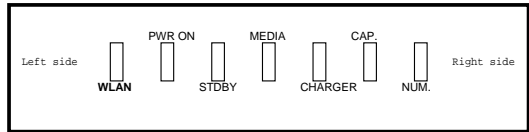
## TOP VIEW



## WEBCAM POWER



## LED Location and Sequence ( The edge of PCB,Top view )



ZZZZ

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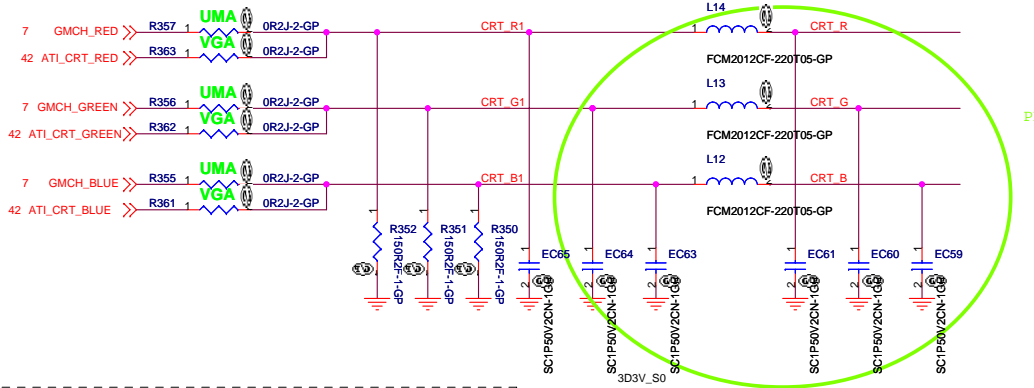
Title: **LCD CONN / LED / WEBCAM**

Size: A3 Document Number: **D45/D46** Rev: **PD**

Date: Friday, March 14, 2008 Sheet 14 of 47

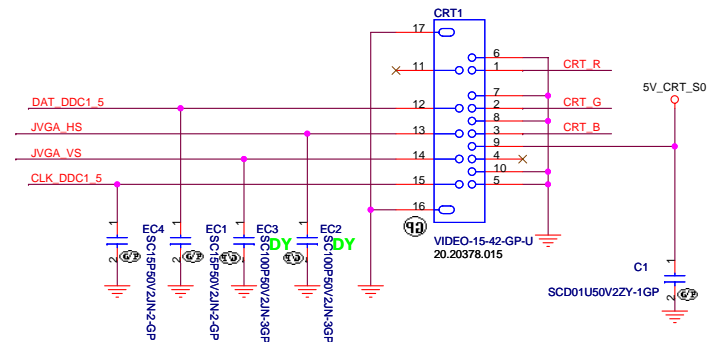


**Layout Note:**  
Place these resistors close to the CRT-out connector

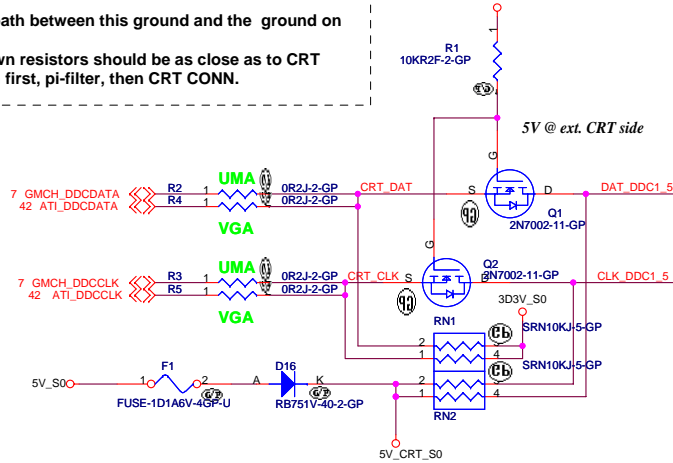


Ferrite bead impedance: 10 ohm@100MHz  
PD use 22 ohm 68.00215.211

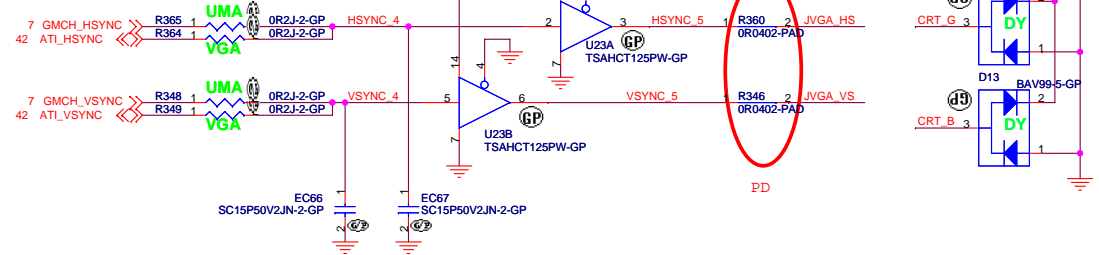
## CRT I/F & CONNECTOR



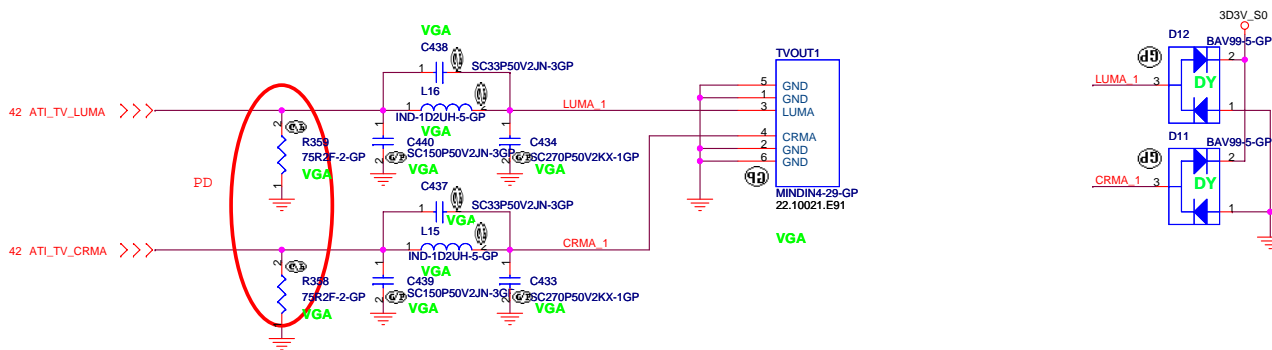
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



### Hsync & Vsync level shift

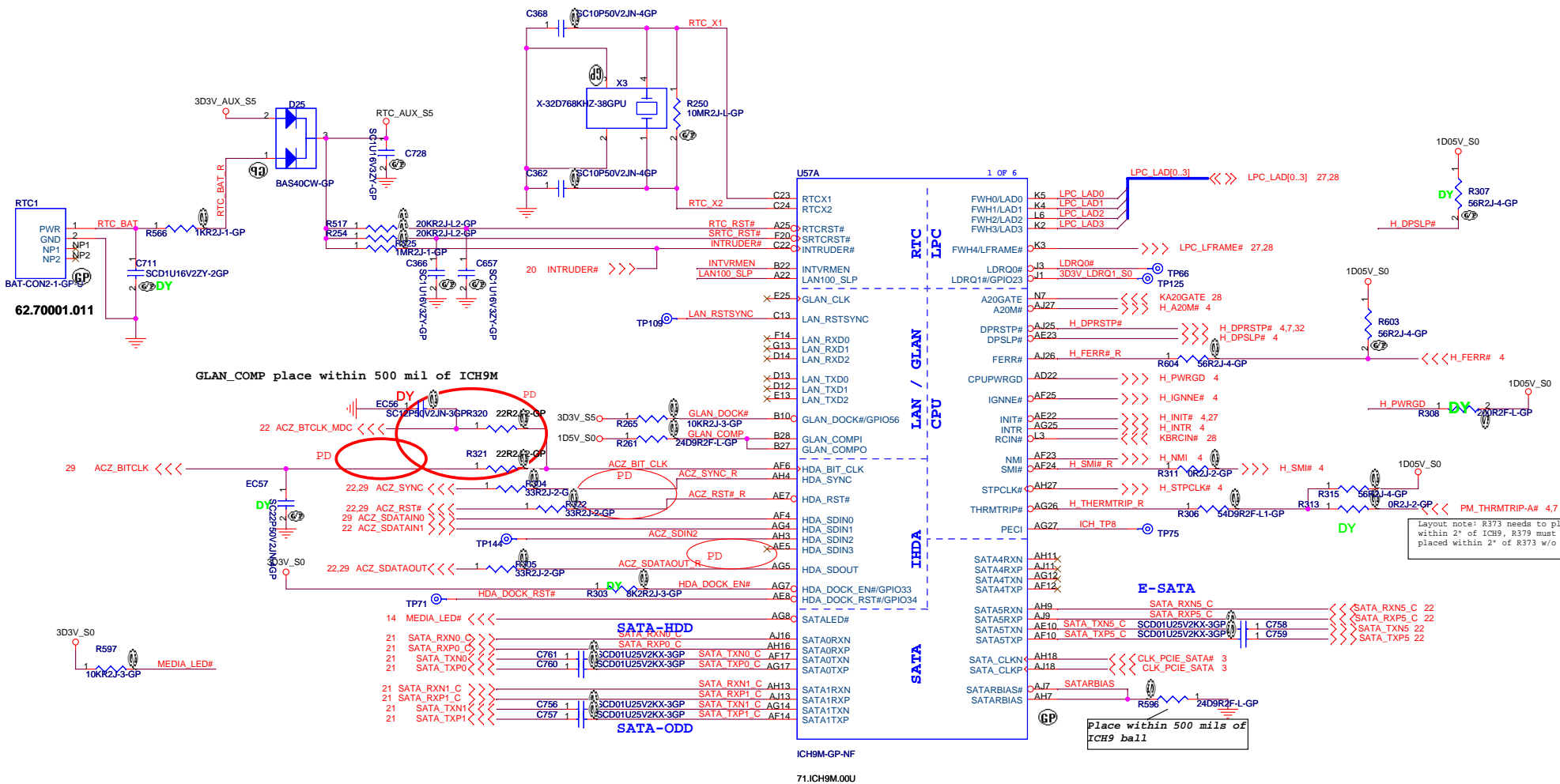


## TV CONN

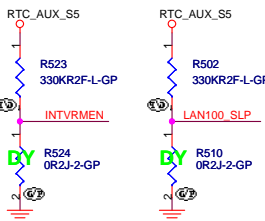


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|                               |                 |     |
|-------------------------------|-----------------|-----|
| Title                         |                 |     |
| <b>CRT/TV Connector</b>       |                 |     |
| Size                          | Document Number | Rev |
|                               | <b>D45/D46</b>  | PD  |
| Date: Tuesday, March 18, 2008 | Sheet 15 of 47  |     |



D4546 SB use 71.ICH9M.E0U



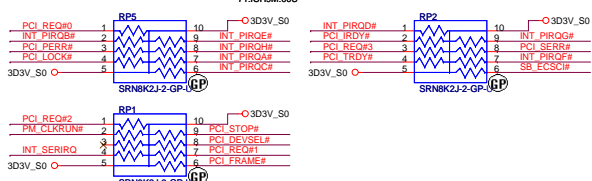
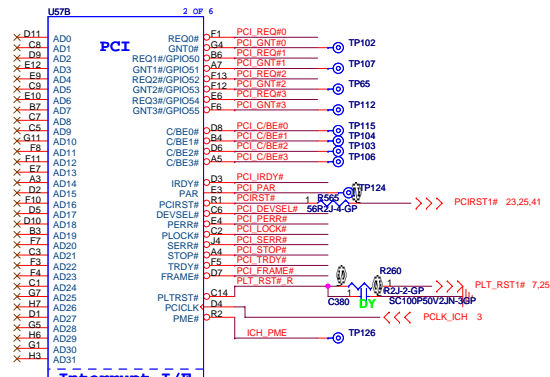
|  |             |             |
|--|-------------|-------------|
| Integrated VccSus1_05,VccSus1_5,VccCl1_5 |             |             |
| INTVRMEN                                 | High=Enable | Low=Disable |
| Integrated VccLan1_05VccCl1_05           |             |             |
| LAN100_SLP                               | High=Enable | Low=Disable |

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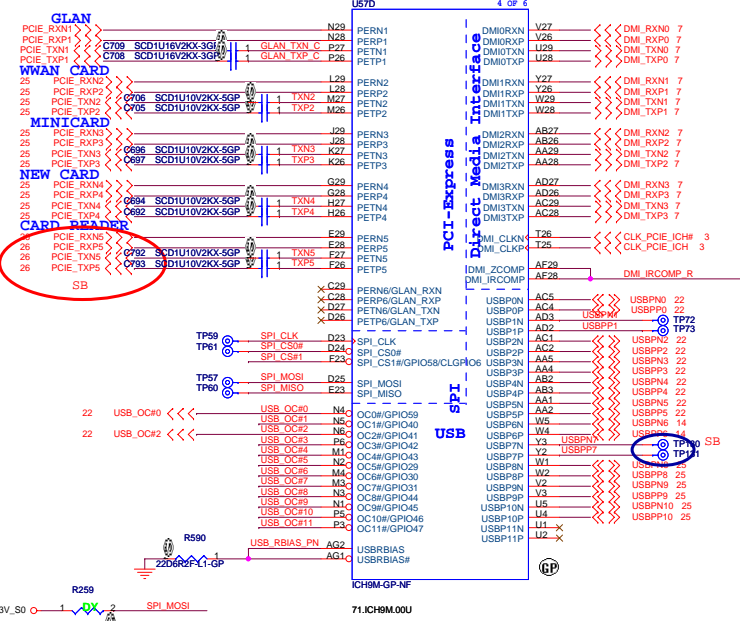
Title: **ICH9-M (1 of 4)**

Size: Document Number: **D45/D46** Rev: **PD**

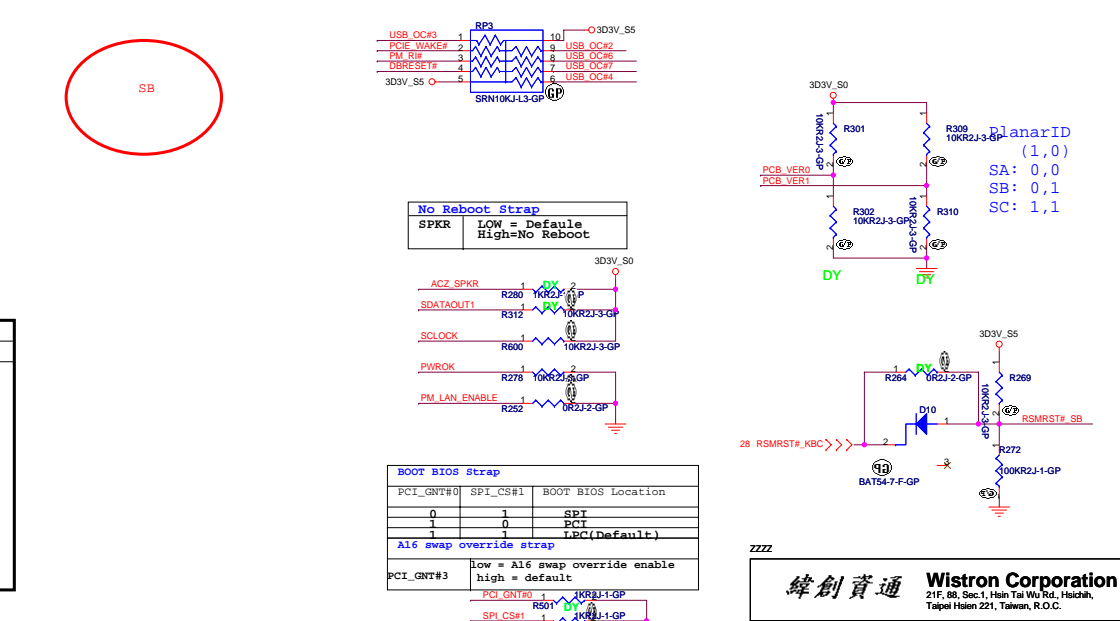
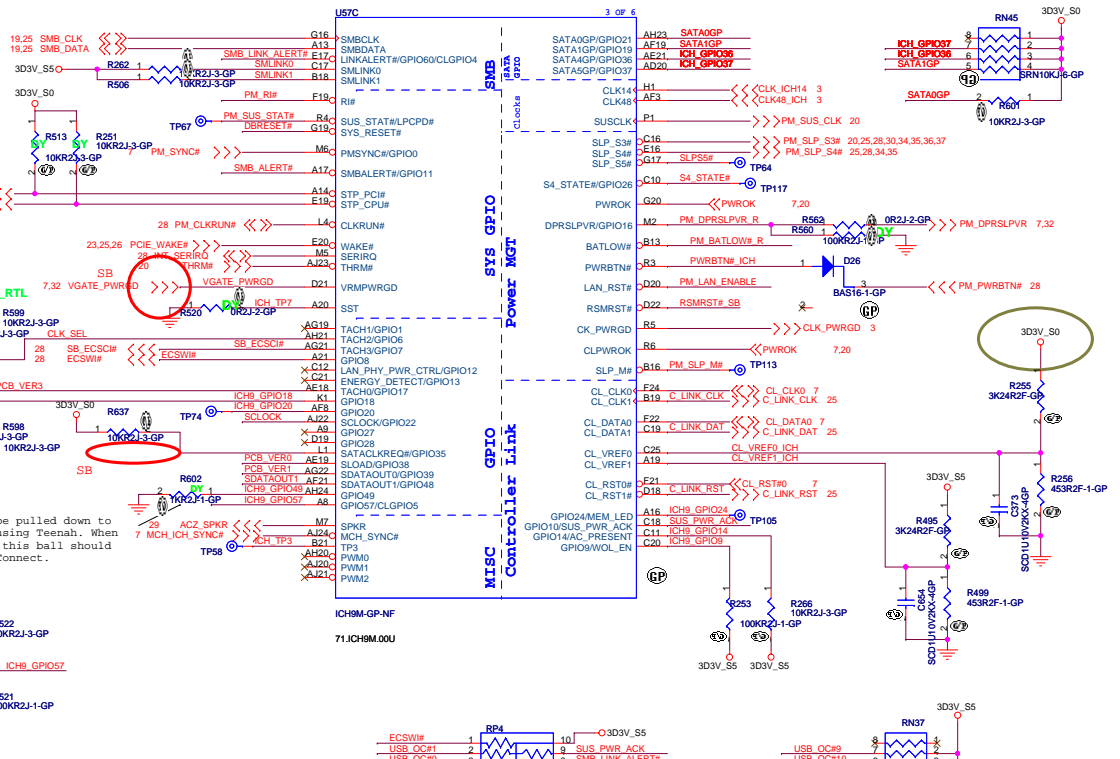
Date: Tuesday, March 25, 2008 Sheet: 16 of 47



Layout Note:  
PCI AC coupling caps  
need to be within 350 mils of the driver.



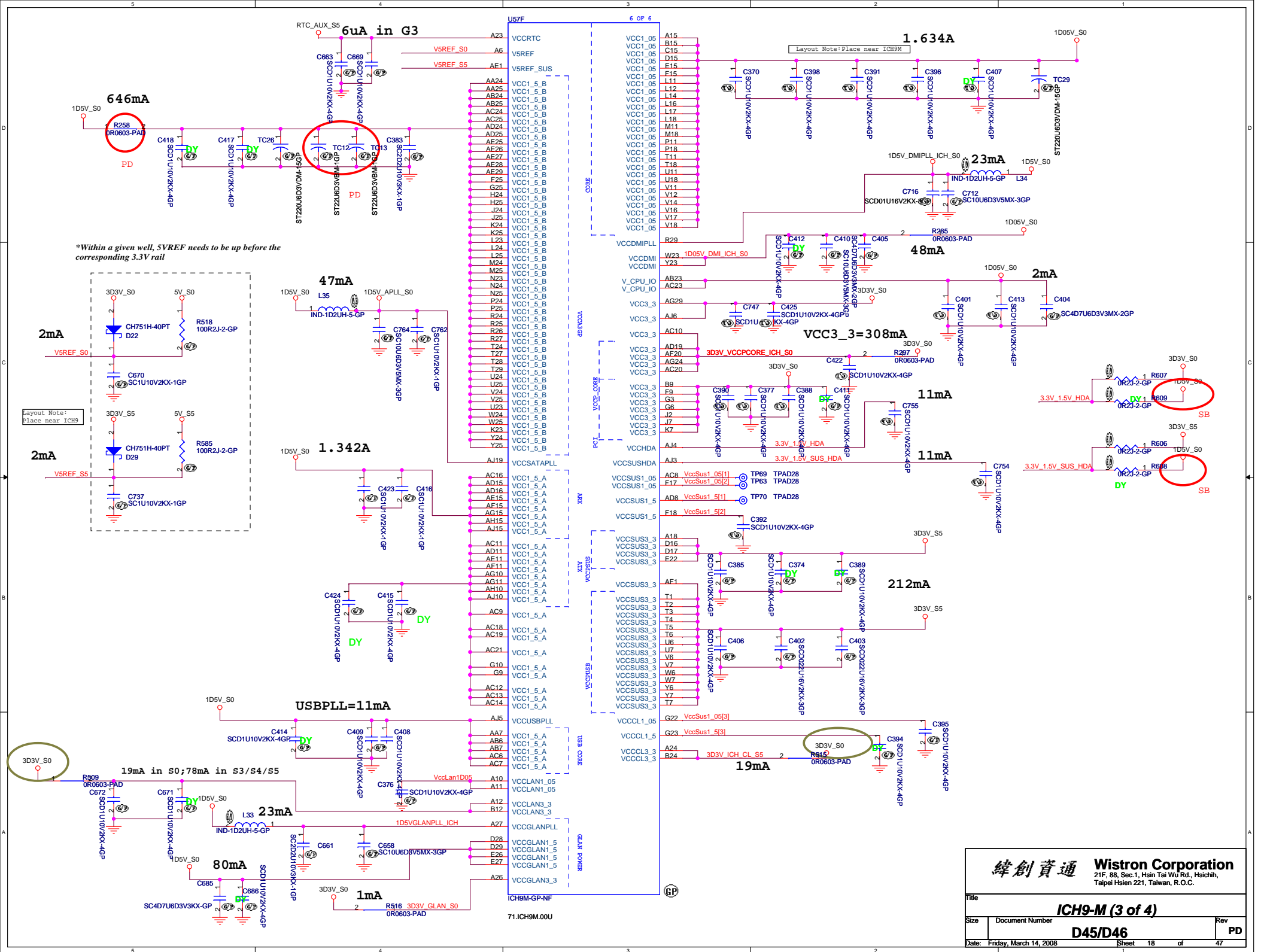
| Pair | Device    |
|------|-----------|
| 0    | USB1      |
| 1    | NC        |
| 2    | USB2      |
| 3    | USB3      |
| 4    | USB4      |
| 5    | BLUETOOTH |
| 6    | WEBCAM    |
| 7    | NC        |
| 8    | MINICARD  |
| 9    | UMTS      |
| 10   | NEW CARD  |

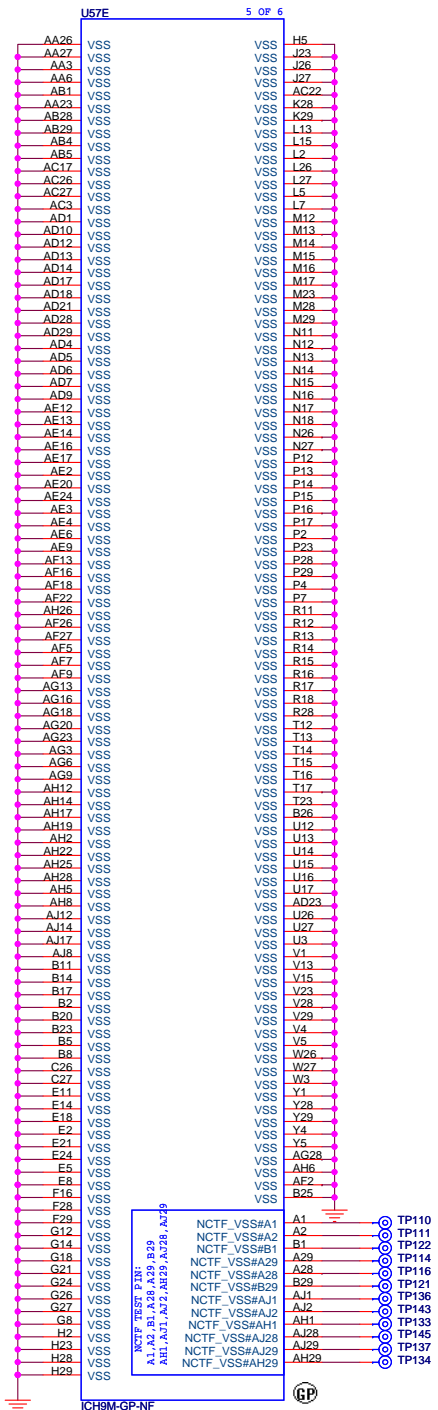


No Reboot Strap  
SPKR LOW = Default  
High = No Reboot

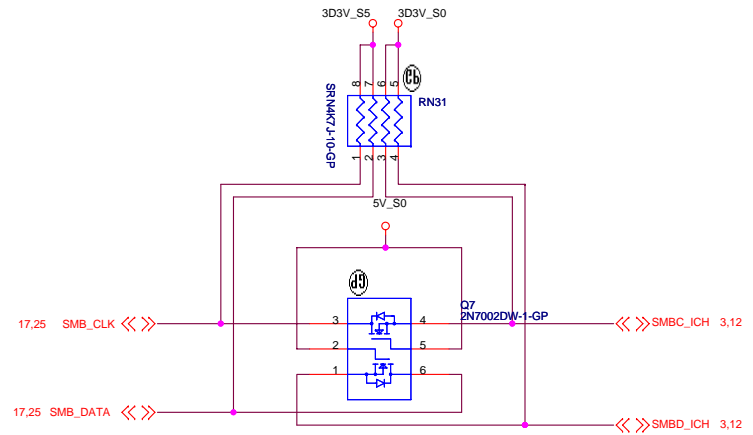
| BOOT BIOS Strap | PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location |
|-----------------|-----------|----------|--------------------|
| 0               | 0         | 0        | SPT                |
| 1               | 1         | 0        | PCT                |
| 1               | 1         | 1        | LDC (Default)      |

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71.ICH9M.00U



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

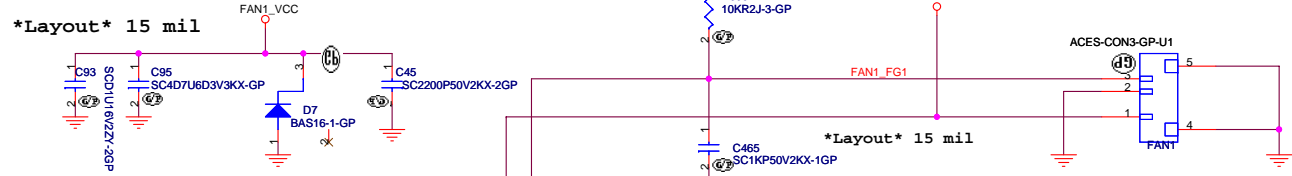
**SMBUS**

|             |  |  |  |
|-------------|--|--|--|
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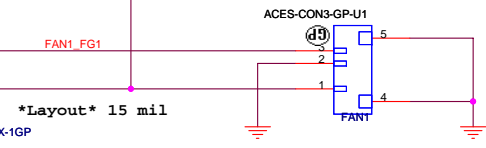
|       |                        |                |                        |
|-------|------------------------|----------------|------------------------|
| Title |                        |                | <b>ICH9-M (4 of 4)</b> |
| Size  | Document Number        | <b>D45/D46</b> |                        |
| Date: | Friday, March 14, 2008 | Sheet          | 19 of 47               |
|       |                        | Rev            | PD                     |

| TEMP.    | Digital Output Data Bits |     |      |     |
|----------|--------------------------|-----|------|-----|
|          | Sign                     | MSB | LSB  | EXT |
| +127.875 | 0                        | 111 | 1111 | 111 |
| +126.375 | 0                        | 111 | 1110 | 011 |
| +25.5    | 0                        | 001 | 1001 | 100 |
| +1.75    | 0                        | 000 | 0001 | 110 |
| +0.5     | 0                        | 000 | 0000 | 100 |
| +0.125   | 0                        | 000 | 0000 | 001 |
| -0.125   | 1                        | 111 | 1111 | 111 |
| -1.125   | 1                        | 111 | 1110 | 111 |
| -25.5    | 1                        | 110 | 0110 | 100 |
| -55.25   | 1                        | 100 | 1000 | 110 |
| -65.000  | 1                        | 011 | 1111 | 000 |

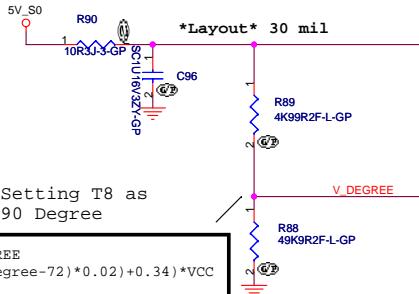
\*Layout\* 15 mil



\*Layout\* 15 mil



\*Layout\* 30 mil

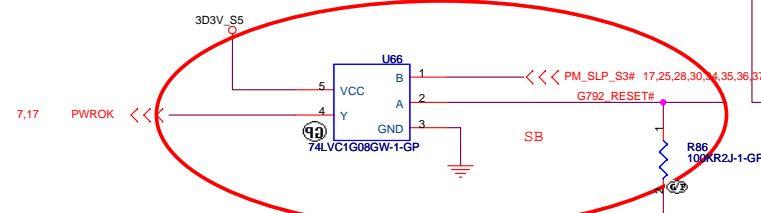


Setting T8 as 90 Degree

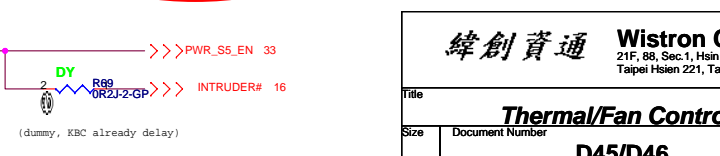
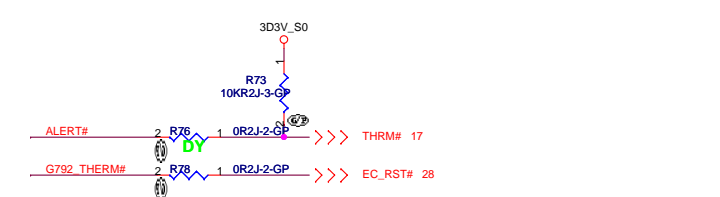
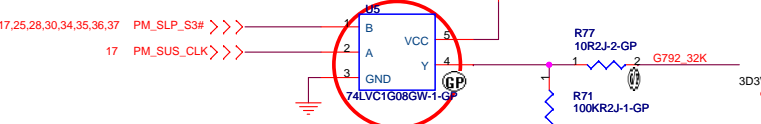
V\_DEGREE  
 $= (((\text{Degree} - 72) * 0.02) + 0.34) * \text{VCC}$

DXP1:108 Degree (CPU)  
 DXP2:H/W Setting 100(System)  
 DXP3:105 Degree (SYSTEM)

Place near chip as close



32K suspend clock output



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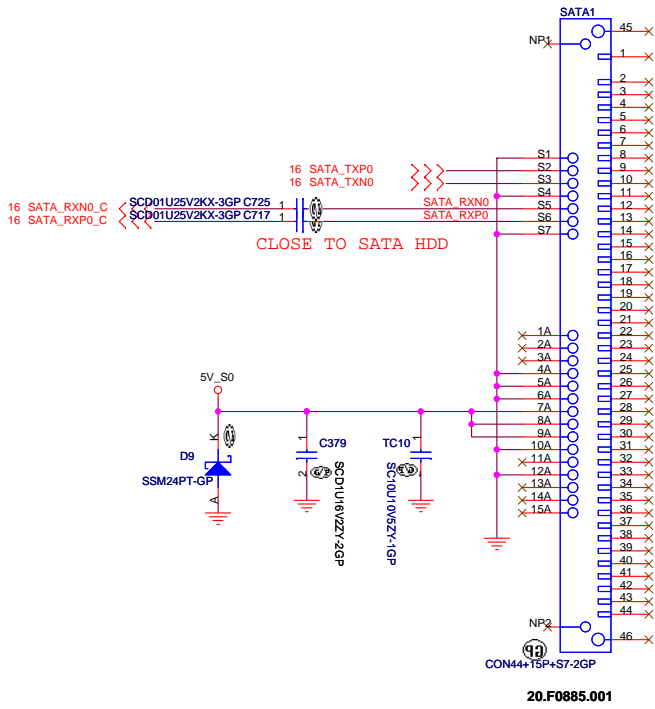
Title: **Thermal/Fan Controller**  
**D45/D46**

Size: Document Number  
 Date: Friday, March 14, 2008

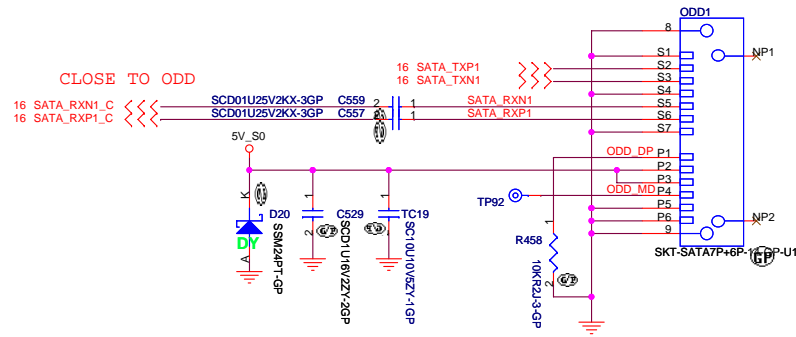
Rev: PD  
 Sheet 20 of 47



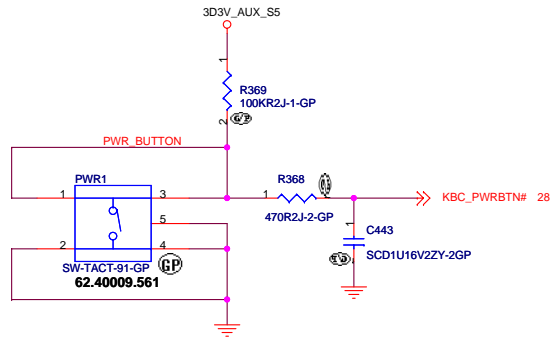
# SATA HD Connector



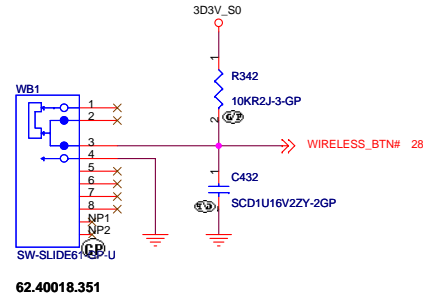
# ODD Connector



# LAUNCH BUTTON



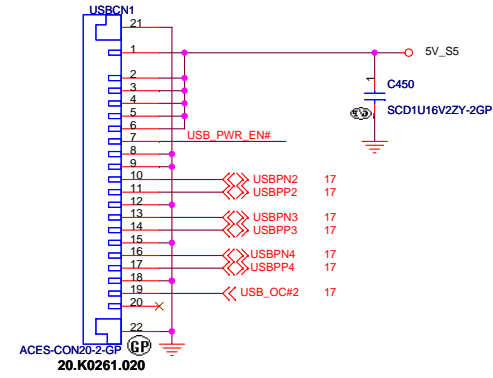
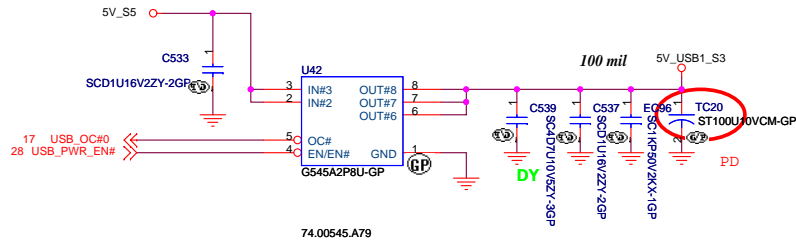
# WIRELESS BUTTON



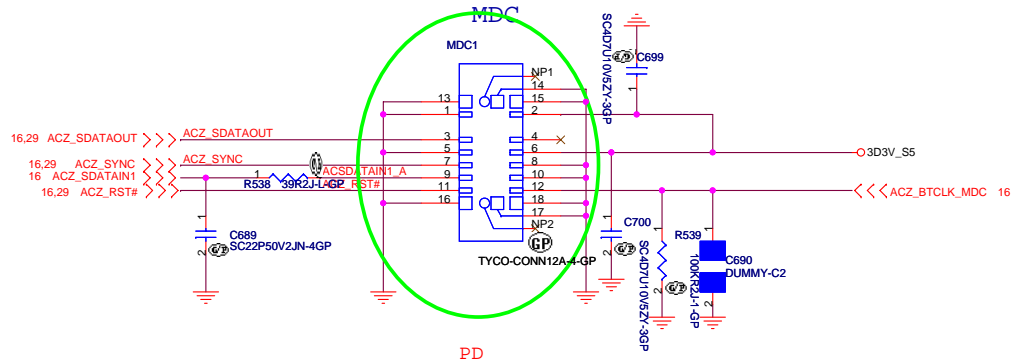
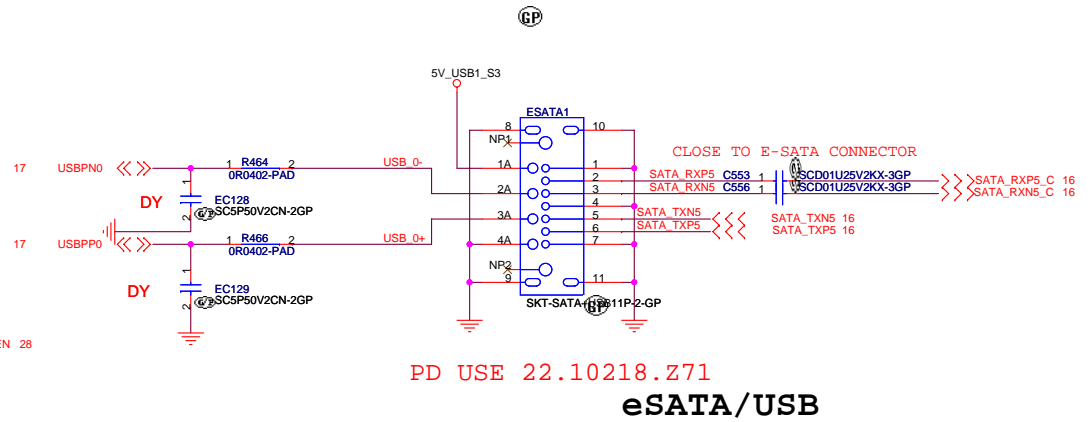
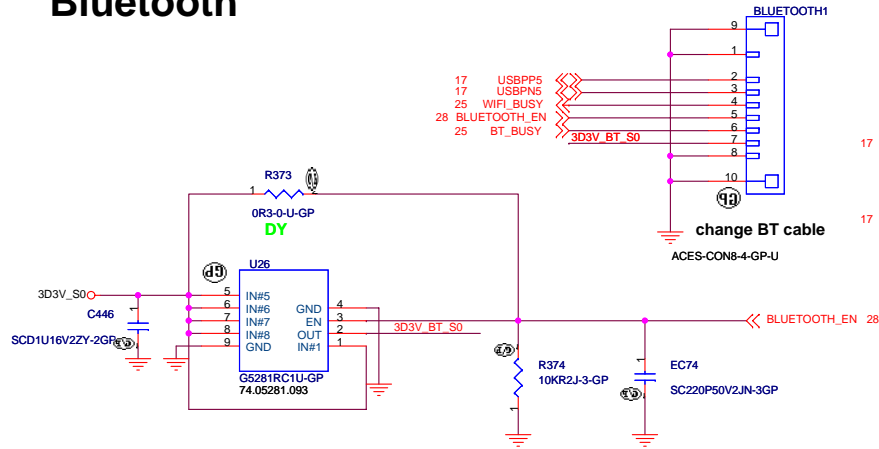
ZZZZ

|                              |                 |  |                  |
|------------------------------|-----------------|--|------------------|
| <b>緯創資通</b>                  |                 | <b>Wistron Corporation</b>   |                  |
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| <b>Title</b>                 |                 |  |                  |
| <b>HDD / CDROM / LAUNCH</b>  |                 |  |                  |
| Size                         | Document Number | <b>D45/D46</b>   | Rev<br><b>PD</b> |
| Date: Friday, March 14, 2008 |                 | Sheet 21   | of 47            |

# USB BOARD CONN

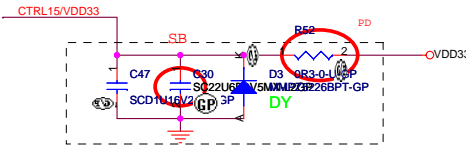
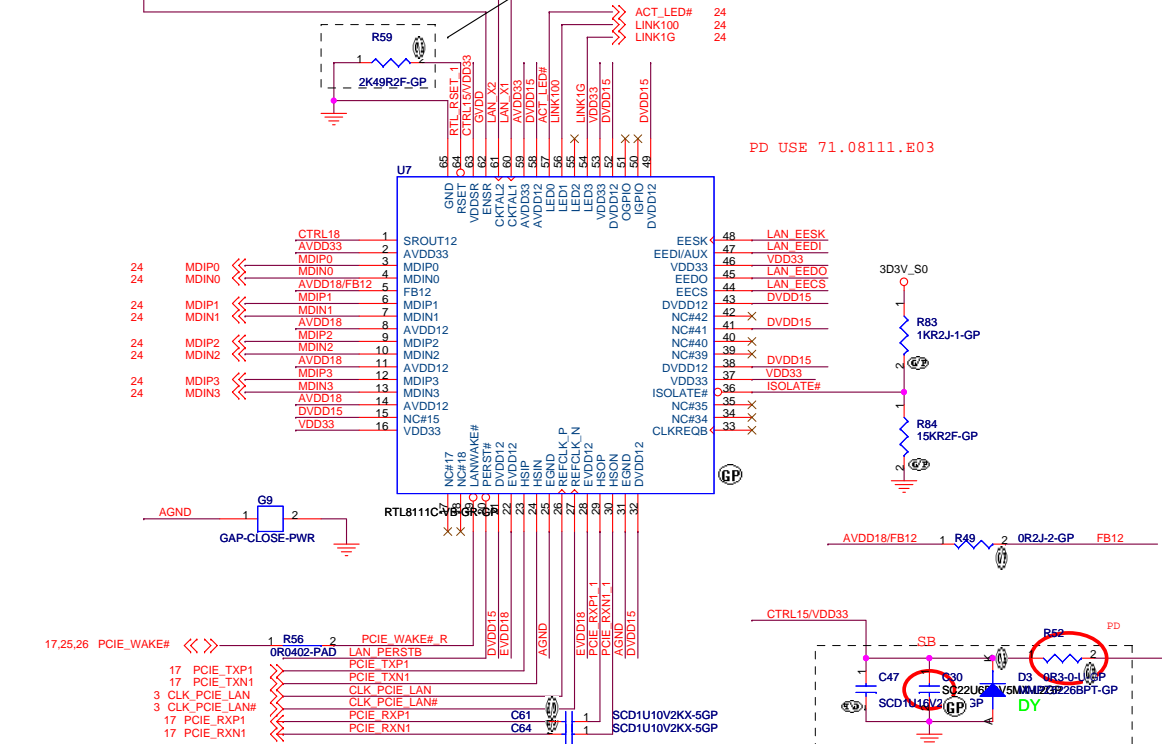
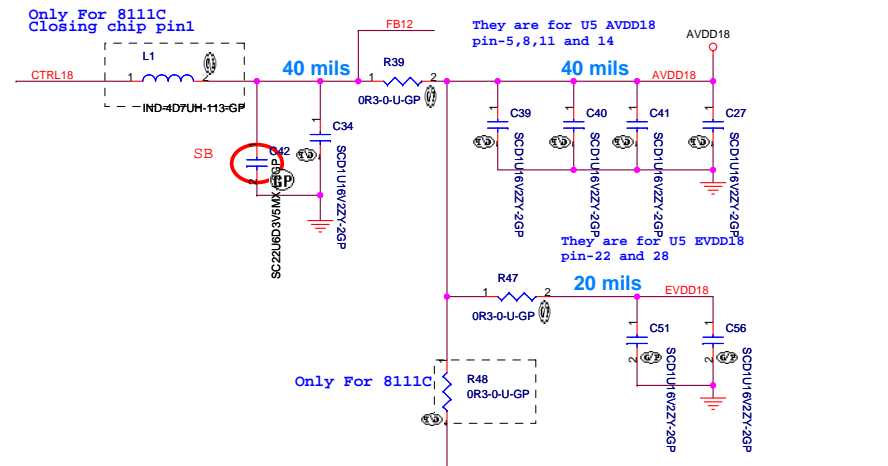
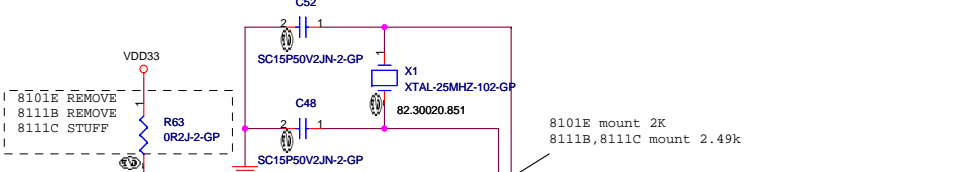
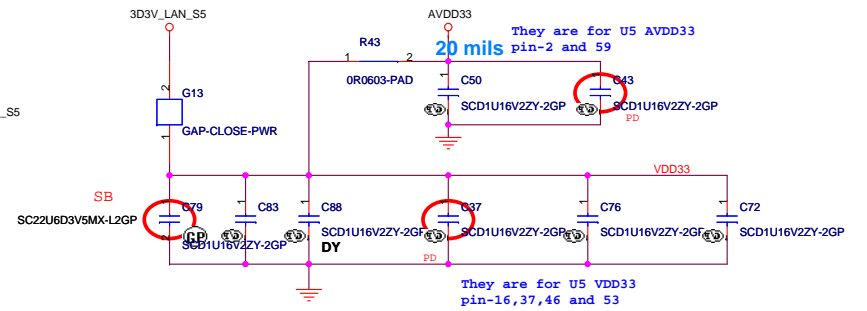
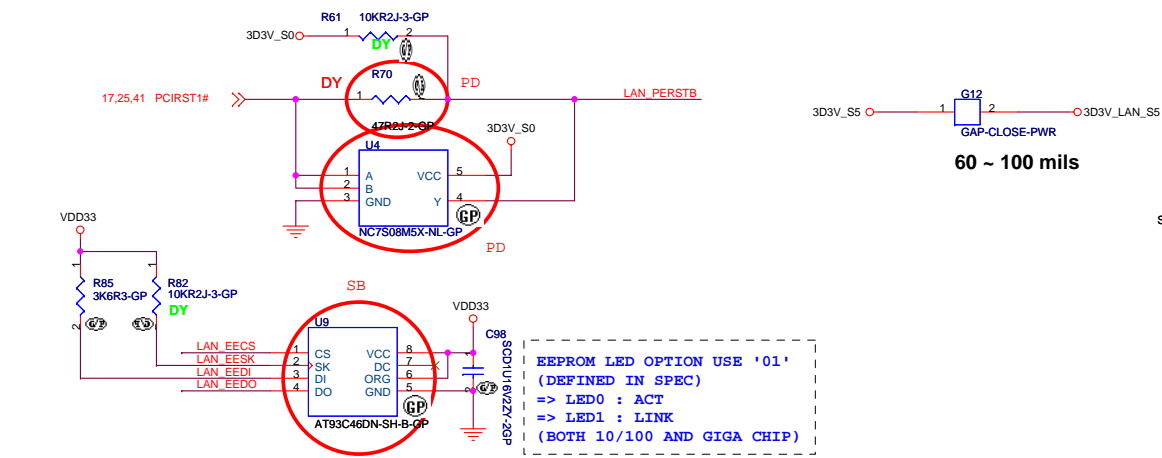


## Bluetooth



ZZZZ

|                                    |                        |  |          |
|------------------------------------|------------------------|--|----------|
| <b>緯創資通</b>                        |                        | <b>Wistron Corporation</b>   |          |
|                                    |                        | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |          |
| Title <b>USB / MDC / BLUETOOTH</b> |                        |  |          |
| Size                               | Document Number        | Rev  | PD       |
|                                    | <b>D45/D46</b>         |  |          |
| Date:                              | Friday, March 14, 2008 | Sheet  | 22 of 47 |



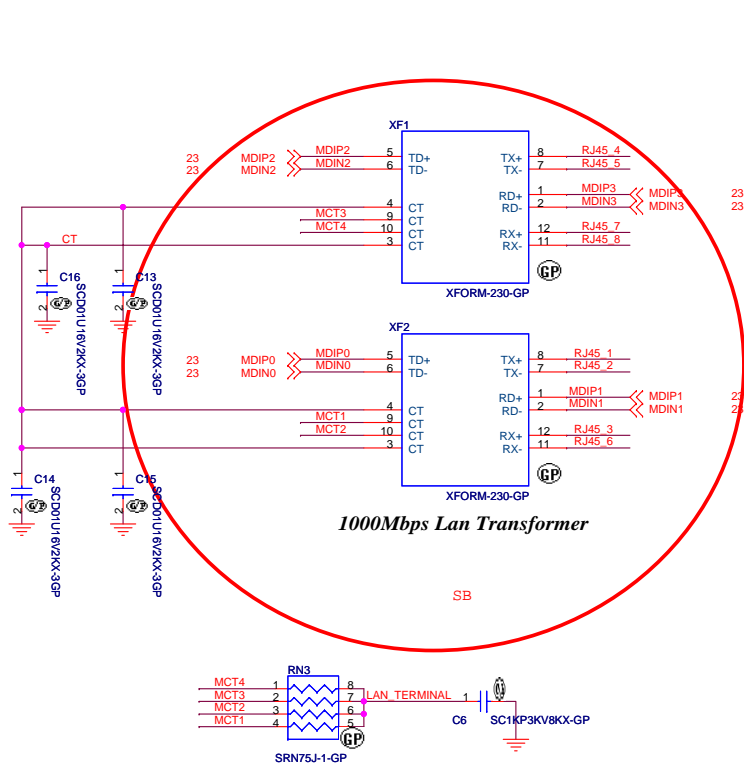
Layout - 1:0.1u first,2: 22u,3:D33

ZZZZ

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Taipei Hsien 221, Taiwan, R.O.C.

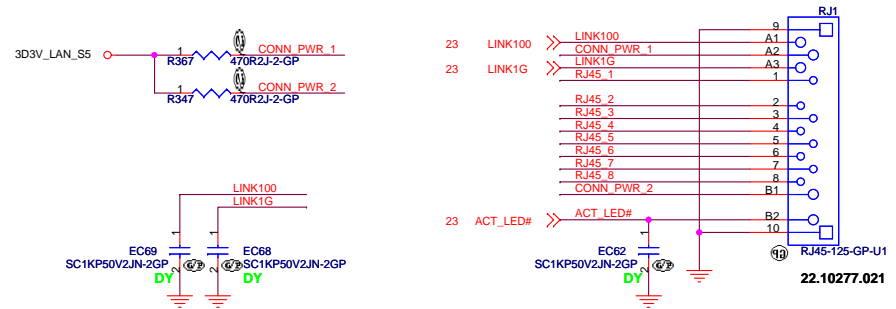
| Title<br><b>LAN RTL8111C</b> |                 |          |                       |
|------------------------------|-----------------|----------|-----------------------|
| Size                         | Document Number |          | Rev<br><b>D45/D46</b> |
| Date: Friday, March 14, 2008 |                 | Sheet 23 | of 47<br><b>PD</b>    |

# Lan Conn

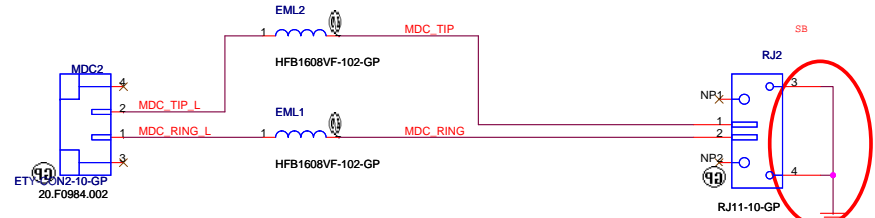


1000Mbps Lan Transformer

SB



22.10277.021



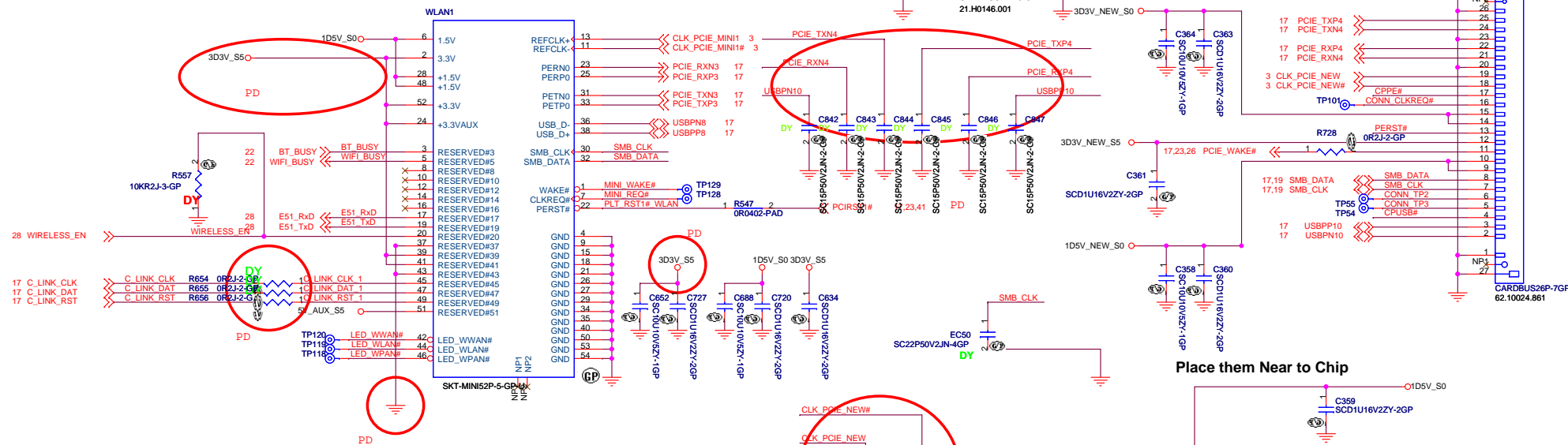
62.10044.201

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

ZZZZ

|                      |                        |  |          |
|----------------------|------------------------|--|----------|
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| <b>LAN Connector</b> |                        |  |          |
| Size                 | Document Number        | Rev  | PD       |
|                      | <b>D45/D46</b>         |  |          |
| Date:                | Friday, March 14, 2008 | Sheet  | 24 of 47 |

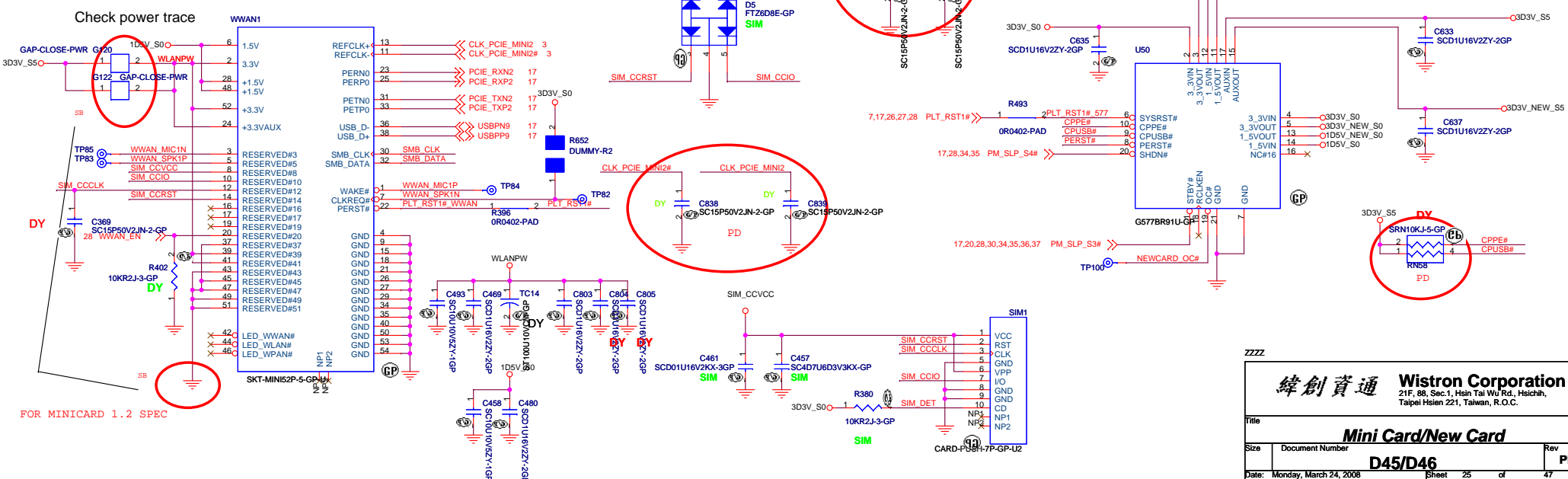
# Mini Card Connector



Place them Near to Chip

# WWAN Connector

(ROBISON RESERVE)



FOR MINICARD 1.2 SPEC

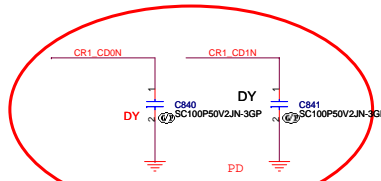
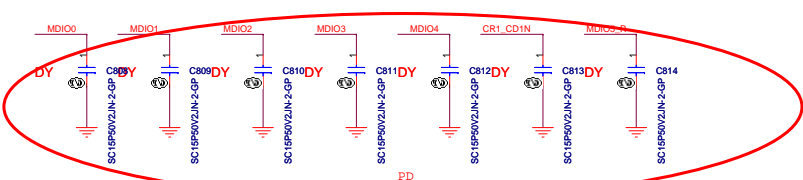
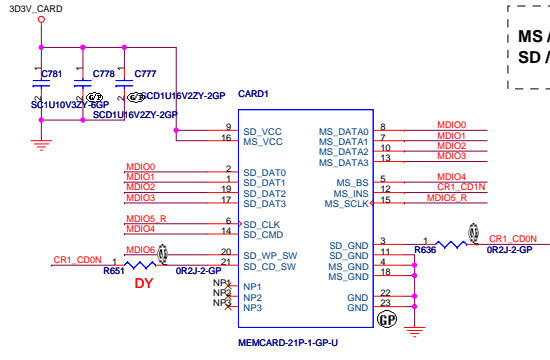
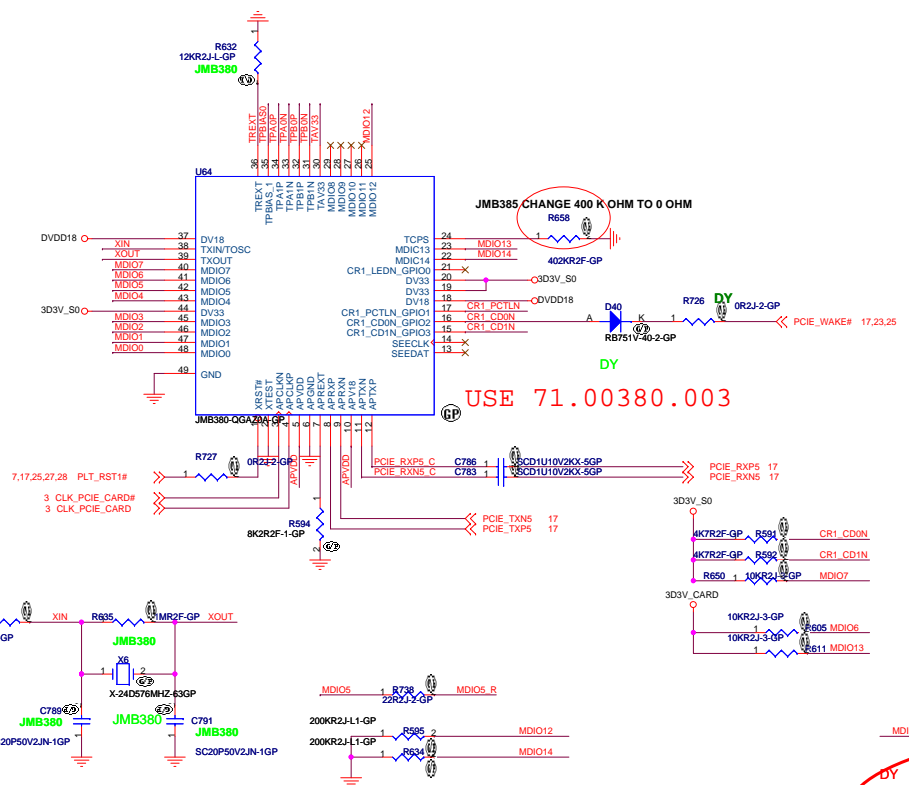
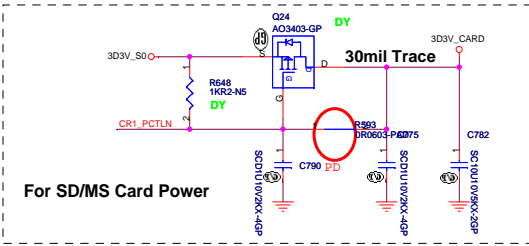
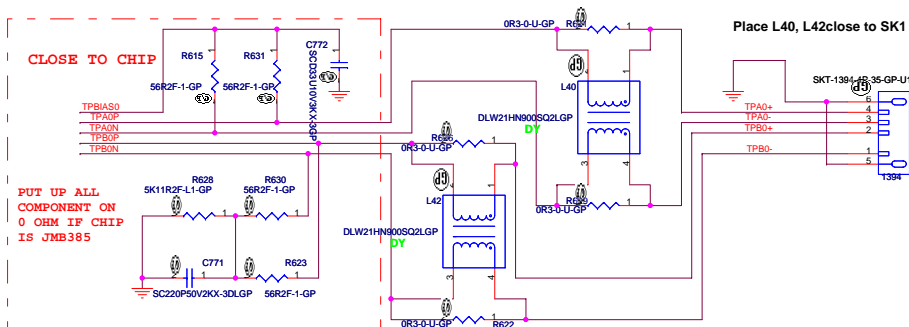
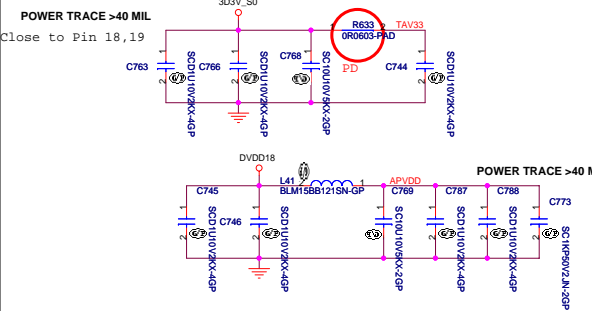
7777

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Title: **Mini Card/New Card**

Size: Document Number: **D45/D46** Rev: **PD**

Date: Monday, March 24, 2008 Sheet: 25 of 47



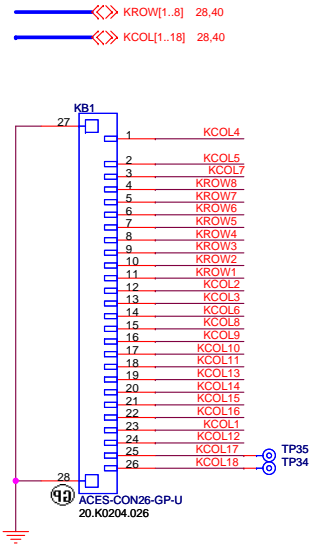
**緯創資通** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Card Reader JM380**

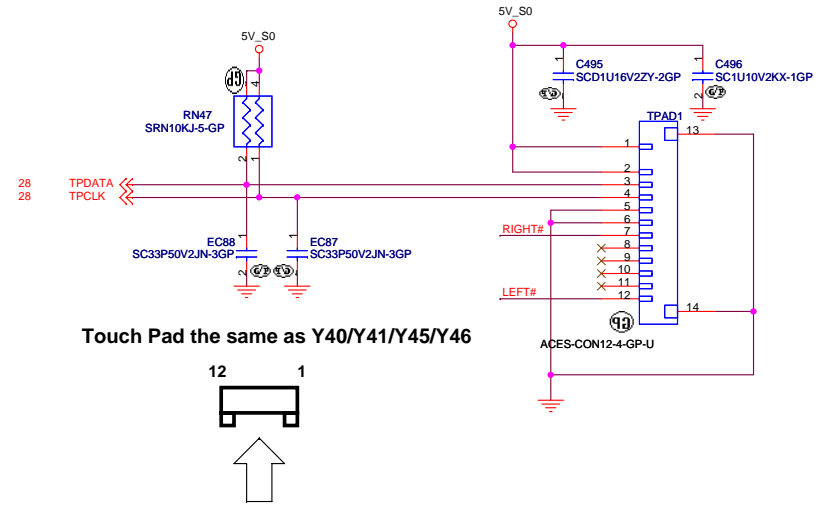
Size: Custom    Document Number:    Rev: PD  
Date: Monday, March 24, 2008    Sheet: 26 of 47



# Internal KeyBoard Connector

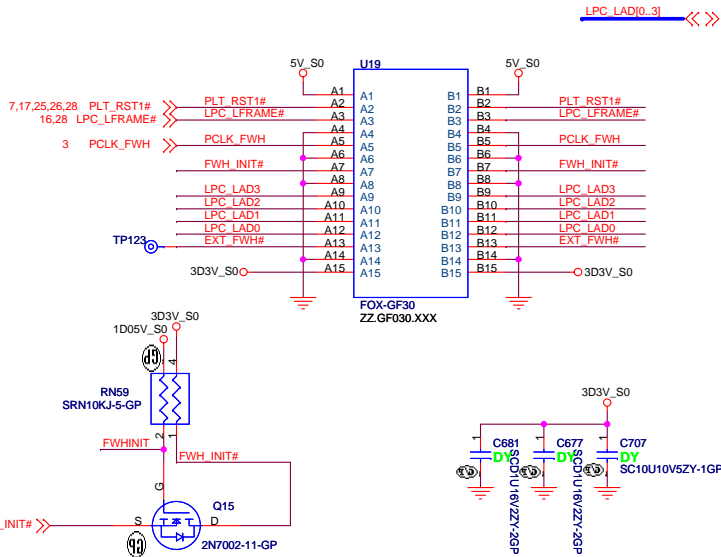


# TouchPad Connector



Touch Pad the same as Y40/Y41/Y45/Y46

# GOLDEN FINGER FOR DEBUG BOARD

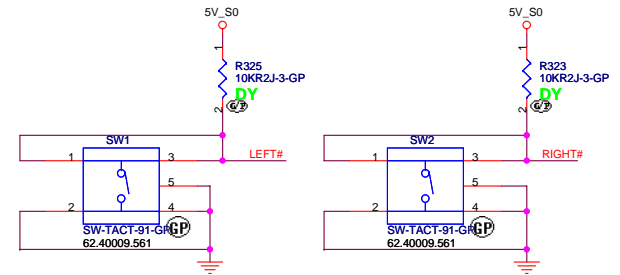


TOP VIEW

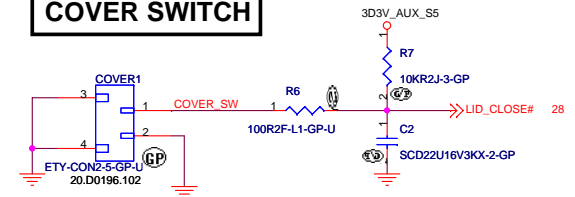
- A15 (B1)
- A14 (B2)
- ...
- A2 (B14)
- A1 (B15)

(BOTTOM VIEW)

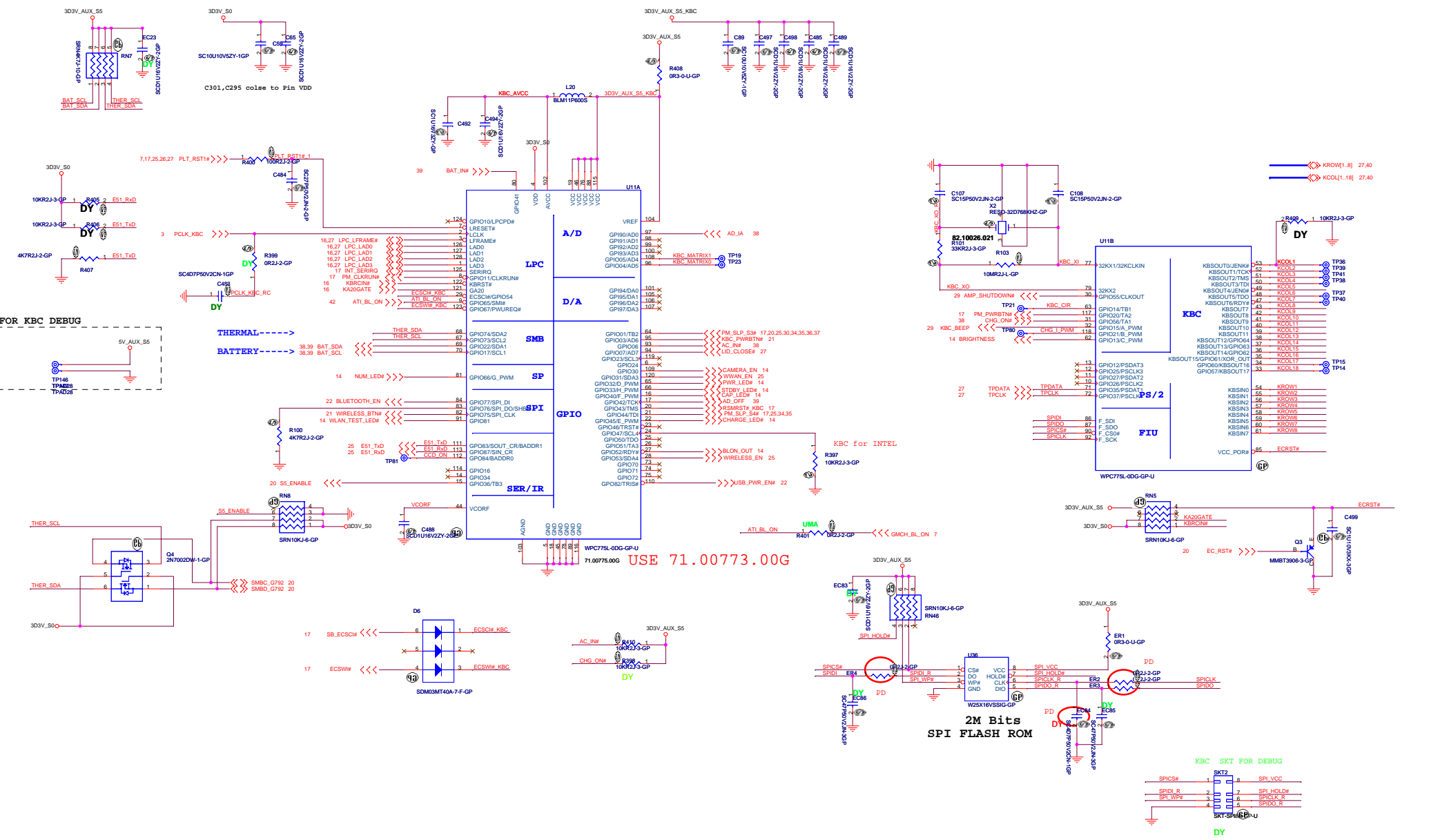
# 15" TOUCHPAD BUTTON SWITCH

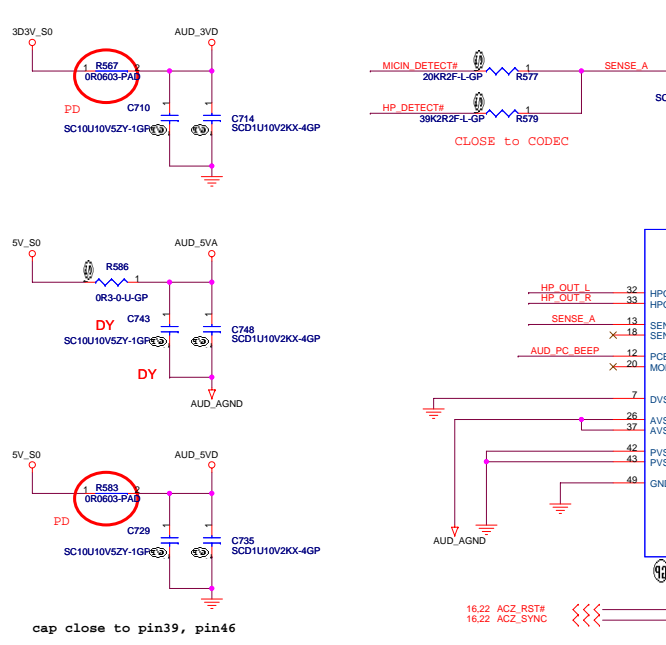


# COVER SWITCH

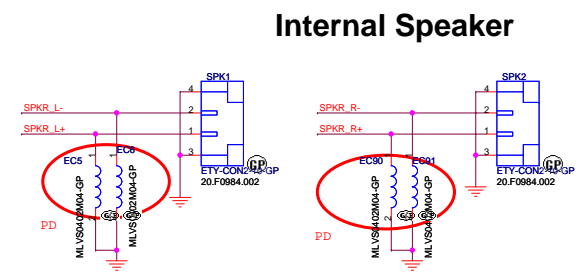
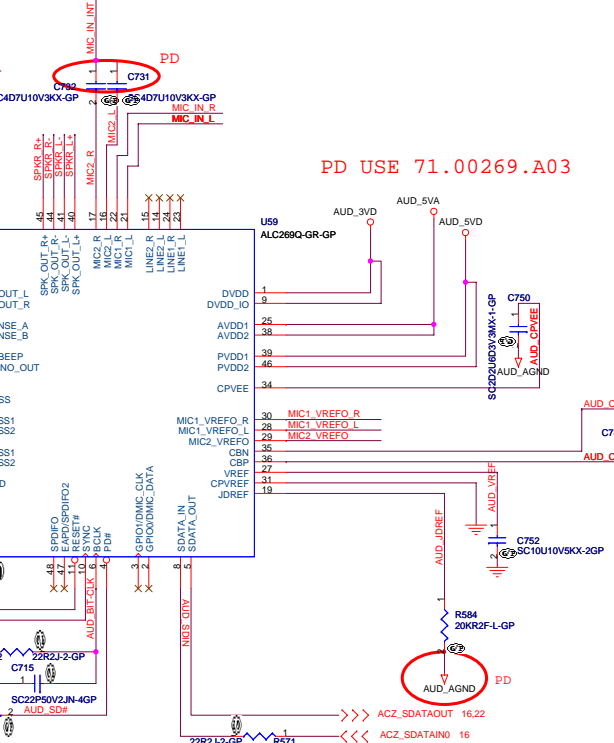


ZZZZ

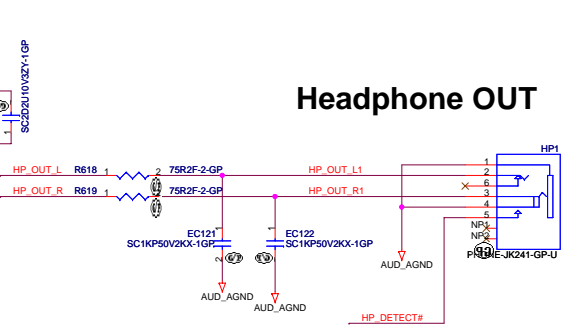




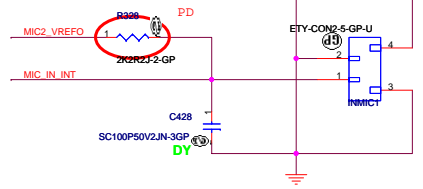
PD USE 71.00269.A03



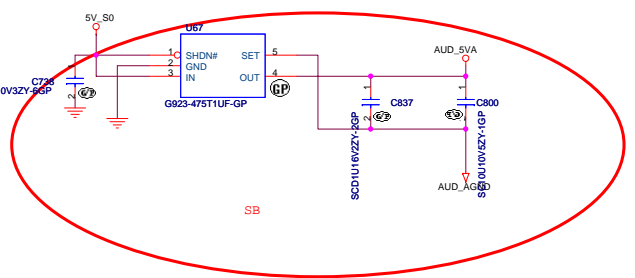
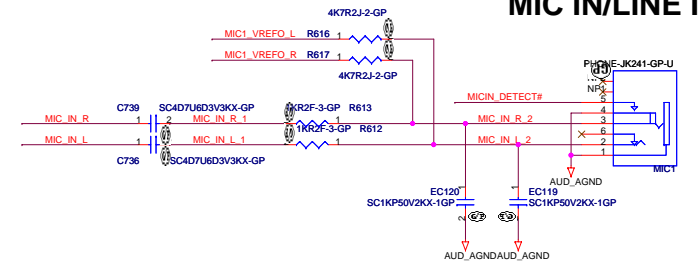
### Headphone OUT



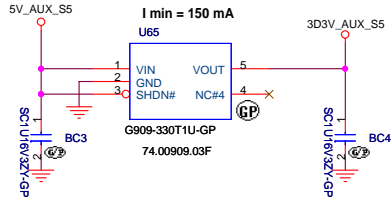
### Internal MIC



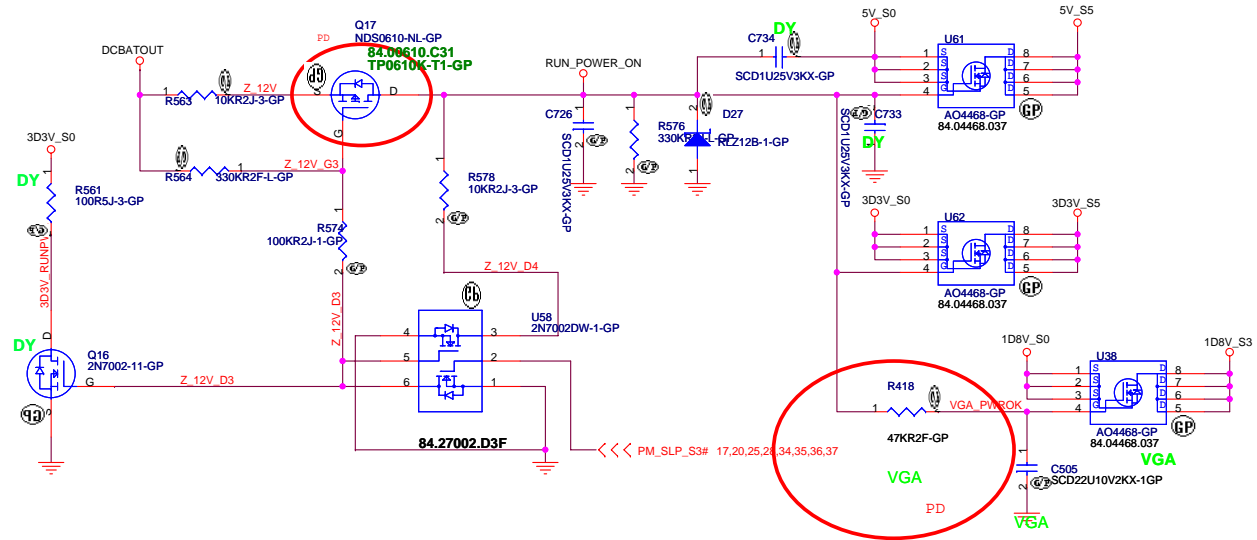
### MIC IN/LINE IN



# Aux Power 3D3V\_AUX\_S5



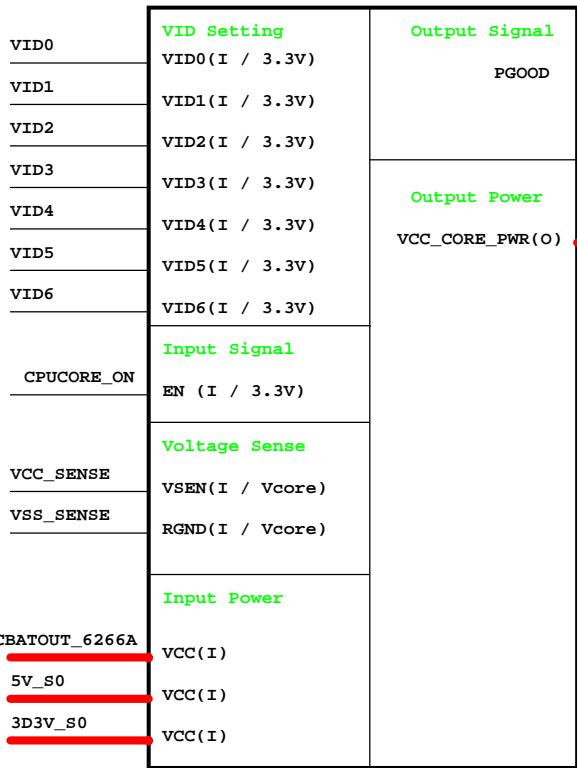
# Run Power



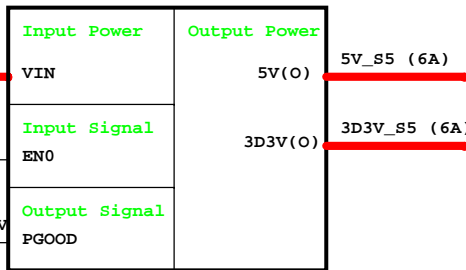
ZZZZ

|  |                 |
|--|-----------------|
| <b>緯創資通 Wistron Corporation</b>  |                 |
| 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C. |                 |
| <b>Title RUN POWER and 3D3V_AUX_S5</b>                                     |                 |
| Size   | Document Number |
| <b>D45/D46</b>   |                 |
| Date: Friday, March 14, 2008   | Rev <b>PD</b>   |
| Sheet 30   | of 47           |

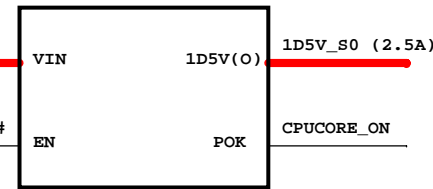
**CPU\_CORE**  
ISL6266A



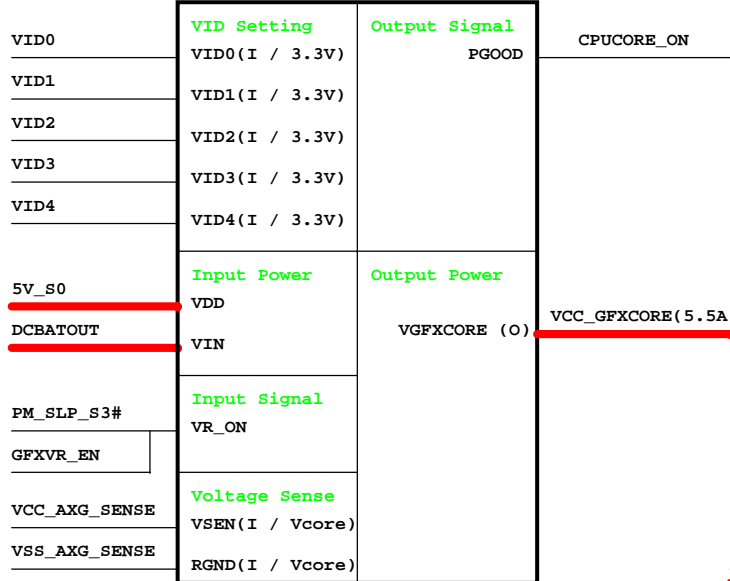
**TPS51125**  
5V/3D3V



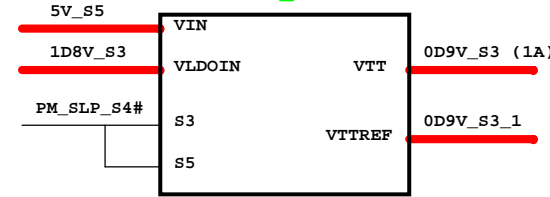
**APL5912**  
1D5V\_S0



**GFX\_CORE**  
ISL6263A



**0D9V\_S0**



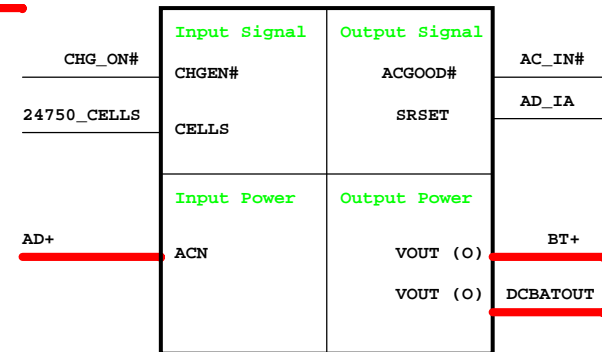
**TPS51100**

**2D5V\_S0**

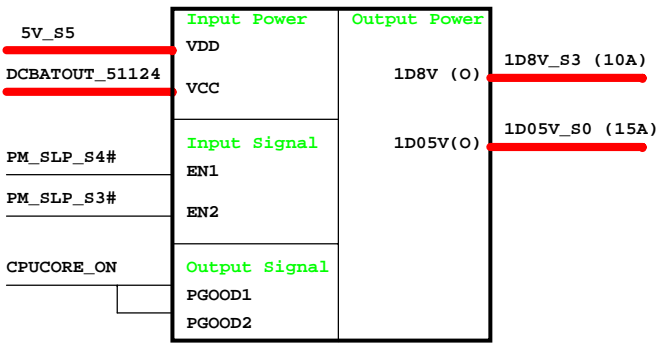


**APL5913**

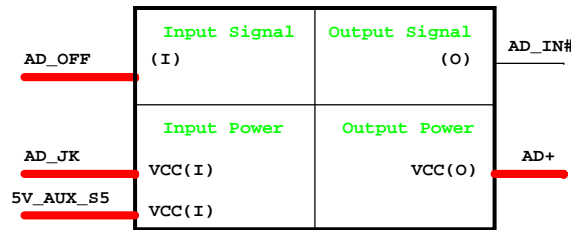
**Charger BQ24750**



**TPS51124**  
1D8V/1D05V



**Adapter**



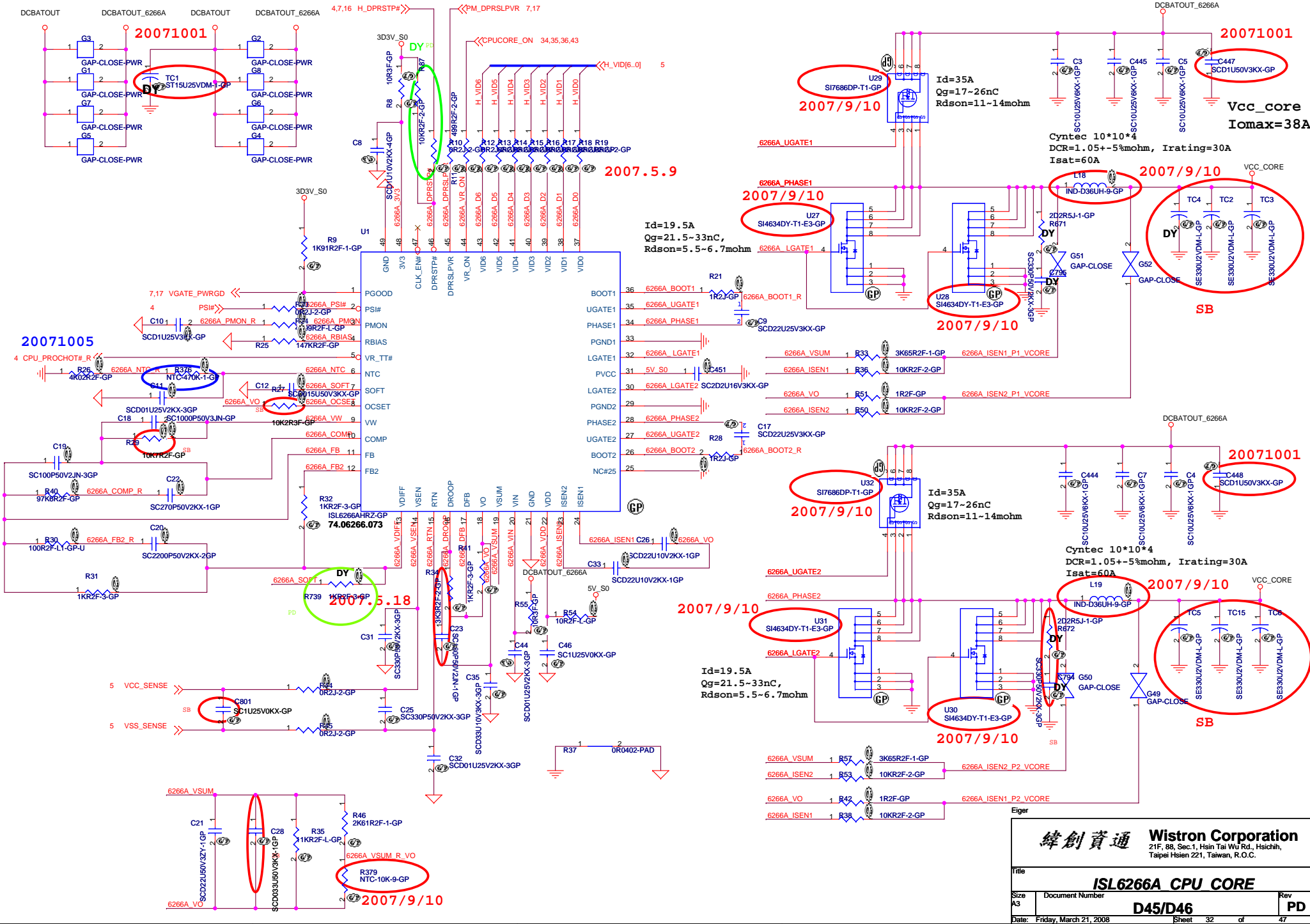
Eiger

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Title: **Power Sequence Logic**

Size B Document Number: **Eiger** Rev PD

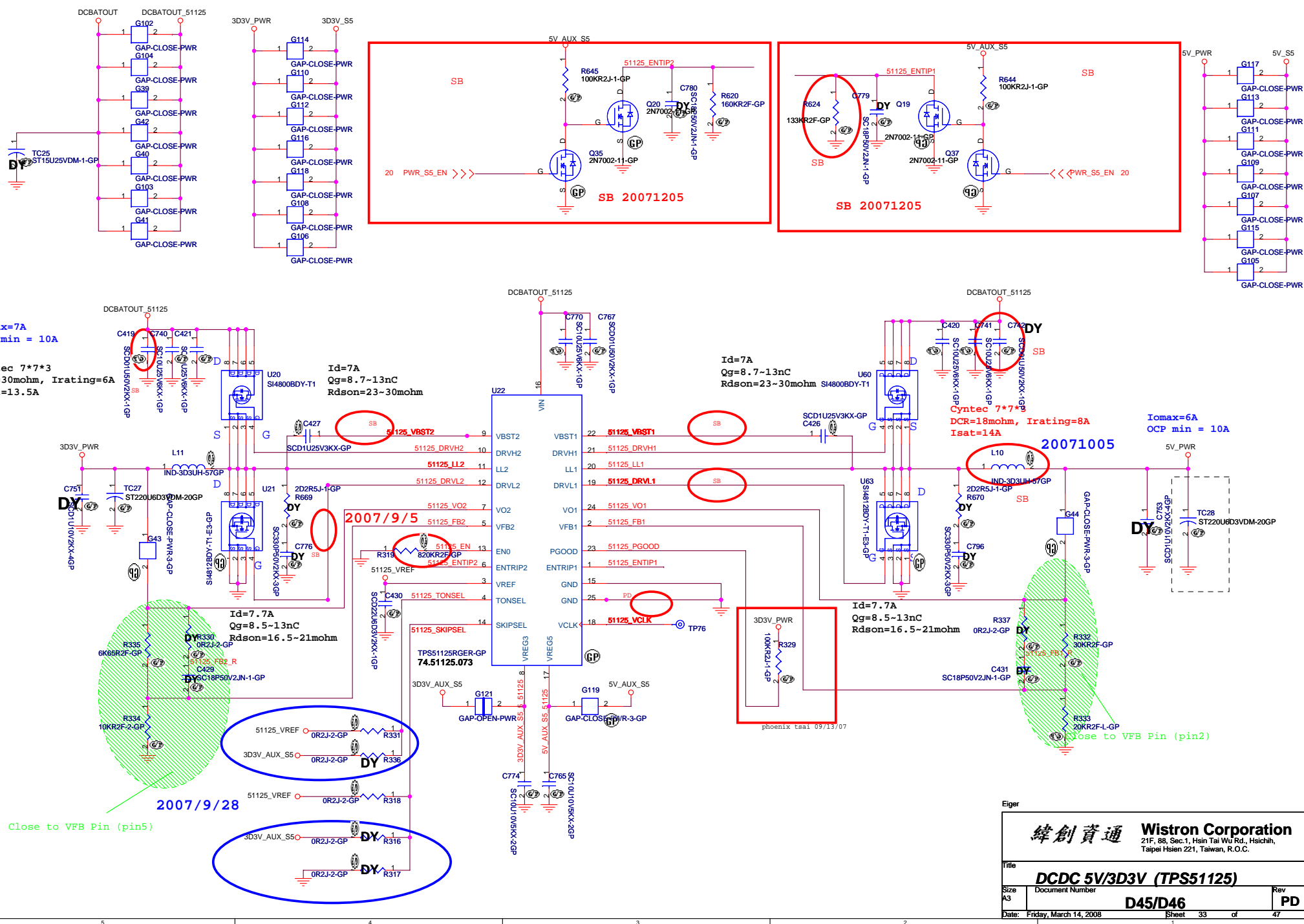
Date: Friday, March 14, 2008 Sheet 31 of 47



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 Taipei Hsien 221, Taiwan, R.O.C.

|                          |                        |                |
|--------------------------|------------------------|----------------|
| Title                    |                        |                |
| <b>ISL6266A CPU CORE</b> |                        |                |
| Size                     | Document Number        | Rev            |
| A3                       | D45/D46                | PD             |
| Date:                    | Friday, March 21, 2008 | Sheet 32 of 47 |





Iomax=7A  
 OCP min = 10A  
 Cyntec 7\*7\*3  
 DCR=30mohm, Irating=6A  
 Isat=13.5A

Iomax=6A  
 OCP min = 10A

Eiger

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 Taipei Hsien 221, Taiwan, R.O.C.

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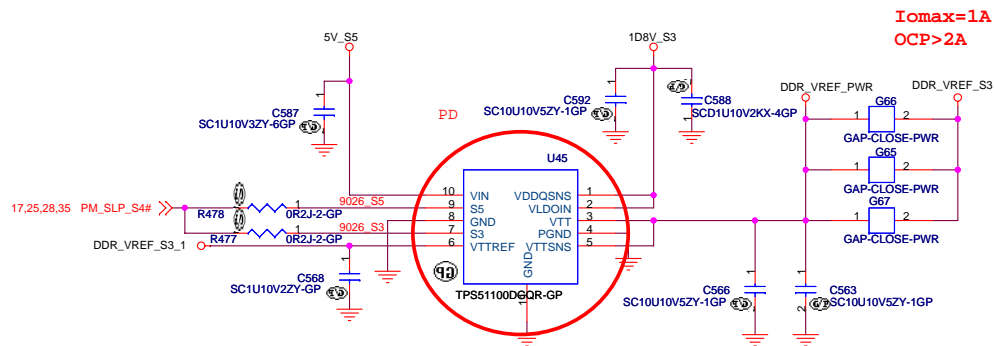
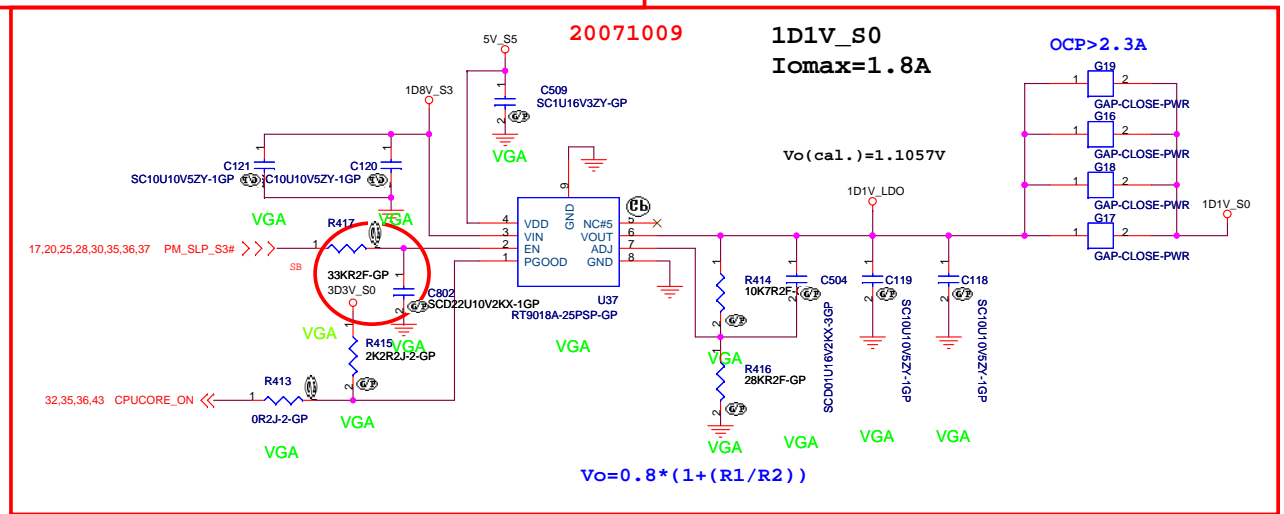
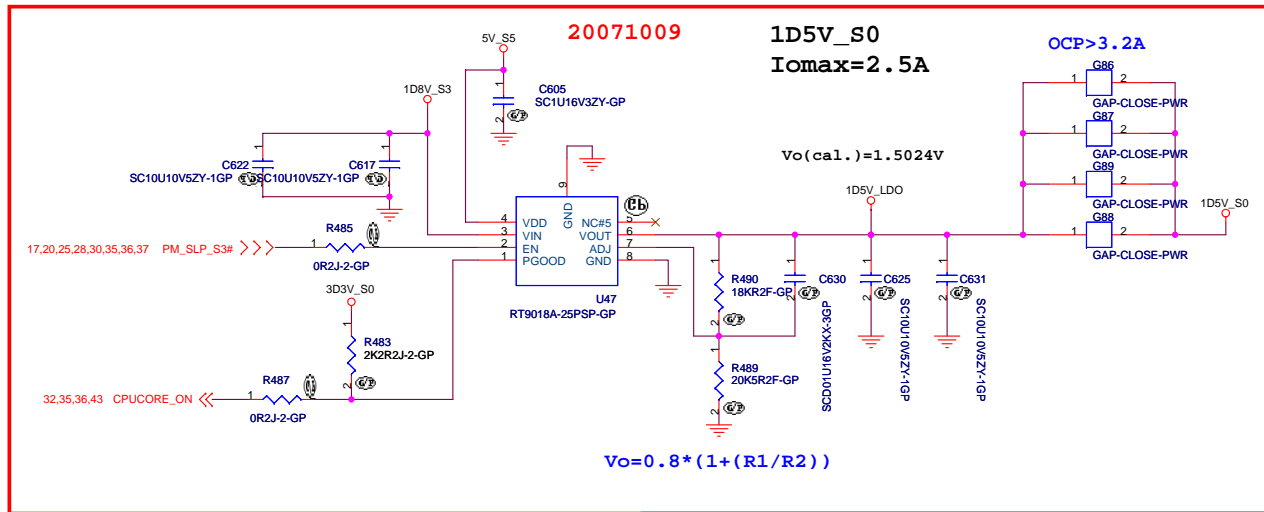
Title  
**DCDC 5V/3D3V (TPS51125)**

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Size A3 Document Number **D45/D46** Rev PD

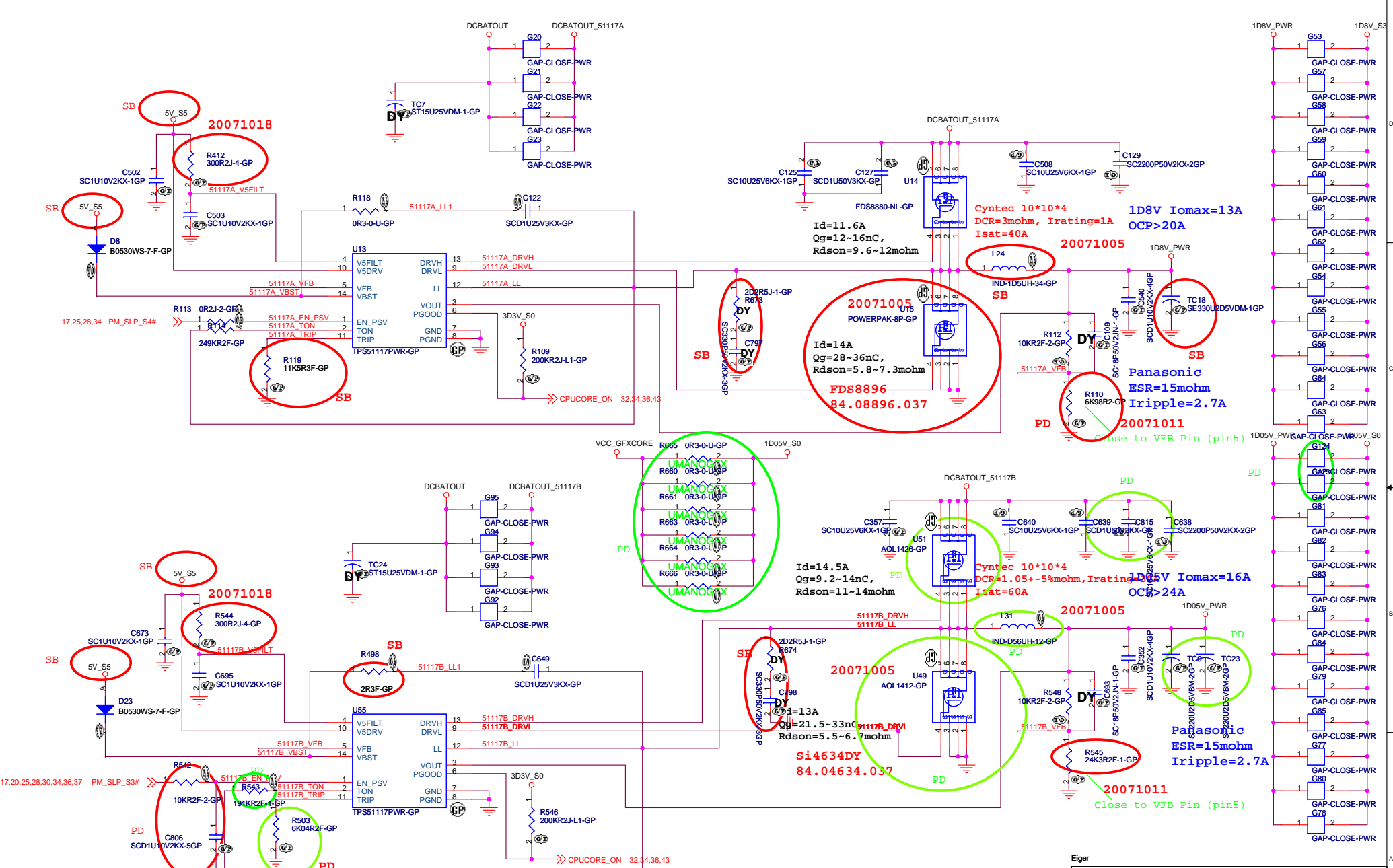
---

Date: Friday, March 14, 2008 Sheet 33 of 47



Eiger

|                              |                 |  |       |
|------------------------------|-----------------|--|-------|
| <b>緯創資通</b>                  |                 | <b>Wistron Corporation</b>   |       |
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| Title                        |                 |  |       |
| <b>1D5V &amp; 0D9V</b>       |                 |  |       |
| Size                         | Document Number |  | Rev   |
| A3                           |                 |  | PD    |
| Date: Friday, March 14, 2008 |                 |  |       |
|                              |                 | Sheet 34   | of 47 |



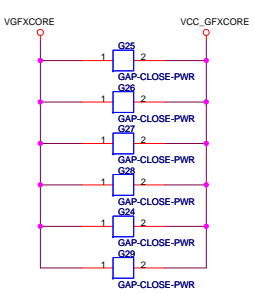
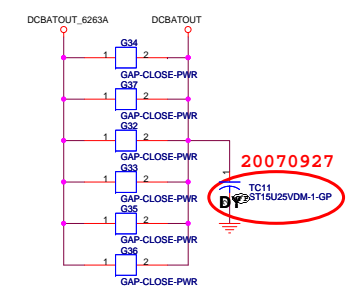
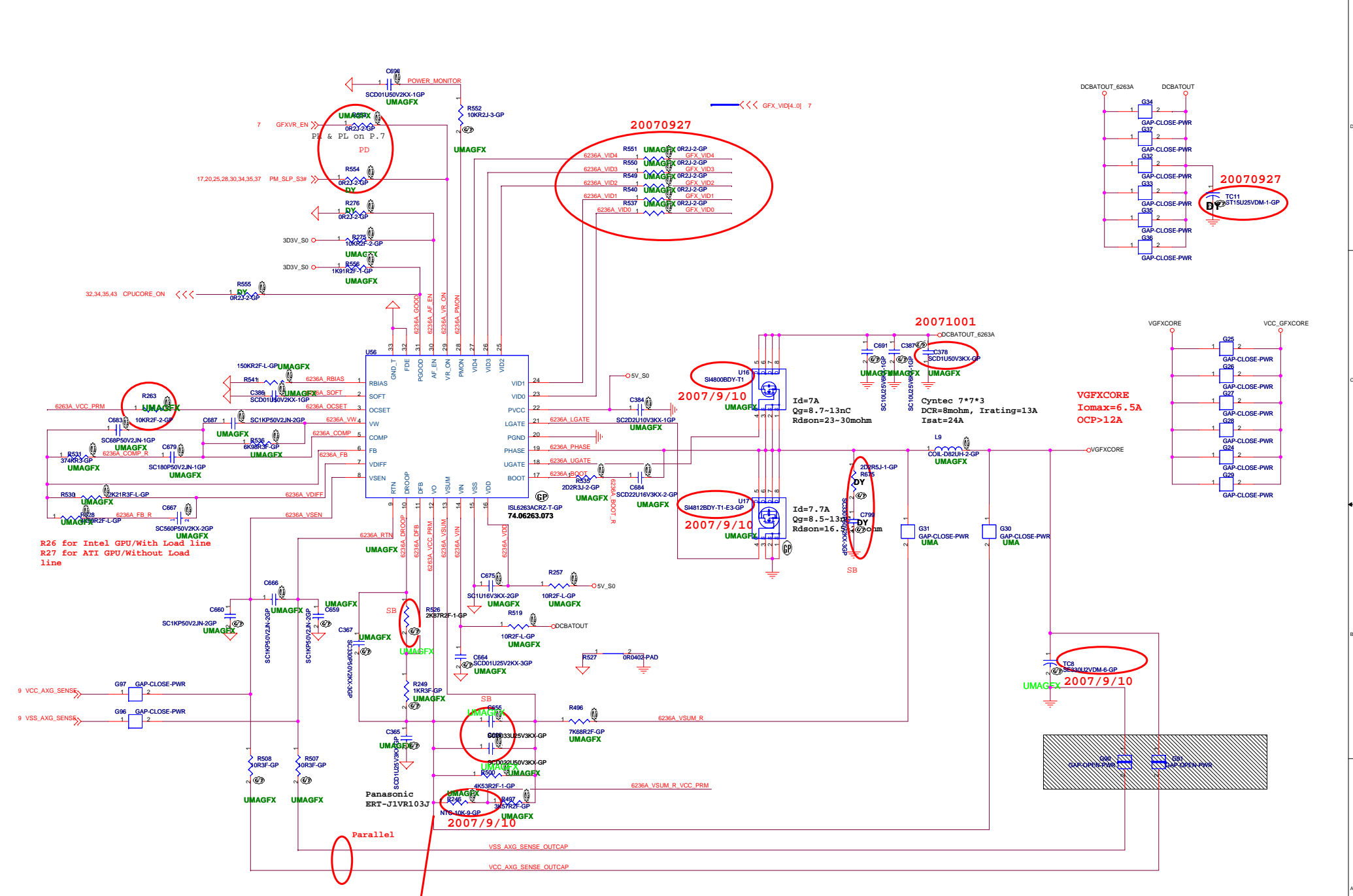
$$V_{out} = 0.75V * (R1 + R2) / R2$$

Eiger

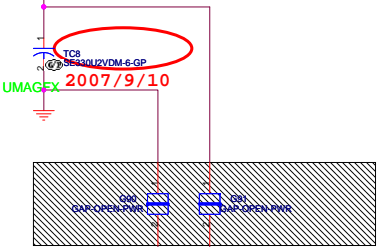
**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

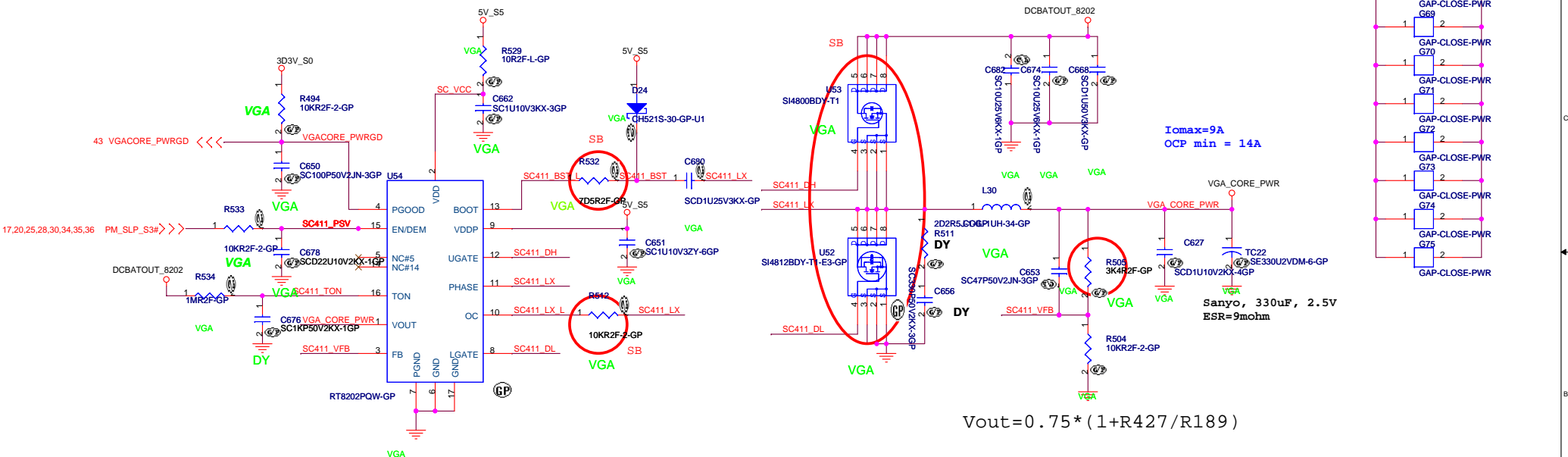
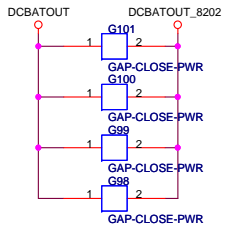
Title: **TPS51117 1D8V 1D05V**

|                              |                 |                |     |           |
|------------------------------|-----------------|----------------|-----|-----------|
| Size A3                      | Document Number | <b>D45/D46</b> | Rev | <b>PD</b> |
| Date: Monday, March 24, 2008 | Sheet           | 35             | of  | 47        |



VGFXCORE  
 I<sub>o</sub>max=6.5A  
 OCP>12A

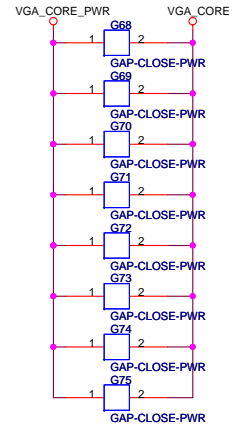




I<sub>omax</sub> = 9A  
OCP min = 14A

Sanyo, 330uF, 2.5V  
ESR=9mohm

$$V_{out} = 0.75 * (1 + R427/R189)$$



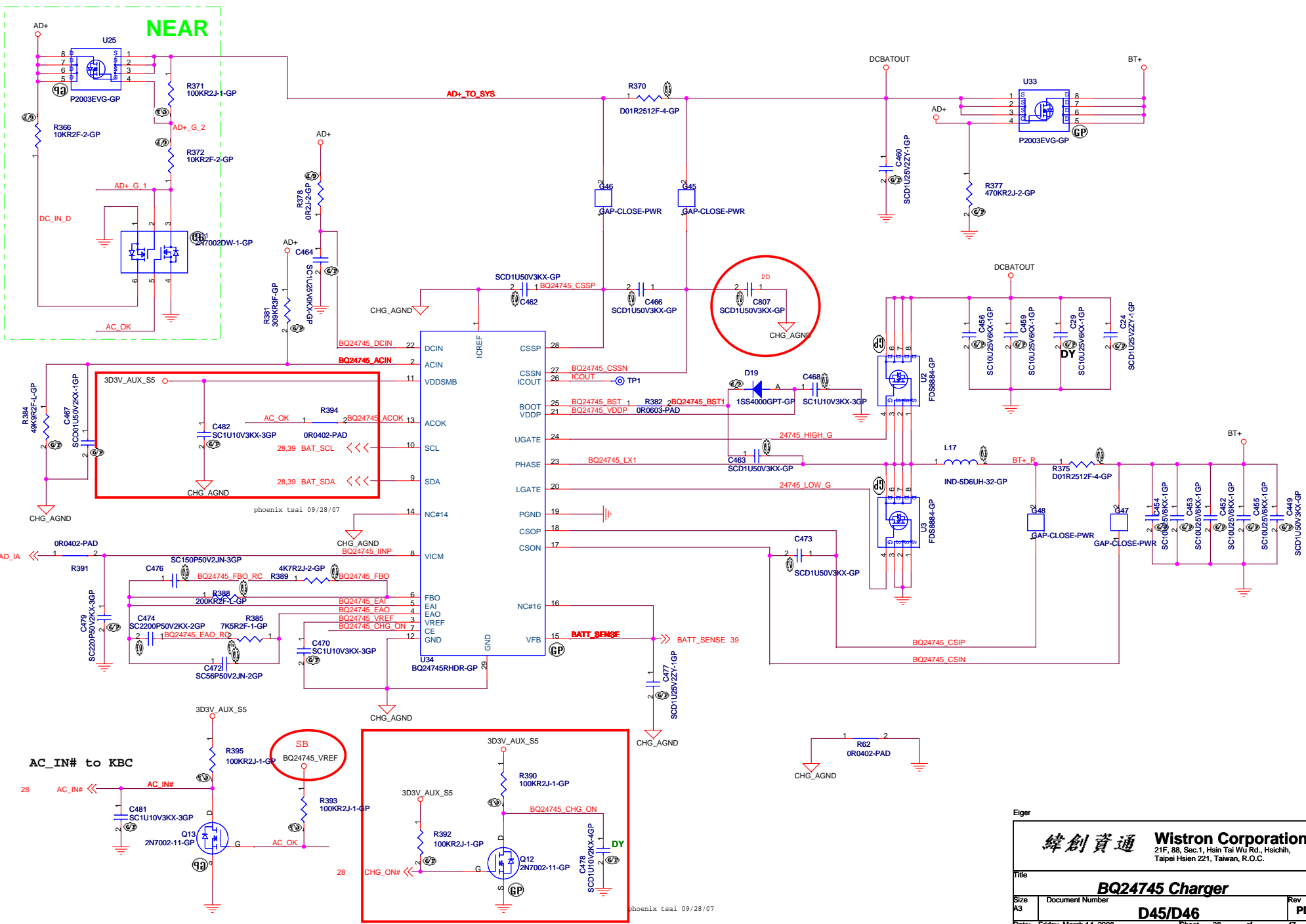
Eiger

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Title: **VGA CORE S0 (UMA)**

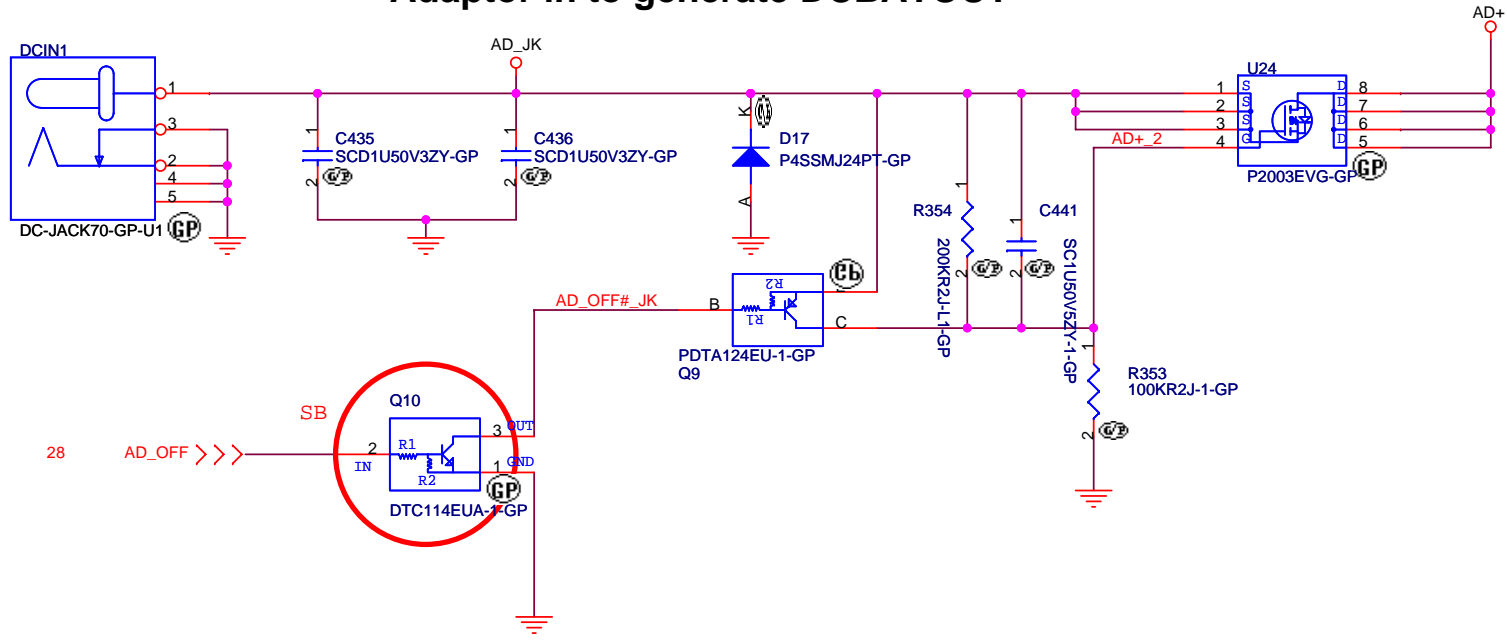
|         |                 |           |
|---------|-----------------|-----------|
| Size A3 | Document Number | Rev       |
|         | <b>D45/D46</b>  | <b>PD</b> |

Date: Friday, March 14, 2008 Sheet 37 of 47

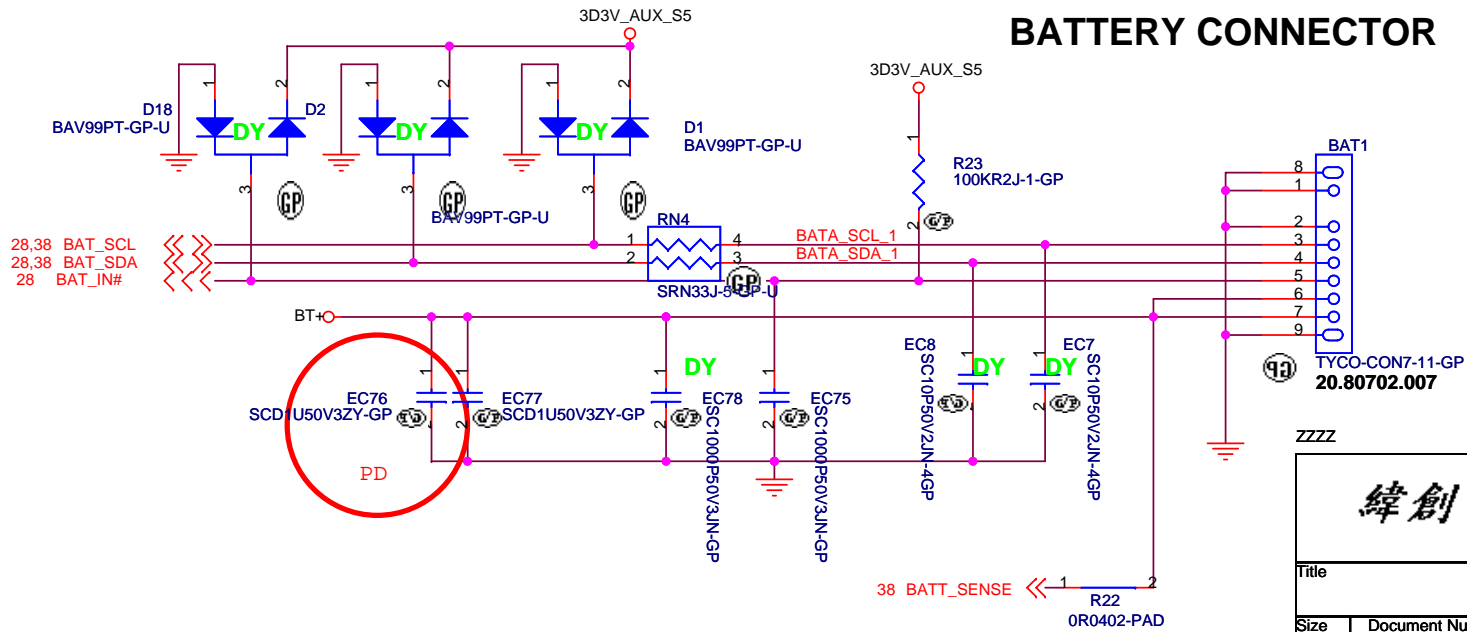


|  |                 |                |
|--|-----------------|----------------|
| Eiger  |                 |                |
| <b>緯創資通 Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                 |                |
| Title  |                 |                |
| <b>BQ24745 Charger</b>   |                 |                |
| Size   | Document Number | Rev            |
| A3   |                 | PD             |
| Date: Friday, March 14, 2008   |                 | Sheet 38 of 47 |

# Adaptor in to generate DCBATOUT



# BATTERY CONNECTOR



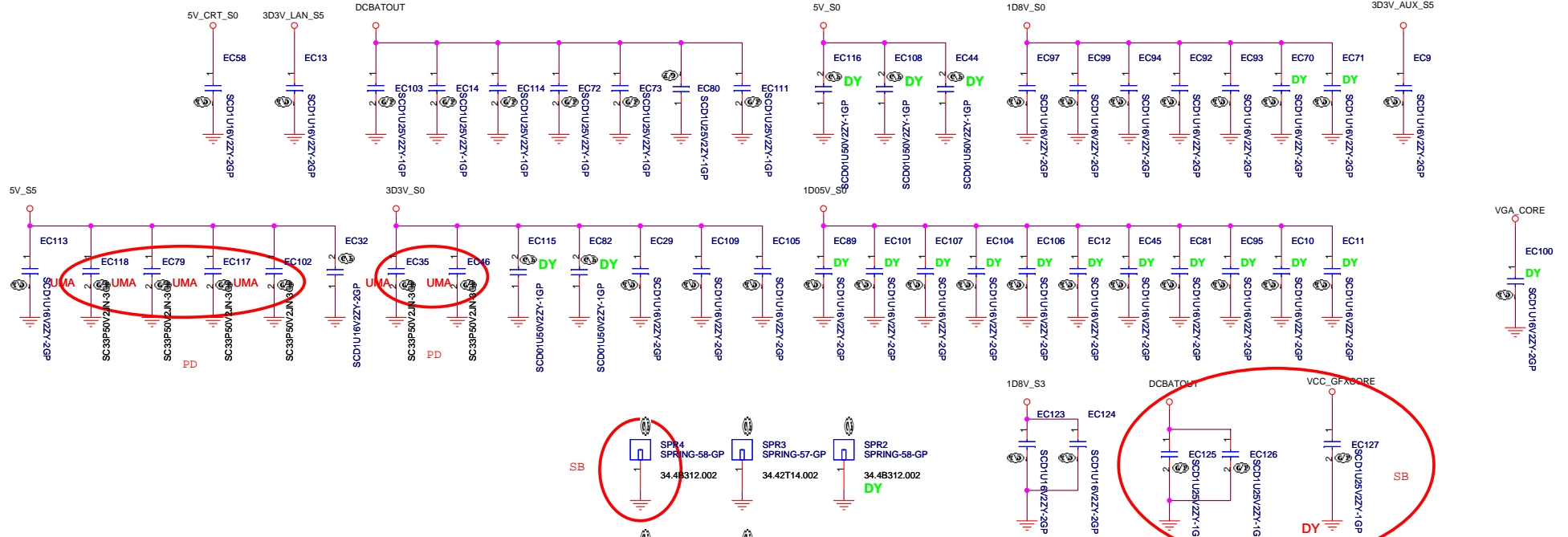
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|       |                 |                     |  |
|-------|-----------------|---------------------|--|
| Title |                 | <b>AD/BATT CONN</b> |  |
| Size  | Document Number | Rev                 |  |
|       | <b>D45/D46</b>  | <b>PD</b>           |  |

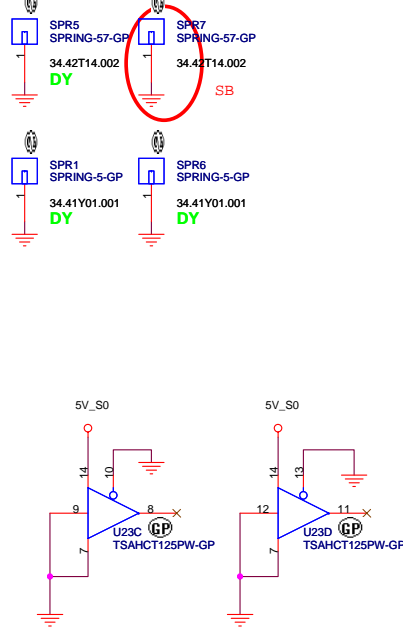
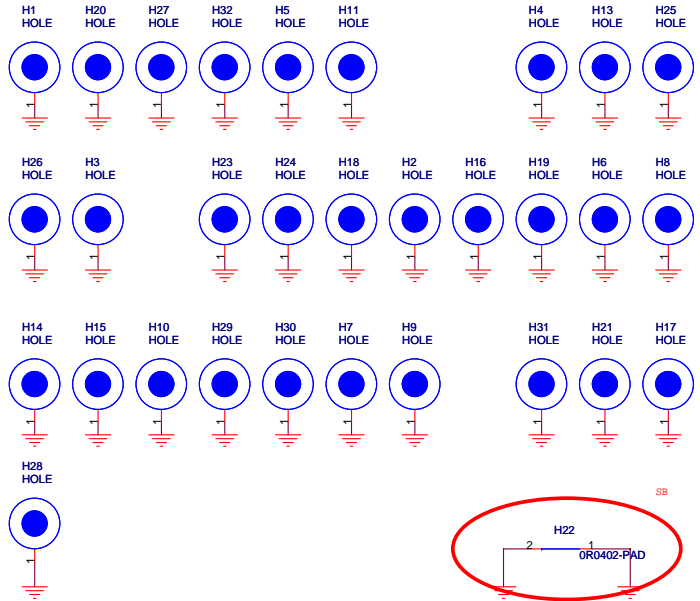
Date: Monday, March 24, 2008 Sheet 39 of 47



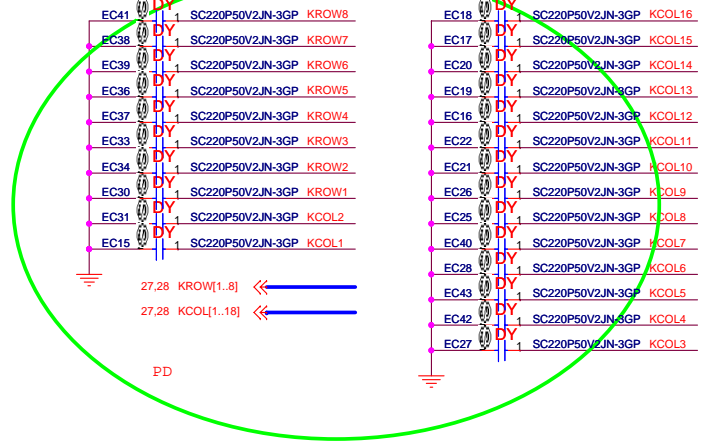
# EMI Caps



# Holes



# Keyboard EMI Caps



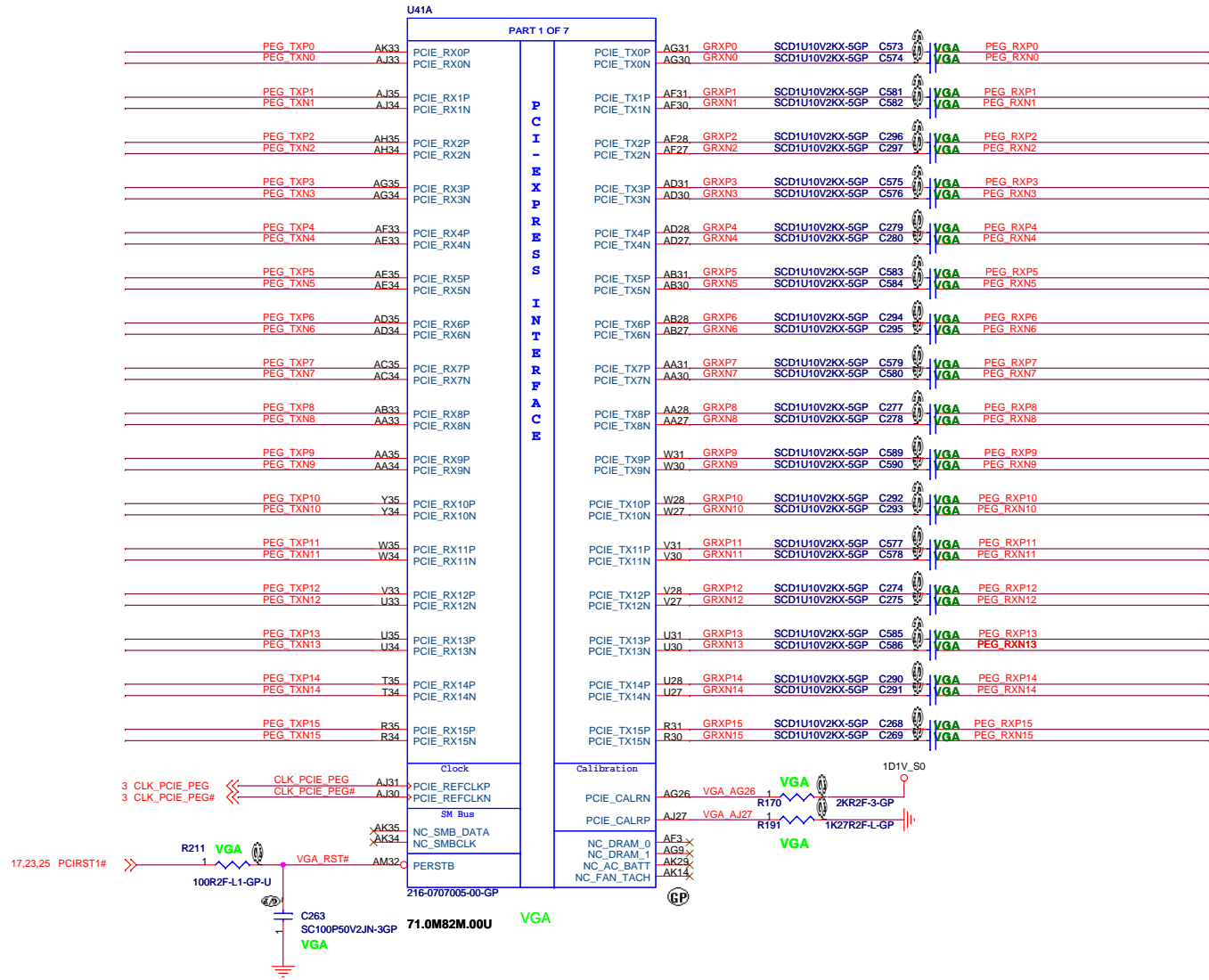
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Title: **EMI/Spring/Boss**

Size: Document Number **D45/D46** Rev **PD**

Date: Monday, March 17, 2008 Sheet 40 of 47

7 PEG\_RXP[15..0] << PEG\_RXP[15..0]  
 7 PEG\_RXN[15..0] << PEG\_RXN[15..0]  
 7 PEG\_TXP[15..0] << PEG\_TXP[15..0]  
 7 PEG\_TXN[15..0] << PEG\_TXN[15..0]



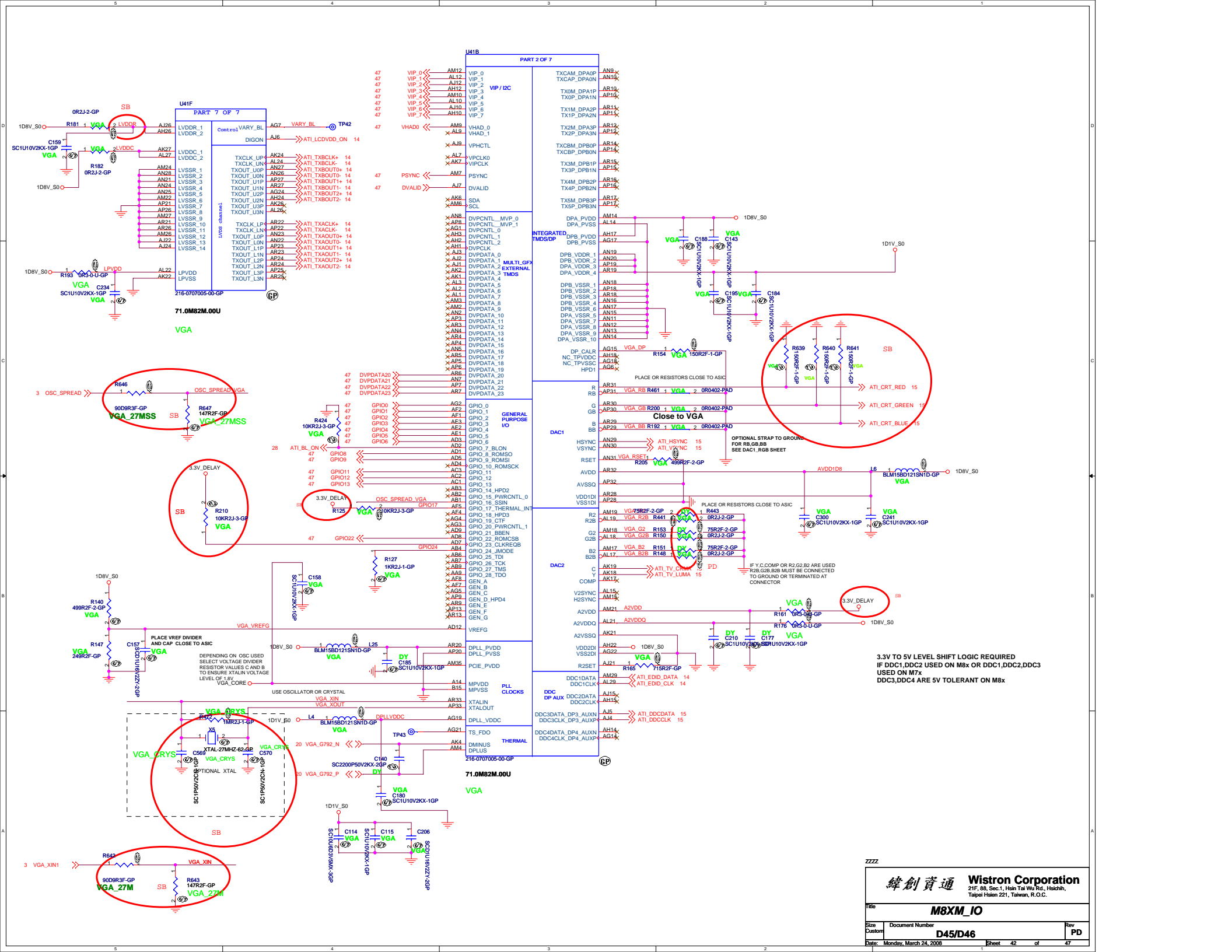
ZZZZ

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Title: **M8XM PCIE**

Size: Document Number **D45/D46** Rev: PD

Date: Friday, March 14, 2008 Sheet 41 of 47



**U41B PART 2 OF 7**

|    |               |      |               |             |      |
|----|---------------|------|---------------|-------------|------|
| 47 | VIP_0         | AM12 | VIP_0         | TXCAM_DPA0P | AN9  |
| 47 | VIP_1         | AL12 | VIP_1         | TXCAP_DPA0N | AN10 |
| 47 | VIP_2         | AM11 | VIP_2         | TXM0_DPA1P  | AR10 |
| 47 | VIP_3         | AH12 | VIP_3         | TXOP_DPA1N  | AP10 |
| 47 | VIP_4         | AM10 | VIP_4         |             |      |
| 47 | VIP_5         | AL10 | VIP_5         |             |      |
| 47 | VIP_6         | AJ10 | VIP_6         | TX1M_DPA2P  | AR11 |
| 47 | VIP_7         | AH10 | VIP_7         | TX1P_DPA2N  | AP11 |
| 47 | VHAD_0        | AM9  | VHAD_0        | TX2M_DPA3P  | AR12 |
| 47 | VHAD_1        | AL9  | VHAD_1        | TX2P_DPA3N  | AP12 |
| 47 | VPHCTL        | AJ9  | VPHCTL        | TXCBM_DP80P | AR14 |
| 47 | VPHCLK0       | AJ7  | VPHCLK0       | TXCBP_DP80N | AP14 |
| 47 | VPHCLK        | AL7  | VPHCLK        | TX3M_DP81P  | AR15 |
| 47 | PSYNC         | AM7  | PSYNC         | TX3P_DP81N  | AP15 |
| 47 | DVALID        | AJ7  | DVALID        | TX4M_DP82P  | AR16 |
| 47 |               | AM6  | DVALID        | TX4P_DP82N  | AP16 |
| 47 |               | AL6  | DVALID        | TX5M_DP83P  | AR17 |
| 47 |               | AJ6  | DVALID        | TX5P_DP83N  | AP17 |
| 47 | DVPCTRL_MVP_0 | AM8  | DVPCTRL_MVP_0 | DPA_VDD     | AM14 |
| 47 | DVPCTRL_MVP_1 | AL8  | DVPCTRL_MVP_1 | DPB_VDD     | AP18 |
| 47 | DVPCTRL_0     | AG1  | DVPCTRL_0     | DPB_VSSR_2  | AM17 |
| 47 | DVPCTRL_1     | AL1  | DVPCTRL_1     | DPB_VSSR_3  | AP17 |
| 47 | DVPCTRL_2     | AG2  | DVPCTRL_2     | DPB_VSSR_4  | AM19 |
| 47 | DVPCLK        | AH1  | DVPCLK        | DPB_VSSR_6  | AM17 |
| 47 | DVPDATA_0     | AJ2  | DVPDATA_0     | DPB_VSSR_8  | AM15 |
| 47 | DVPDATA_1     | AL2  | DVPDATA_1     | DPB_VSSR_10 | AM13 |
| 47 | DVPDATA_2     | AG3  | DVPDATA_2     | DPA_VSSR_7  | AN11 |
| 47 | DVPDATA_3     | AM2  | DVPDATA_3     | DPA_VSSR_8  | AN12 |
| 47 | DVPDATA_4     | AL2  | DVPDATA_4     | DPA_VSSR_9  | AN13 |
| 47 | DVPDATA_5     | AG3  | DVPDATA_5     | DPA_VSSR_10 | AN14 |
| 47 | DVPDATA_6     | AM3  | DVPDATA_6     |             |      |
| 47 | DVPDATA_7     | AL1  | DVPDATA_7     |             |      |
| 47 | DVPDATA_8     | AG2  | DVPDATA_8     |             |      |
| 47 | DVPDATA_9     | AM2  | DVPDATA_9     |             |      |
| 47 | DVPDATA_10    | AL2  | DVPDATA_10    |             |      |
| 47 | DVPDATA_11    | AG3  | DVPDATA_11    |             |      |
| 47 | DVPDATA_12    | AM3  | DVPDATA_12    |             |      |
| 47 | DVPDATA_13    | AL3  | DVPDATA_13    |             |      |
| 47 | DVPDATA_14    | AG4  | DVPDATA_14    |             |      |
| 47 | DVPDATA_15    | AM4  | DVPDATA_15    |             |      |
| 47 | DVPDATA_16    | AL3  | DVPDATA_16    |             |      |
| 47 | DVPDATA_17    | AG5  | DVPDATA_17    |             |      |
| 47 | DVPDATA_18    | AM5  | DVPDATA_18    |             |      |
| 47 | DVPDATA_19    | AL3  | DVPDATA_19    |             |      |
| 47 | DVPDATA_20    | AG6  | DVPDATA_20    |             |      |
| 47 | DVPDATA_21    | AM7  | DVPDATA_21    |             |      |
| 47 | DVPDATA_22    | AL4  | DVPDATA_22    |             |      |
| 47 | DVPDATA_23    | AG7  | DVPDATA_23    |             |      |

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED  
 IF DDC1, DDC2 USED ON M8x OR DDC1, DDC2, DDC3  
 USED ON M7x  
 DDC3, DDC4 ARE 5V TOLERANT ON M8x

ZZZZ

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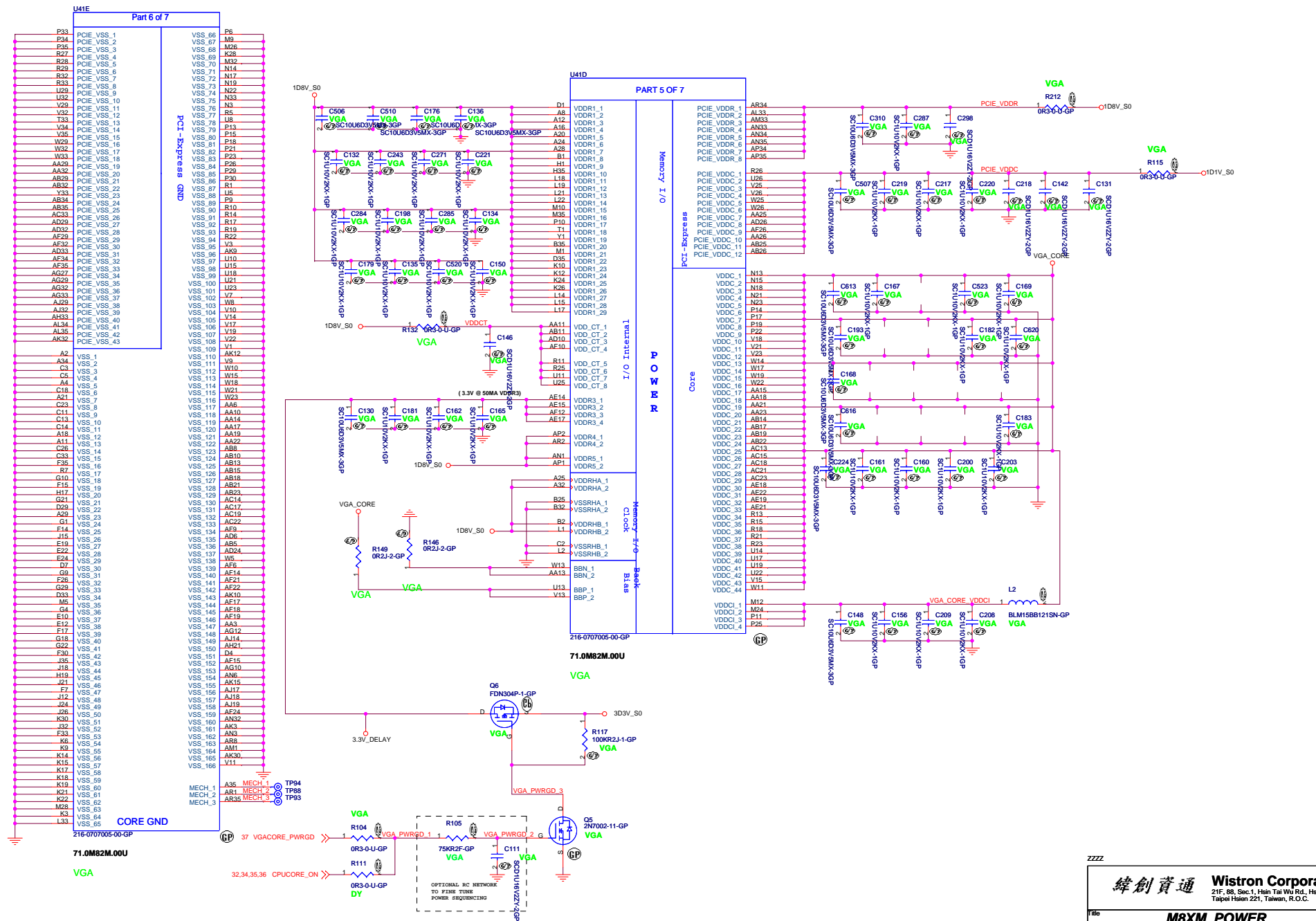
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Title **M8XM\_IO**

Size     Document Number

Custom     **D45/D46**     Rev. **PD**

Date: Monday, March 24, 2009     Sheet 42 of 47



71.0M82M.00U

32,34,35,36 CPUCORE\_ON

OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING

Wistron Corporation

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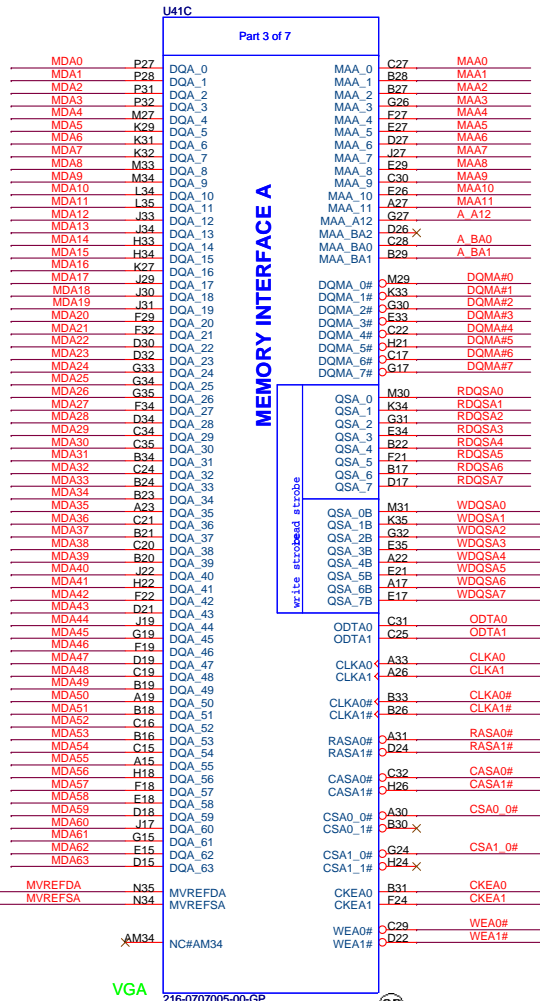
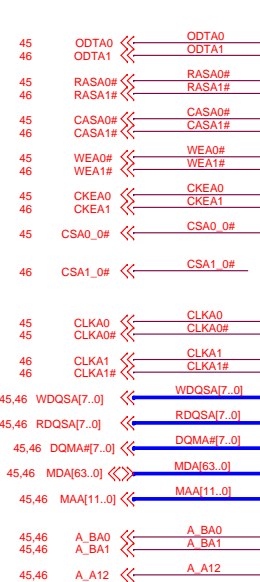
M8XM\_POWER

Document Number: D45/D46

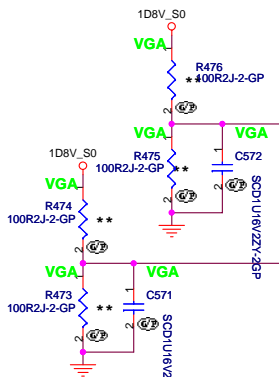
Rev: PD

Date: Friday, March 14, 2008

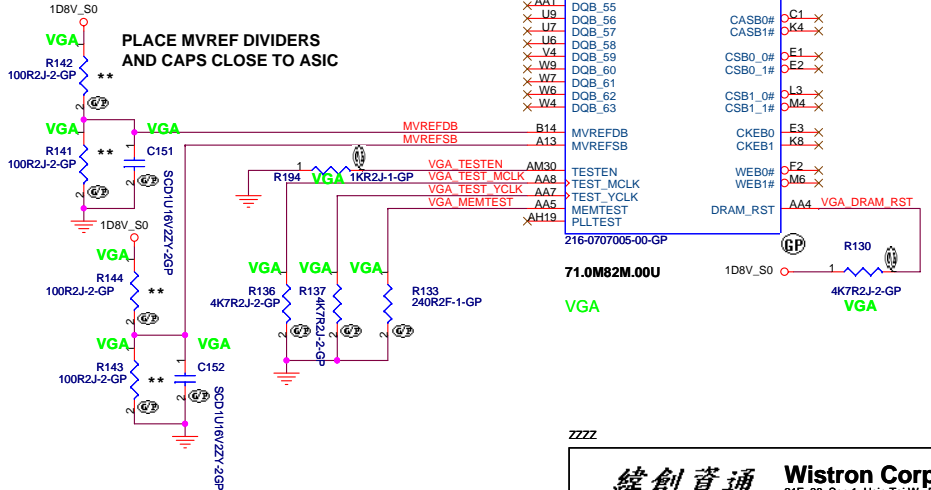
Sheet 43 of 47



**PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC**

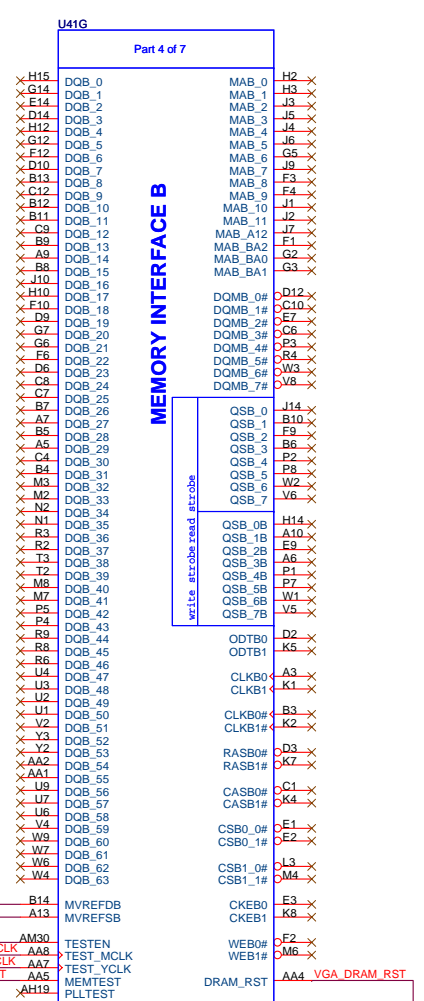


NOTE: FOR DUAL RANK CONNECTIONS USE THE CSxxB\_1 CHIP SELECT PINS



71.0M82M.00U

| ** DIVIDER RESISTORS | DDR2 | DDR3  |
|----------------------|------|-------|
| MVREF TO 1.8V        | 100R | 40.2R |
| MVREF TO GND         | 100R | 100R  |

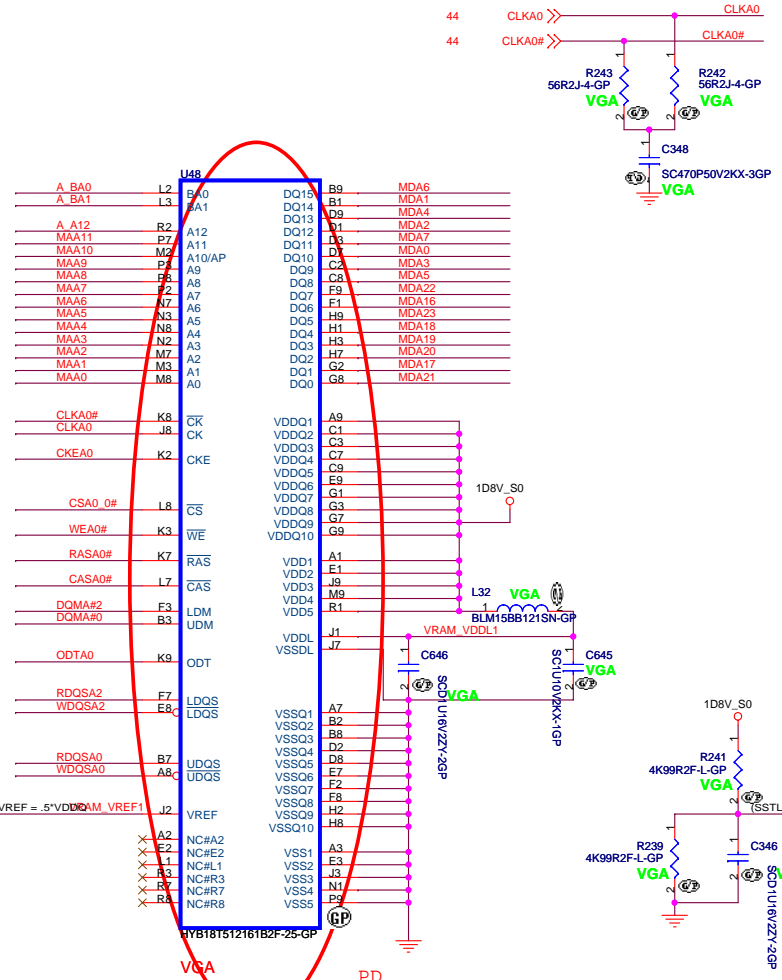


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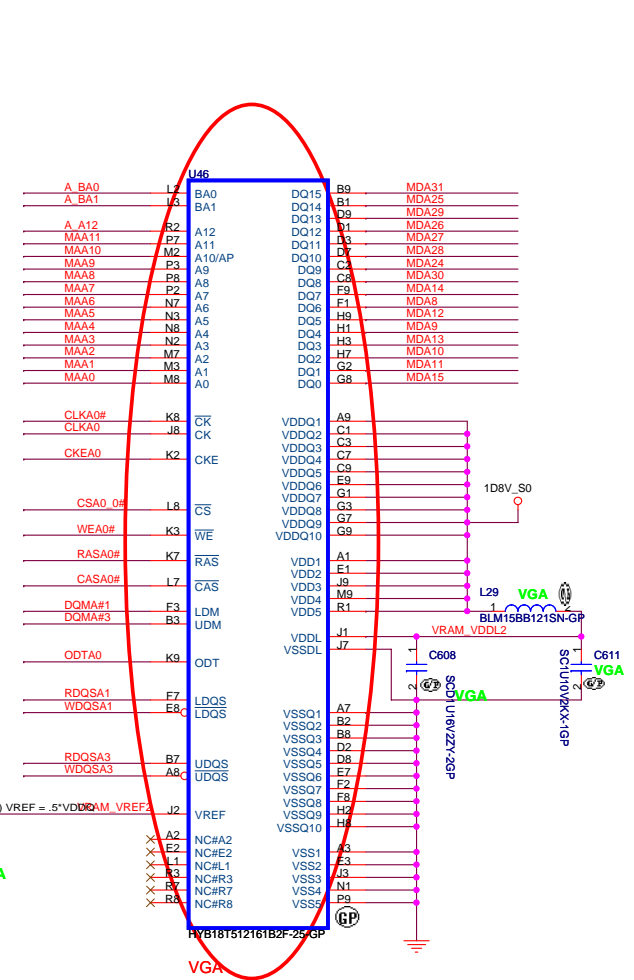
Title: **M8XM\_MEMORY**

Size: A3 Document Number: **D45/D46** Rev: PD

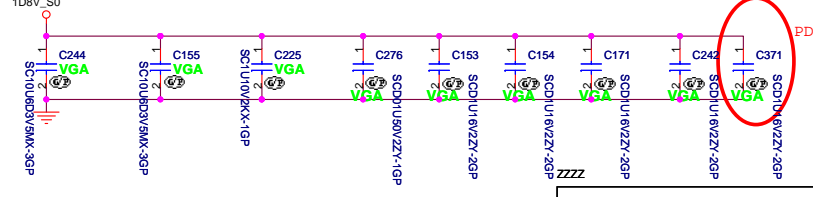
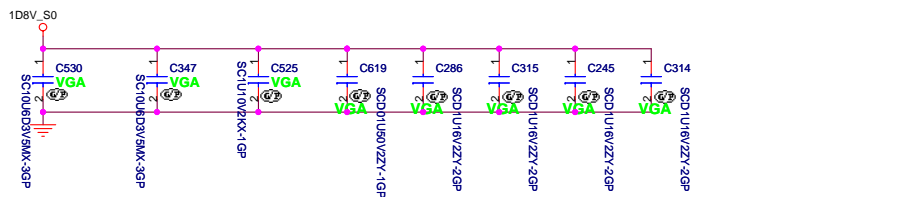
Date: Friday, March 14, 2008 Sheet: 44 of 47



2nd source 72.55162.00U



- 44 RASA0# >> RASA0#
- 44 CASA0# >> CASA0#
- 44 WEA0# >> WEA0#
- 44 CKEA0 >> CKEA0
- 44 CSA0\_0# >> CSA0\_0#
- 44 ODTA0 >> ODTA0
- 44.46 WDQSA[7..0] >> WDQSA[7..0]
- 44.46 RDQSA[7..0] >> RDQSA[7..0]
- 44.46 DQMA[7..0] >> DQMA[7..0]
- 44.46 MDA[63..0] >> MDA[63..0]
- 44.46 MAA[11..0] >> MAA[11..0]
- 44.46 A\_BA1 >> A\_BA1
- 44.46 A\_BA0 >> A\_BA0
- 44.46 A\_A12 >> A\_A12

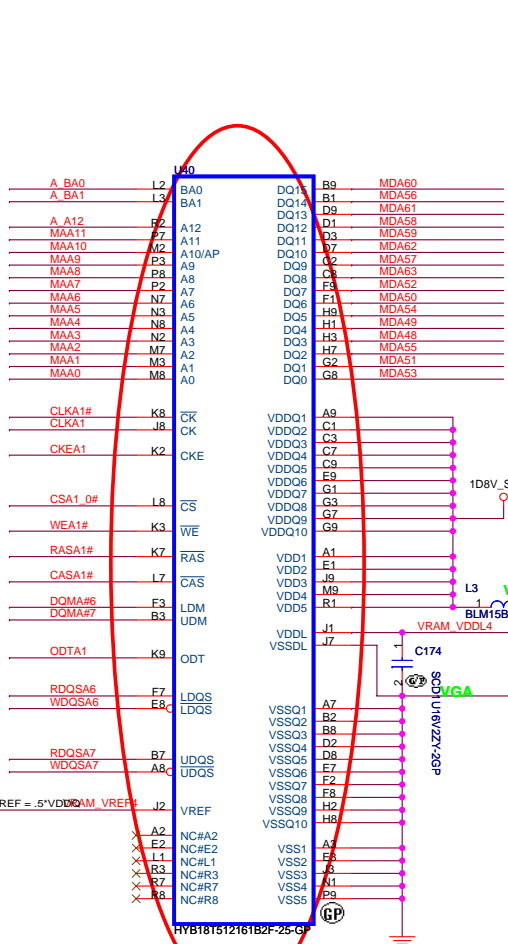
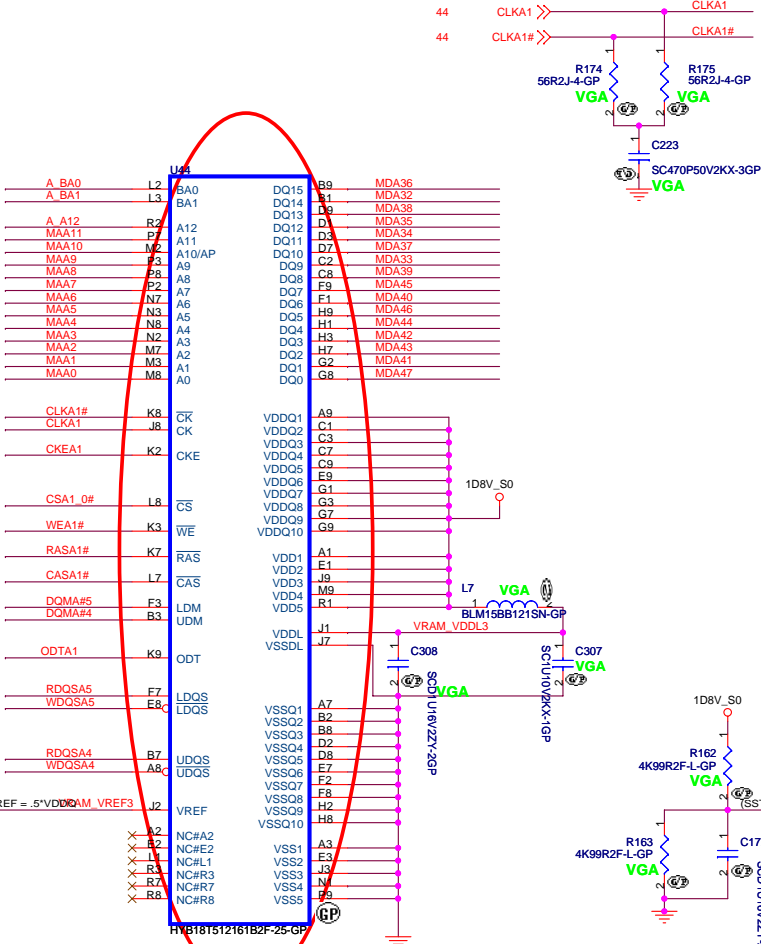


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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM DDR2 A**

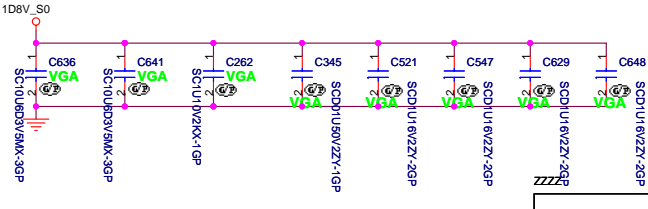
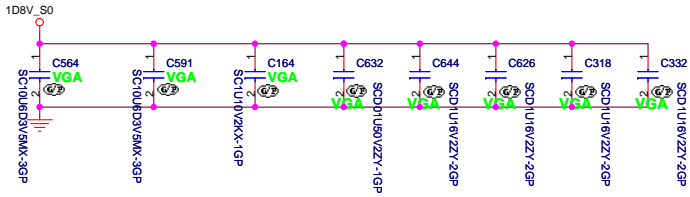
Size: A3 Document Number: **D45/D46** Rev: **PD**

Date: Monday, March 24, 2008 Sheet: 45 of 47



|       |             |   |             |
|-------|-------------|---|-------------|
| 44    | RASA1#      | 》 | RASA1#      |
| 44    | CASA1#      | 》 | CASA1#      |
| 44    | WEA1#       | 》 | WEA1#       |
| 44    | CKEA1       | 》 | CKEA1       |
| 44    | CSA1_0#     | 》 | CSA1_0#     |
| 44    | ODTA1       | 》 | ODTA1       |
| 44,45 | WDQSA[7..0] | 》 | WDQSA[7..0] |
| 44,45 | RDQSA[7..0] | 》 | RDQSA[7..0] |
| 44,45 | DQMA[7..0]  | 》 | DQMA[7..0]  |
| 44,45 | MDA[63..0]  | 》 | MDA[63..0]  |
| 44,45 | MAA[11..0]  | 》 | MAA[11..0]  |
| 44,45 | A_BA1       | 》 | A_BA1       |
| 44,45 | A_BA0       | 》 | A_BA0       |
| 44,45 | A_A12       | 》 | A_A12       |

2nd source 72.55162.000

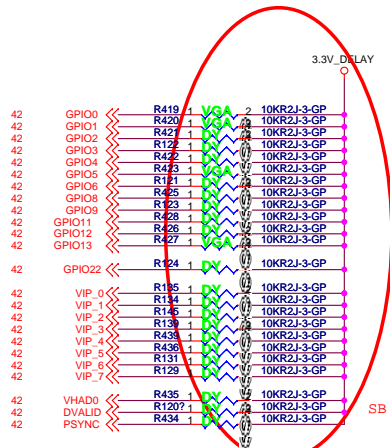


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|                              |                                   |                  |
|------------------------------|-----------------------------------|------------------|
| Title<br><b>VRAM DDR2 B</b>  |                                   |                  |
| Size<br>A3                   | Document Number<br><b>D45/D46</b> | Rev<br><b>PD</b> |
| Date: Monday, March 24, 2008 | Sheet 46 of 47                    |                  |



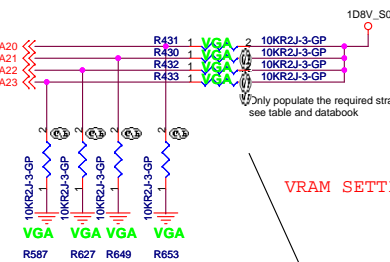
Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M  
 Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X



| CONFIGURATION STRAPS  |   |   |         | RECOMMENDED SETTINGS  |  |
|---|---|---|---------|---|--|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET |   |   |         | G= DO NOT INSTALL RESISTOR<br>1= INSTALL 10K RESISTOR<br>X = DESIGN DEPENDANT<br>NA = NOT APPLICABLE<br>RSVD = ATI RESERVED<br>(DO NOT INSTALL) |  |
| STRAPS  | PIN   | DESCRIPTION OF DEFAULT SETTINGS                 | M8x     | M7x   |  |
| BIF_MSI_DIS   | VIP1  | MESSAGE SIGNAL INTERRUPT ENABLED                | NA      | 0   |  |
| BIF_AUDIO_EN  | VIP3  | ENABLE HD AUDIO (M7Xm and M86M ONLY) Note:1     | X       | X   |  |
| BIF_64BAR_EN_A  | VIP5  | 64 BIT BARS DISABLED                            | NA      | 0   |  |
| TX_PWRS_ENB   | GPIO0   | PCIe FULL TX OUTPUT SWING                       | X       | X   |  |
| TX_DEEMPH_EN  | GPIO1   | PCIe TRANSMITTER DE-EMPHASIS ENABLED            | X       | X   |  |
| BIF_DEBUG_ACCESS  | GPIO4   | DEBUG SIGNALS MUXED OUT                         | 0       | 0   |  |
| BIF_AUDIO_EN  | GPIO8   | ENABLE HD AUDIO (M82M ONLY) Note:2              | X       | RSVD  |  |
| BIF_GEN2_EN_A   | GPIO5   | Allows either PCIe 2.5GT/s or 5.0GT/s operation | X       | 0   |  |
| BIOS_ROM_EN   | GPIO_22_ROMCSB  | DISABLE EXTERNAL BIOS ROM                       | NA      | X   |  |
| ROMIDCFG(3:0)   | GPIO[13:11,9]   | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT  | XX X X  | X X X X   |  |
| VIP_DEVICE_STRAP_ENA  | VSYN  | IGNORE VIP DEVICE STRAPS                        | 0       | 0   |  |
| BIF_VGA_DIS   | PSYN  | VGA ENABLED                                     | 0       | 0   |  |
| BIF_HDMI_EN   | HSYN  | HDMI ENABLE (SEE NOTE 2)                        | X       | X   |  |
| DEBUG_I2C_ENABLE  | GPIO6   | Internal use only                               | 0       | 0   |  |
| MEM_TYPE  | ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20,23 IN THIS DESIGN | MEMORY TYPE,MAKE AND SIZE INFO                  | X X X X | X X X X   |  |

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT



VRAM SETTING

| ATI RESERVED CONFIGURATION STRAPS  |          |              |      |      |      |       |        |
|--|----------|--------------|------|------|------|-------|--------|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET        |          |              |      |      |      |       |        |
| VHAD0  | VIP0     | VIP2         | VIP4 | VIP6 | VIP7 | GPIO2 | GPIO3  |
|  |          |              |      |      |      |       | H2SYNC |
| PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET |          |              |      |      |      |       |        |
| GPIO_28_TDO  | GENERICC | GPIO21_BB_EN |      |      |      |       |        |

For Hynix ↑R431,R430,R432,R433 (63.10334.1DL)  
 Delete R587,R627,R649,R653  
 For Qimonda ↑R431,R430,R432,R587 (63.10334.1DL)  
 Delete R433,R627,R649,R653  
 For Samsung ↑R431,R430,R627,R433 (63.10334.1DL)  
 Delete R587,R432,R649,R653

|           |   |                         |
|-----------|---|-------------------------|
| DVPDATA20 | 1 |                         |
| DVPDATA21 | 1 | HY5PS121621CFP-25 Hynix |
| DVPDATA22 | 1 | 72.51216.F0U            |
| DVPDATA23 | 1 |                         |

|           |   |                            |
|-----------|---|----------------------------|
| DVPDATA20 | 1 |                            |
| DVPDATA21 | 1 | HYB18T512161B2F-25 Qimonda |
| DVPDATA22 | 1 | 72.18512.M0U               |
| DVPDATA23 | 0 |                            |

|           |   |                         |
|-----------|---|-------------------------|
| DVPDATA20 | 1 |                         |
| DVPDATA21 | 1 | K4N51163QE-ZC25 SamSung |
| DVPDATA22 | 0 | 72.45116.A0U            |
| DVPDATA23 | 1 |                         |

|           |   |                 |
|-----------|---|-----------------|
| DVPDATA20 | 1 | H5PS5162FFR-25C |
| DVPDATA21 | 1 | HYNIX           |
| DVPDATA22 | 0 |                 |
| DVPDATA23 | 0 | 72.55162.00U    |

| 手動改D45 BOM       | 手動改共同BOM         | 手動改NET           |
|------------------|------------------|------------------|
| U43 71.CNTIG.H0U | DM2 62.10017.G31 |                  |
| U57 71.ICH9M.E0U | U49 84.04634.037 | DM2 62.10017.G31 |
|                  | U15 84.08896.037 |                  |
|                  | H29 34.4B417.001 | U35 62.10053.401 |
|                  | H30 34.4B417.001 |                  |
|                  | H27 34.4F403.001 |                  |
|                  | H31 34.4F403.001 |                  |
|                  | H7 34.4F403.001  |                  |
|                  | H9 34.4F403.001  |                  |
|                  | H10 34.4G501.001 |                  |
|                  | U11 71.00773.00G |                  |
|                  | U64 71.00380.003 |                  |
|                  | U35 62.10053.401 |                  |
|                  | U7 71.08111.E03  |                  |
| 手動改D46 BOM       |                  |                  |
| U43 71.CNTIG.G0U |                  |                  |
| U57 71.ICH9M.E0U |                  |                  |

D45 VRAM SELECT

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