

# Compal confidential

## Schematics Document

### ClawHammer AMD K8 with nVIDIA Chrush K8

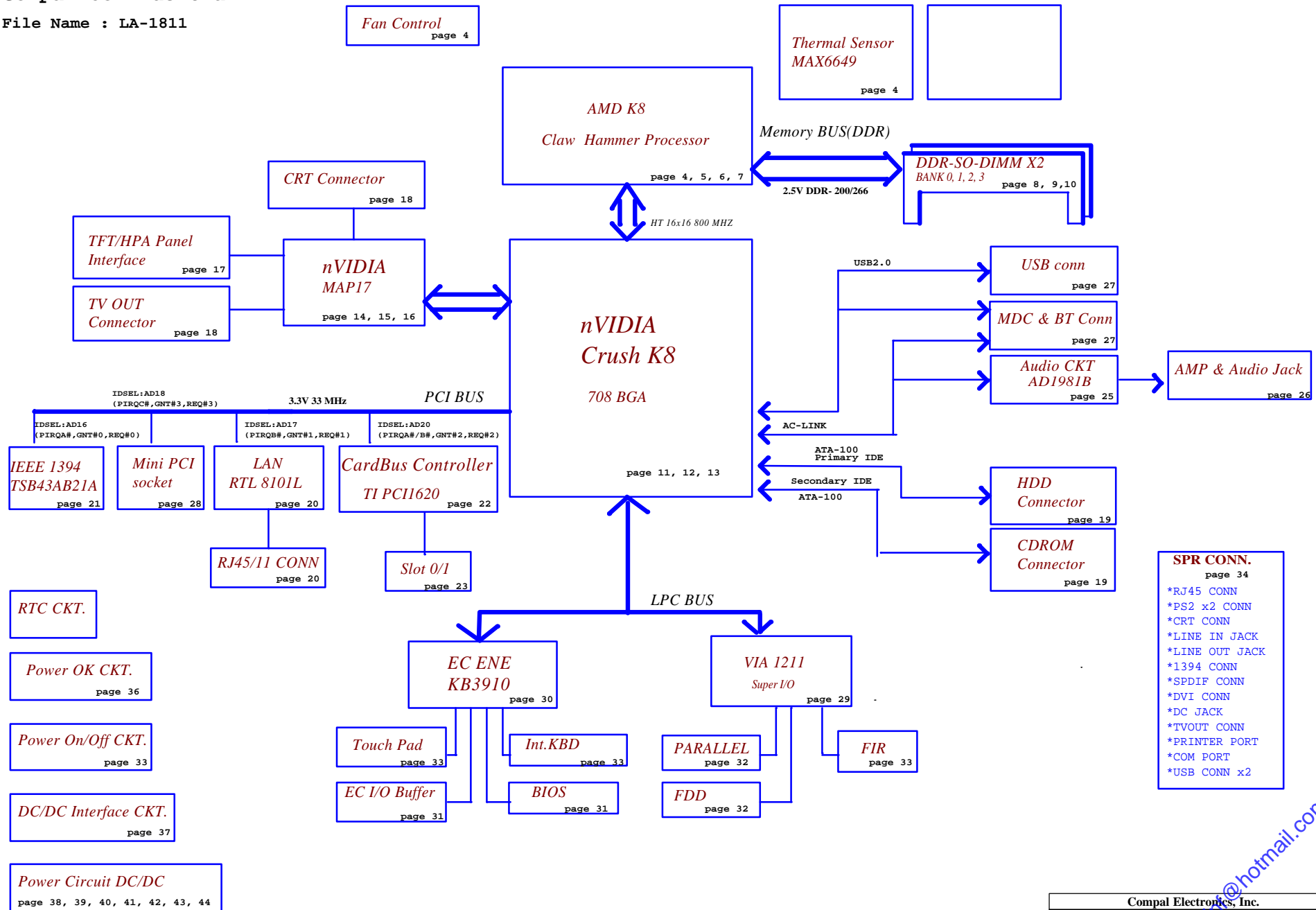
2003-10-15

REV:0.5

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Title		
Cover Sheet		
Doc No	Document Number	Rev
	LA-1851	0.5
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Compal Electronics, Inc.		
Title	Block Diagram	
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## Voltage Rails

power plane \ State	+1.2VALW +3VALW +5VALW 12VALW	+1.25V +2.5V +3V +5V	+1.2V_HT +1.2VS +1.5VS +2.5VS +3VS +5VS
S0	O	O	O
S1	O	O	O
S3	O	O	X
S5 S4/AC	O	X	X
S5 S4/AC don't exist	X	X	X

O MEANS ON  
X MEANS OFF

## PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
<b>INTERNAL</b>				
USB 2.0	2	AD13	N/A	G
AC97 MODEM	6	AD17	N/A	M
AC97	6	AD17	N/A	L
ATA 100	8	AD20	N/A	
ETHERNET	5	AD16	N/A	K
LPC I/F	1	AD12	N/A	
SMBUS	1	AD12	N/A	F
<b>EXTERNAL</b>				
VGA	0	AD16	N/A	E
1394	0	AD16	0	A
LAN	1	AD17	1	B
CARD BUS	4	AD20	2	A, B
Wireless LAN	2	AD18	3	C
Mini-PCI (no use)	3	AD19	4	D

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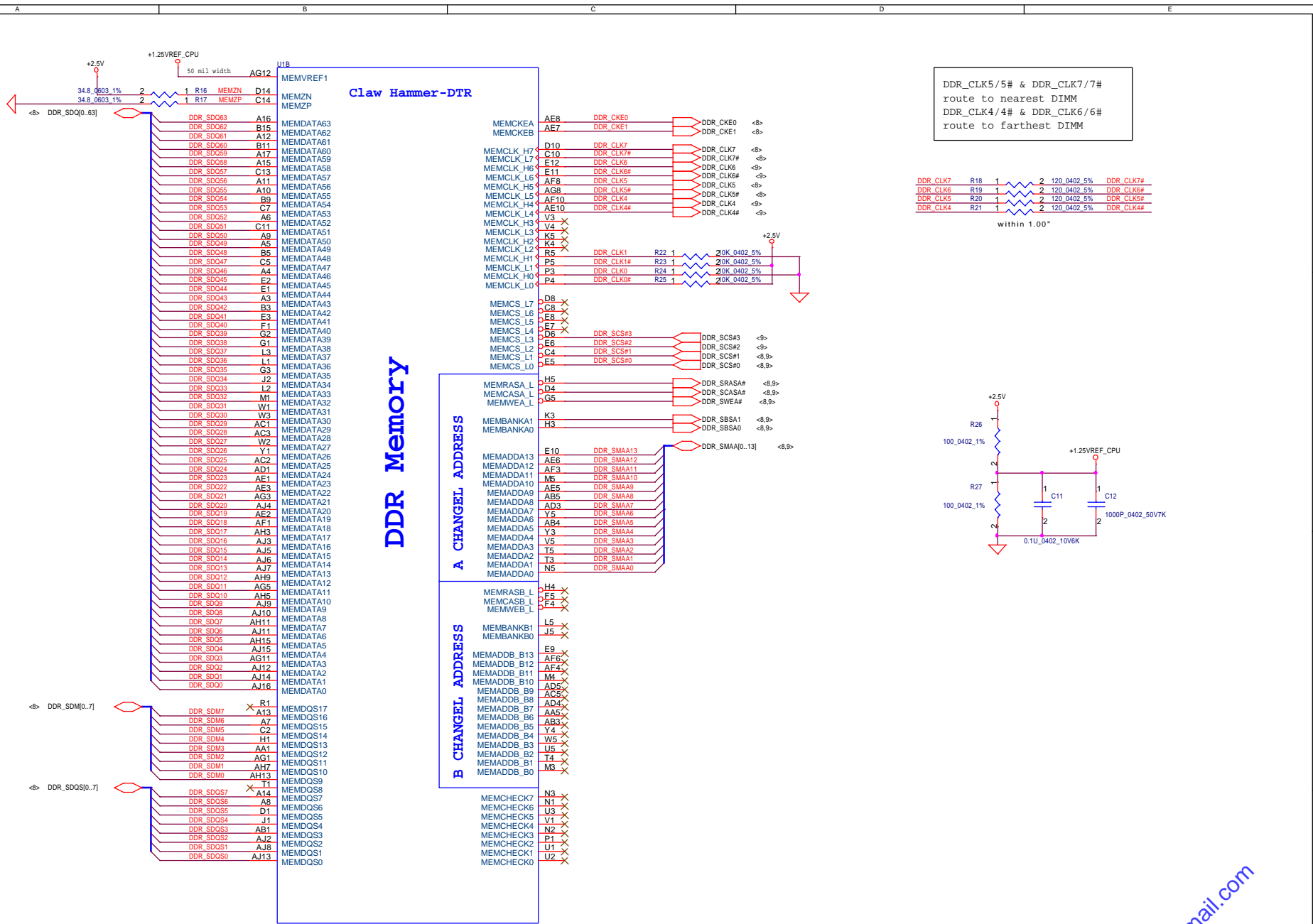
Notes List

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DDR\_CLK5/5# & DDR\_CLK7/7#  
route to nearest DIMM  
DDR\_CLK4/4# & DDR\_CLK6/6#  
route to farthest DIMM

DDR\_CLK7 R18 1 2 120 0402 5% DDR\_CLK7#  
DDR\_CLK6 R19 1 2 120 0402 5% DDR\_CLK6#  
DDR\_CLK5 R20 1 2 120 0402 5% DDR\_CLK5#  
DDR\_CLK4 R21 1 2 120 0402 5% DDR\_CLK4#  
within 1.00"

Claw Hammer-DTR

DDR Memory

A CHANGE ADDRESS

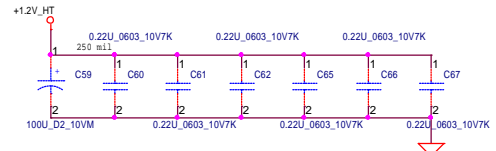
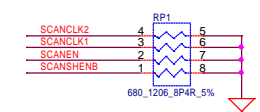
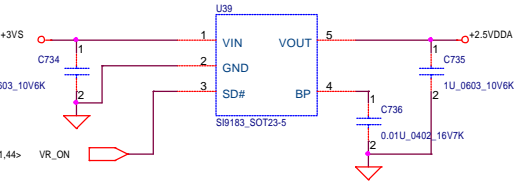
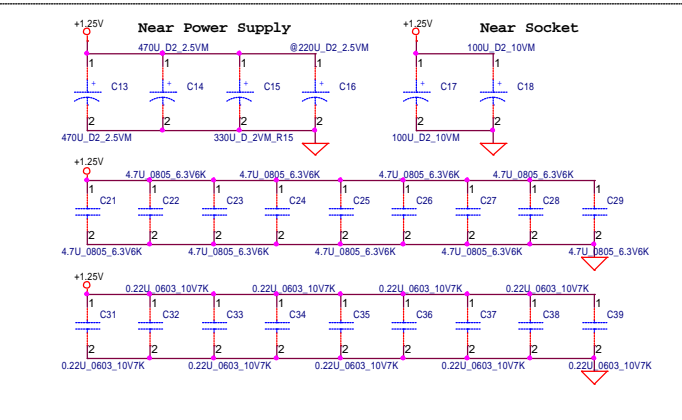
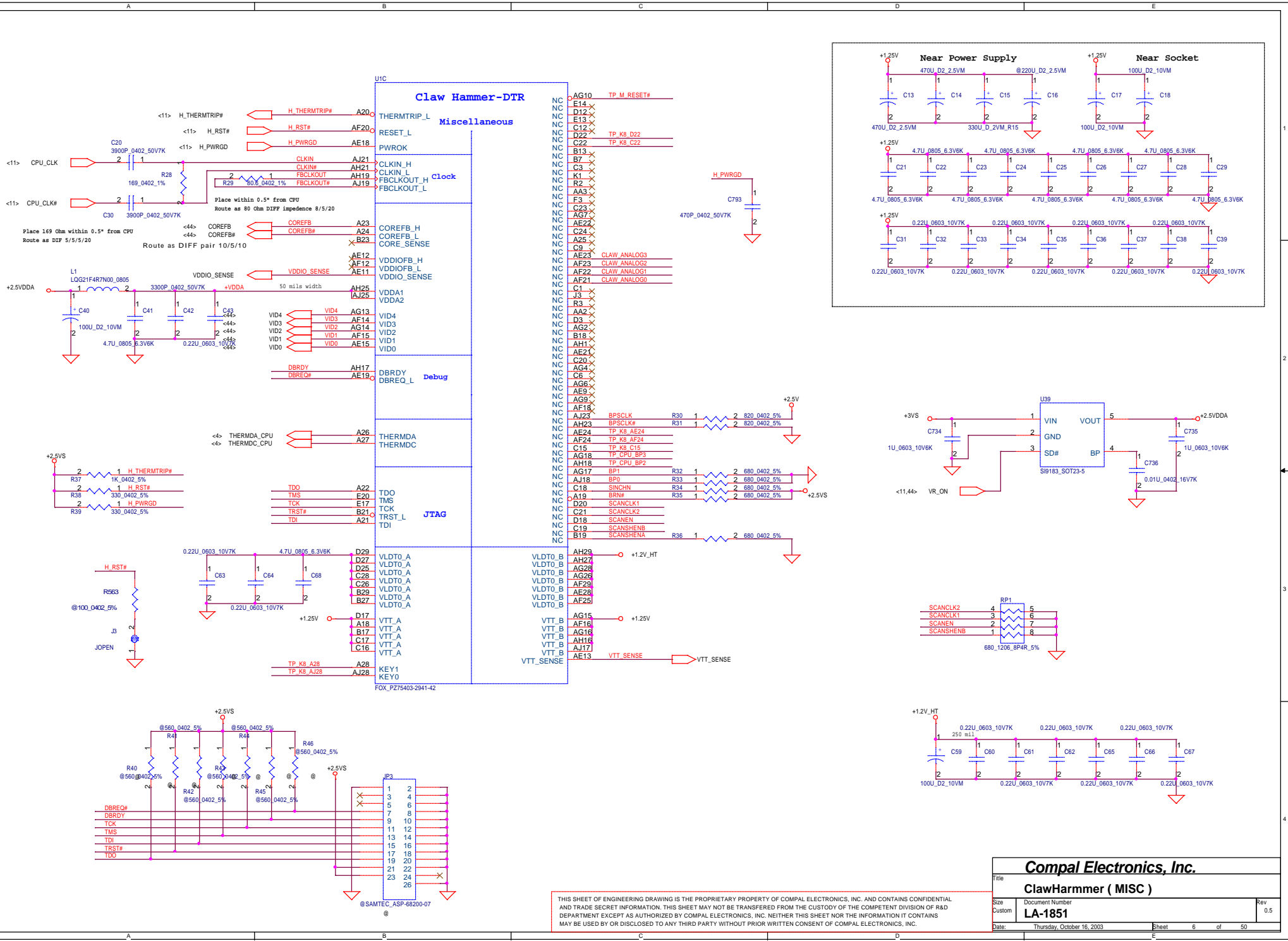
B CHANGE ADDRESS

FOX\_P275403-2941-42

<b>Compal Electronics, Inc.</b>		
<b>Claw Hammer (MEMORY BUS)</b>		
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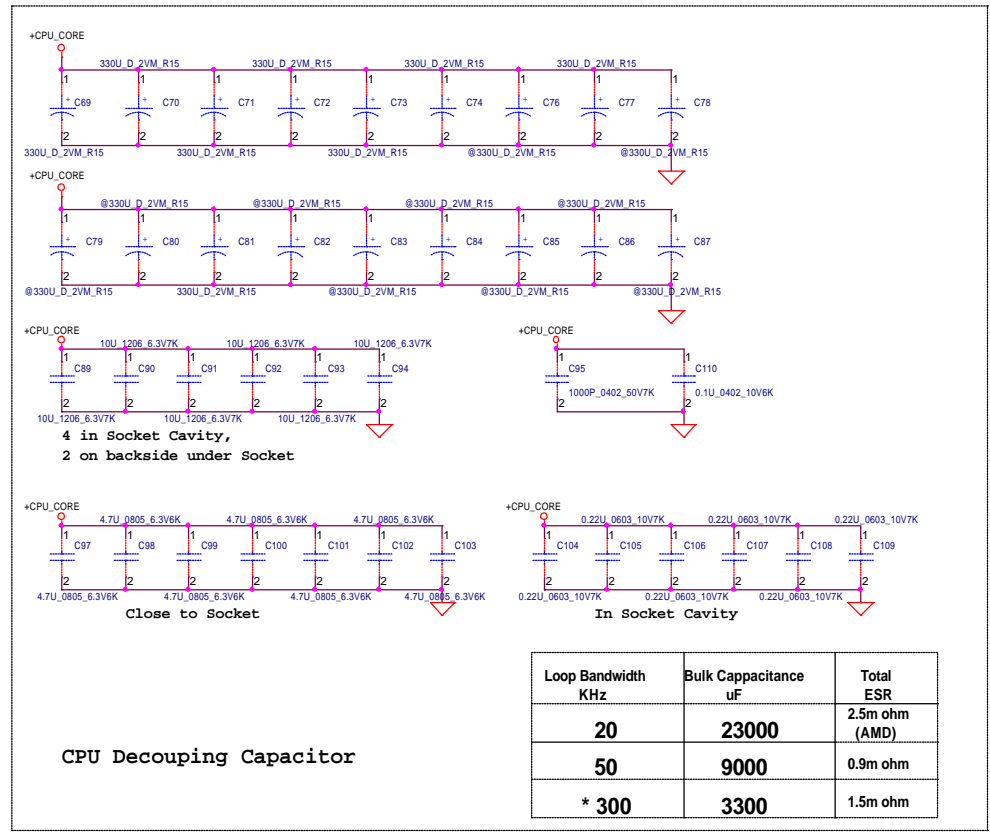
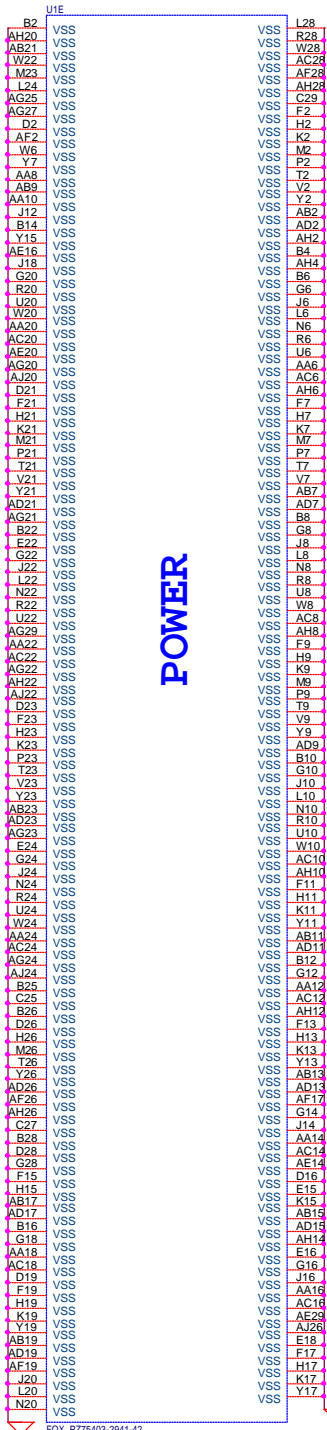
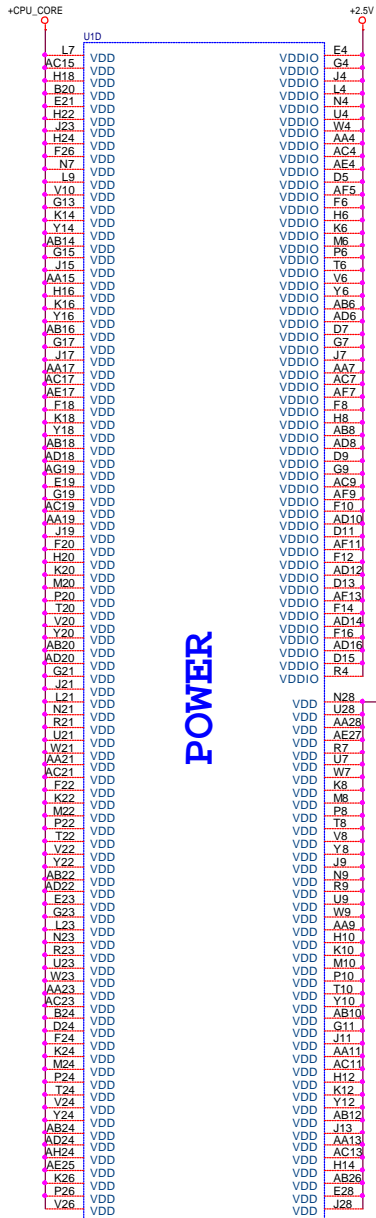
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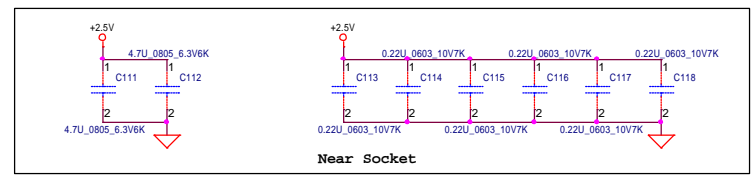
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<b>ClawHammer ( MISC )</b>		
File	Document Number	Rev
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Custom		
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CPU Decoupling Capacitor

Loop Bandwidth KHz	Bulk Cappacitance uF	Total ESR
20	23000	2.5m ohm (AMD)
50	9000	0.9m ohm
* 300	3300	1.5m ohm



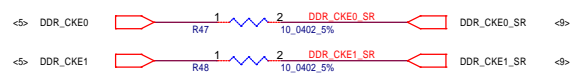
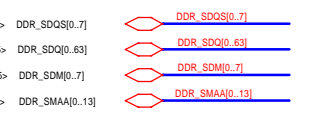
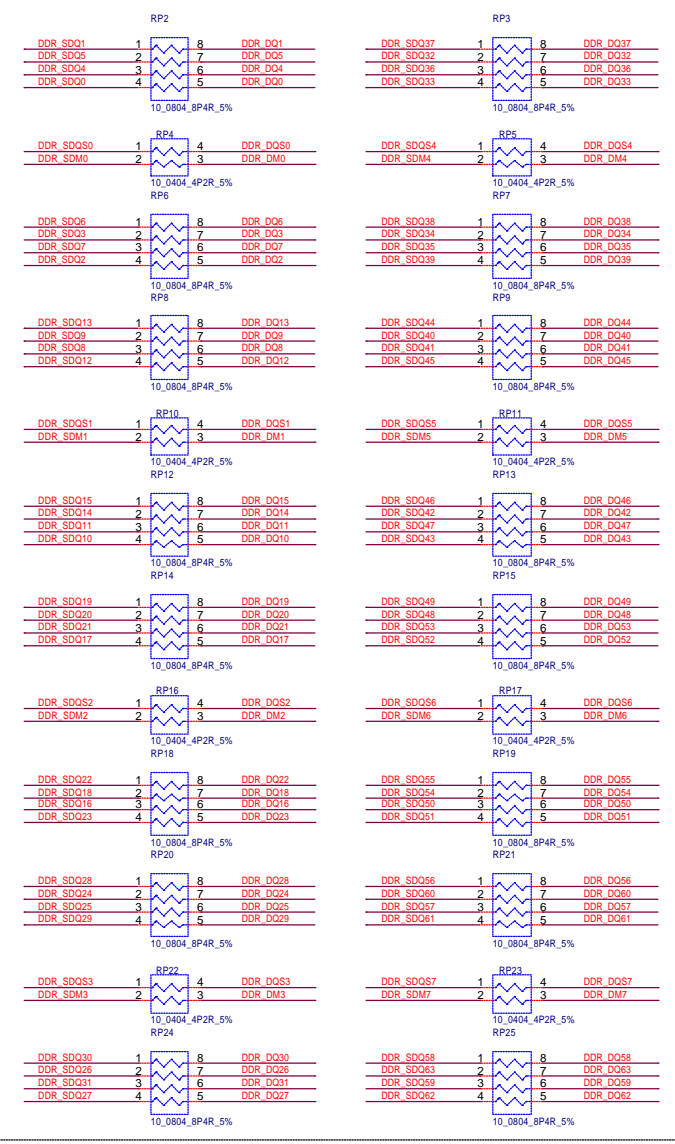
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**Compal Electronics, Inc.**  
**Claw Hammer (Power & Ground)**

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Note:  
 DDR\_SMAA13 Recommend for AMD

Layout note  
 Place these resistors  
 close to DIMM0,  
 all trace length < 500 mil

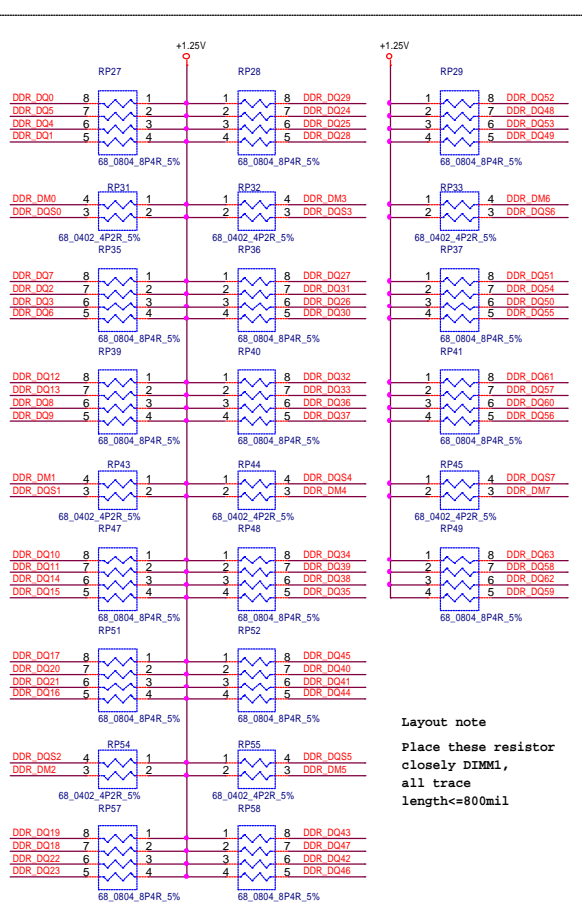


<b>Compal Electronics, Inc.</b>		
<b>DDR-SODIMM SLOT0</b>		
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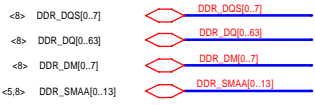
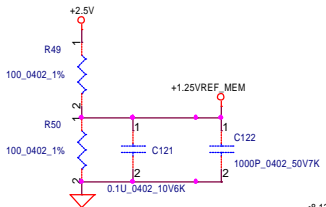
SO-DIMM0  
 REVERSE



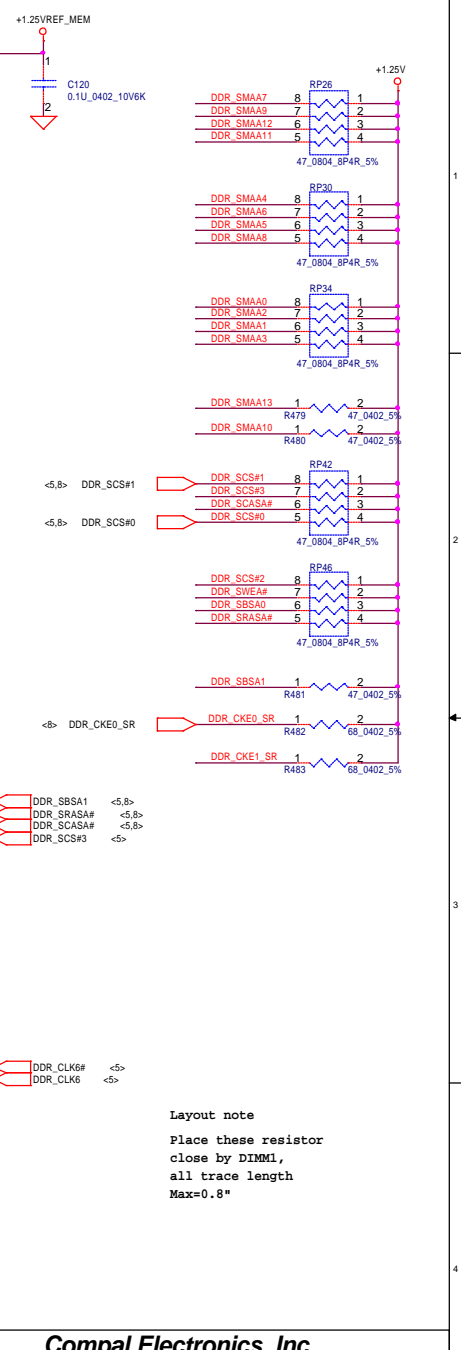
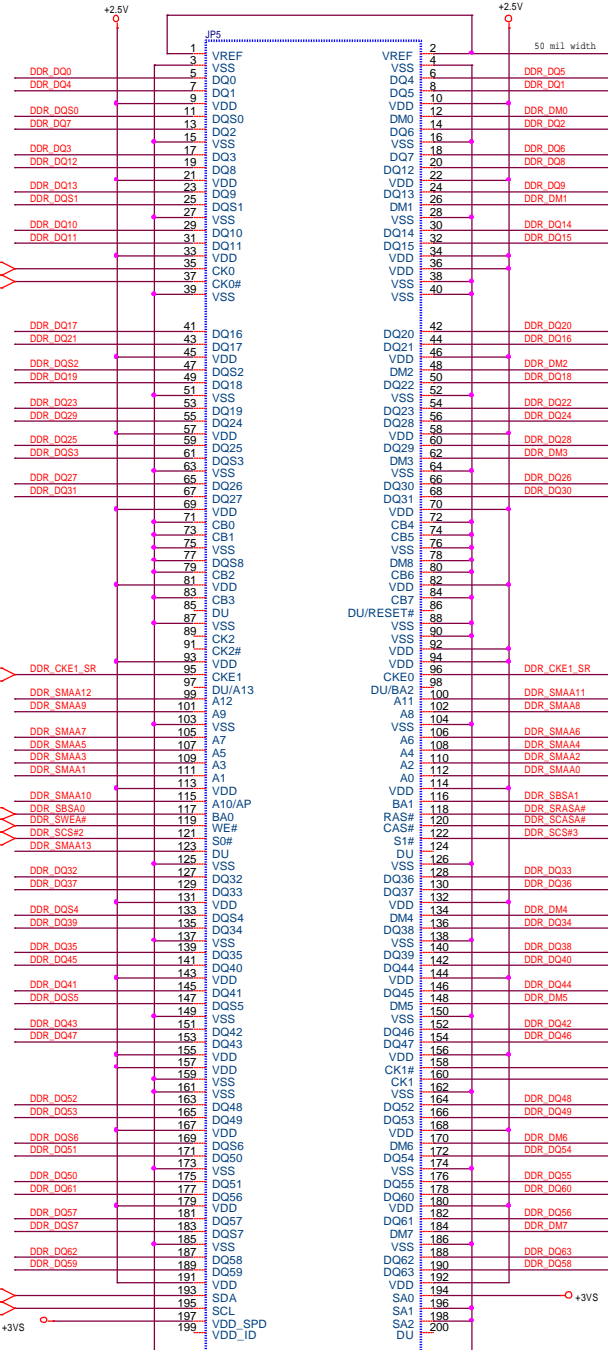


**Layout note**  
Place these resistor close by DIMM1, all trace length<=800mil

**Note:**  
DDR\_SMAA13 Recommend for AMD.



<8.12> DIMM\_SMDATA  
<8.12> DIMM\_SMCLK

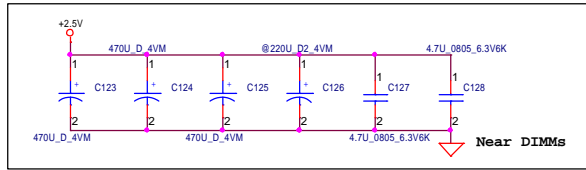


**Layout note**  
Place these resistor close by DIMM1, all trace length Max=0.8"

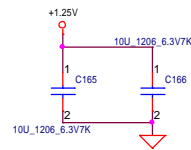
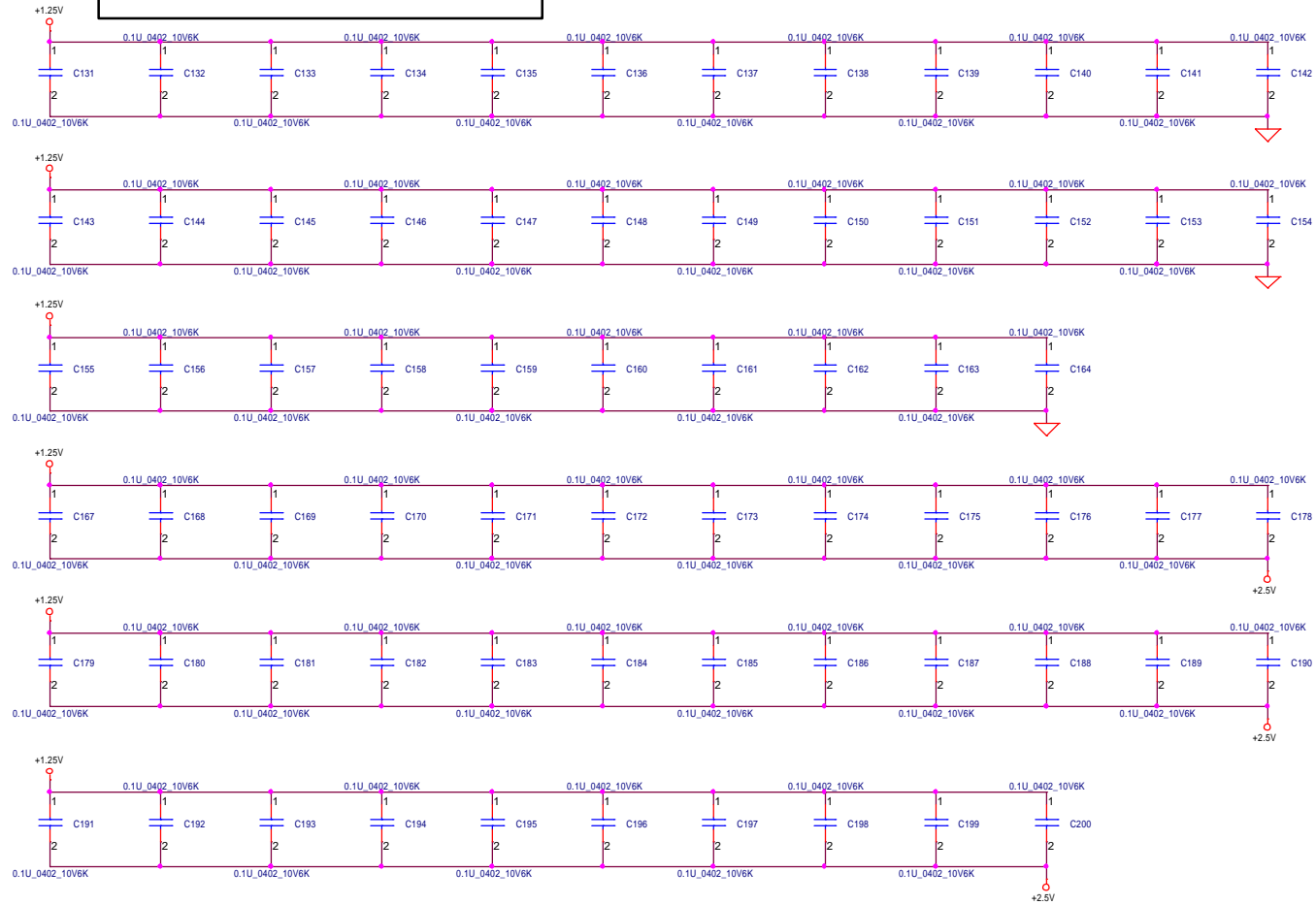
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Title	<b>DDR-SODIMM SLOT1</b>	
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AMP 1565917-1  
**DIMM1 STANDARD**



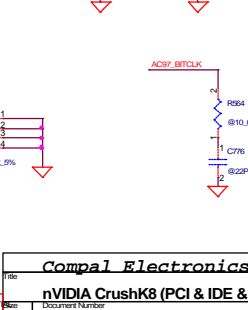
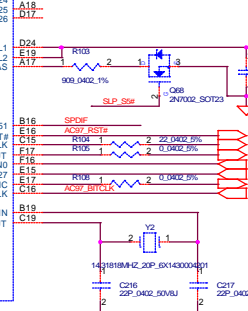
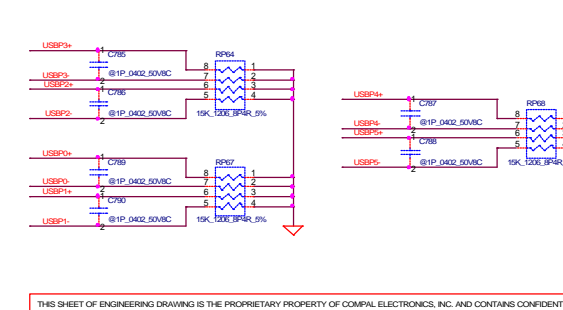
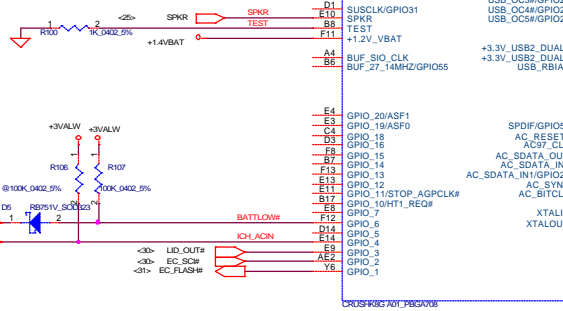
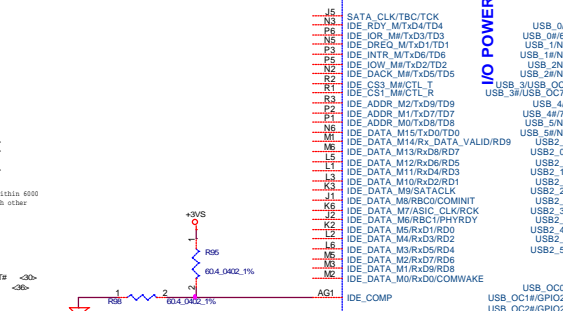
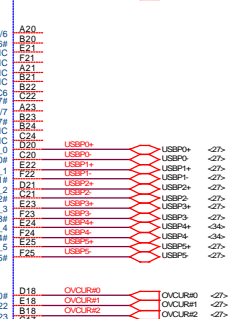
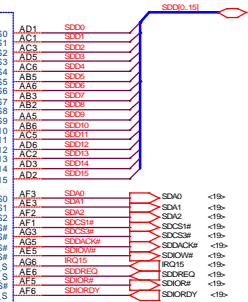
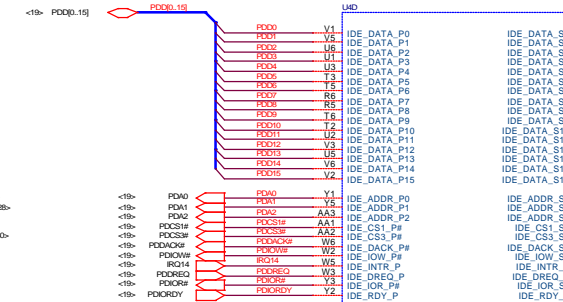
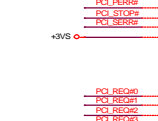
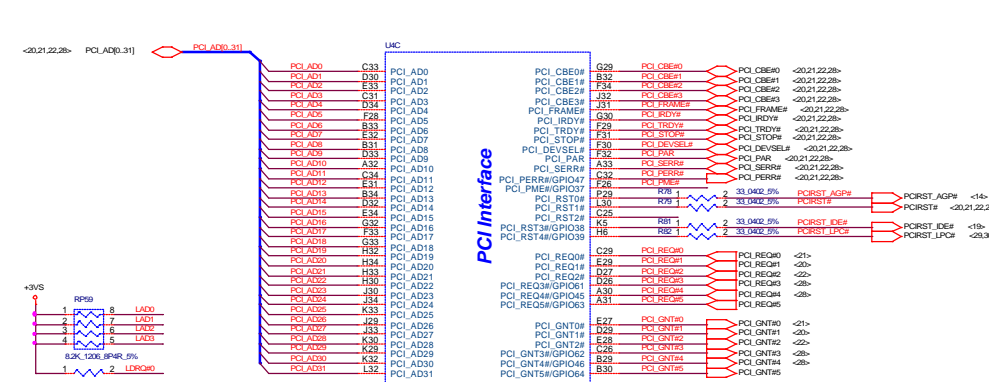
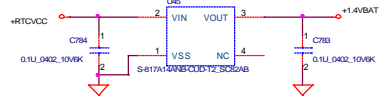
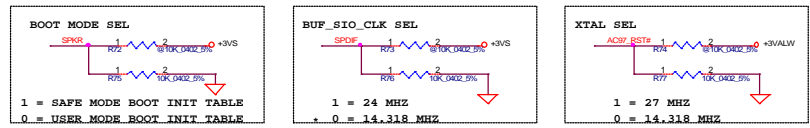
**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25VS



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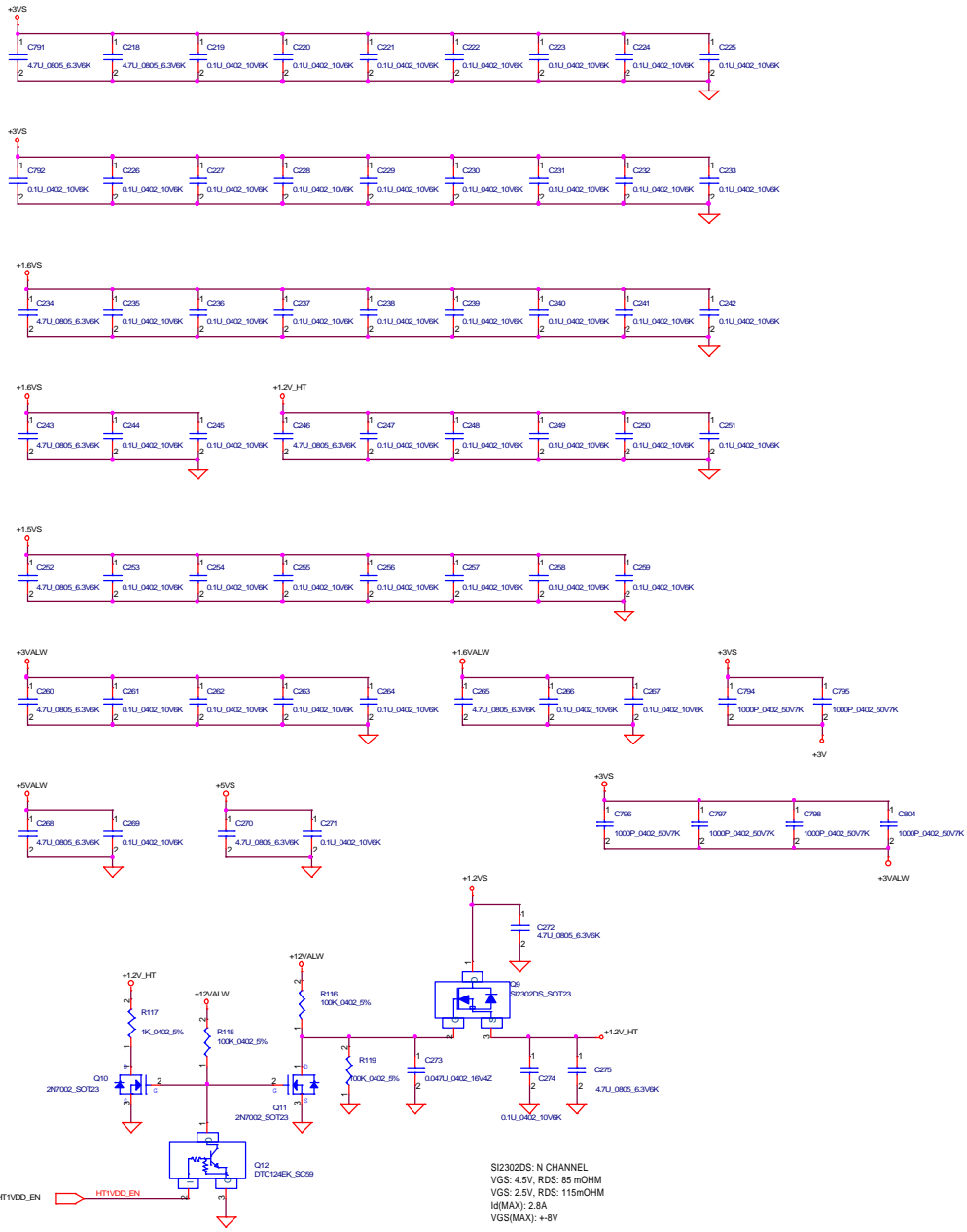
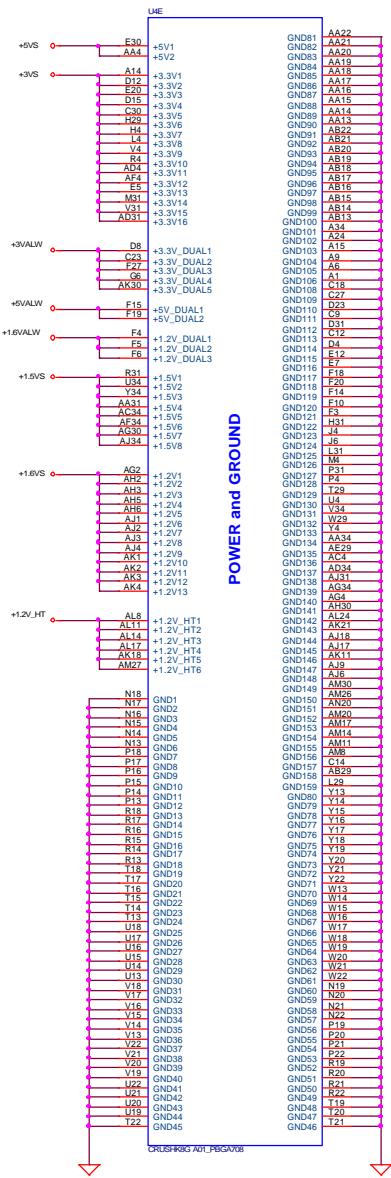
<b>Compal Electronics, Inc.</b>		
<b>DDR SODIMM Decoupling</b>		
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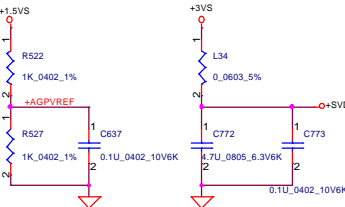
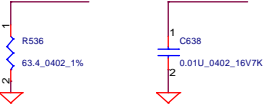
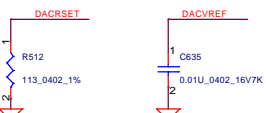
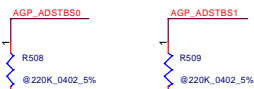
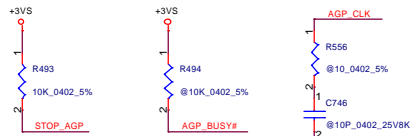




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**nVIDIA CrushK8 (PCI & IDE & USB & MISC)**  
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- AGP\_AD0 AD00
- AGP\_AD1 AE01
- AGP\_AD2 AD02
- AGP\_AD3 AE03
- AGP\_AD4 AE04
- AGP\_AD5 AC05
- AGP\_AD6 AF06
- AGP\_AD7 AC07
- AGP\_AD8 AH08
- AGP\_AD9 AC09
- AGP\_AD10 AH10
- AGP\_AD11 AE11
- AGP\_AD12 AB12
- AGP\_AD13 AC13
- AGP\_AD14 AC14
- AGP\_AD15 AC15
- AGP\_AD16 AE16
- AGP\_AD17 AB17
- AGP\_AD18 AH18
- AGP\_AD19 AC19
- AGP\_AD20 AH20
- AGP\_AD21 AF21
- AGP\_AD22 AH22
- AGP\_AD23 AK23
- AGP\_AD24 AC24
- AGP\_AD25 AB25
- AGP\_AD26 AG16
- AGP\_AD27 AK19
- AGP\_AD28 AH19
- AGP\_AD29 AB18
- AGP\_AD30 AF19
- AGP\_AD31 AK18

- PCIBCE#0 AH28
- AGP\_CBE#1 AK27
- AGP\_CBE#2 AK25
- AGP\_CBE#3 AF21
- PCIRST# AH12
- PCIGNT# AK12
- PCIFRAME# AH24
- PCIRDY# AH25
- PCITRDY# AH27
- PCIDVSEL# AH27
- PCISTOP# AK11
- PCINT# AH12
- AGP\_RBF# AJ13
- AGP\_WBF# AG18
- AGP\_BUSY# AF10
- STOP\_AGP AG10
- +AGP\_VREF AC30

- AGPSBSTB AH16
- AGPSBSTB AH17
- AGPSBA0 AJ15
- AGPSBA1 AF15
- AGPSBA2 AK15
- AGPSBA3 AG16
- AGPSBA4 AK16
- AGPSBA5 AF16
- AGPSBA6 AJ16
- AGPSBA7 AH18

- AGP\_ADSTBF1 AK21
- AGP\_ADSTBS1 AJ21
- AGP\_ADSTBF0 AK28
- AGP\_ADSTBS0 AJ28
- AGP\_ST0 AF12
- AGP\_ST1 AF13
- AGP\_ST2 AG13

- CRT\_R AJ9
- CRT\_G AJ10
- CRT\_B AH8
- CRT\_HSYNC AH10
- CRT\_VSYNC AH9
- DACRSET AJ8
- DACVREF AK9
- TV\_CRMA Y2
- TV\_LUMA AA2
- TV\_COMPS V6
- AG3 Y3
- DAC2HSYNC DAC2VSYNC
- DAC2RSET DAC2VREF

- XTALIN AJ7
- XTALOUT AK7
- XTALSSIN AH7
- XTALSSIN XTALSSINBUFF
- STRAP0 B30
- STRAP1 B29
- STRAP2 A30
- STRAP3 A29
- AG AJ9
- AG3 AJ3
- TESTMODE SA000040300(0304231100)

**GPIO/VIP Interface**

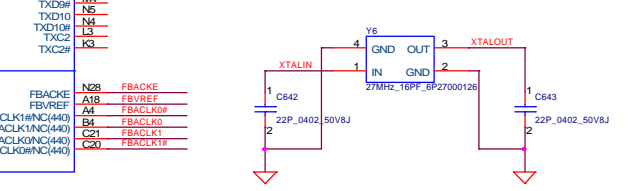
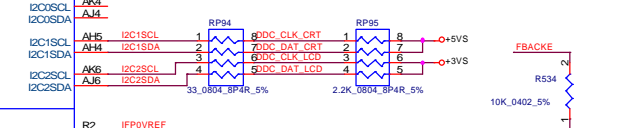
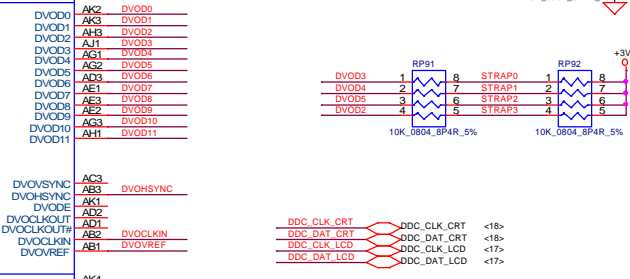
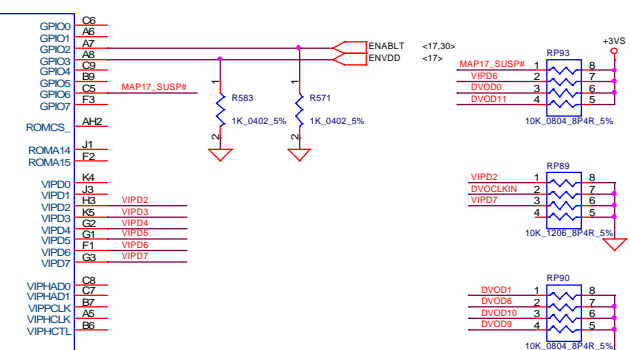
**PCI/AGP BUS Interface**

**I2C**

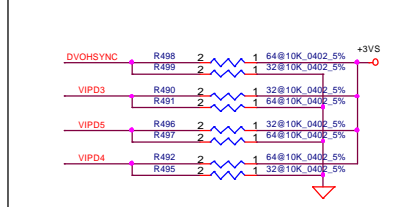
**LVDS/TMDS**

**DAC**

**CLOCK**



DV0HSYNC	VIPD3	VIPD5	VIPD4	DEVICE
1	1	0	1	MAP17-116 (16MB)
0	1	1	0	* MAP17-232 (32MB)
1	0	0	1	MAP17-464 (64MB)



**CRYSTAL**

DV0D8	DV0D7	TVMODE
0	0	SECAM
0	1	* NTSC
1	0	PAL
1	1	VGA

**SST Ratio selection table for W180**

Modulation setting	SST Ratio
0	1.25%
1	3.75%

**Compal Electronics, Inc.**

**MAP17 AGP Interface(1/3)**

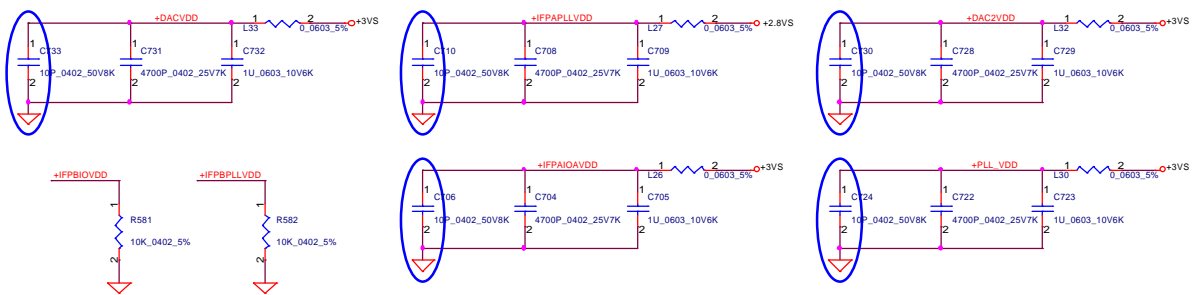
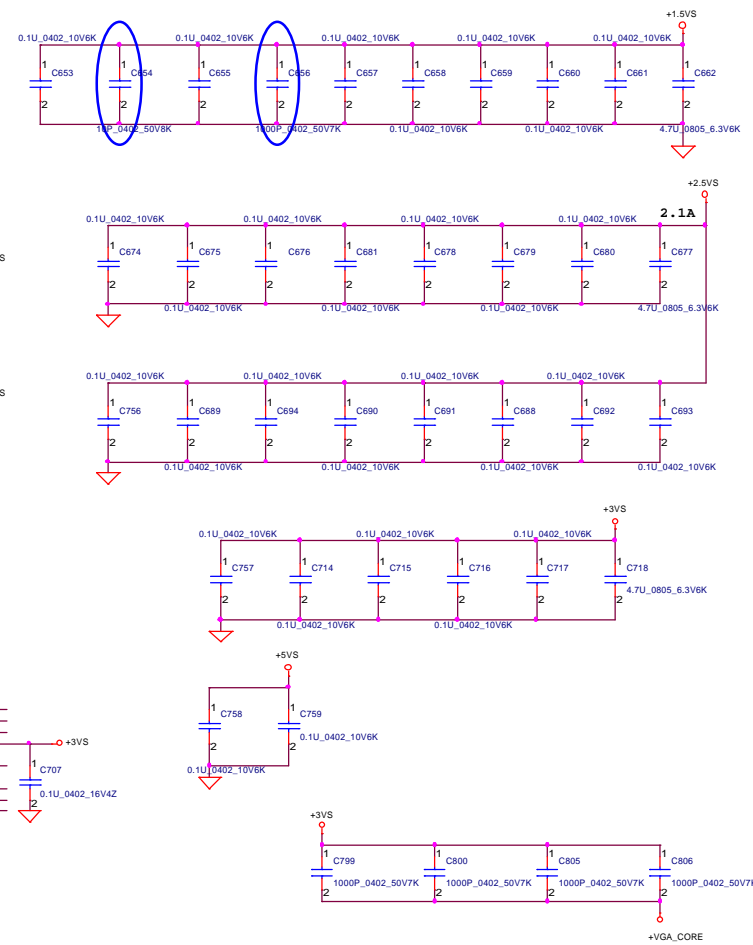
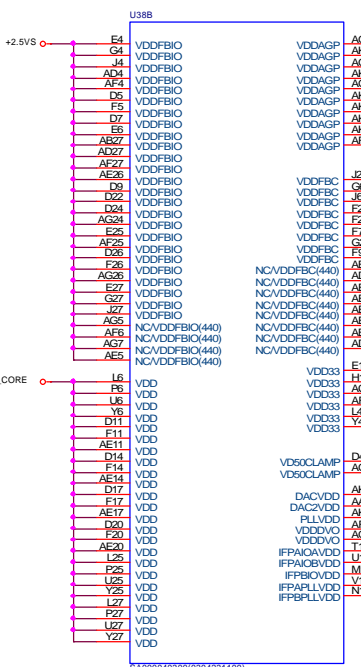
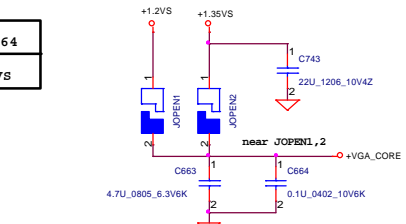
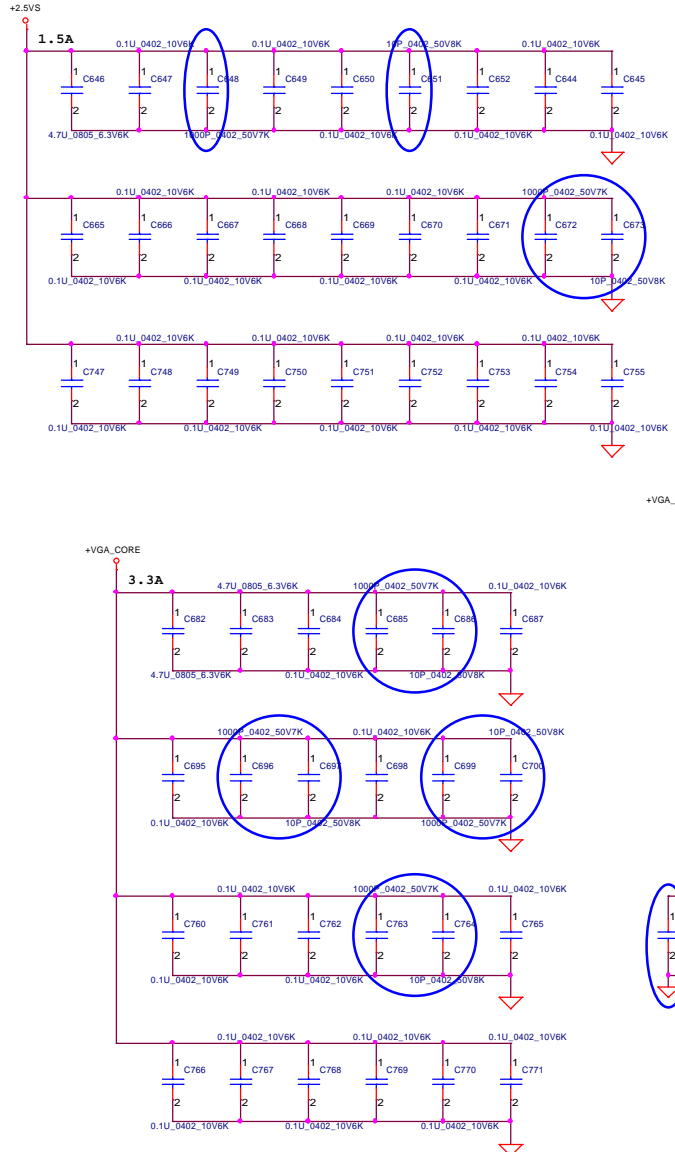
Document Number: LA-1851

Date: Thursday, October 16, 2003

Sheet 14 of 50

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	MAP17-116/232	MAP17-464
+VGA_CORE	* +1.2VS	+1.35VS



**Compal Electronics, Inc.**

**MAP17 Power (2/3)**

Document Number: LA-1851

Rev: 0.5

Date: Thursday, October 16, 2003

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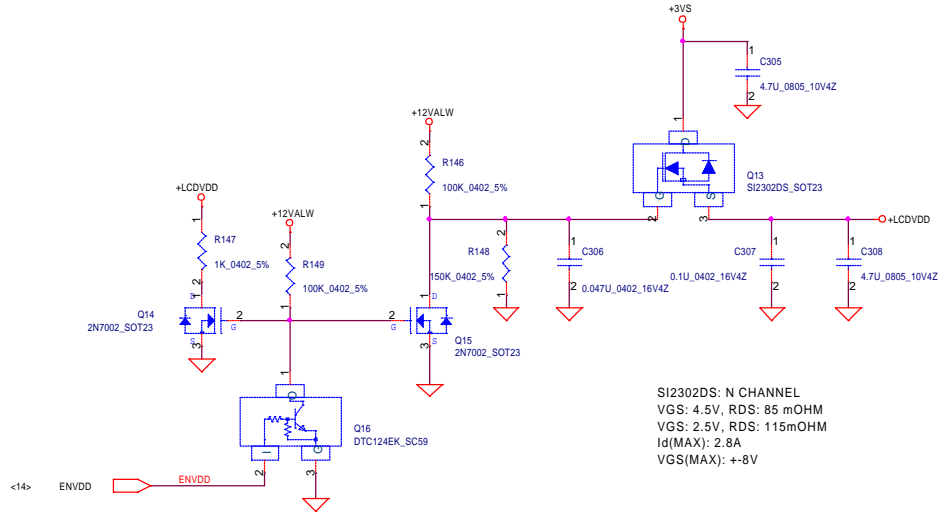
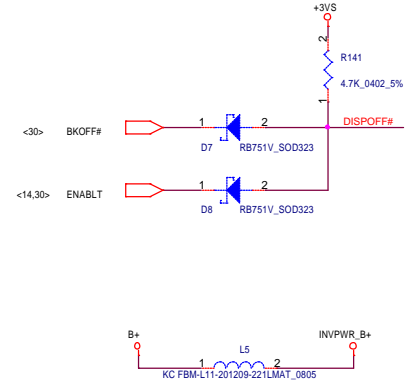
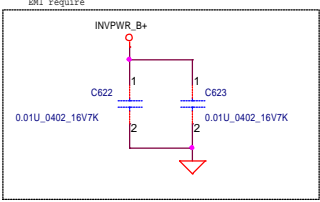
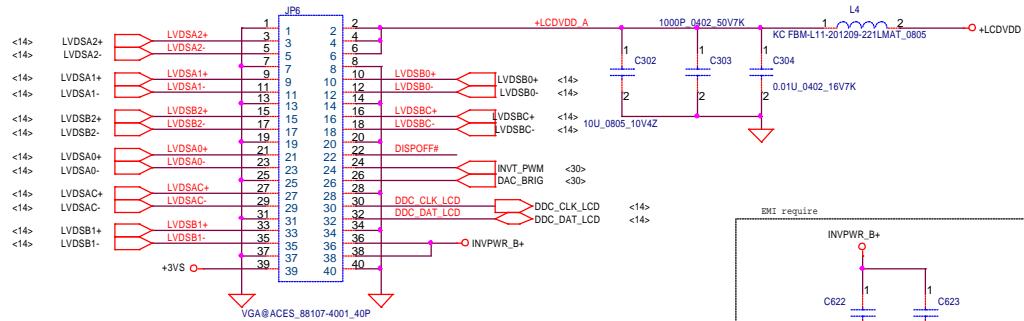
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# LCD Panel Connector

The cap.'s colsely to LCD CONN.

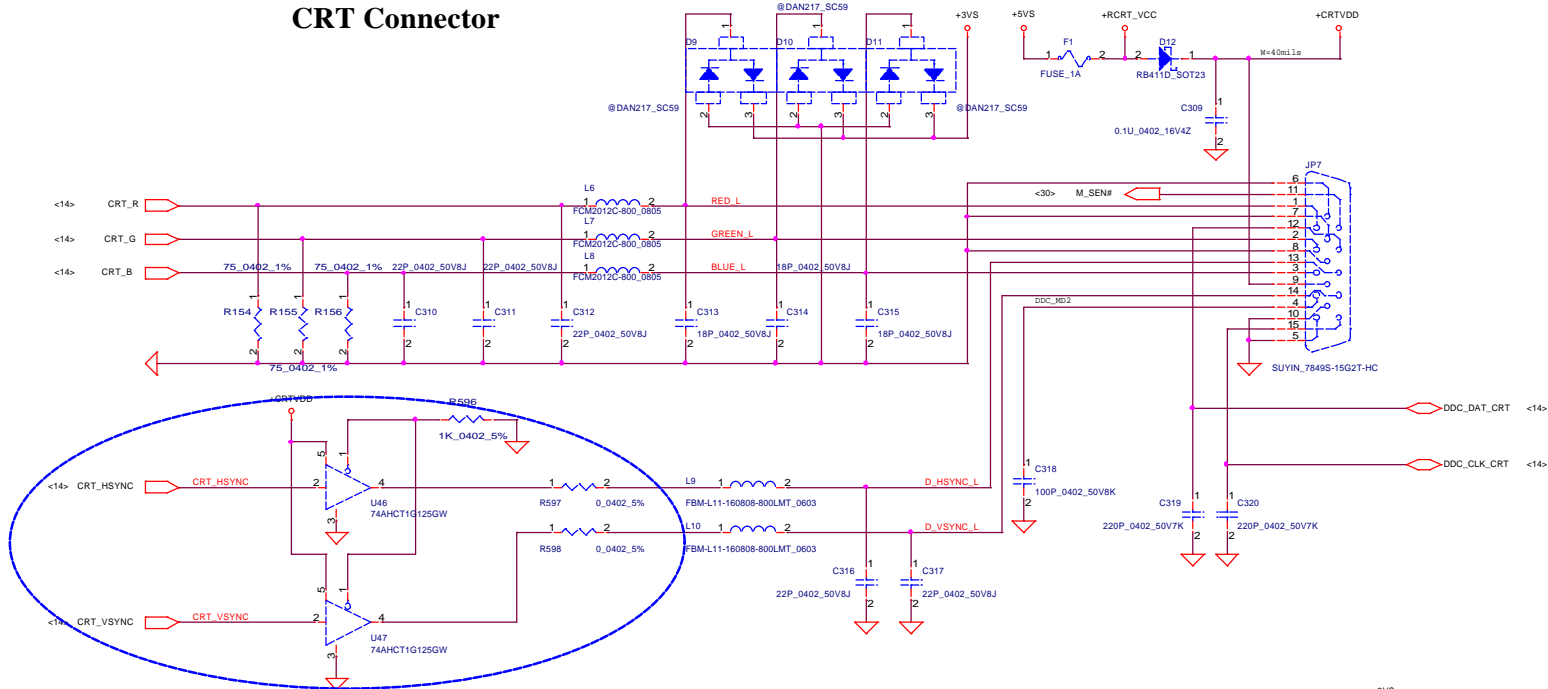


SI2302DS: N CHANNEL  
 VGS: 4.5V, RDS: 85 mOHM  
 VGS: 2.5V, RDS: 115mOHM  
 Id(MAX): 2.8A  
 VGS(MAX): +-8V

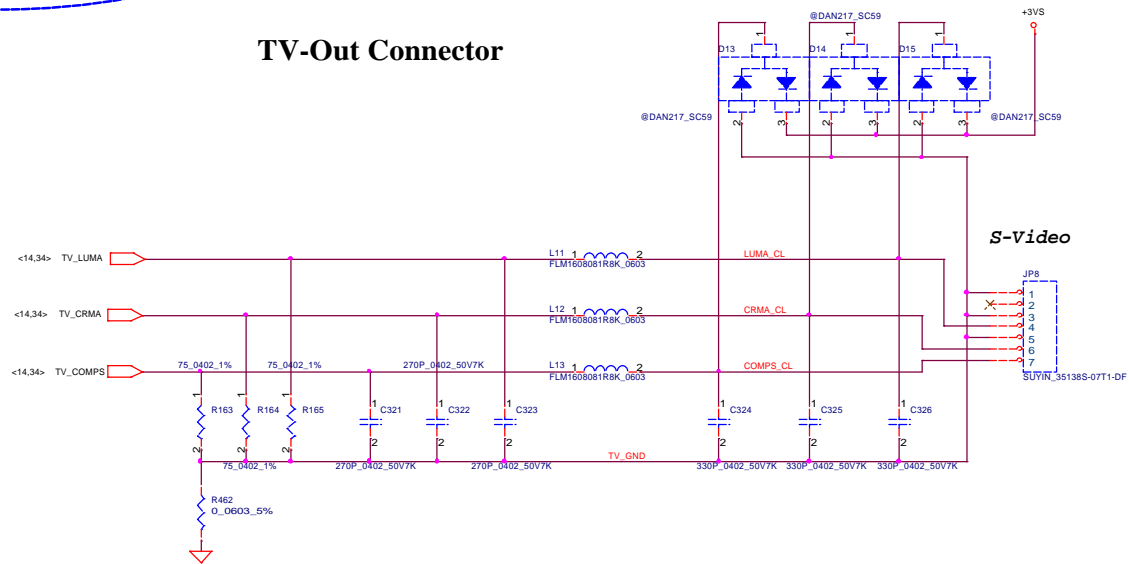
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Compal Electronics, Inc.		
Title: LVDS Connector		
Size: LA-1851	Document Number: LA-1851	Rev: 0.5
Date: Thursday, October 16, 2003	Sheet: 17	of 50

# CRT Connector



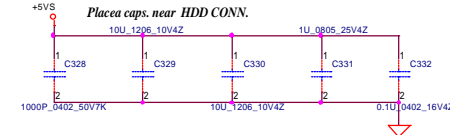
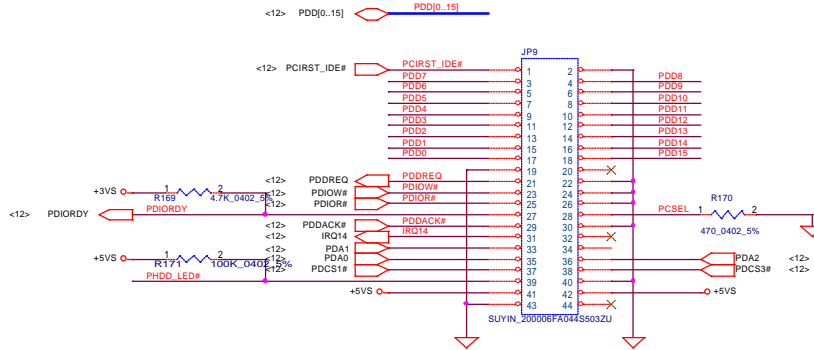
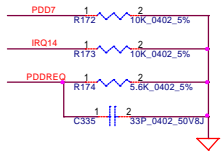
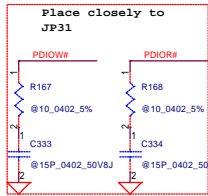
# TV-Out Connector



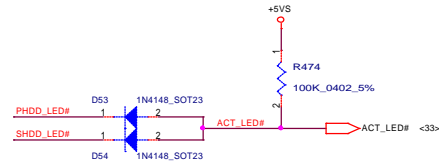
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<b>Compal Electronics, Inc.</b>		
<b>CRT &amp; TVout Connector</b>		
Doc No	Document Number	Rev
	<b>LA-1851</b>	0.5
Date:	Thursday, October 16, 2003	Sheet 18 of 50

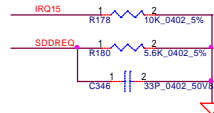
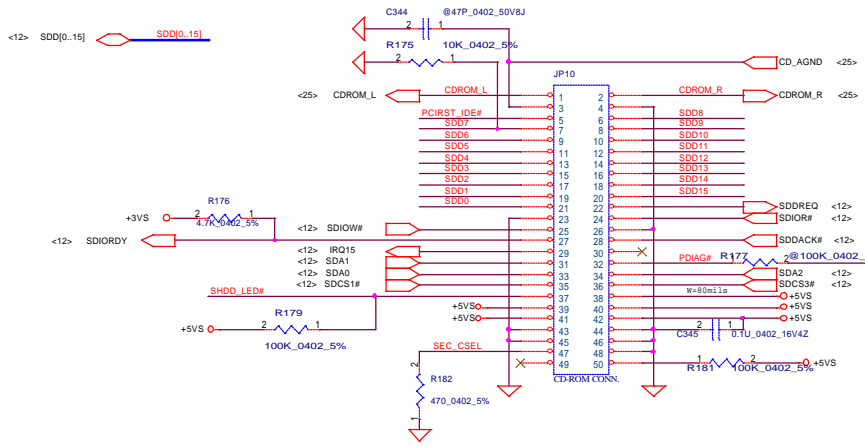
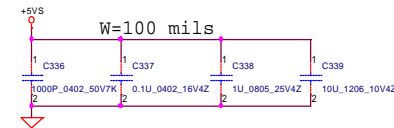
### HDD Connector



### CD-ROM Connector



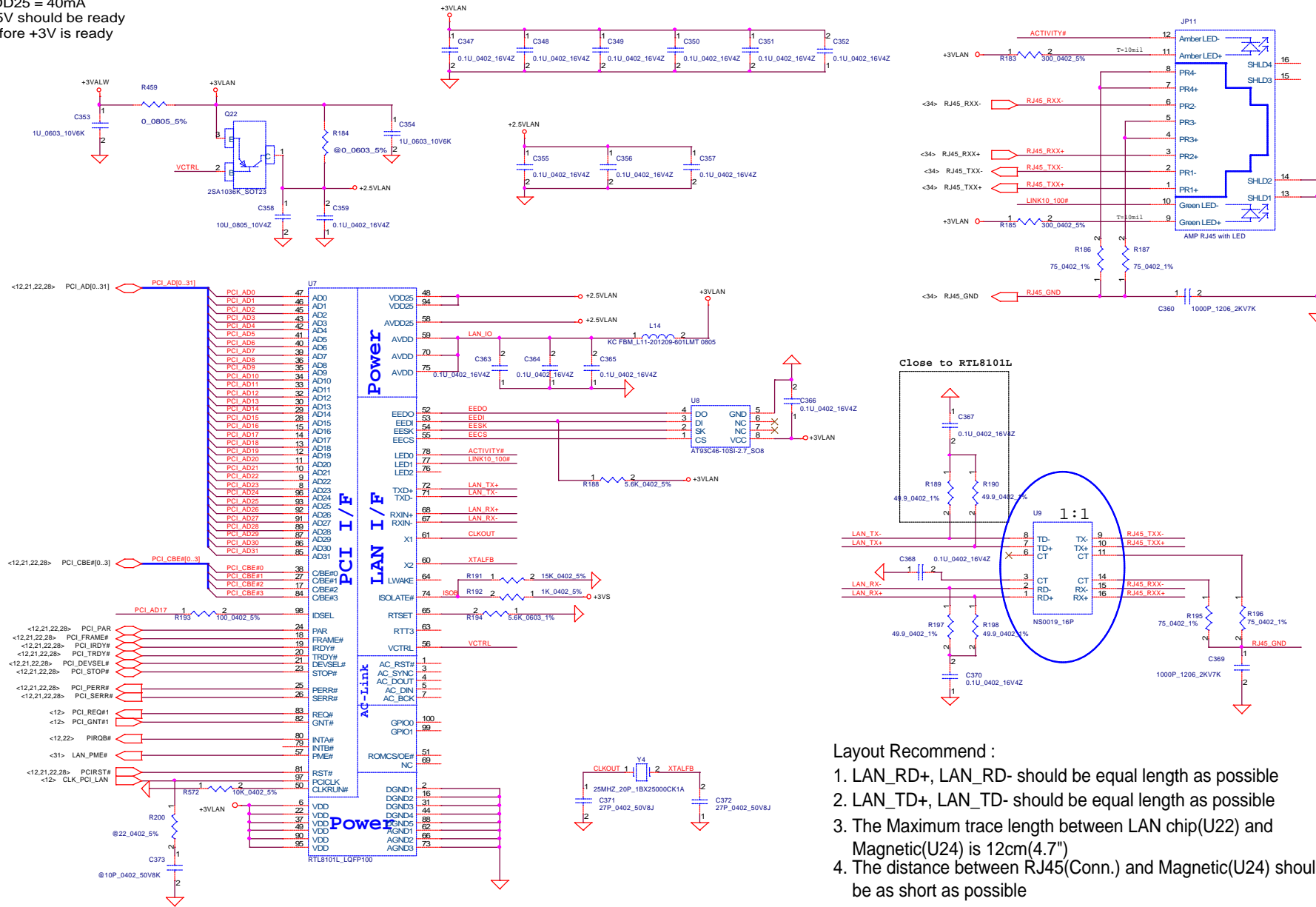
Place caps. near CDROM CONN.



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<b>Compal Electronics, Inc.</b>		
Title <b>IDE/FDD/CD-ROM Module</b>		
Size	Document Number	Rev
Custom	<b>LA-1851</b>	0.5
Date:	Thursday, October 16, 2003	Sheet 19 of 50

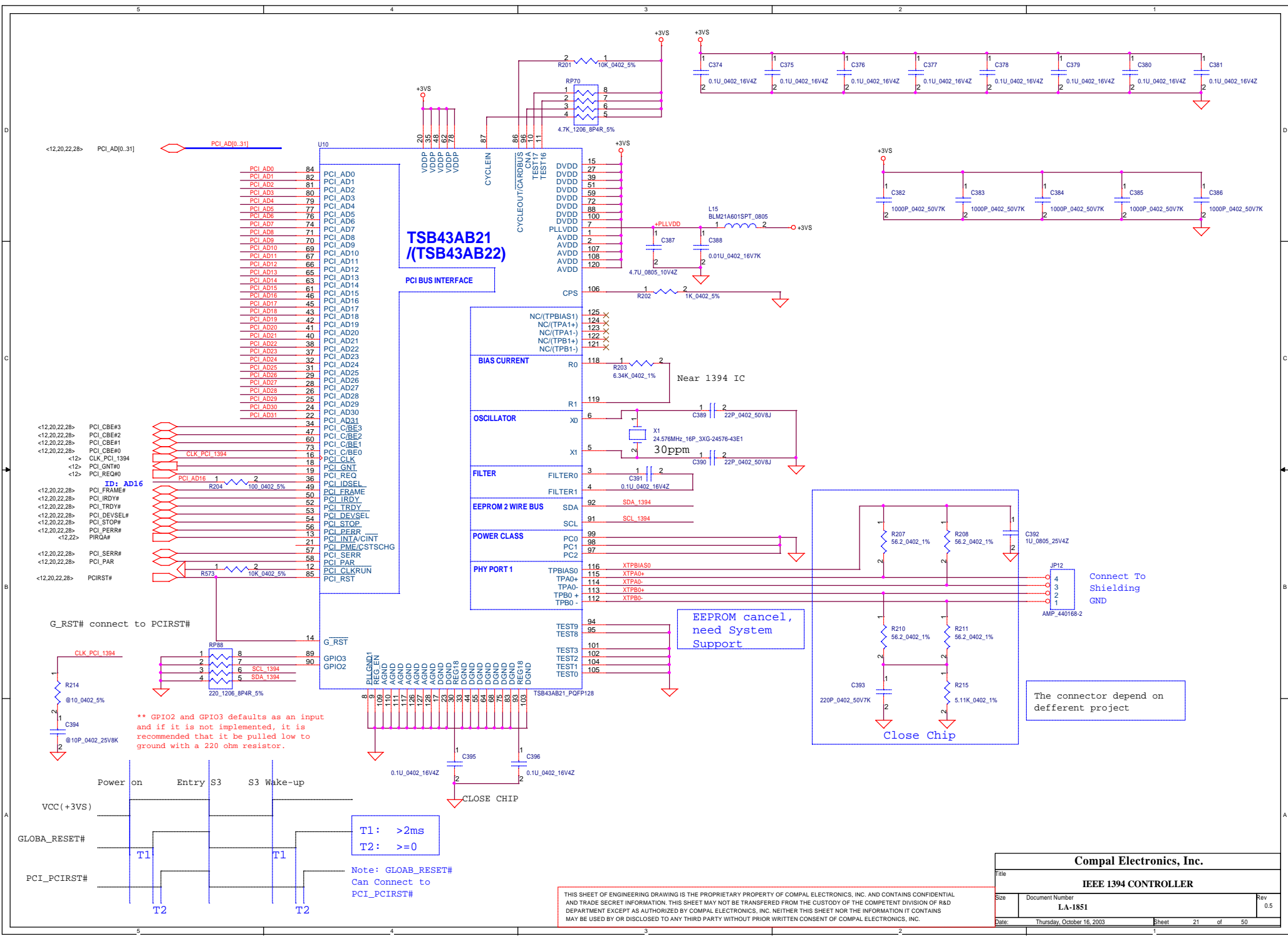
Note : I<sub>max</sub> for VDD25 = 40mA  
 2.5V should be ready before +3V is ready



- Layout Recommend :
1. LAN\_RD+, LAN\_RD- should be equal length as possible
  2. LAN\_TD+, LAN\_TD- should be equal length as possible
  3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
  4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

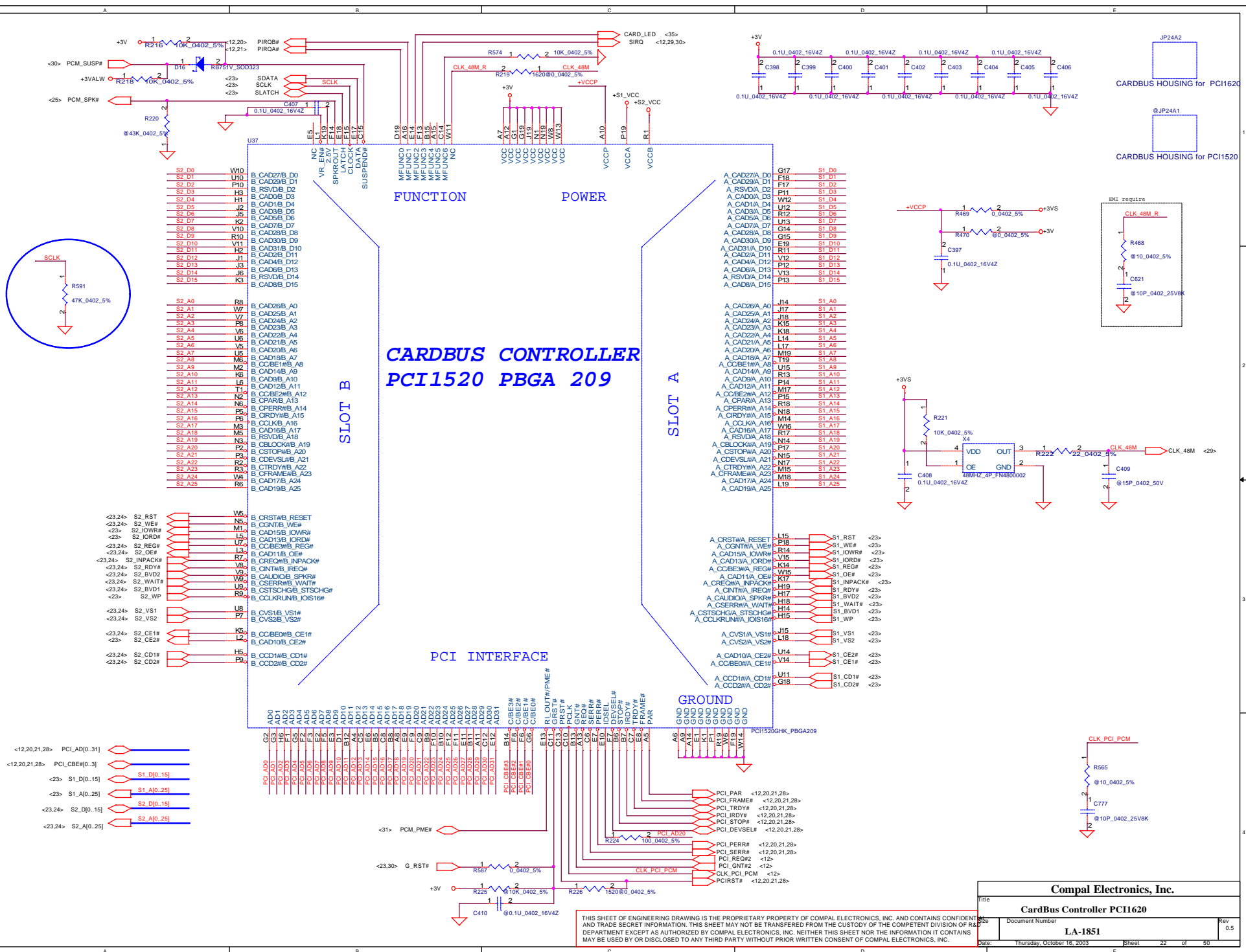
<b>Compal Electronics, Inc.</b>		
LAN RealTech8100BL		
Document Number	Rev	0.5
LA-1851		
Date: Thursday, October 16, 2003	Sheet	20 of 50

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Compal Electronics, Inc.		
Title: IEEE 1394 CONTROLLER		
Size	Document Number	Rev
	LA-1851	0.5
Date:	Thursday, October 16, 2003	Sheet 21 of 50

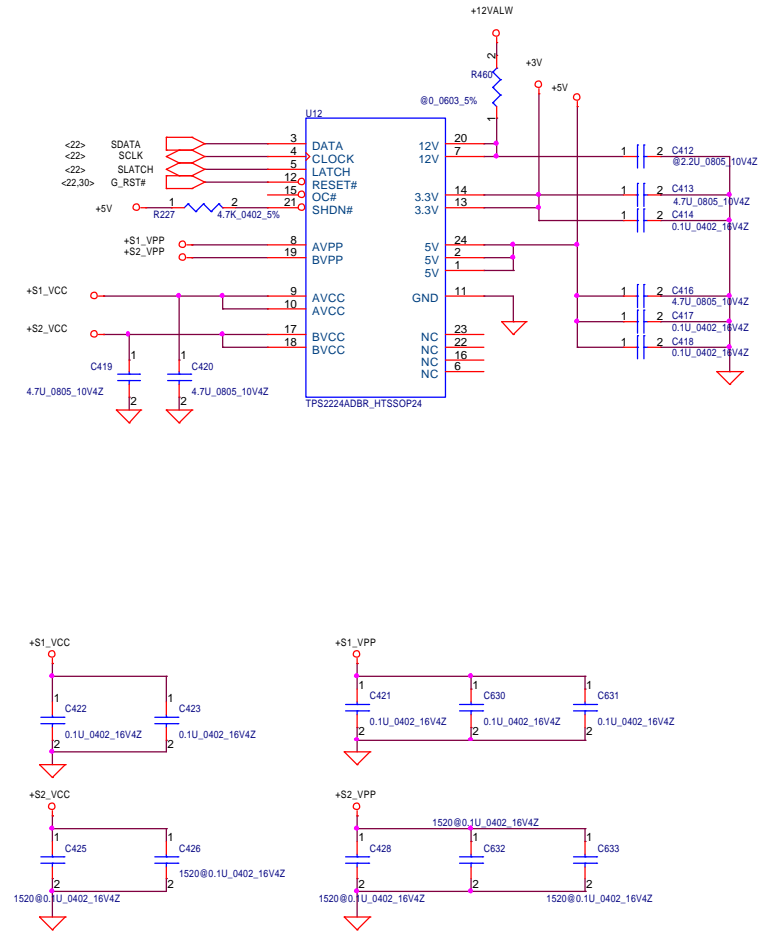
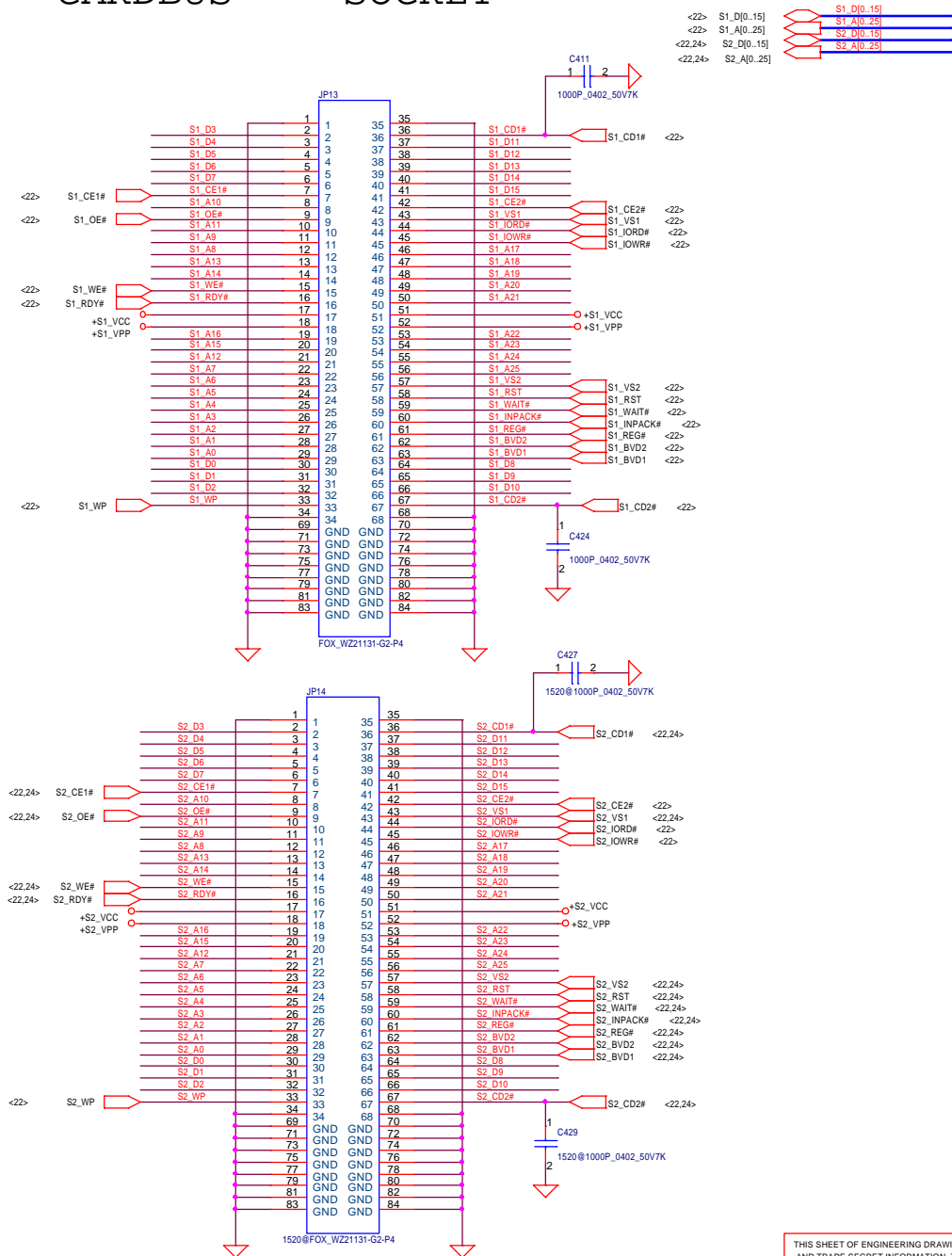


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<b>Compal Electronics, Inc.</b>		
<b>CardBus Controller PCI1620</b>		
Docu	Document Number	Rev
	<b>LA-1851</b>	0.5
Date:	Thursday, October 16, 2003	Sheet 22 of 50

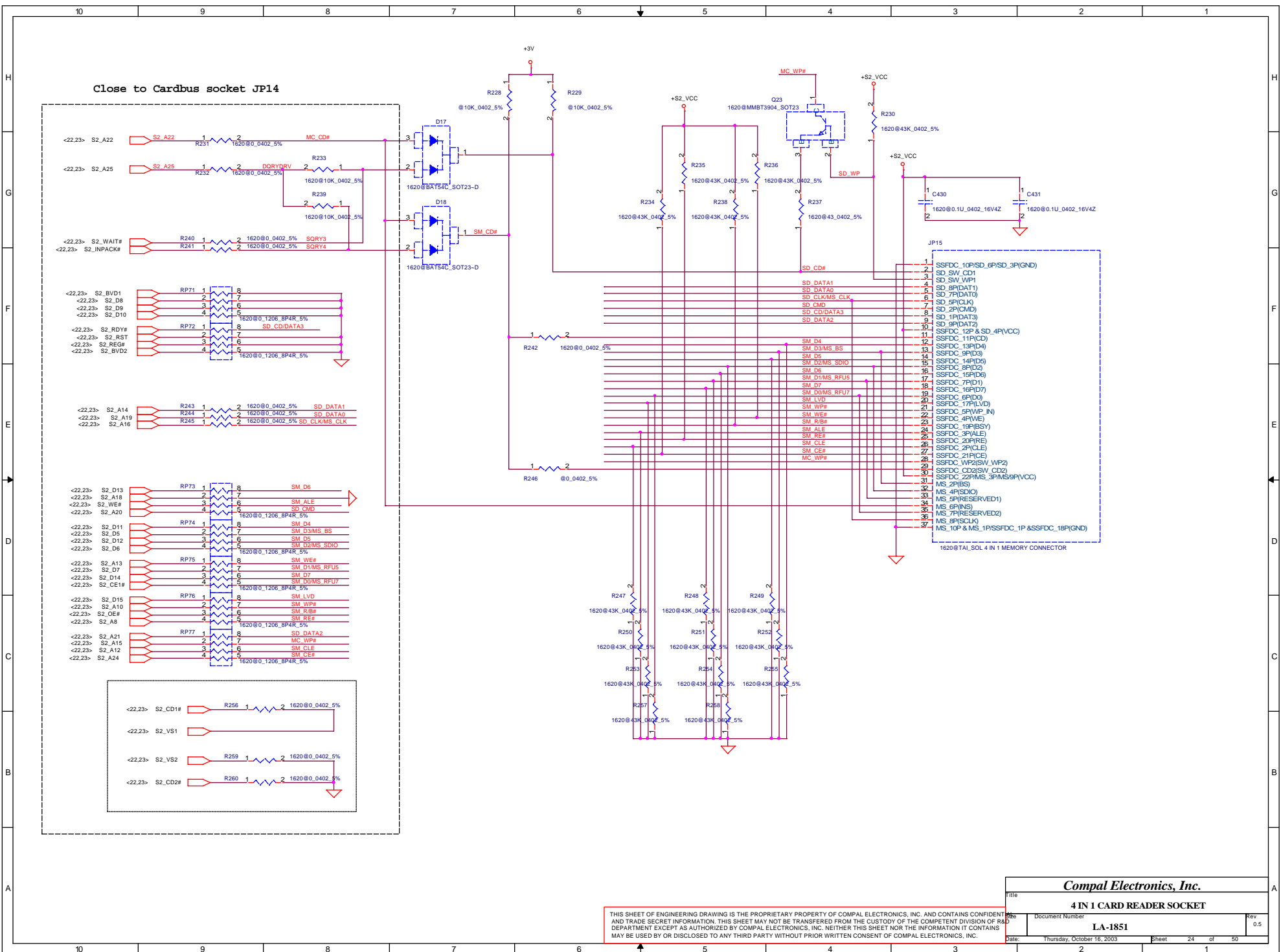
# PCMCIA POWER CTRL.

## CARDBUS SOCKET



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Compal Electronics, Inc.		
File	CARD BUS SOCKET	
Size	Document Number	Rev
	LA-1851	0.5
Date:	Thursday, October 16, 2003	Sheet 23 of 50



Close to Cardbus socket JP14

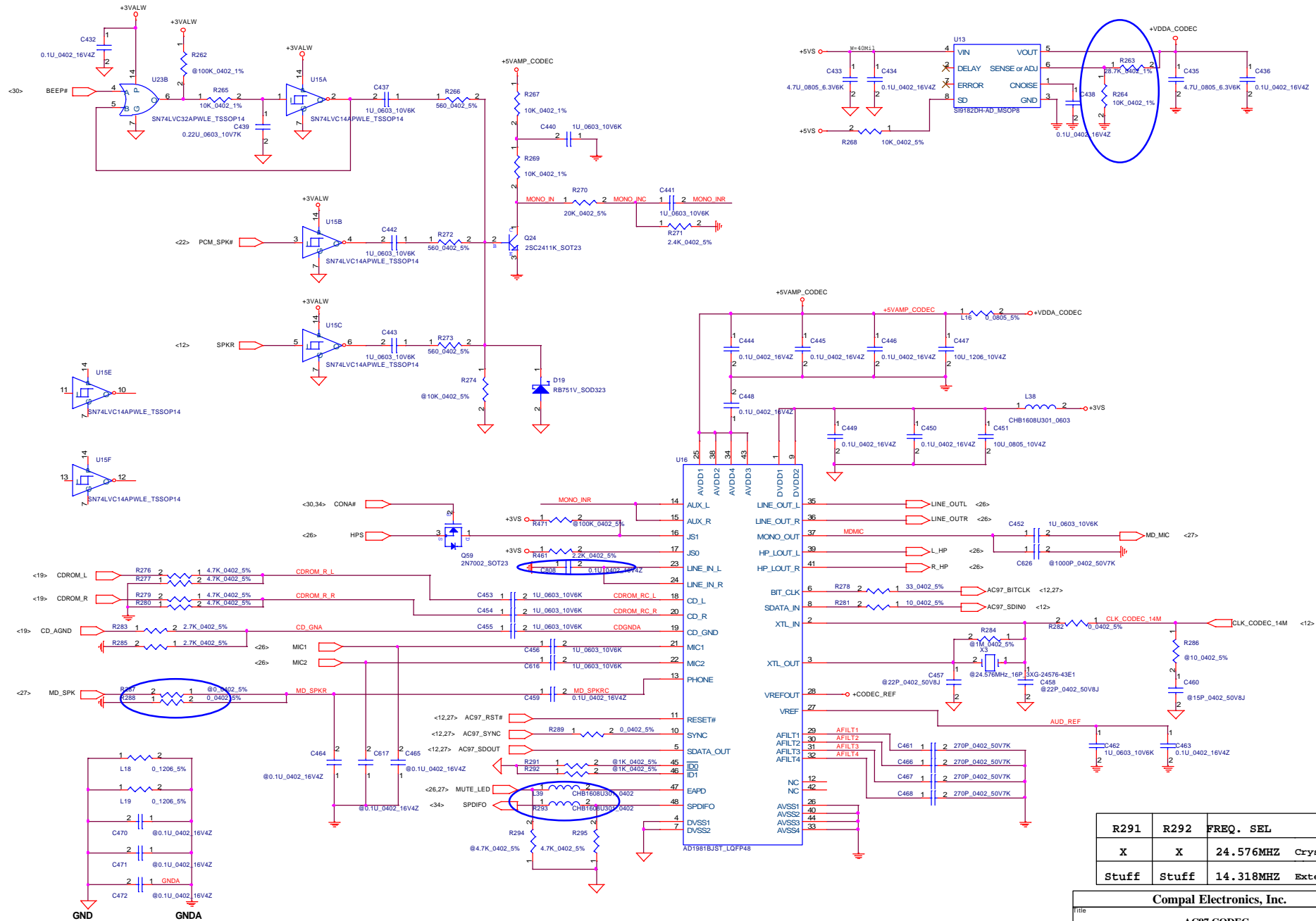
Compal Electronics, Inc.

4 IN 1 CARD READER SOCKET

File	Document Number	Rev
	LA-1851	0.5
Date	Thursday, October 16, 2003	Sheet 24 of 50

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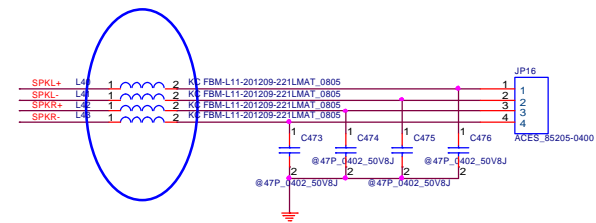
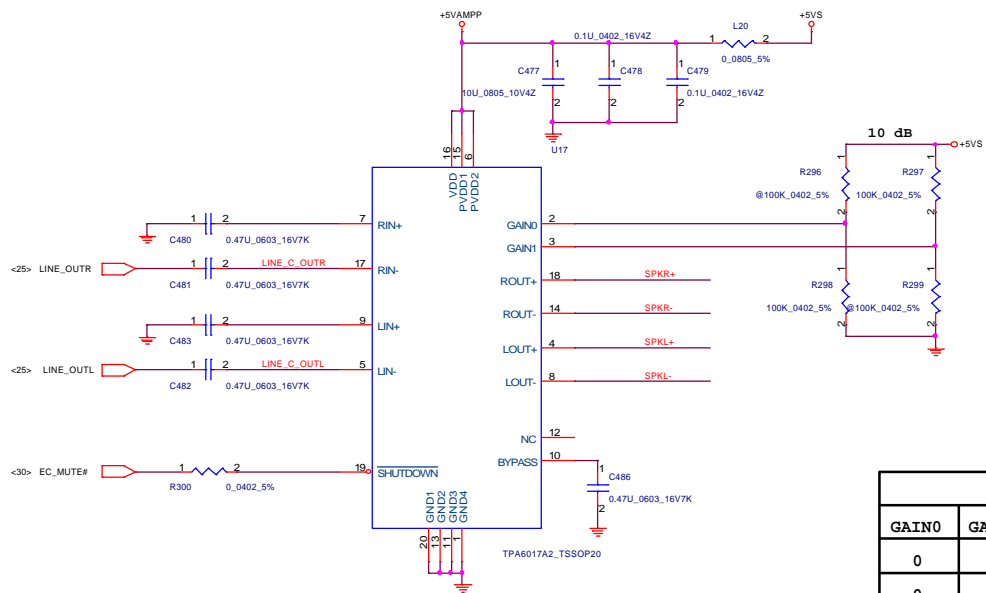




R291	R292	FREQ. SEL	
X	X	24.576MHZ	Crystal
Stuff	Stuff	14.318MHZ	External

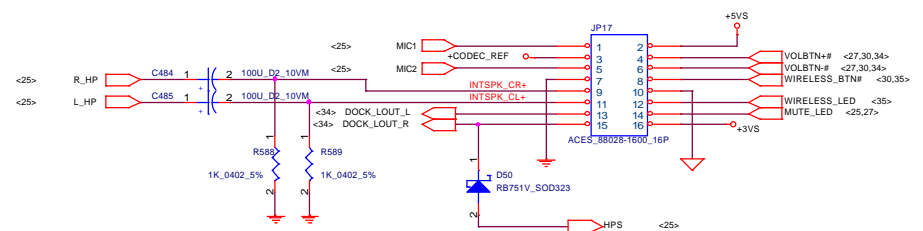
<b>Compal Electronics, Inc.</b>			
<b>AC97 CODEC</b>			
Title	Document Number	Rev	
	<b>LA-1851</b>	0.5	
Date	Thursday, October 16, 2003	Sheet	25 of 50

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Gain Settings		
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

**AUDIO CONNECTOR**



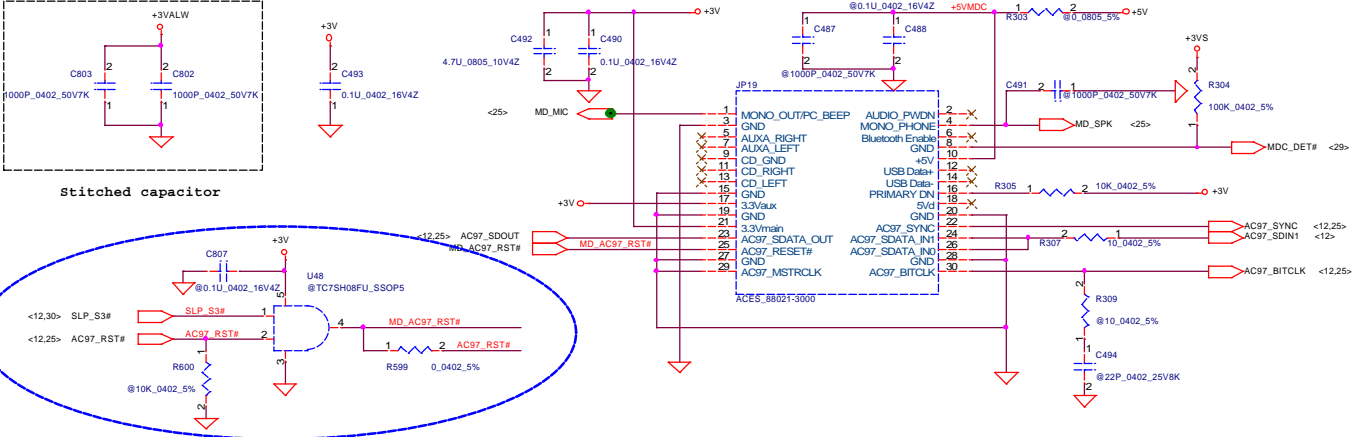
**Compal Electronics, Inc.**

**AMP & Audio Jack**

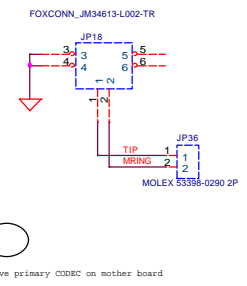
Title	Document Number	Rev
	<b>LA-1851</b>	0.5
Stamp	Thursday, October 16, 2003	Sheet 28 of 50

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**MDC Conn.**

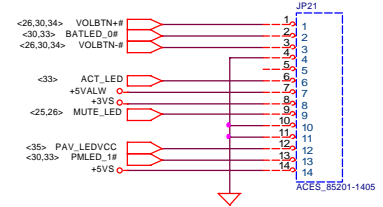


**RJ11 CONN.**

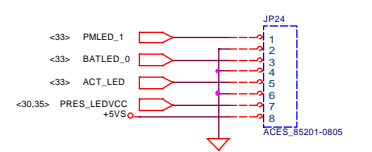


0: Have primary CODEC on mother board

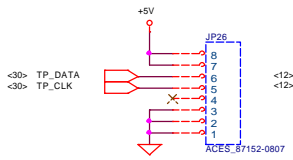
**Front Board CONNECTOR Pavilion only**



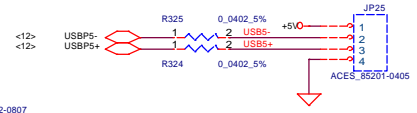
**Front Board CONNECTOR PRESARIO only**



**TP CONNECTOR**

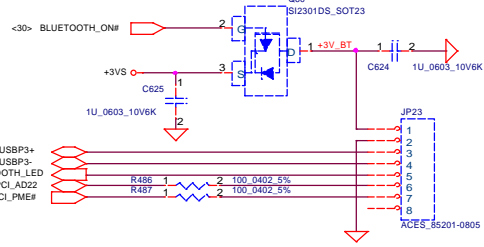


**USB KEY**

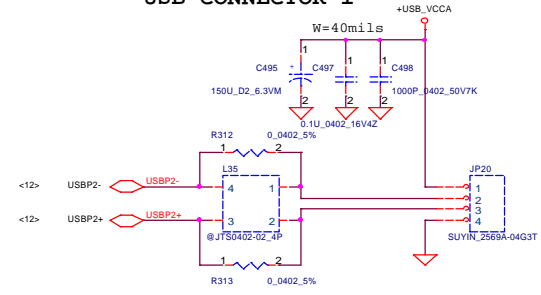


Note: PLACE CLOSE TO EACH USB PORT

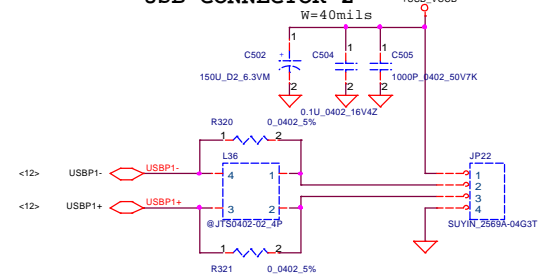
**BT CONNECTOR**



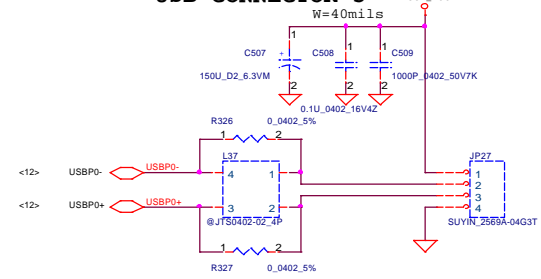
**USB CONNECTOR 1**



**USB CONNECTOR 2**

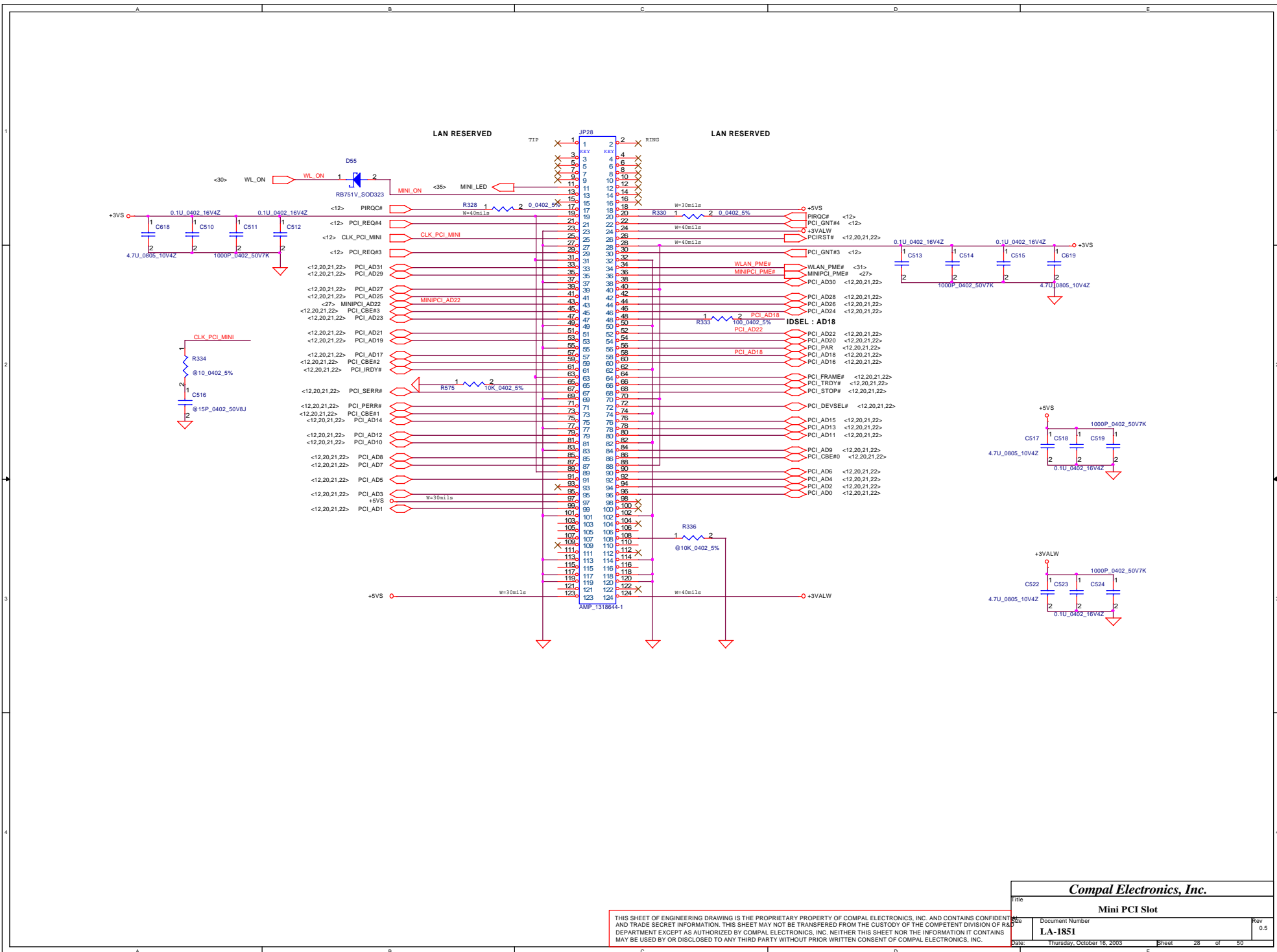


**USB CONNECTOR 3**



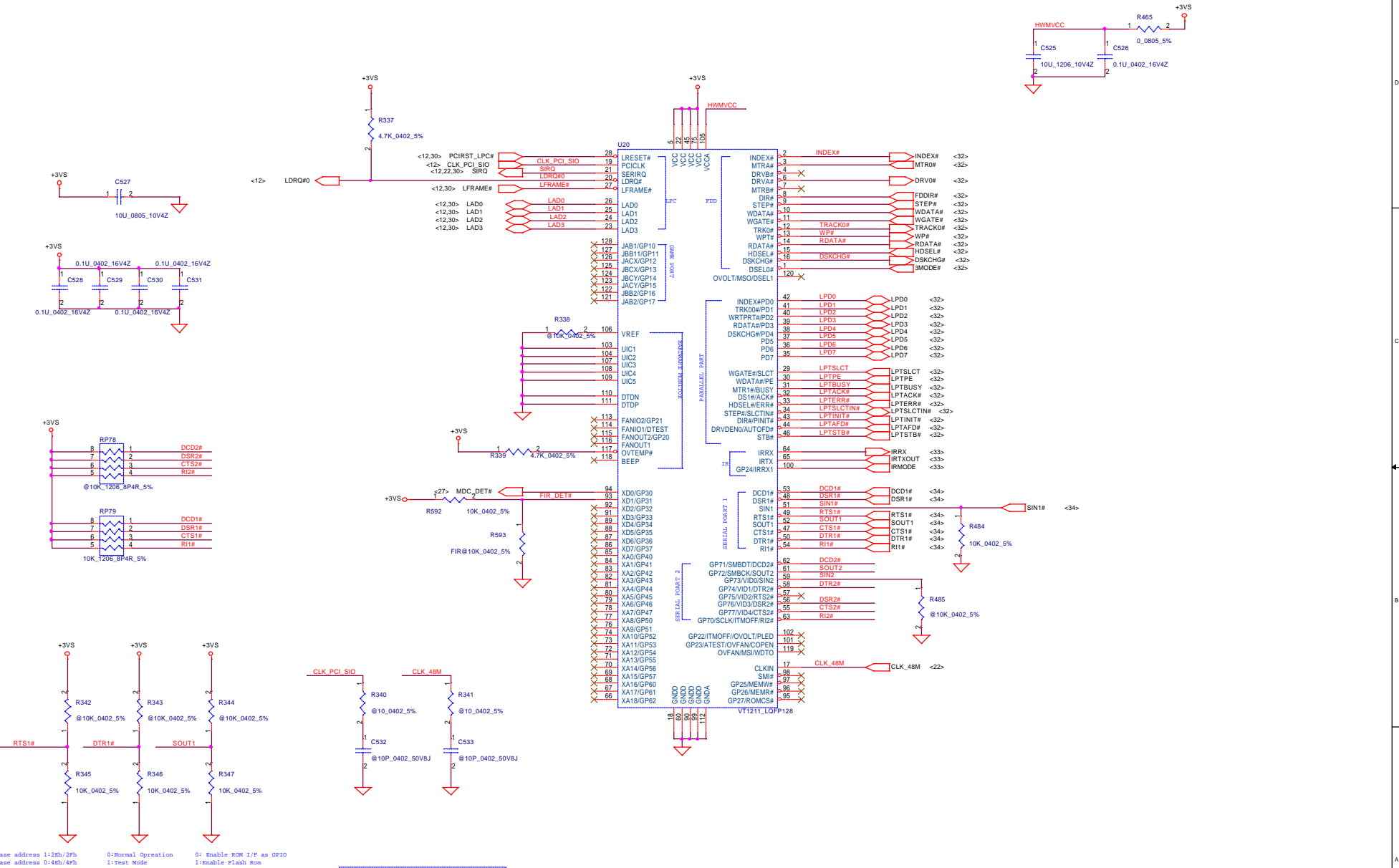
<b>Compal Electronics, Inc.</b>		
<b>MDC , Bluetooth &amp; USB CONN.</b>		
File	Document Number	Rev
	<b>LA-1851</b>	0.5
Date	Friday, October 17, 2003	Sheet 27 of 50

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<b>Compal Electronics, Inc.</b>		
<b>Mini PCI Slot</b>		
Doc No	Document Number	Rev
	<b>LA-1851</b>	0.5
Date:	Thursday, October 16, 2003	Sheet 28 of 50

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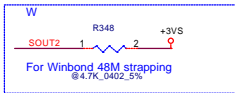


Base address 1:2Kh/3Ph  
 Base address 0:4Kh/4Ph

0:Normal operation  
 1:Test Mode

0: Enable ROM I/P as GP10  
 1:Enable Flash Rom

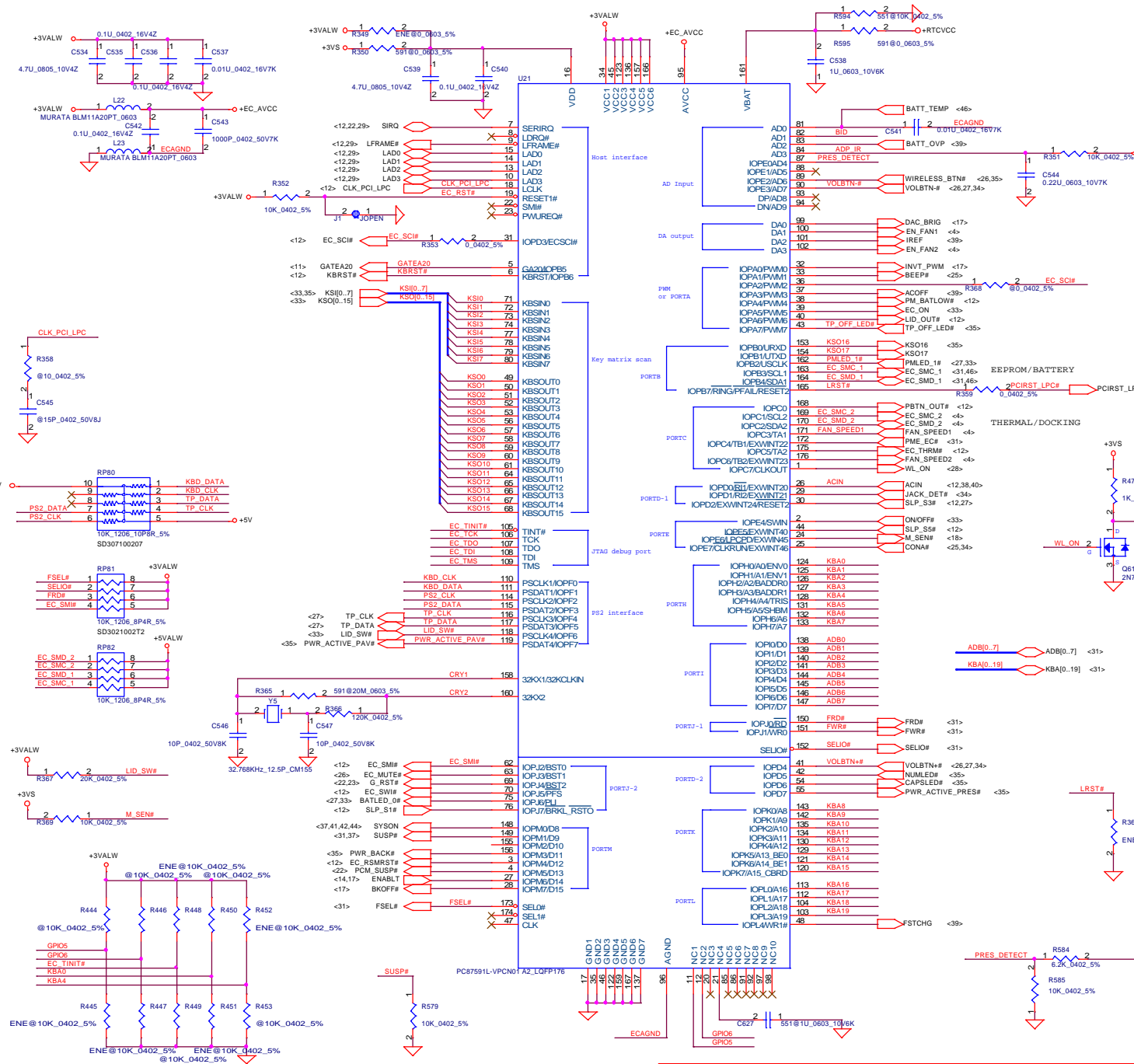
Super I/O strapping for VT1211



For Winbond 48M strapping @4.7K\_0402\_5%

<b>Compal Electronics, Inc.</b>		
Title <b>LPC SUPER I/O VIA VT1211</b>		
Size	Document Number	Rev
	<b>LA-1851</b>	0.5
Date	Thursday, October 16, 2003	Sheet 29 of 50

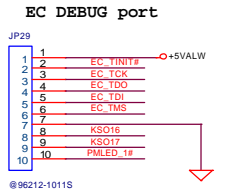
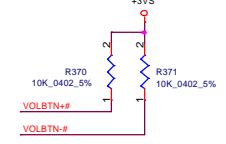
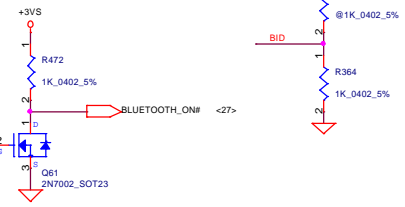
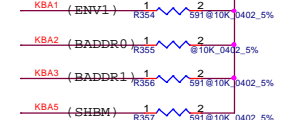
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T/O Address		
BADDR1_0	Index	Data
0 0	2E	2F
0 1	4E	4F
0 0	(HCFGBAH_HCFGBAL)	(HCFGBAH_HCFGBAL+1)
1 1	Reserved	

IRE	ENV0	ENV1	TRIS
0	0	0	0
1	0	1	0
0	1	0	0
1	1	1	0

SHBM=1: Enable shared memory with host BIOS  
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

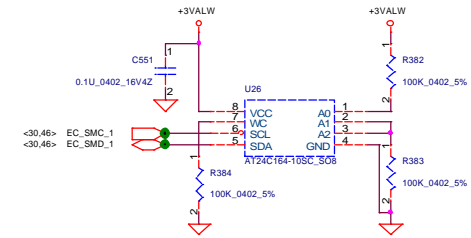
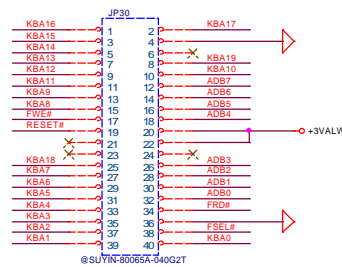
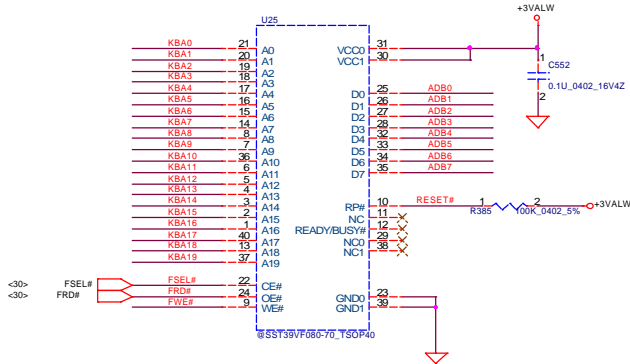
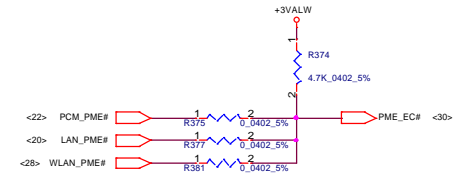
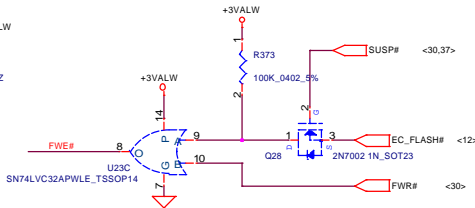
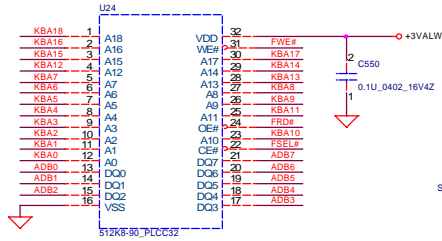
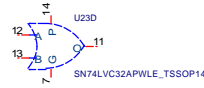
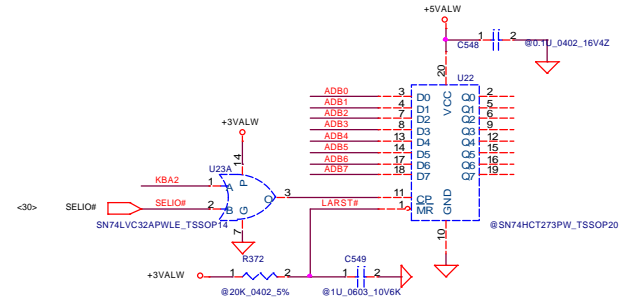


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INPUT

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 <30> KBA[0..19] KBA[0..19]

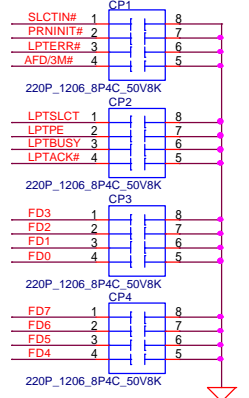
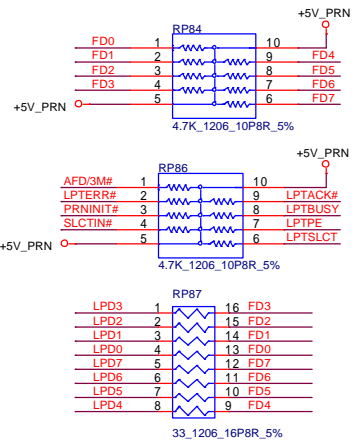
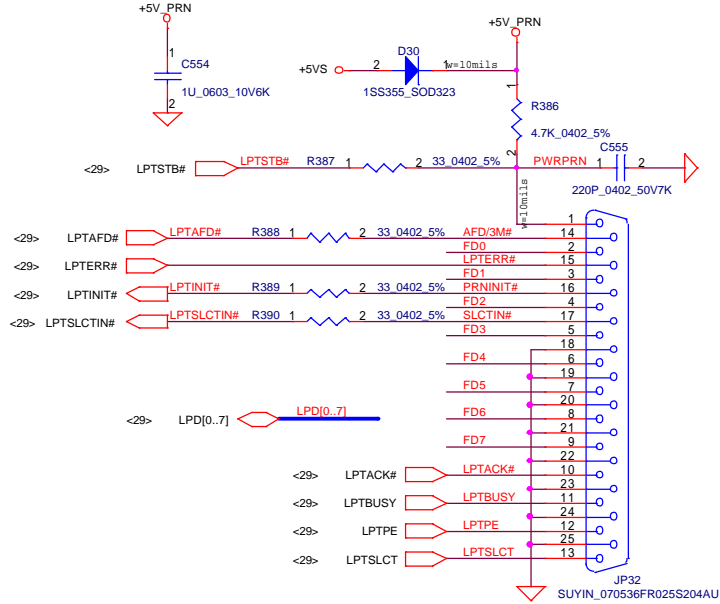
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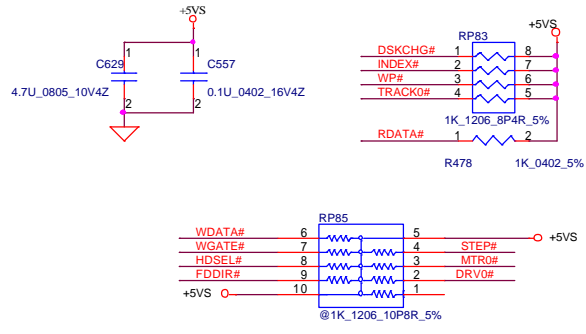
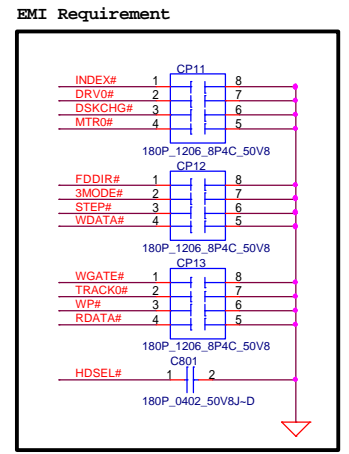
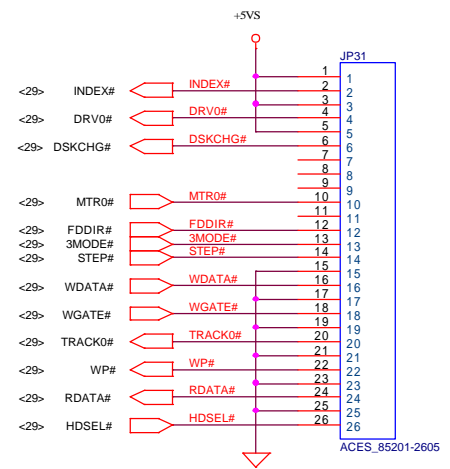
<b>Compal Electronics, Inc.</b>		
<b>BIOS &amp; EC I/O Port</b>		
Part Number	Document Number	Rev
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# Parallel Port



# FDD CONN.

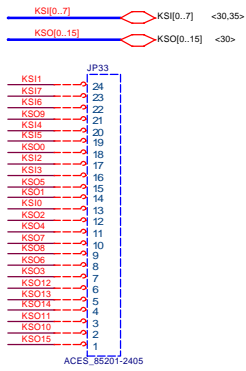


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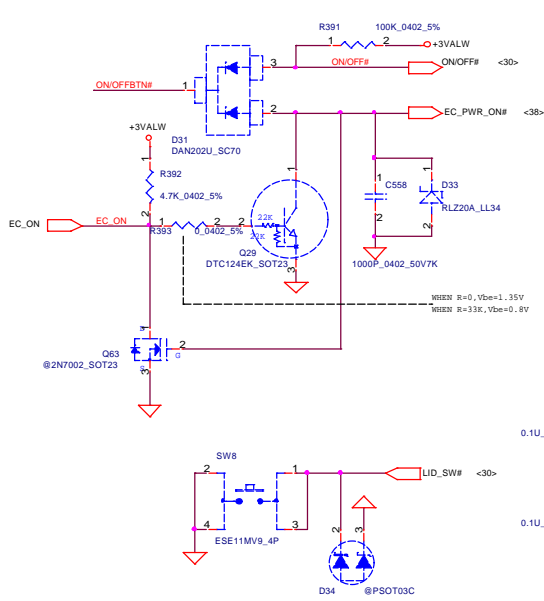
Title		
Parallel port & FDD Connector		
Size	Document Number	Rev
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Date:	Thursday, October 16, 2003	Sheet 32 of 50



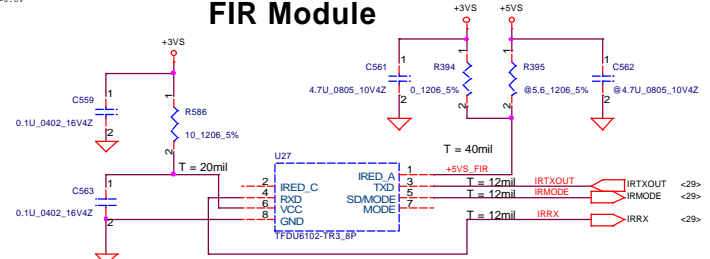
**INT\_KBD CONN.**



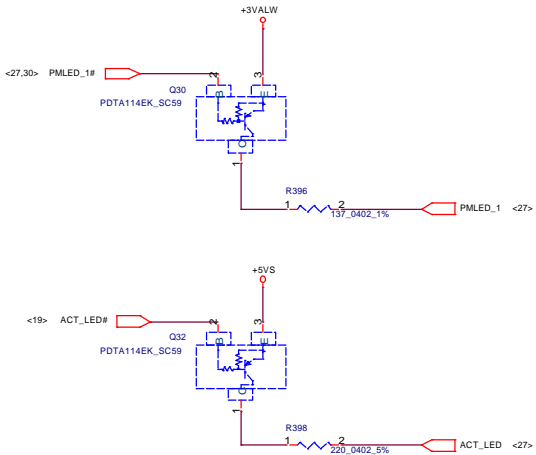
**Power BTN**



**FIR Module**

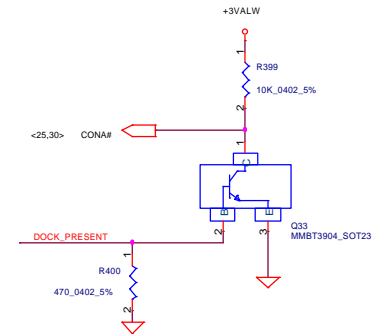
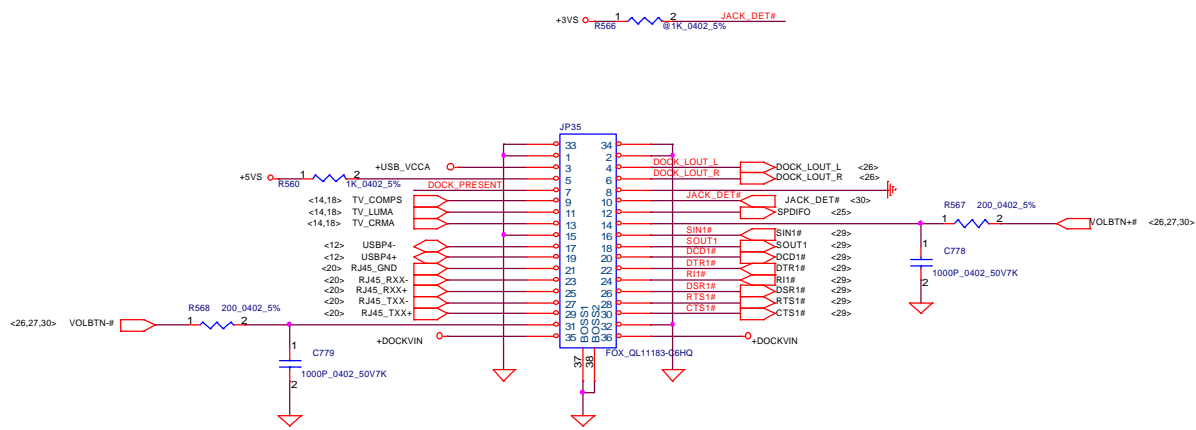


**Touch Pad & Status LED Conn.**

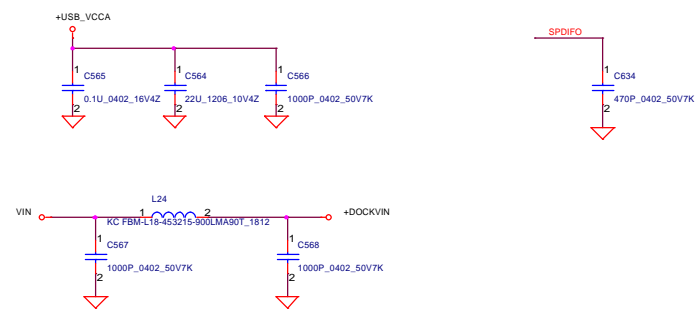
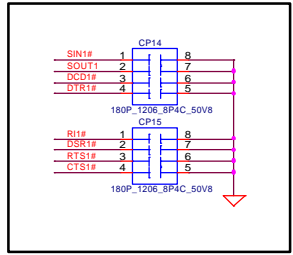


<b>Compal Electronics, Inc.</b>		
<b>KBD,ON/OFF,T/P,LED &amp; FIR</b>		
Doc#	Document Number	Rev
	<b>LA-1851</b>	0.5
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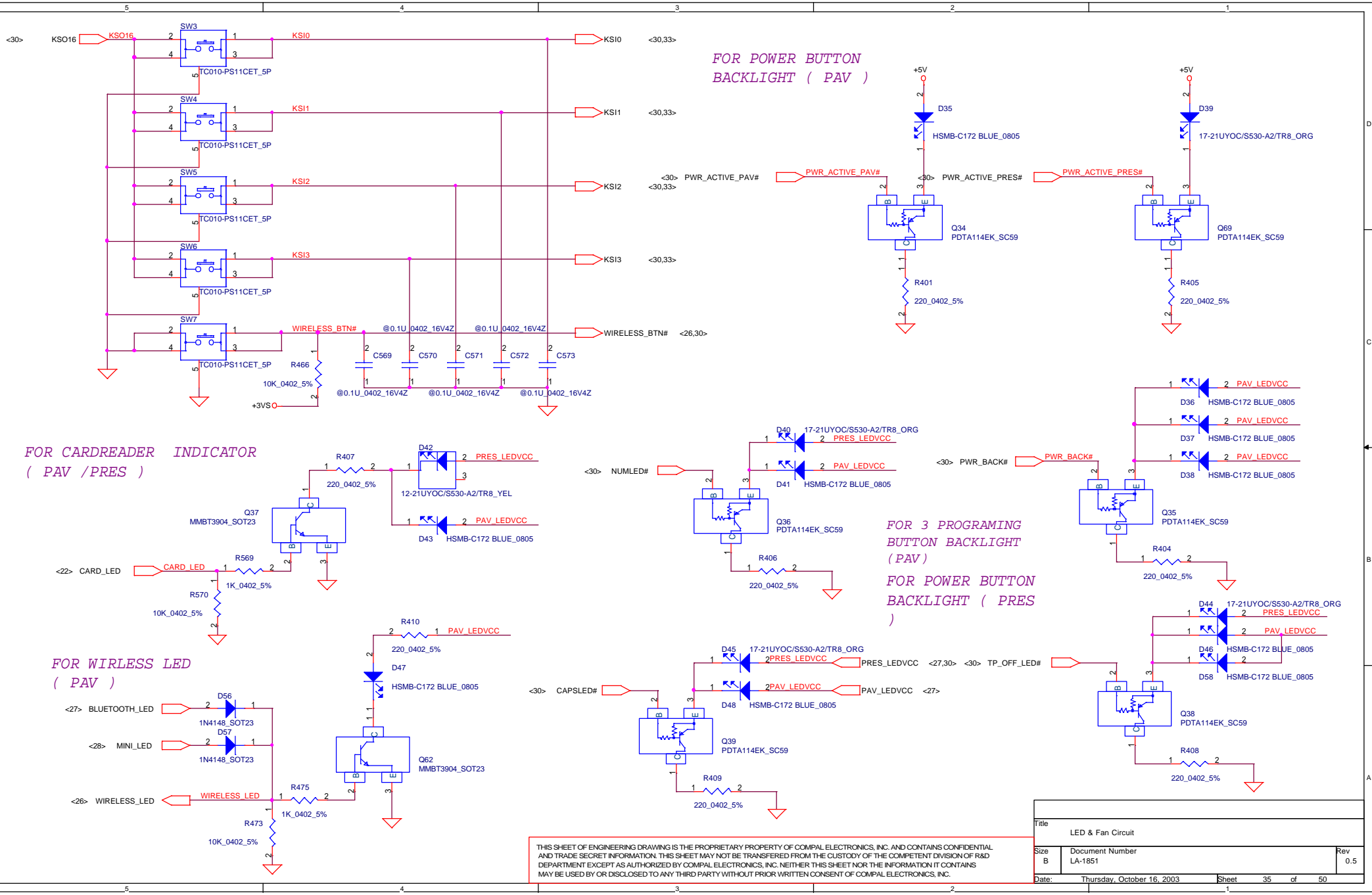


**EMI Requirement**



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<b>Compal Electronics, Inc.</b>		
<b>SPR Connector</b>		
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FOR POWER BUTTON  
BACKLIGHT ( PAV )

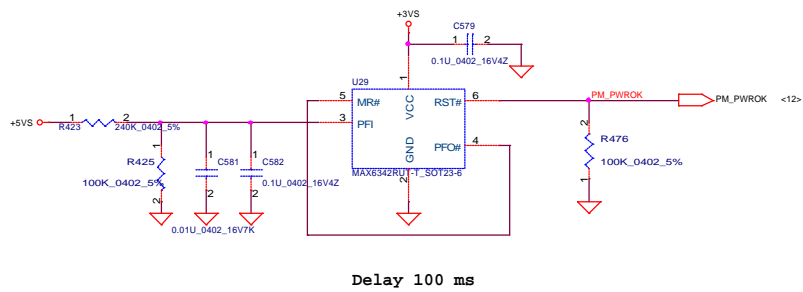
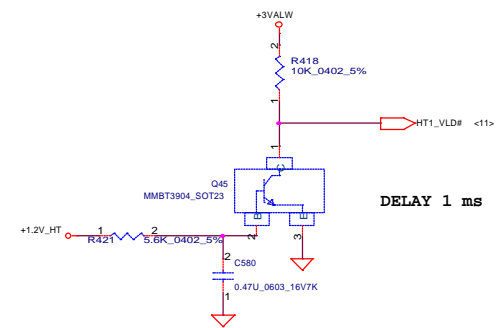
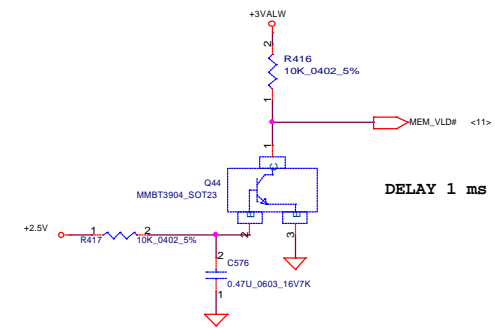
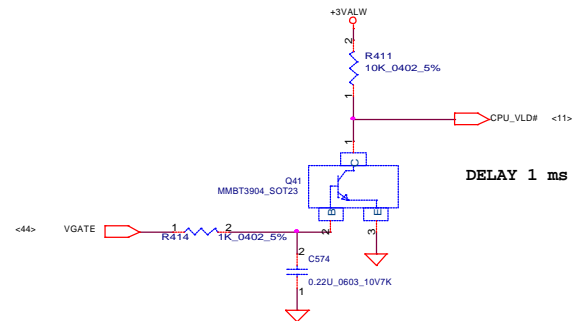
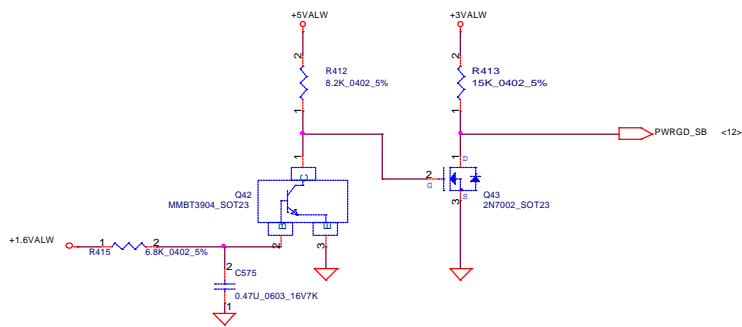
FOR CARDREADER INDICATOR  
( PAV /PRES )

FOR 3 PROGRAMING  
BUTTON BACKLIGHT  
( PAV )  
FOR POWER BUTTON  
BACKLIGHT ( PRES )

FOR WIRLESS LED  
( PAV )

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Title		
LED & Fan Circuit		
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Delay 100 ms

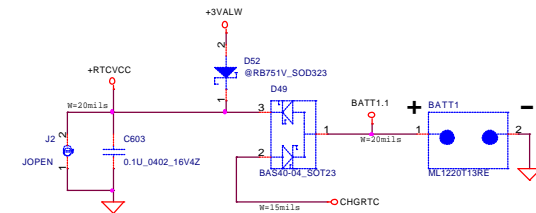
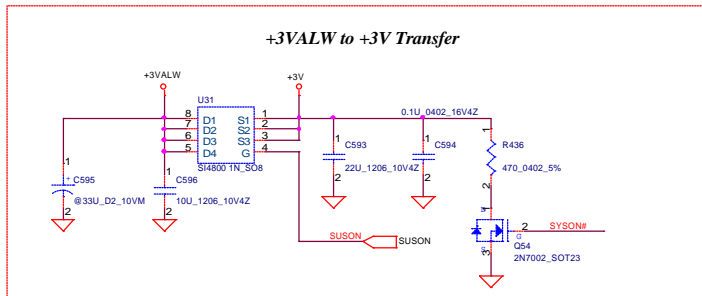
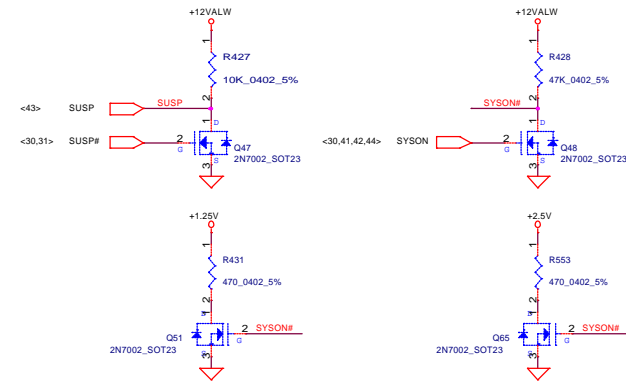
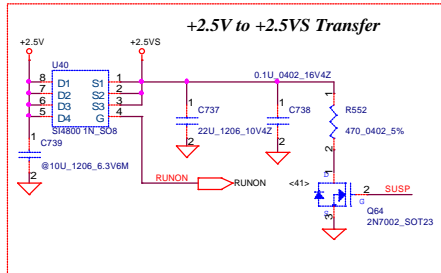
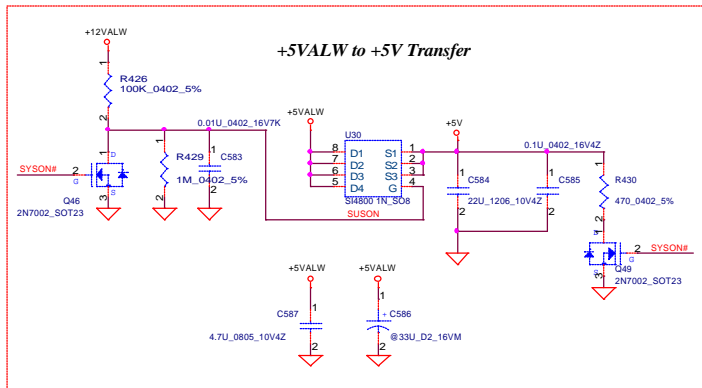
DELAY 1 ms

DELAY 1 ms

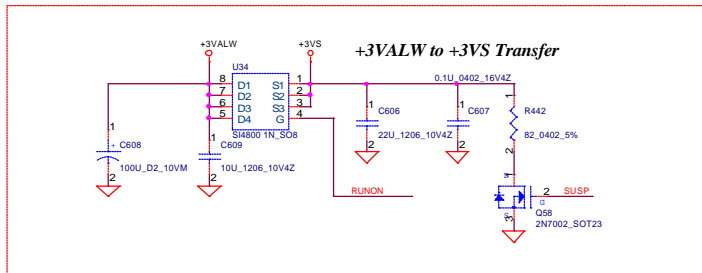
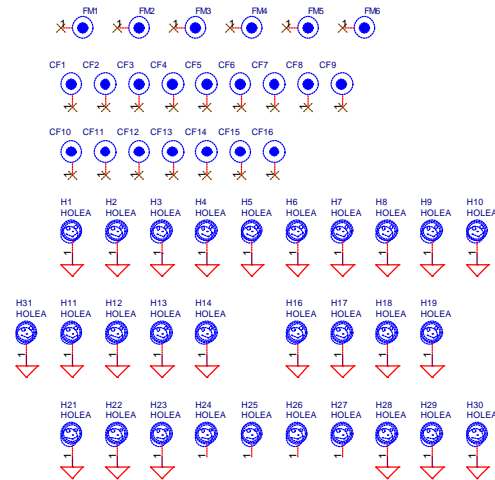
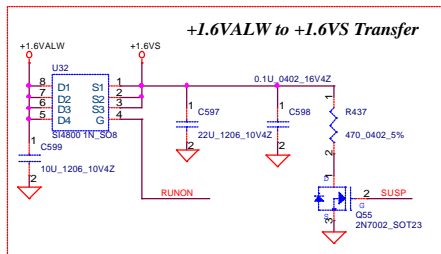
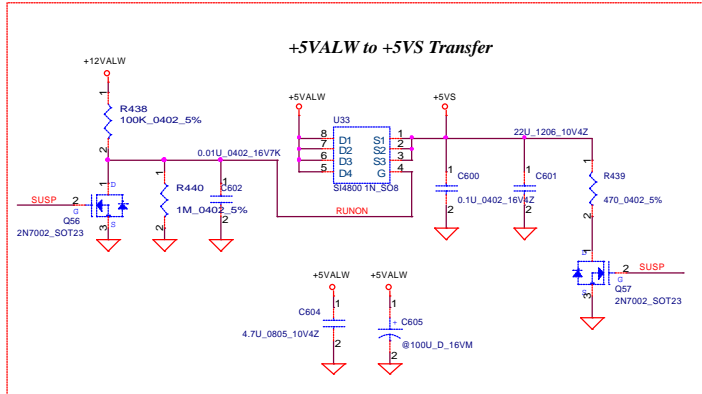
DELAY 1 ms

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<b>Compal Electronics, Inc.</b>	
<b>Power OK/Reset Conn.&amp; MUTE Switch</b>	
File	Document Number
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For customer request  
,they don't wanna  
charge RTC

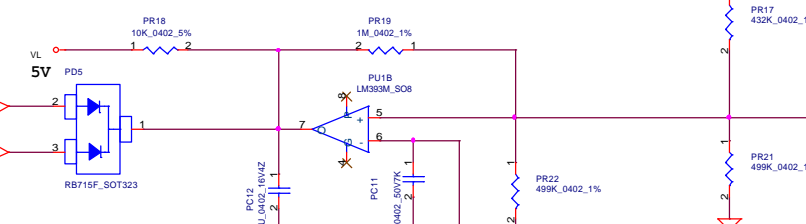
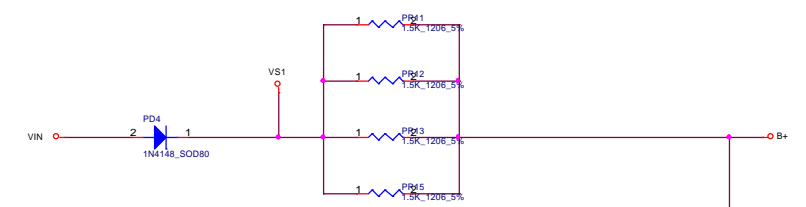
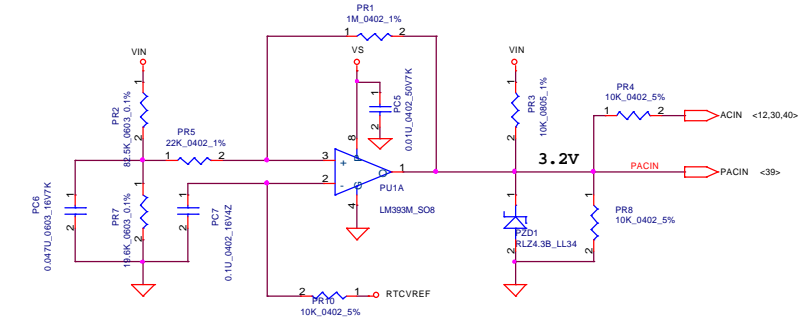


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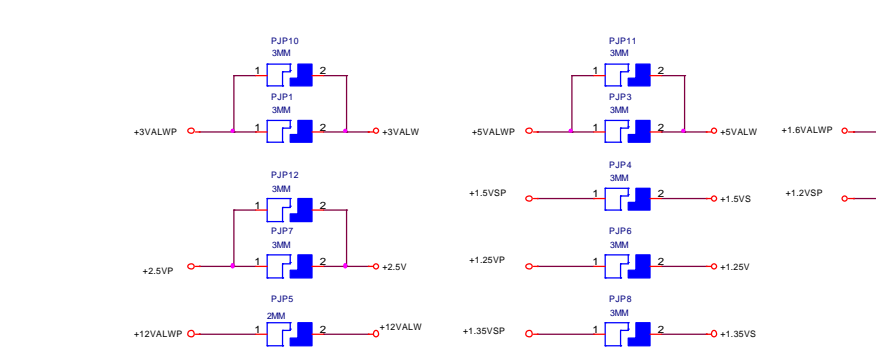
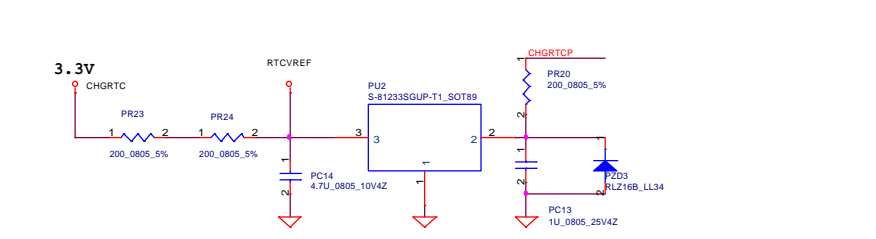
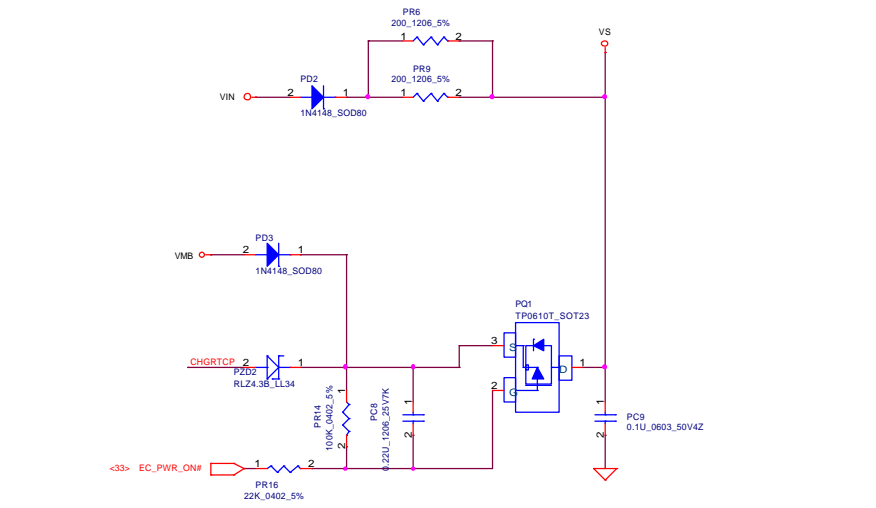
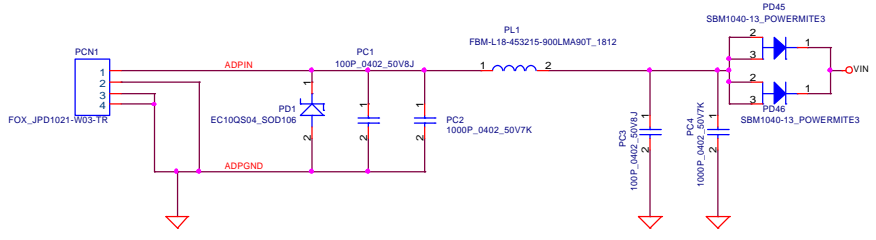
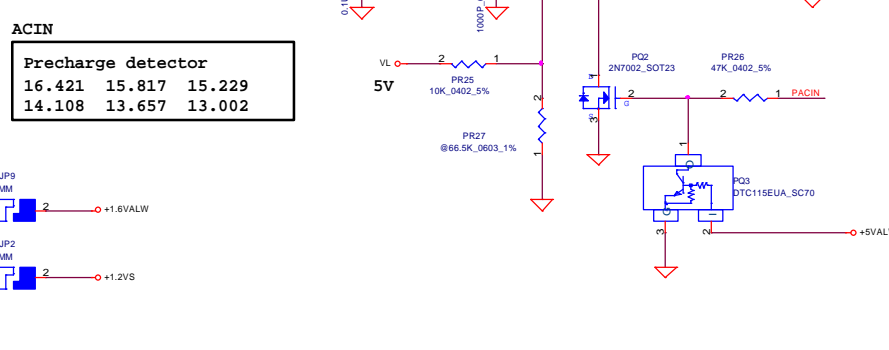
<b>Compal Electronics, Inc.</b>			
<b>DC/DC Circuit</b>			
File	Document Number	Rev	
	<b>LA-1851</b>	0.5	
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# Detector

**VIN detector**  
 17.945 17.343 16.757  
 17.372 16.782 16.207



**ACIN**  
 Precharge detector  
 16.421 15.817 15.229  
 14.108 13.657 13.002



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Compal Electronics, Inc.		
Title	Detector	
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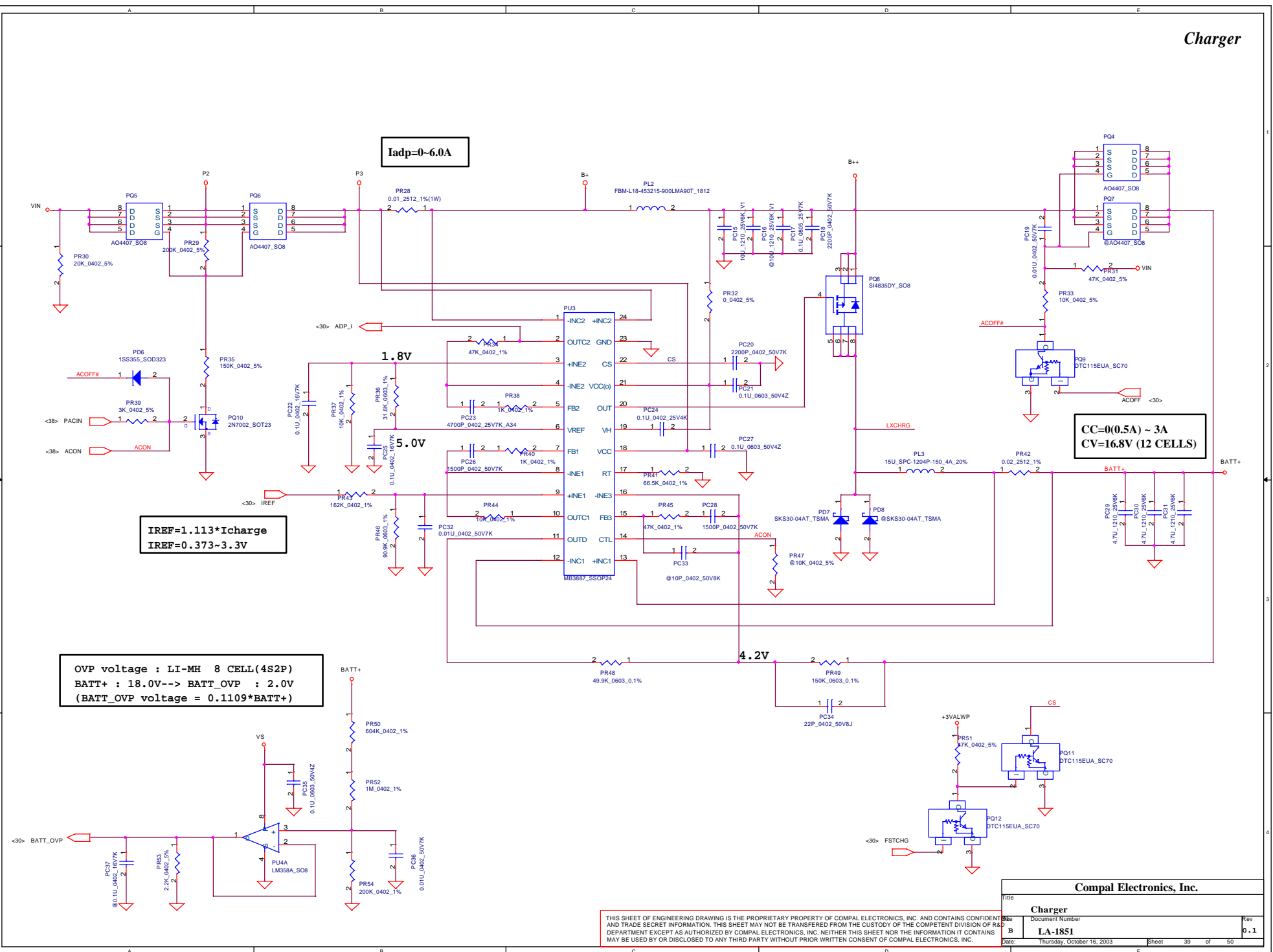
# Charger

**I<sub>adp</sub>=0-6.0A**

**CC=(0.5A) ~ 3A  
CV=16.8V (12 CELLS)**

**I<sub>REF</sub>=1.113\*I<sub>charge</sub>  
I<sub>REF</sub>=0.373~3.3V**

**OVP voltage : LI-MH 8 CELL(4S2P)  
BATT+ : 18.0V--> BATT\_OVP : 2.0V  
(BATT\_OVP voltage = 0.1109\*BATT+)**



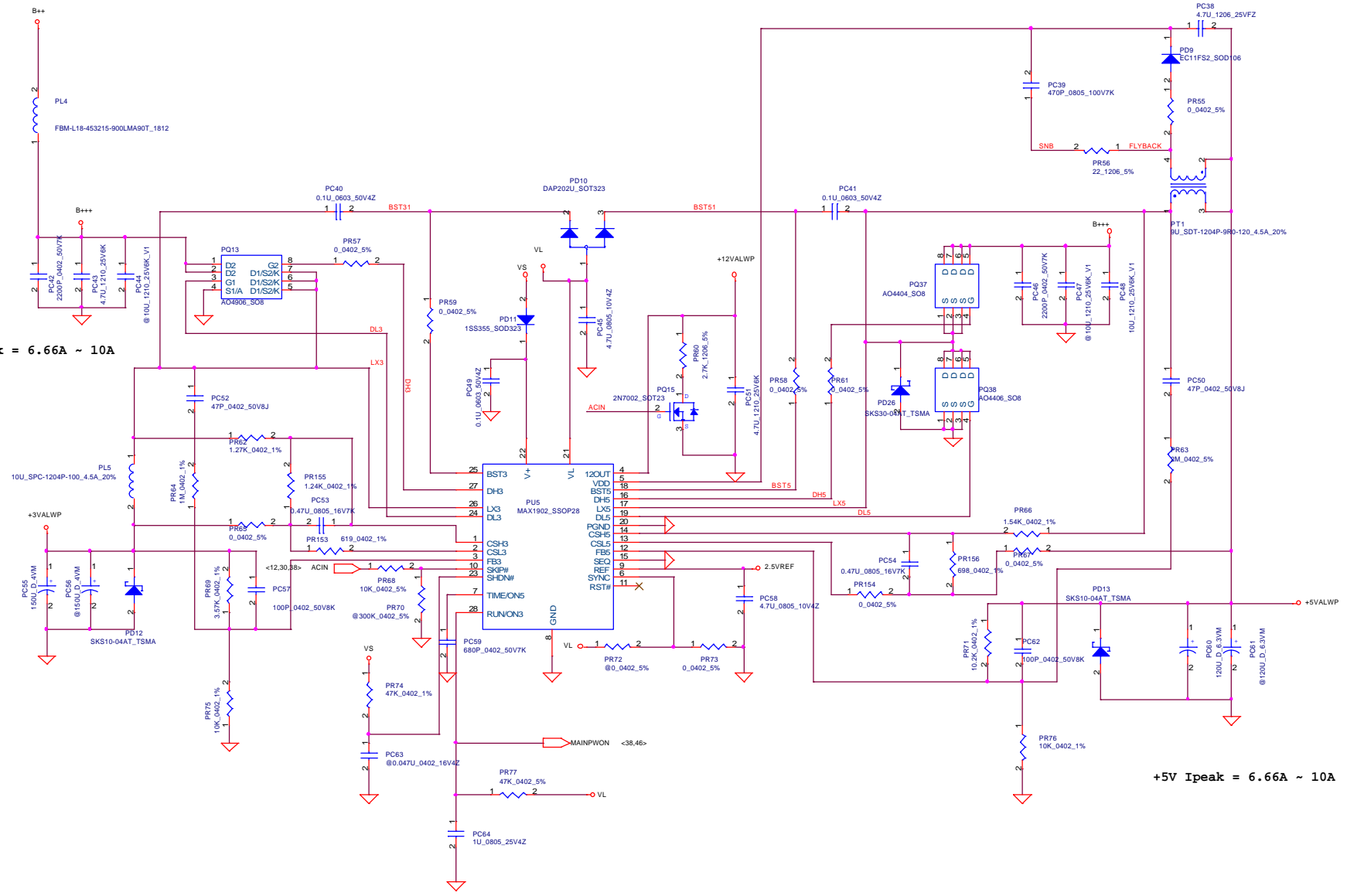
<b>Compal Electronics, Inc.</b>		
<b>Charger</b>		
File	Document Number	Rev
	<b>LA-1851</b>	<b>0.1</b>
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+3.3V/+5V/+12V

+3.3V Ipeak = 6.66A ~ 10A

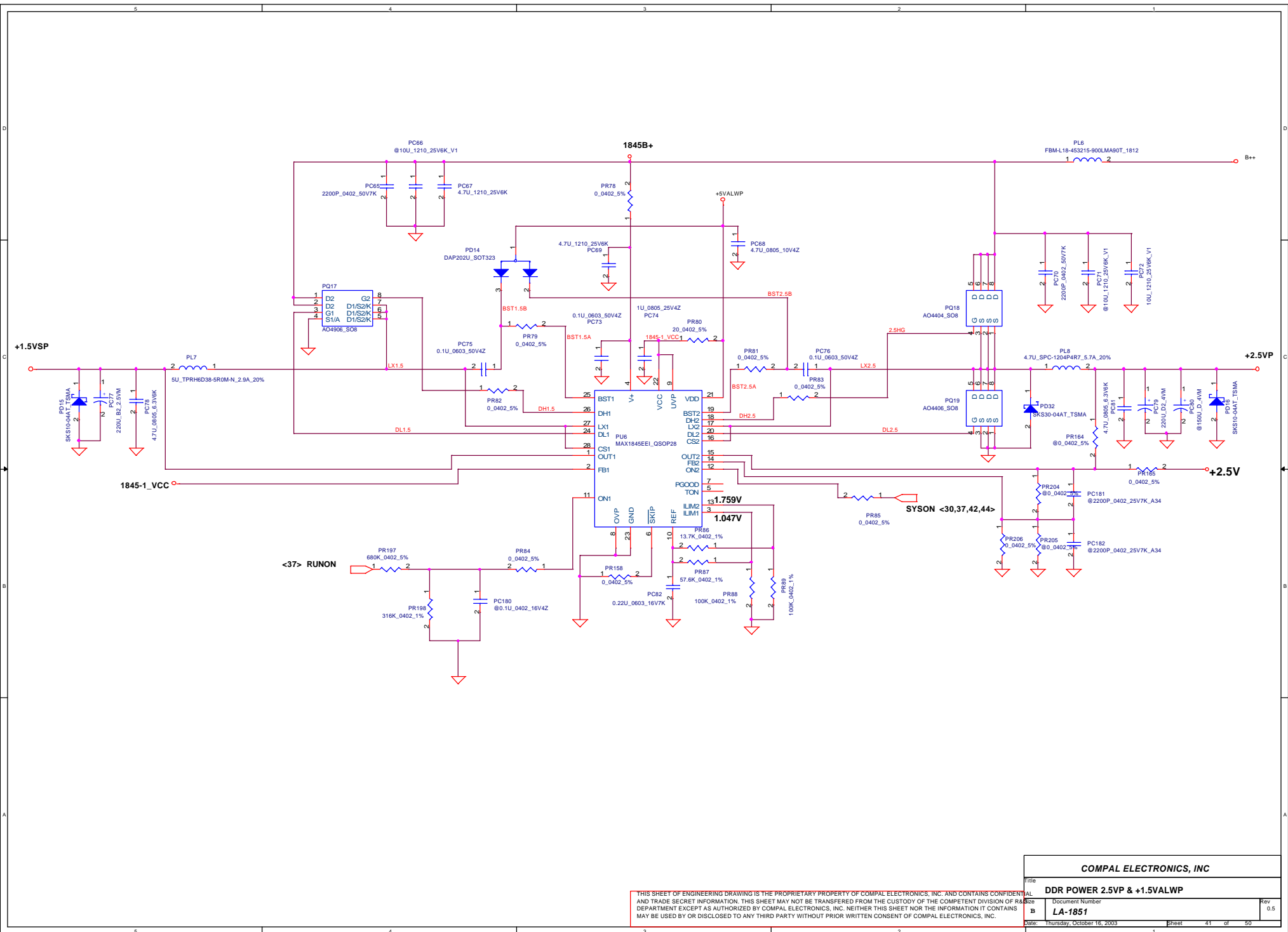
+5V Ipeak = 6.66A ~ 10A



<b>Compal Electronics, Inc.</b>	
Title	<b>3.3V / 5V / 12V</b>
Rev	Document Number
<b>B</b>	<b>LA-1851</b>
Date:	Thursday, October 16, 2003
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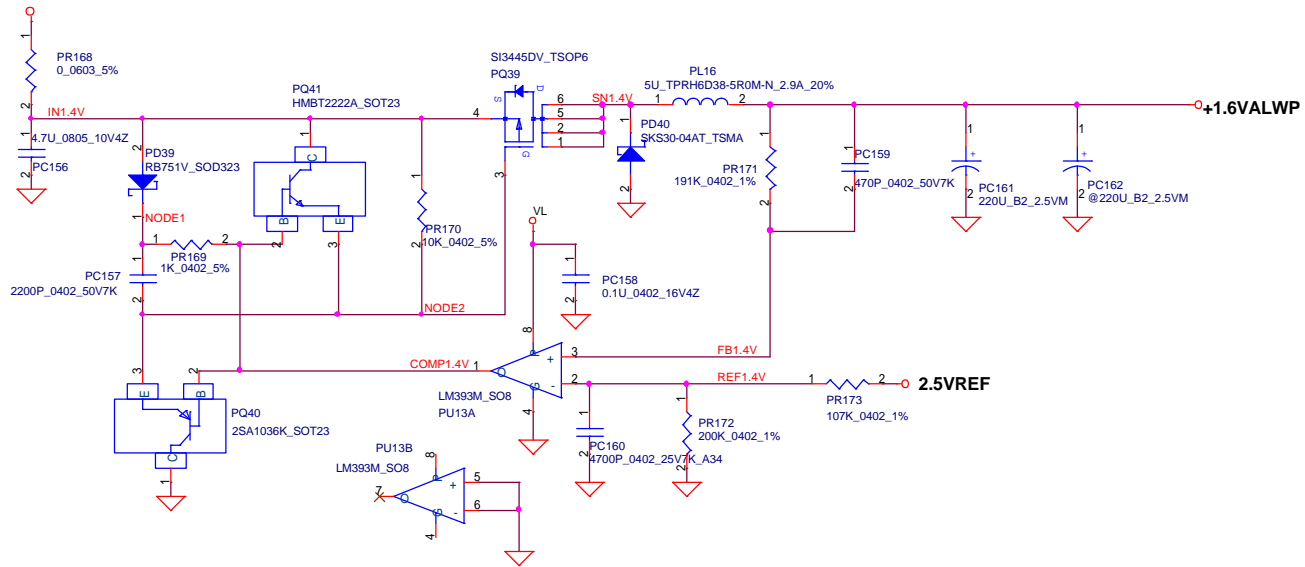




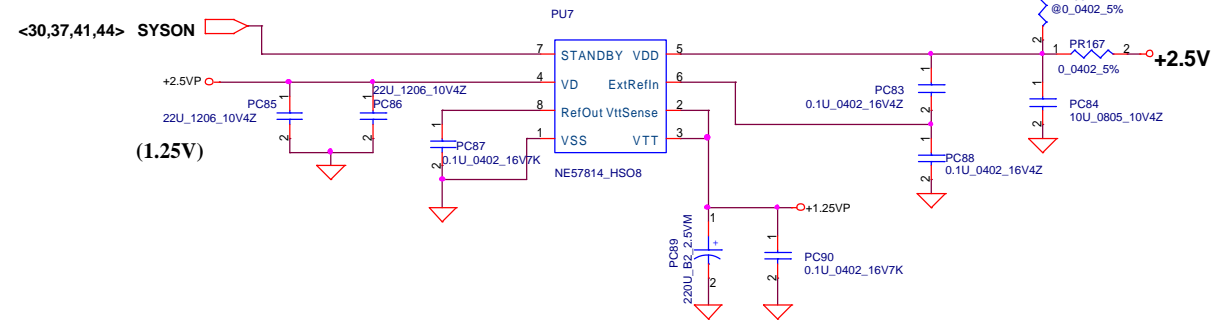
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<b>COMPAL ELECTRONICS, INC</b>		
Title		
<b>DDR POWER 2.5VP &amp; +1.5VALWP</b>		
Document Number		
<b>LA-1851</b>		
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Rev	0.5	

**+5VALWP**

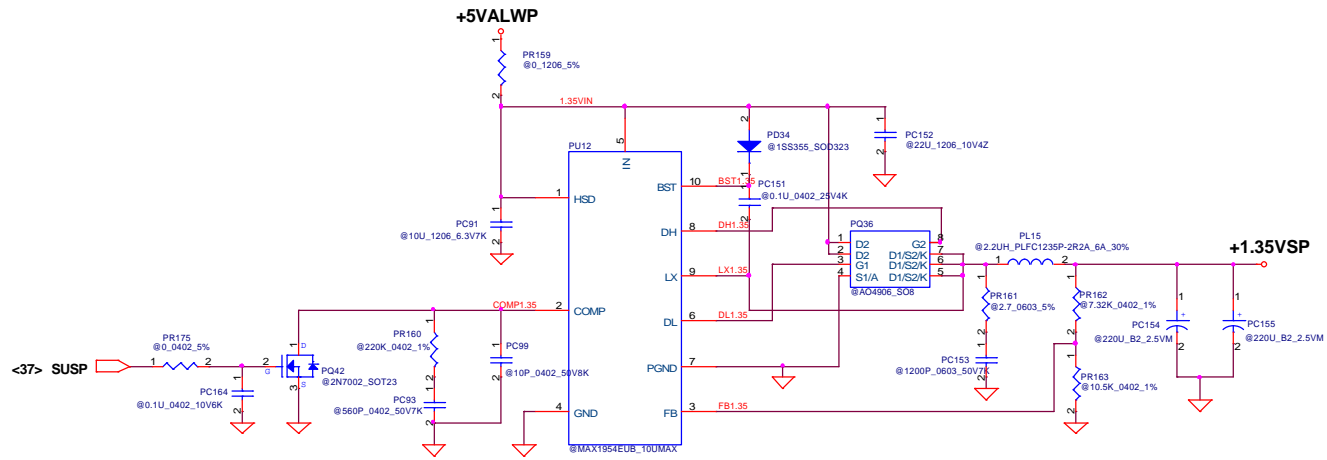
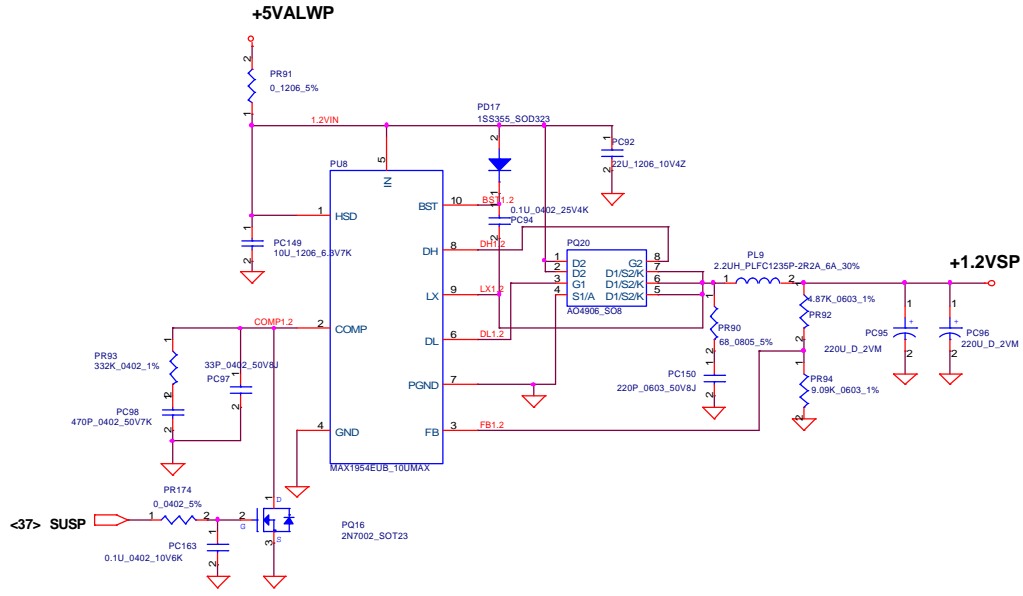


**+2.5VP**



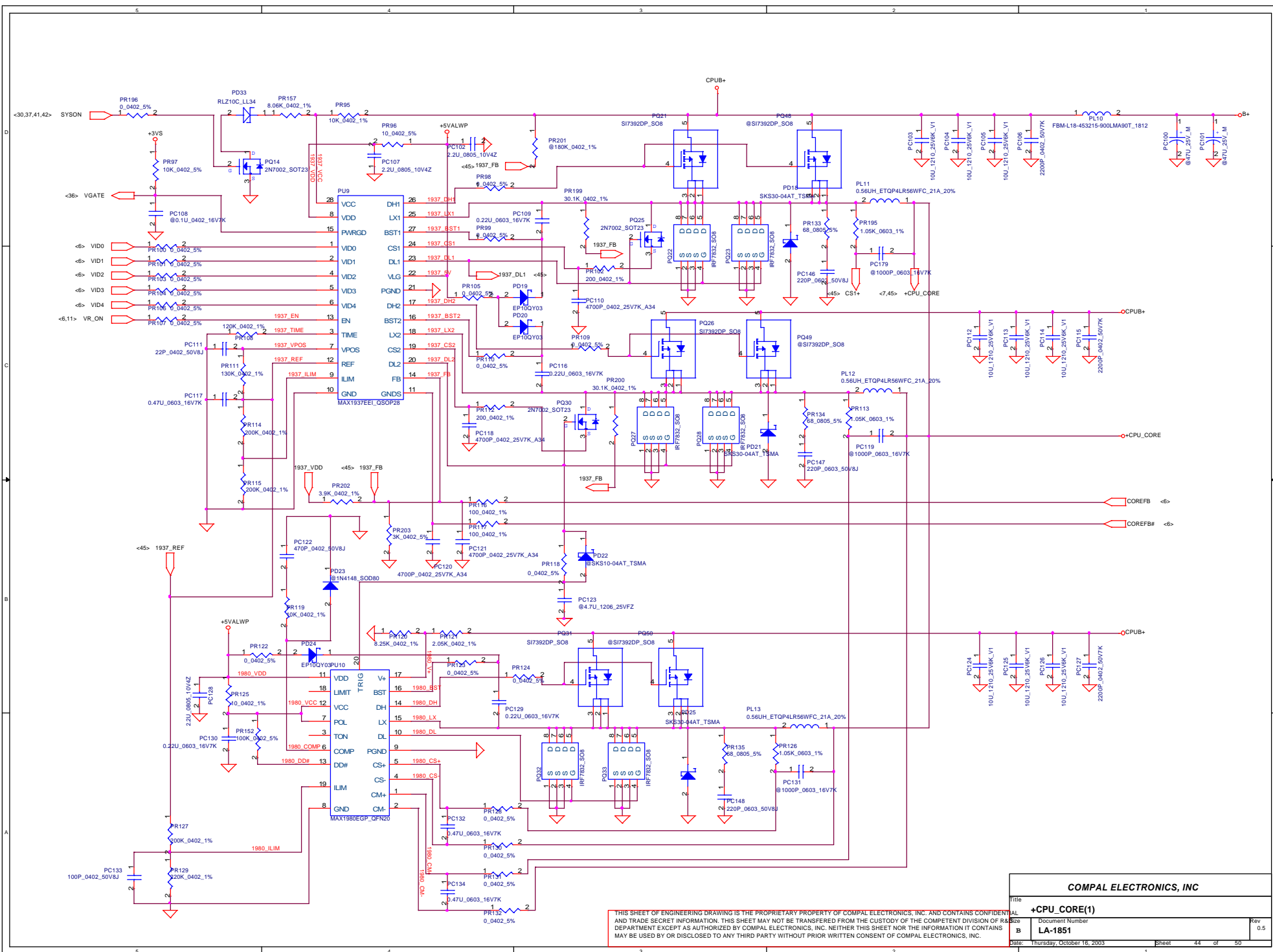
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COMPAL ELECTRONICS, INC		
Title		
<b>+1.6VALWP &amp; +1.25VP</b>		
Size	Document Number	Rev
B	LA-1581	0.5
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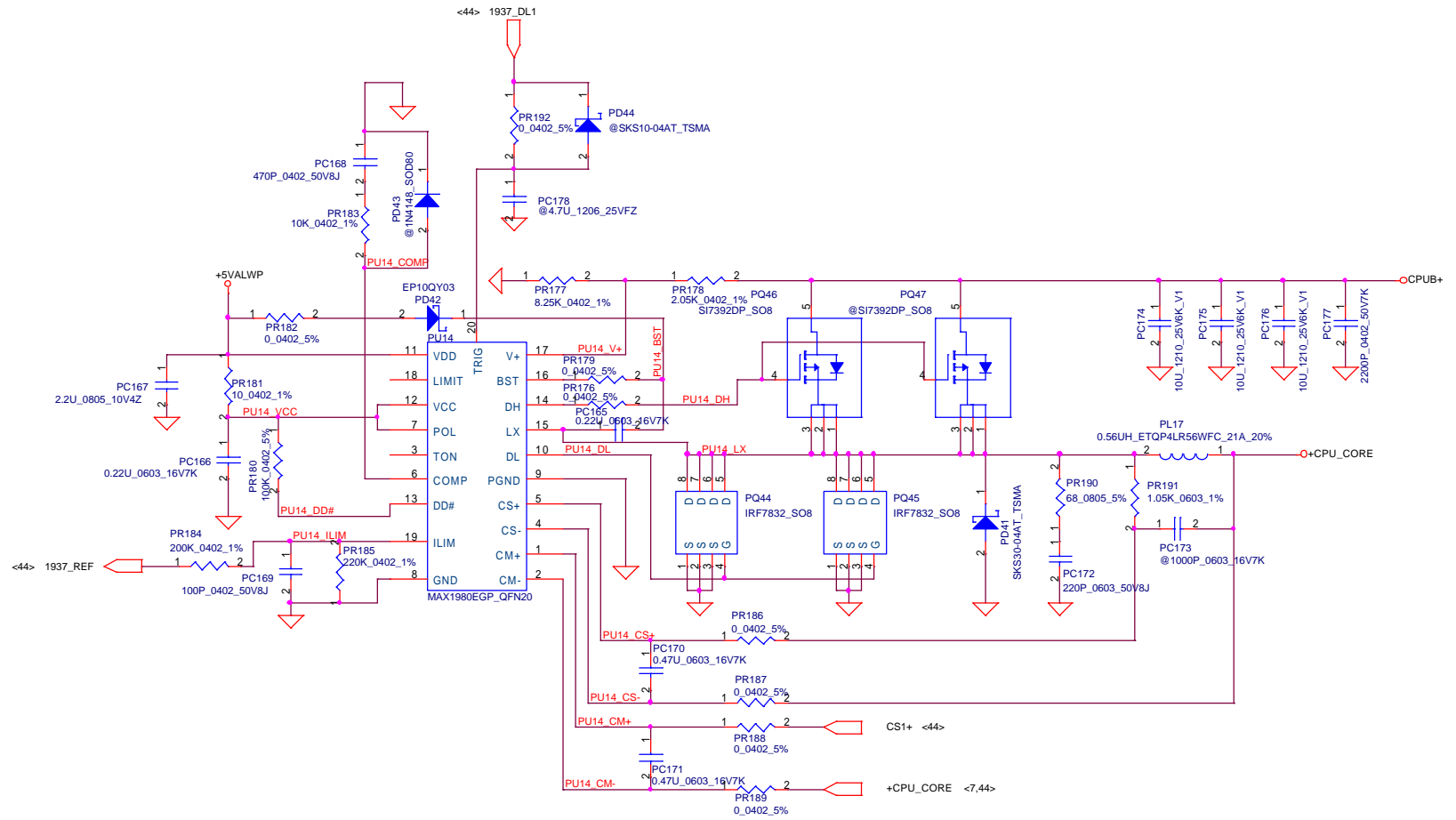
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<b>COMPAL ELECTRONICS, INC</b>	
File: <b>1.25V / VGA_CORE</b>	
Doc No: <b>LA-1851</b>	Rev: <b>0.5</b>
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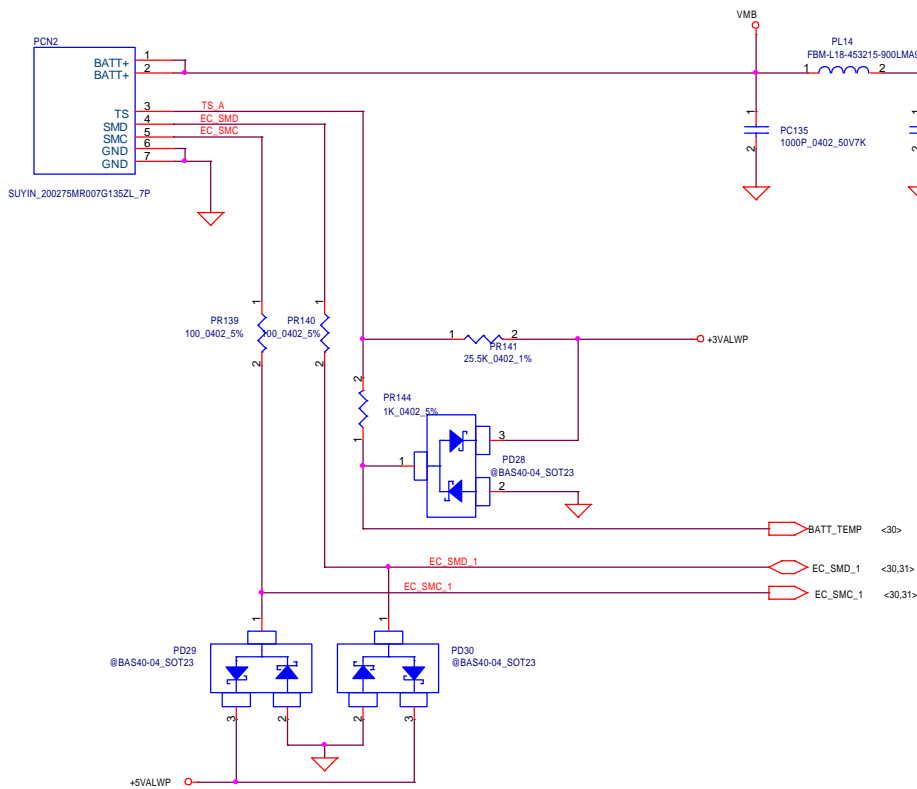
<b>COMPAL ELECTRONICS, INC</b>	
Title: <b>+CPU_CORE(1)</b>	
Document Number:	Rev: 0.5
<b>LA-1851</b>	
Date: Thursday, October 16, 2003	Sheet 44 of 50

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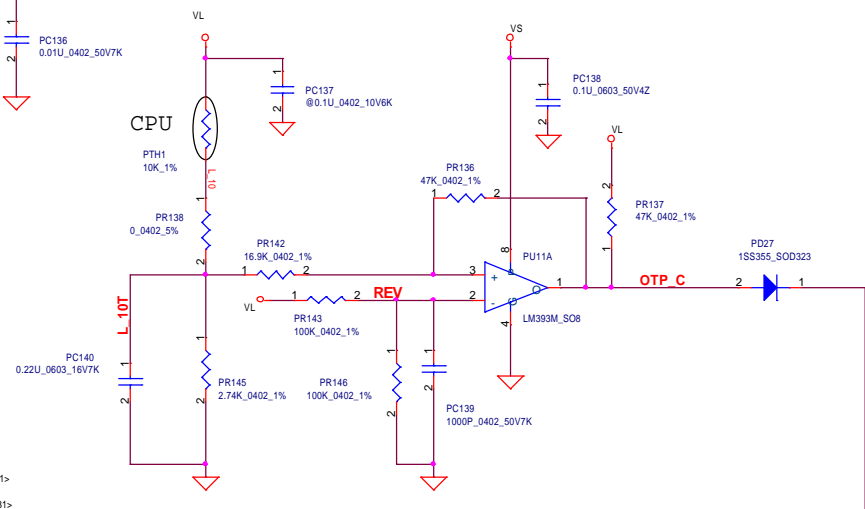


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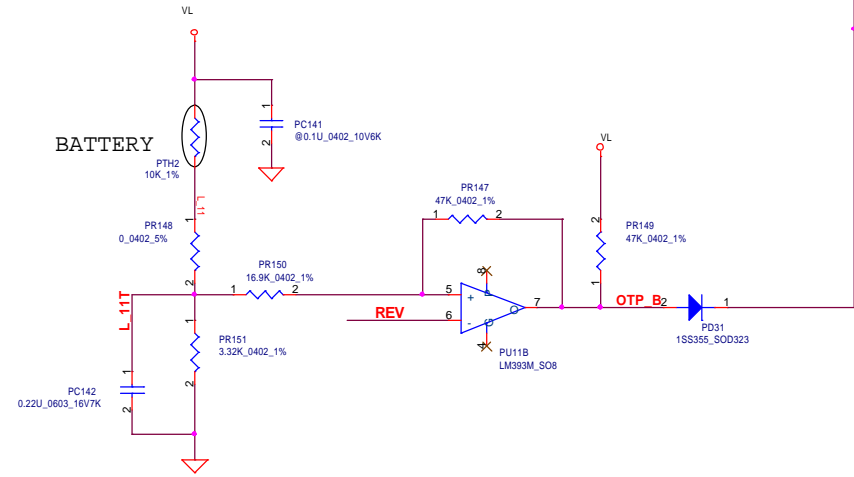
<b>COMPAL ELECTRONICS, INC</b>		
Title		
<b>+CPU_CORE(2)</b>		
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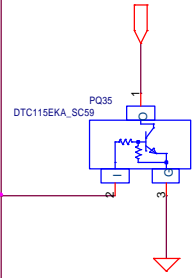
**PH1 under CPU botten side :**  
 CPU thermal protection at 90 +-3 degree C  
 Recovery at 50 +-3 degree C



**PH2 near main Battery CONN :**  
 BAT. thermal protection at 84 +-3 degree C  
 Recovery at 45 +-3 degree C



<38,40> MAINPWON



<b>COMPAL ELECTRONICS, INC</b>		
Title		
<b>BATTERY CONN / OTP/1.8V</b>		
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# POWER PIR LIST

PHASE	page	Reason for change	Modify list
DB2	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of DOCK issue	Change PR2 from 174K_0603_1% to 150K_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvement noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Fixed USB 1.1 rising/falling time error	P12	Delete C785, C786, C787, C788, C789, & C790	0.3
2		Fixed TV-out no display	P14	Swap TV_CRMA and TV_COMPS	0.3
3		Prevent PCI1620 latched up	P22	Reserve G_RST# to pin U37.C11	0.3
4		Design change (solve for HR60 audio issue)	P26	Move two load resistors from sub-board to M/B and swap JP17.2 and JP17.3	0.3
5		Supported wake up from TP	P27	Change TP connector JP26's power pin from +5VS to +5V	0.3
6		EMI required (solve for 48 MHz noise from FDD connector)	P32	Add CP11, CP12, CP13, and C801	0.3
7		Design change (TFDU6102 design guide)	P33	Delete C560 and C562 & add R586 Change C561 from 10uf to 4.7uf	0.3
8		EMI required (solve for 48 MHz noise from serial port)	P34	Add CP14, and CP15	0.3
9		ID required (for Pavillion)	P35	Add D58	0.3
10		EMI required	P25	Add L38, and L39	0.3
11		Add bypass cap. to solve for AC97 link cross a split plane	P27	Add C802, C803, C804, C805, and C806	0.3
12		Design change (reserve space for power placement and no need too many caps.)	P07	Delete C75, and C88	0.3
13		RealTech 8101L design guide	P20	Change R194 to 5.6K +/- 1%	0.3
14		Solve for SPDIF no output	P34	Delete C634	0.3
15		CPU_CLK is current drive from CK8. So, delete damping resistors.	P11	Change R69, and R70 from 15 ohm to 0 ohm	0.3
16		Solve for burst frequency error	P14	Change C642, and C643 from 18 pF to 22 pF	0.3
17		Solve for chrominance and burst level	P18	Change L11, L12, and L13 to 1.8uH	0.3

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		AMD change Tdiode spec up to 127 degree	P4	Change U3 from MAX6649 to ADM1032	0.4
2		Support wake from Lan	P20	Populate R188	0.4
3		To avoid PCI1620 unknow action	P22	Reserve R591	0.4
4		To restrain audio noise	P25	Change R267 pull up to +5VAMP_CODEEC, and delete C626	0.4
5		USB_OC# high should be between 2.5V to 5.5V	P27	Change R310 and R315 to 10K / R314 and R319 to 20K	0.4
6		To detect FIR	P29	Add R592 and R593	0.4
7		TP should be pull up to +5V	P30	RP80 pull up to +5V	0.4
8		In order to compatible with NS97551 -- changing pin87 - 90 to GPIO	P30	BID routed from pin88 to pin82	0.4
9		In order to compatible with NS97551 -- removing +RTCVCC	P30	Add R594 and R595	0.4
10		To prevent noise generated from FAN to +5VS cause audio noise while shut down	P4	Delete D1 and D3 / add C3, C8, C612, and C614	0.4
11		Solve for PCI1620 working abnormal -- fine tune G_RST# timing	P22	Populate R587, delete R225, C410	0.4
12		Double mount issue, already exist at audio board.	P30	Delete D28 and D29	0.4
13		Fast power on for battery only	P33	Change R392 from 100K to 4.7K	0.4
14		Presario LED color should be amber	P35	Change D39, D40, D42, D44, and D45 from XX_GRN to XX_ORG	0.4
15		To develop S19182 max effect	P25	Change C438 from 0.01UF to 0.1UF	0.4
16		For EMI	P26	Add L40, L41, L42, and L43 / delete C473, C474, C475, and C476	0.4
17		For VGA HSYNC/VSYNC average peak to peak issue	P18	Add R159 and R160	0.4
18		For 512MB non-JEDEC module ( 16 chips )	P9	Change RP42, RP46, and R481 from 68 Ohm to 47 Ohm	0.4

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**Version change list (P.I.R. List)**

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		To use the same source as HR60	P4	Change U3 footprint to SOP8	0.5
2		To reset CK8 while boot up control by EC	P12	Add R97 to link EC_RSMRST# and PWRGD_SB	0.5
3		For EMI	P15	Change C648, C672, C685, C696, C699, C763, and C656 to 1000P Change C651, C673, C686, C697, C700, C764, C654, C733, C710, C730, C706, and C724 to 10P	0.5
4		To solve voltage level of HSYNC and VSYNC is over spec	P18	Add U46 and U47, and R596, R597, and R598 on CRT_HSYNC and CRT_VSYNC	0.5
5		Solve for data lost while transfer data from LAN	P20	Change U9 from NS0013 to NS0019	0.5
6		TI recommendation --- avoid unknow state while initiate	P22	Populate R591	0.5
7		Mechanical restricted area	P25	R263 and R264 change footprint to R_0402	0.5
8		For EMI	P25	L39 and R293 change to CHB1608U301_0402	0.5
9		For EMI	P26	L40, L41, L42, and L43 change to KC FBM-L11-201209-221LMAT_0805	0.5
10		nVIDIA recommendation for WOR	P27	Add U48, C807, R599, and R600	0.5
11		Due to MD_SPK is no longer use, so prevent input pin floating.	P25	Delete R287 and change R288 to 0_0402_5%. Also add C808.	0.5

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