

# Compal confidential

## Schematics Document

Mobile AMD S1G3 CPU with ATI  
RS880M(NB) & SB710(SB) core logic

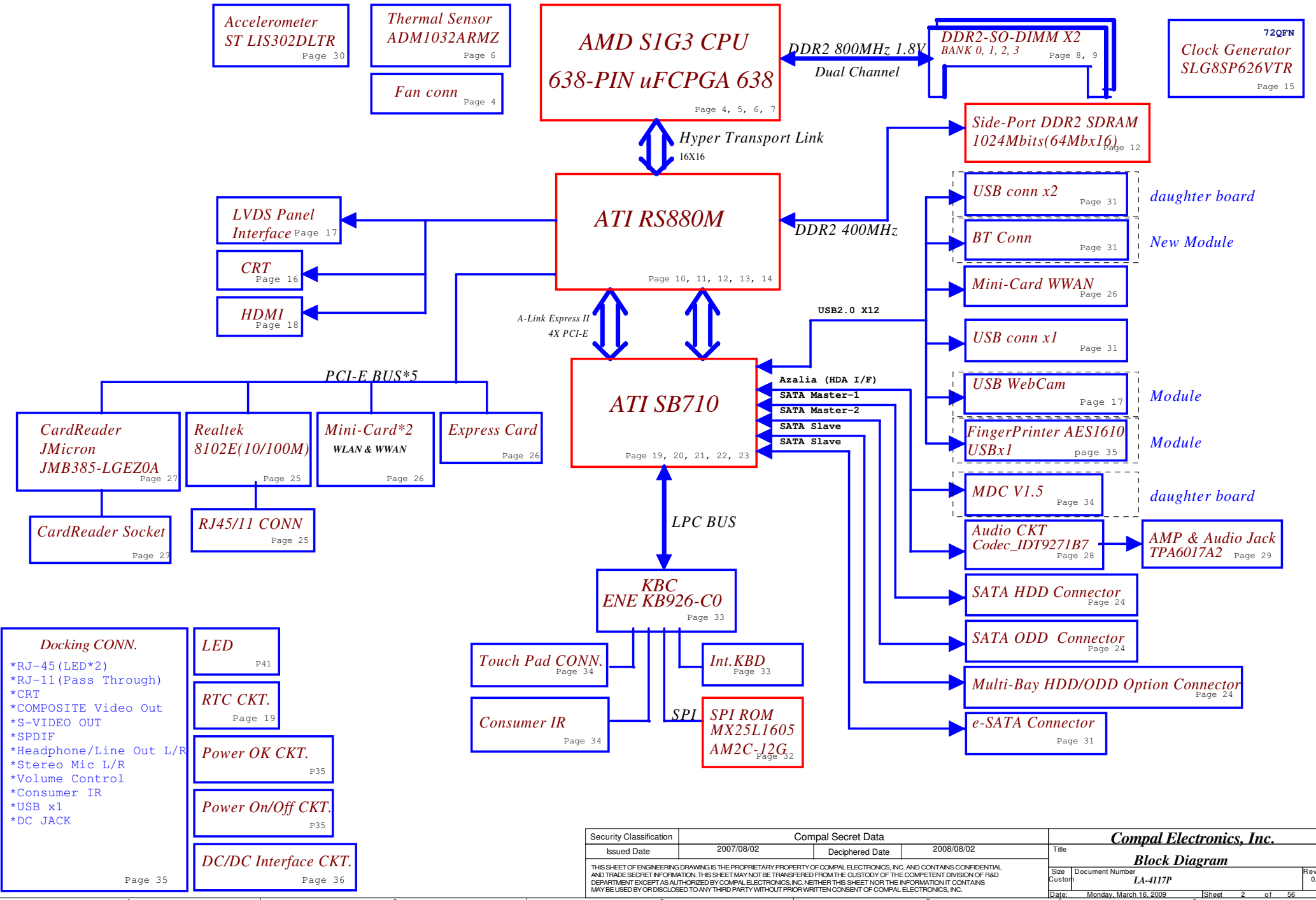
2009-03-15

REV: 0.3



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# Consumer AMD 14" UMA - Ripley 2.0 (NBW20)



- Docking CONN.**
- \*RJ-45 (LED\*2)
  - \*RJ-11 (Pass Through)
  - \*CRT
  - \*COMPOSITE Video Out
  - \*S-VIDEO OUT
  - \*SPDIF
  - \*Headphone/Line Out L/R
  - \*Stereo Mic L/R
  - \*Volume Control
  - \*Consumer IR
  - \*USB x1
  - \*DC JACK
- Page 35

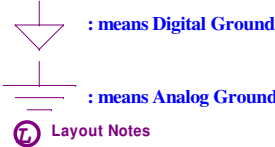
- LED** P41
- RTC CKT.** Page 19
- Power OK CKT.** P35
- Power On/Off CKT.** P35
- DC/DC Interface CKT.** Page 36

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				<b>Block Diagram</b>		
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**Voltage Rails**    O MEANS ON    X MEANS OFF

power plane	+B	+5VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE
		+3VALW		+VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
State				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

**Symbol Note :**



Please see VGA@ as no install. No support RX780M.

⊖ : Question Area Mark.(Wait check)

- \*\*\* as default BOM setting
- \*PA@ : means install when Ripley PA.
- PR@ : means install when Ripley PR.
- RM@ : means install when Rachman.
- \*RP@ : means install when Ripley.
- SIDE@ : means install when SidePort support.
- @ : means just reserve , no build
- 45@ : Install when 45 level Assy

R3 NB and SB: RS780R3@,SBR3@  
 R1 NB and SB: RS780R1@,SBR1@

**1.1**

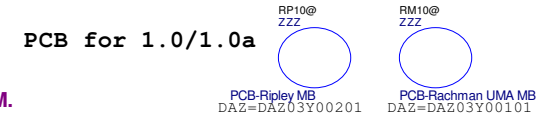
For Riply PA-> PA@, RP@,RPZ@  
 For Riply PR-> PR@, RP@, PRM@,RPZ@  
 For Rachman UMA-> RM@, PRM@,RMZ@

**2.0**

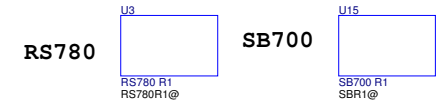
For Riply PA-> PA@/RP@/RPZ@  
 For Rachman UMA-> RM@/PRM@/RMZ@

**1.0/1.0a**

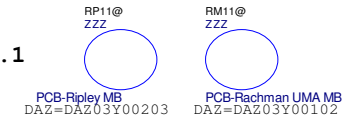
For Riply PA-> PA@, RP@  
 For Riply PR-> PR@, RP@, PRM@  
 For Rachman UMA-> RM@, PRM@



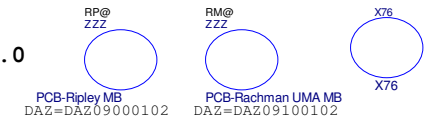
RP11@,RM11@:For 1.A PCB  
 RP10@,RM10@:For 1.0 PCB.



**PCB for 1.1**



**PCB for 2.0**



**SMBUS Control Table**

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI_CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	V CPU	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V ADM1032	X	X	X	X	X	X
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	X
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	V
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X

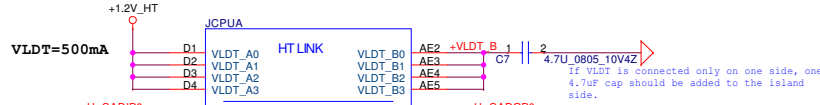
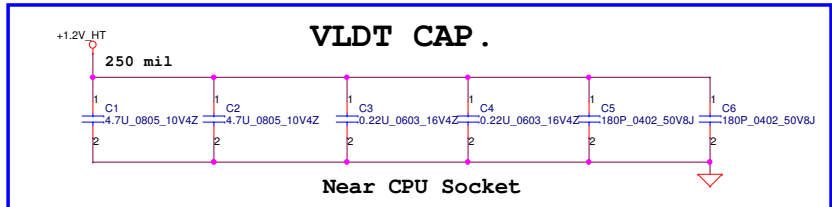
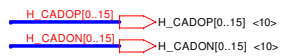
**I2C / SMBUS ADDRESSING**

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

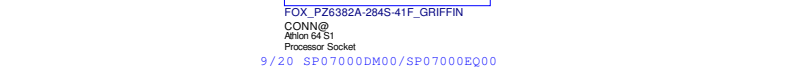
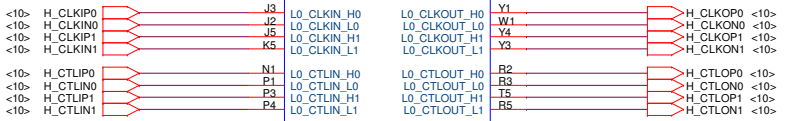
**EC SM Bus1 address      EC SM Bus2 address**

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	CPU	98H	1001 100X b
24C16	A0H	1010 000X b	ADI1032-2 CPU	9AH	1001 101X b

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			Sheet 3 of 56	Rev 0.3

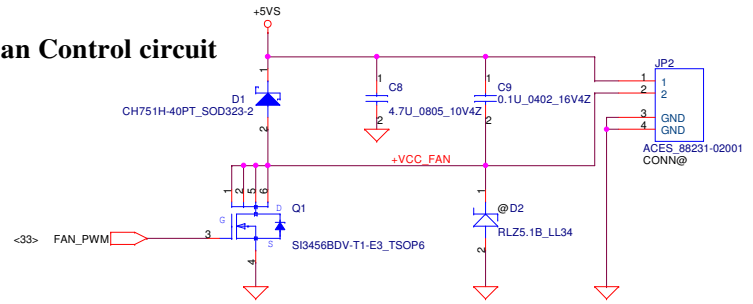


H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	Y1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15



FOX\_PZ6382A-284S-41F\_GRIFFIN  
 CONN@  
 Athlon 64 S1  
 Processor Socket  
 9/20\_SP07000DM00/SP07000EQ00

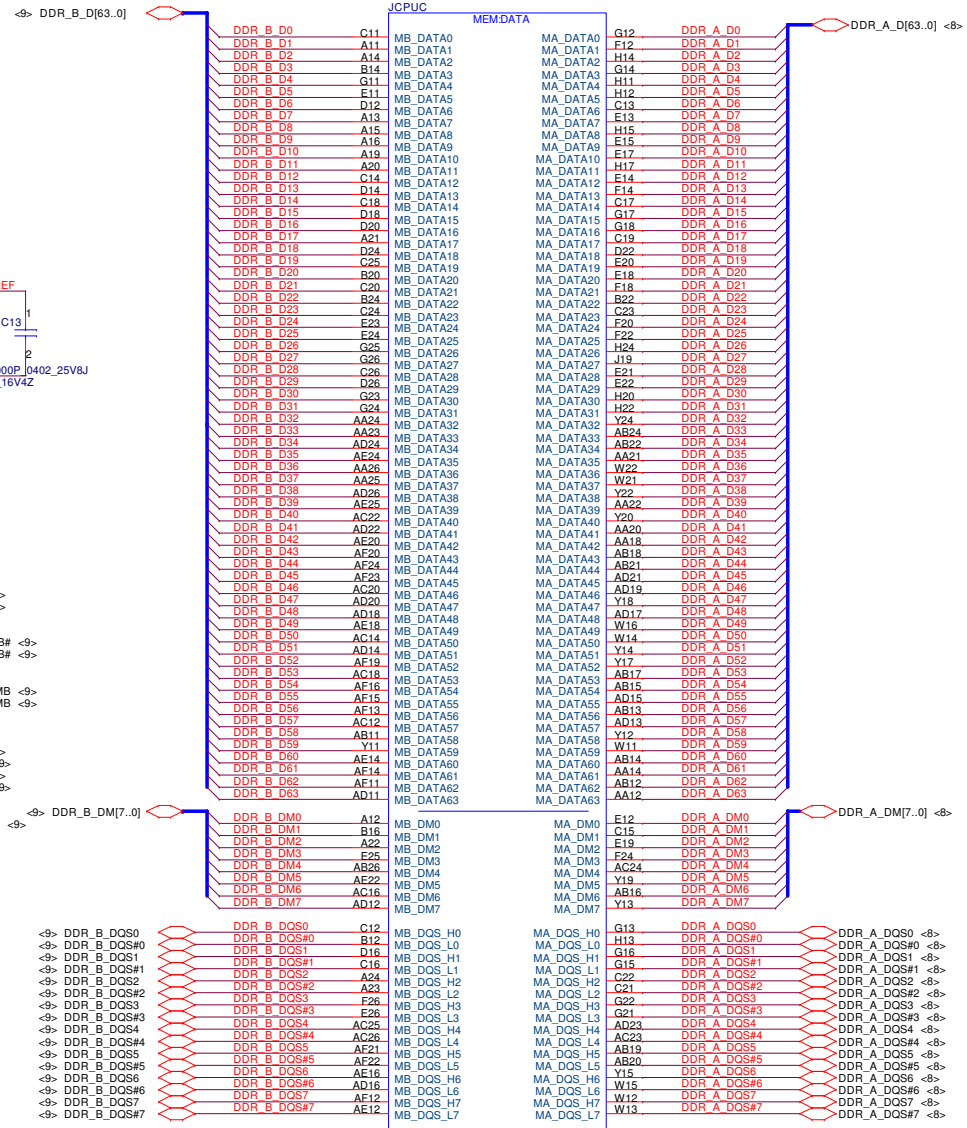
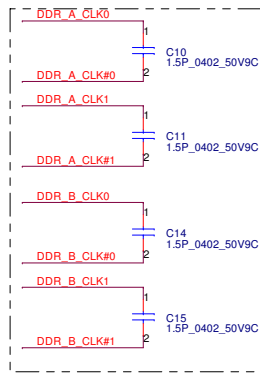
**PWM Fan Control circuit**



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# Processor DDR2 Memory Interface

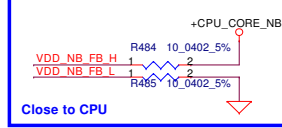
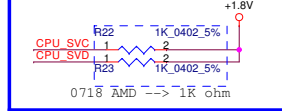
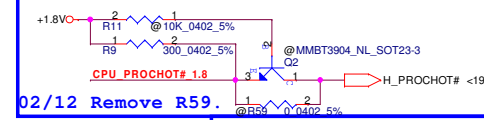
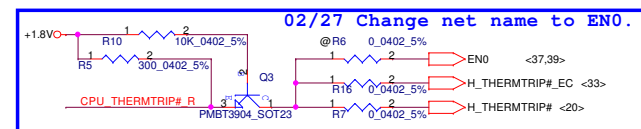
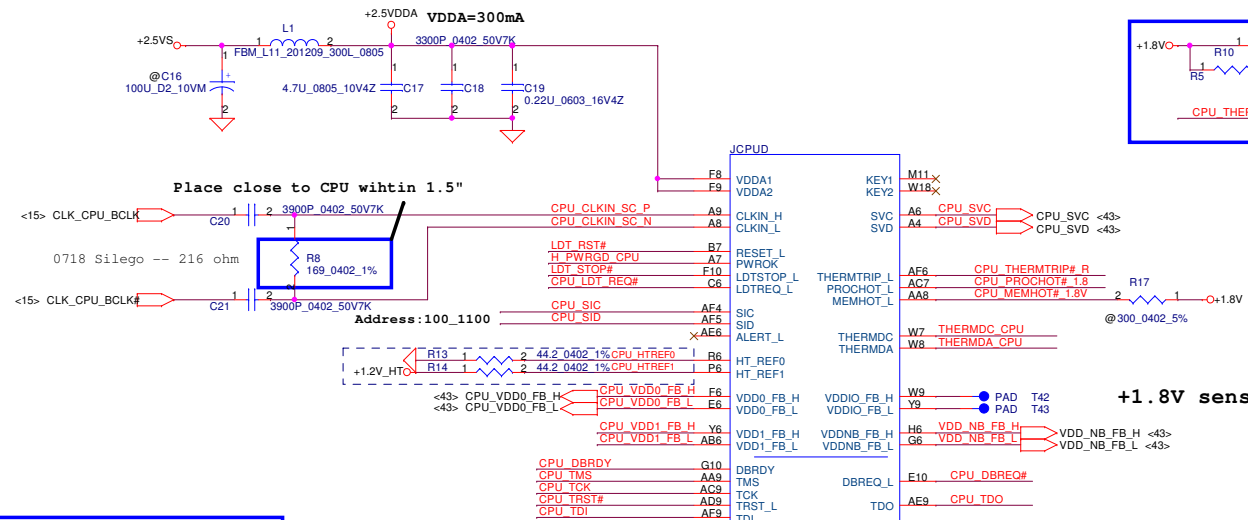
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



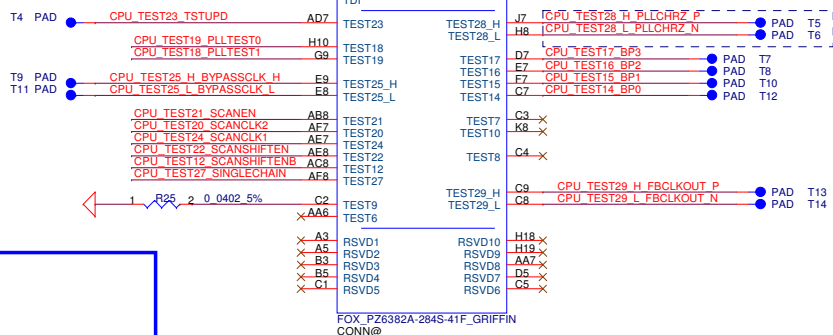
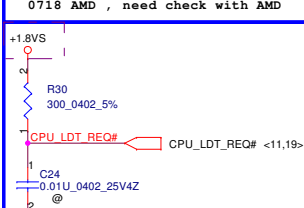
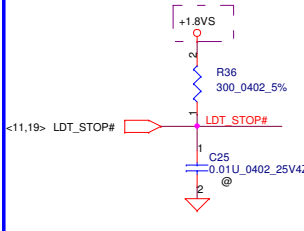
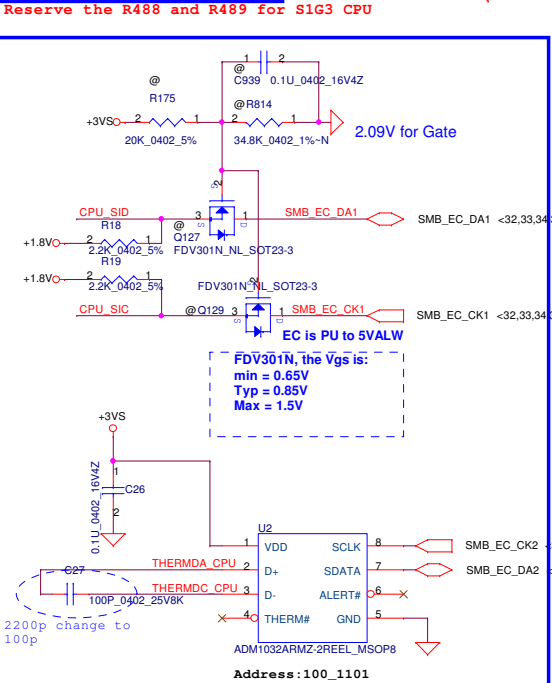
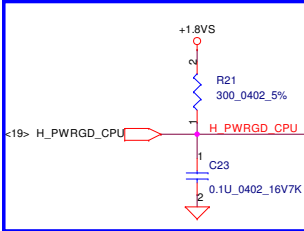
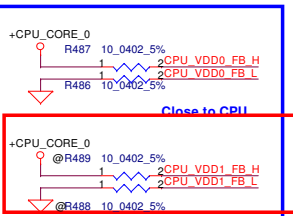
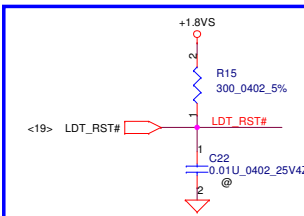
FOX\_PZ6382A-284S-41F\_GRIFFIN  
Athlon 64 S1  
Processor  
Socket  
CONN@

FOX\_PZ6382A-284S-41F\_GRIFFIN  
Athlon 64 S1  
Processor Socket  
CONN@

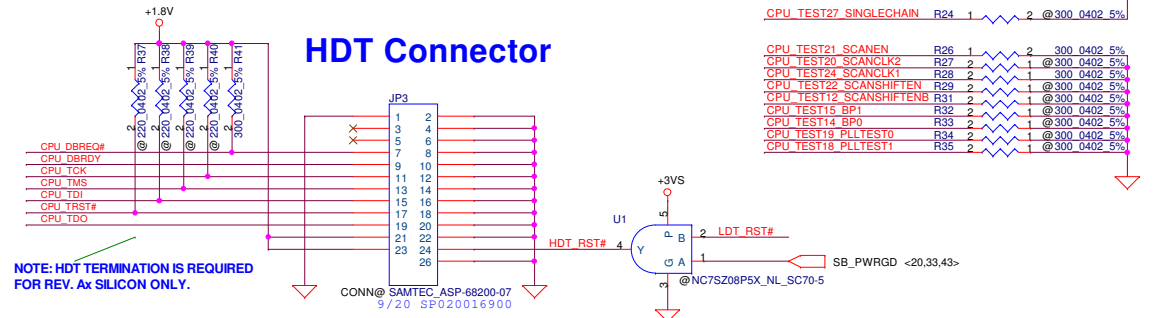
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+1.8V sense no support



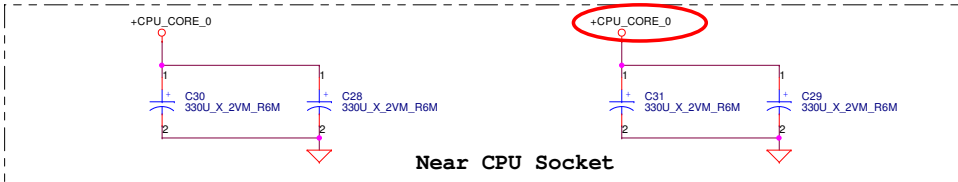
02/15 Follow Trinity design.  
02/15 Change R18 and R19 from 390 to 2.2K ohm.  
03/04 Reserve R175, R814, C939, Q127 and Q129.



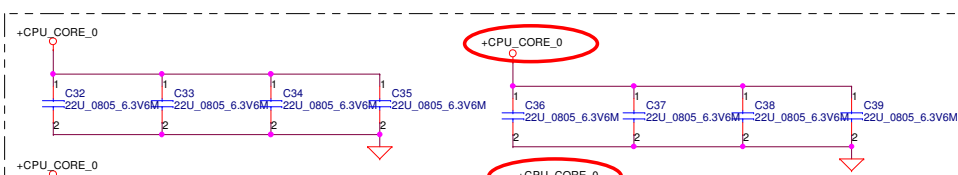
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# VDD (+CPU\_CORE) decoupling.

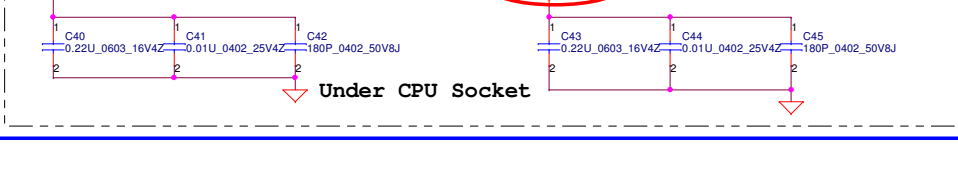
01/18 Change the net name from +CPU\_CORE\_1 to +CPU\_CORE\_0



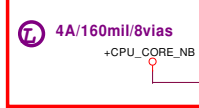
Near CPU Socket



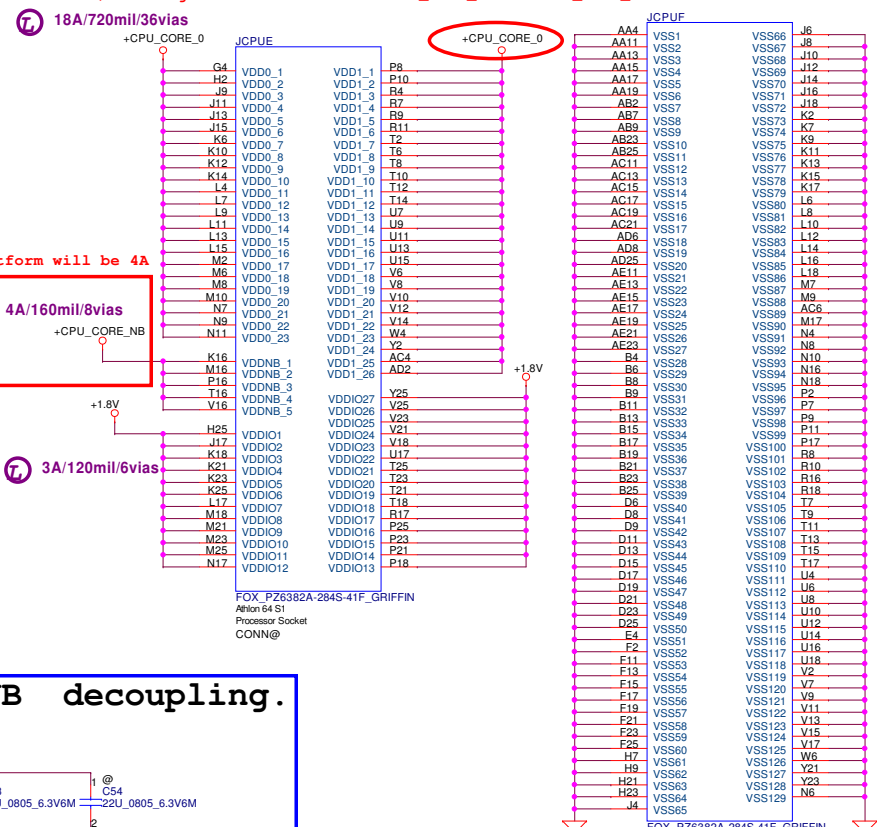
Under CPU Socket



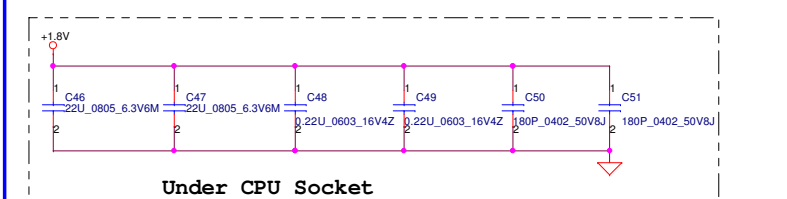
Tigris platform will be 4A



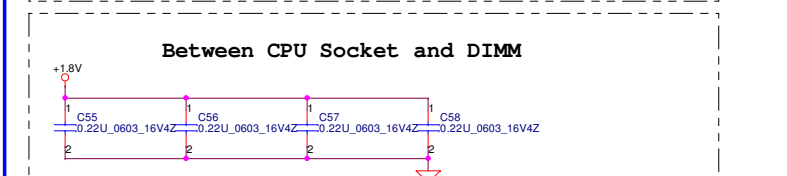
01/18 Change the net name from +CPU\_CORE\_1 to +CPU\_CORE\_0



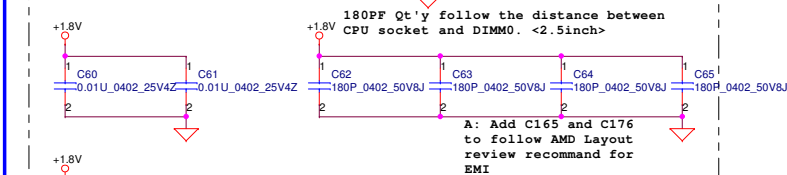
# VDDIO decoupling.



Under CPU Socket

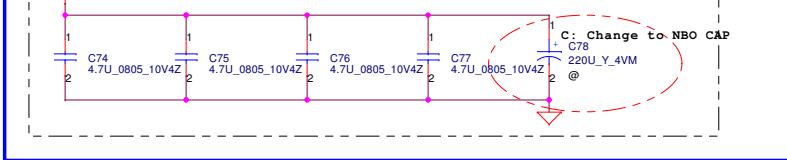


Between CPU Socket and DIMM

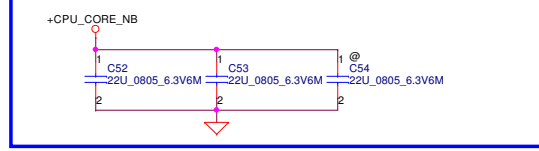


180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch>

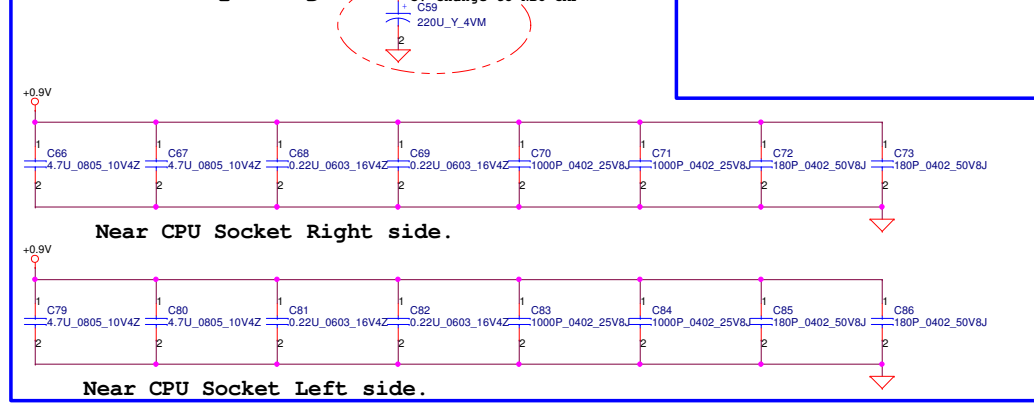
A: Add C165 and C176 to follow AMD Layout review recommend for EMI



# +CPU\_CORE\_NB decoupling.



# VTT decoupling.



Near CPU Socket Right side.

Near CPU Socket Left side.

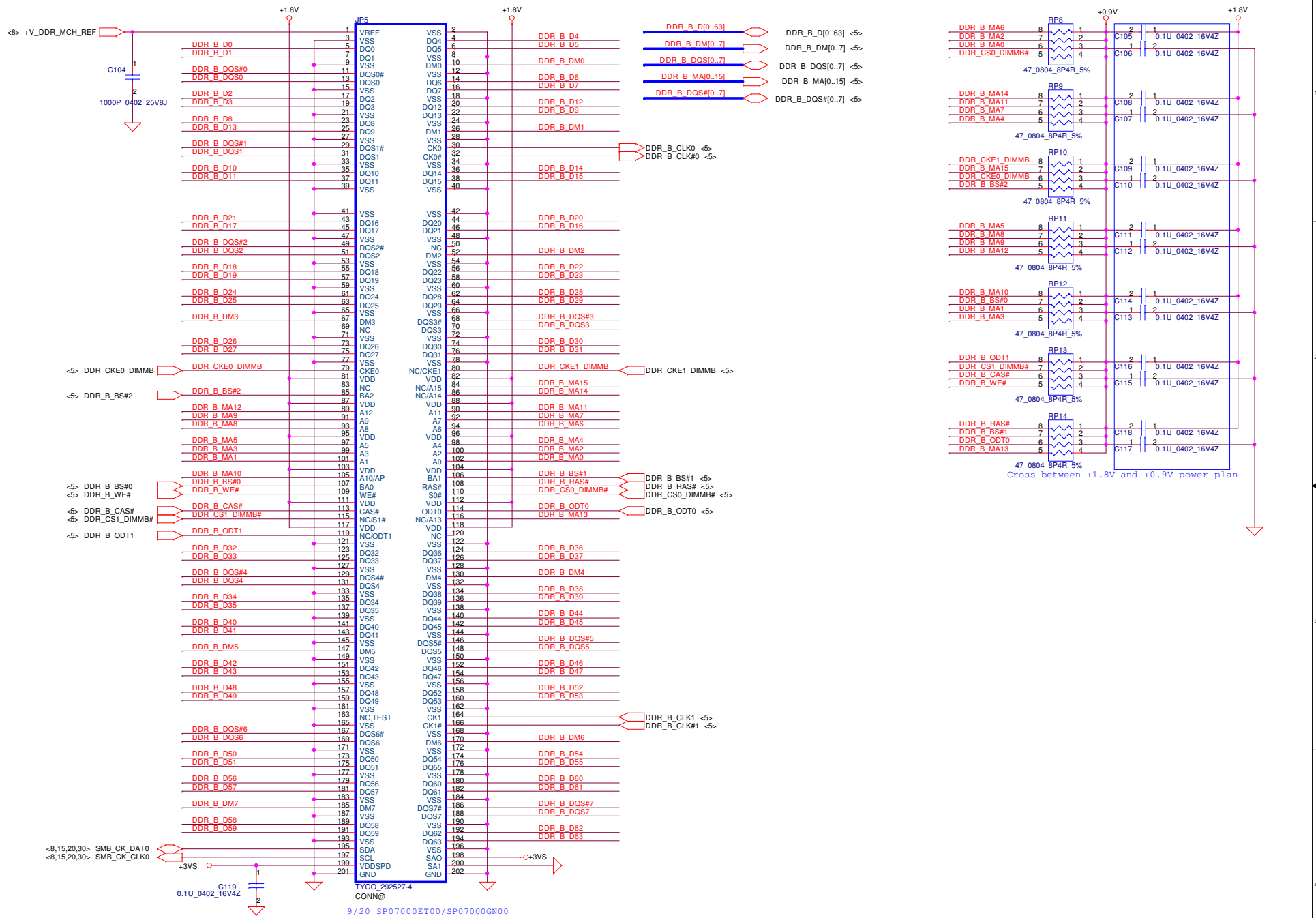
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AMD CPU SIG2 PWR & GND		
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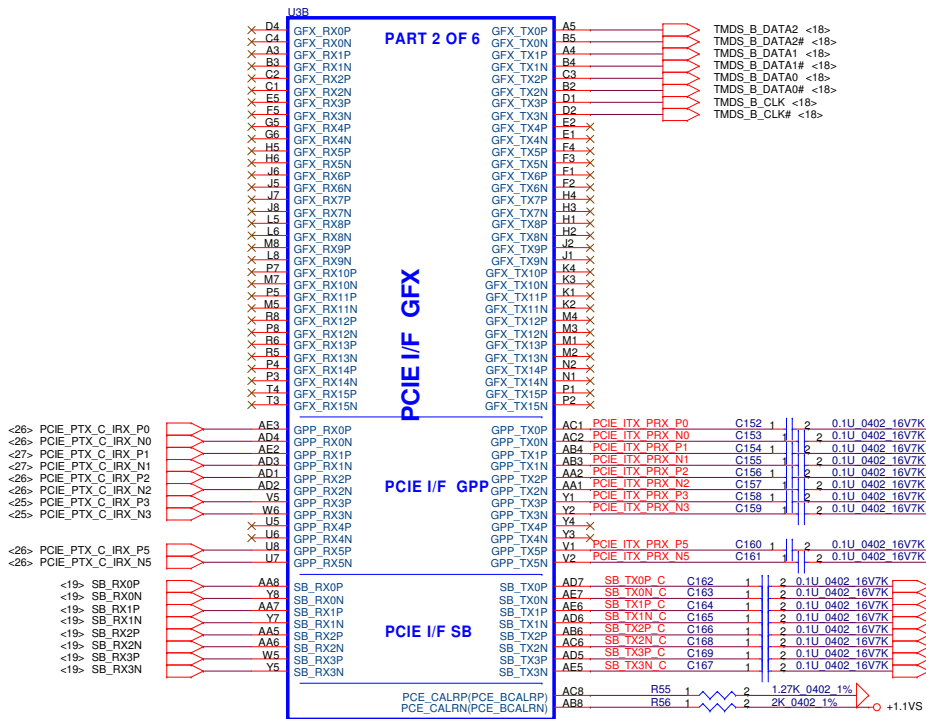






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Title	Compal Electronics, Inc.		
DDR II SO-DIMM I			
Size	Document Number	Rev	
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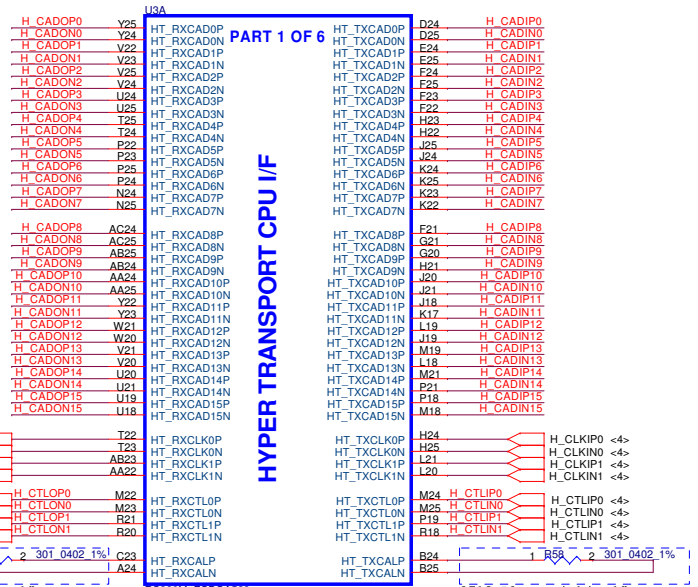


RS880M\_FCBGA528  
RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

9/20 SA00001ZG00(A11) S IC 216-0674001-00/RS780M FCBGA528P 0FH

New Card  
CardReader  
WLAN  
LAN10/100  
TV Tuner

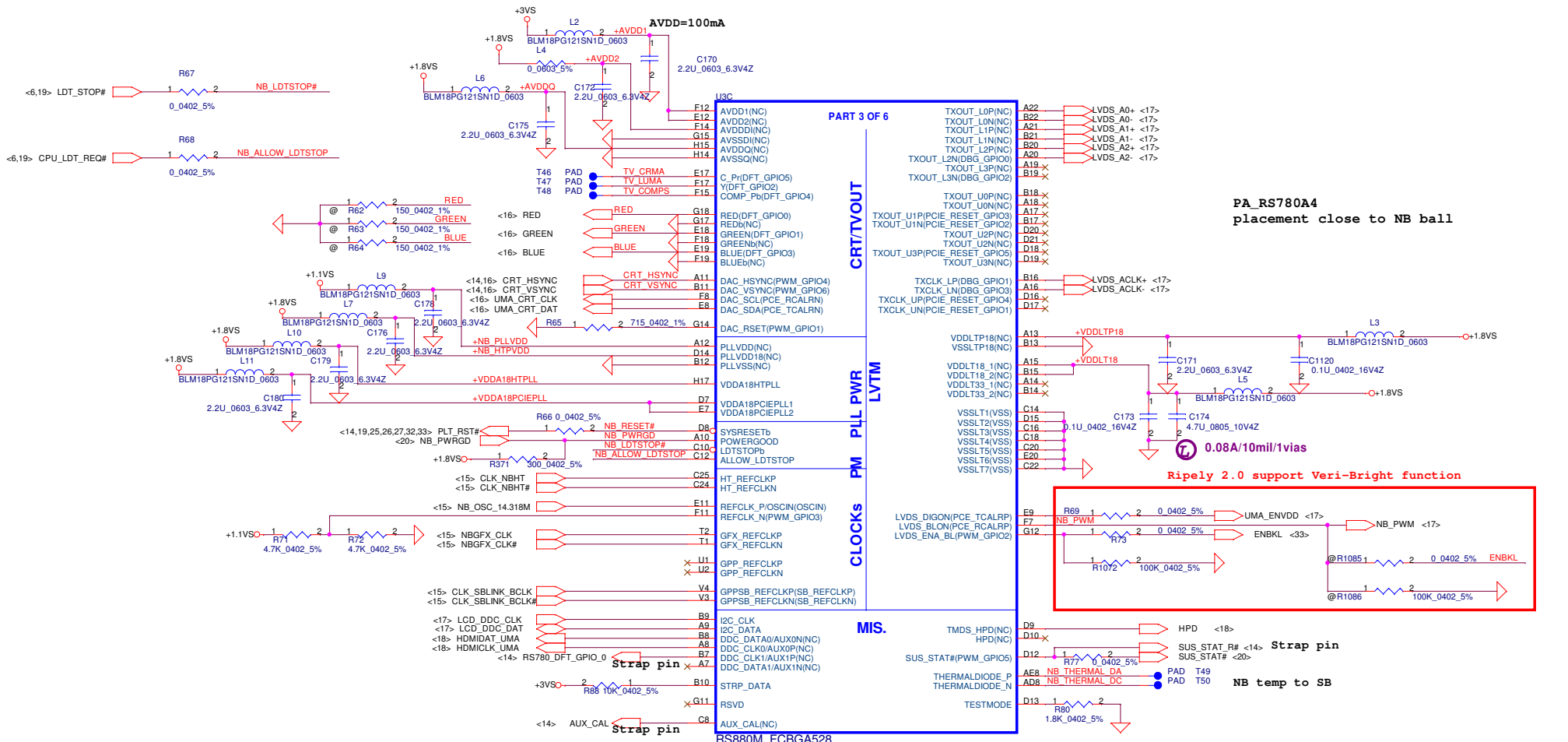


0718 Place within 1" layout 1:2

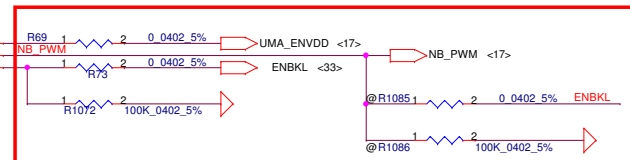
0718 Place within 1" layout 1:2

**NEED CHECK R68 & R69 WITH AMD**

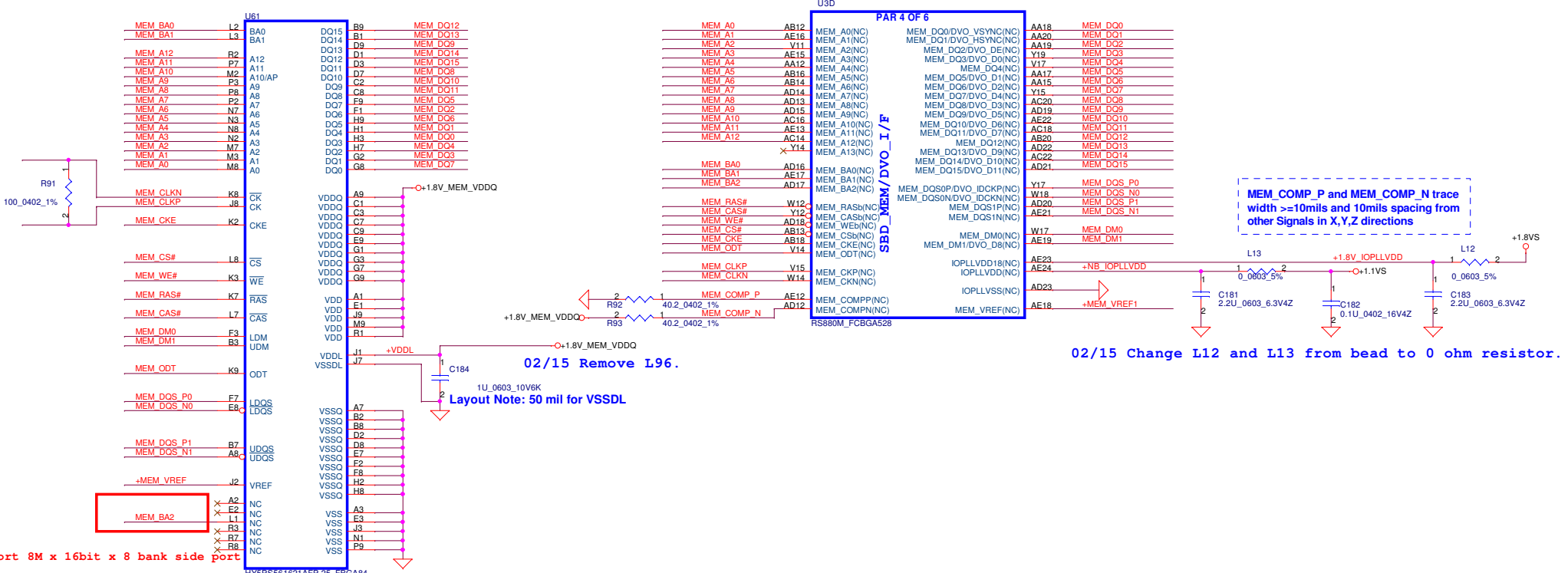
Security Classification	Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	RS880-HT/PCIE
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Date:	Monday, March 16, 2009	Sheet	10 of 56	



PA\_RS780A4 placement close to NB ball



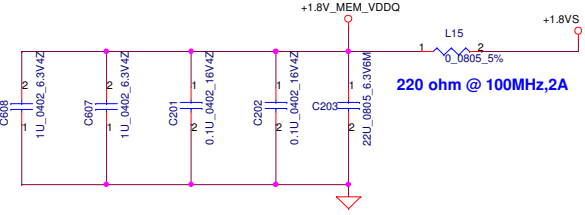
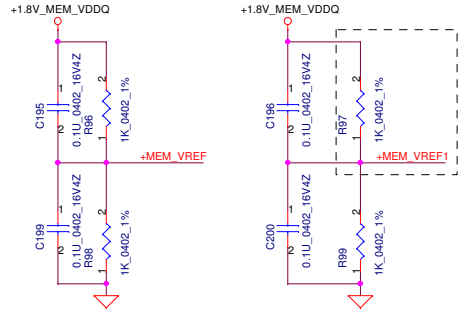
R	Veri-Bright	Non Veri-Bright
R73		@
R1072		@
R1085	@	
R1086	@	



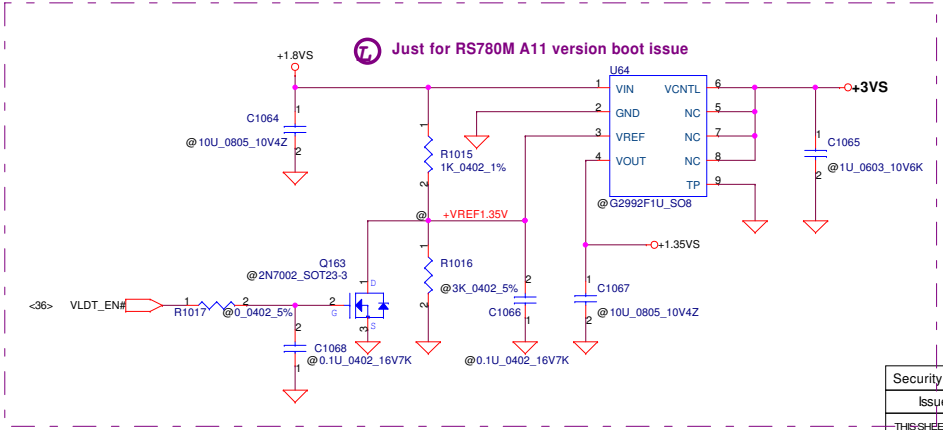
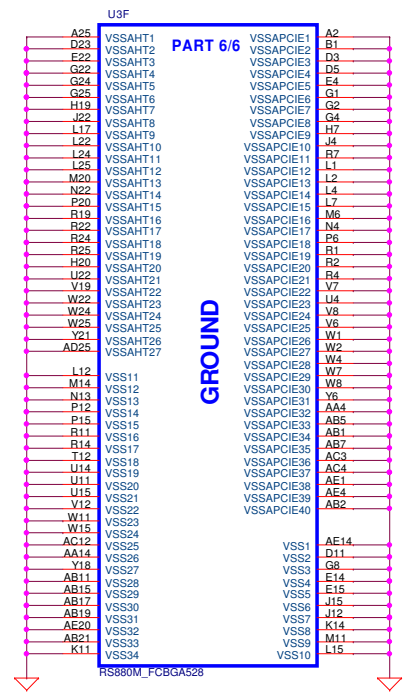
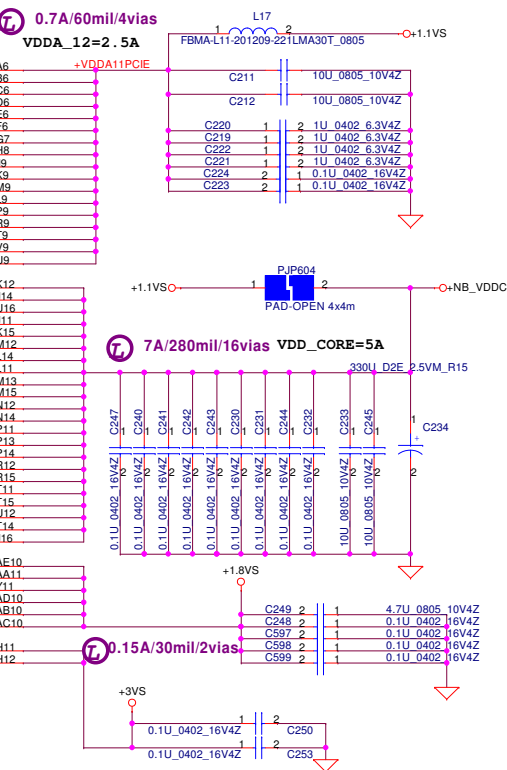
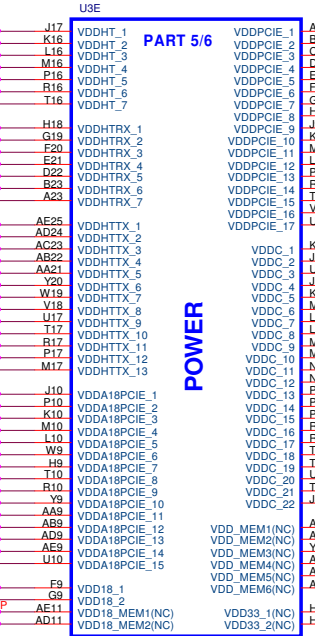
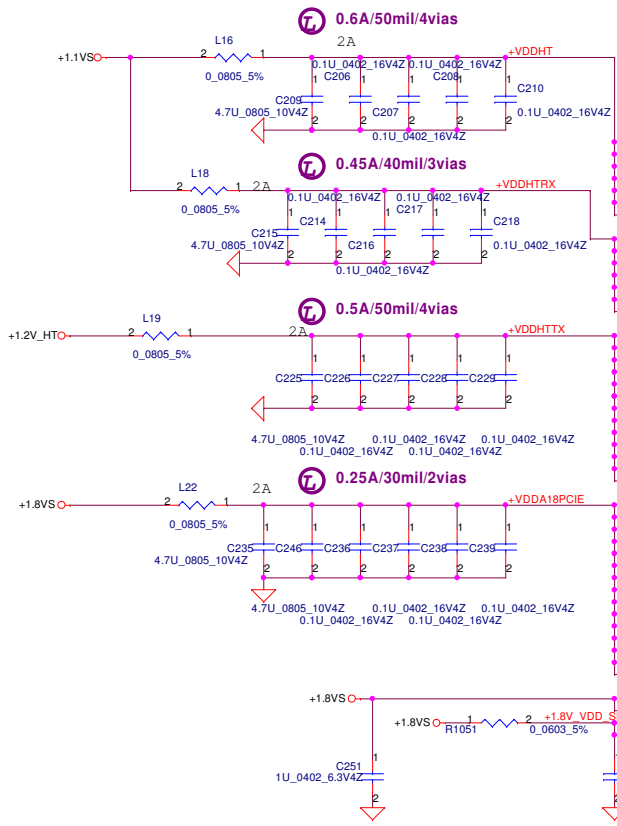
Support 8M x 16bit x 8 bank side port

9/20 SA000012G20 S IC D2 32M16 HY5PS121621CFP-25 FBGA 84P

Side Port disable, VREF need connect to +1.8VS for DDR2



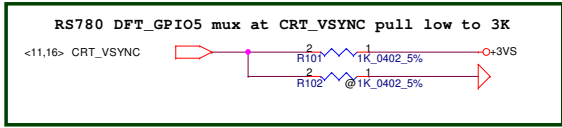
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	<b>Compal Electronics, Inc.</b> <b>RS880 Side-Port DDR2 SDRAM</b>	
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Customer	Document Number	Date		LA-4117P	0.3
Date: Monday, March 16, 2009				Sheet	12 of 56



Security Classification	Compal Secret Data	
Issued Date	2007/08/02	Deciphered Date
		2008/08/02

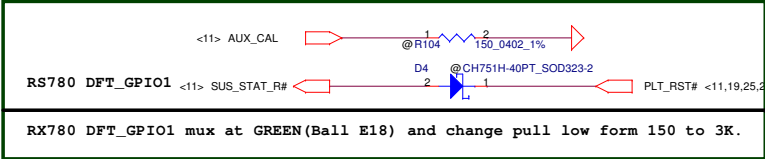
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Title		
Compal Electronics, Inc.		
RS880 PWR/GND		
Size	Document Number	Rev
Custom	LA-4117P	0.3
Date	Monday, March 16, 2009	Sheet 13 of 56



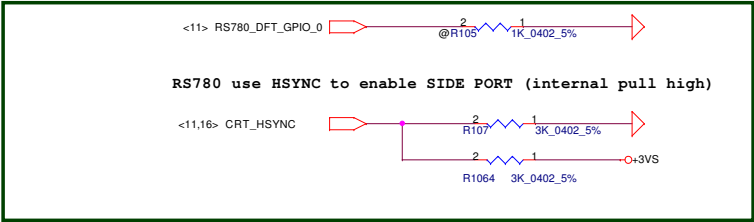
**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO.  
 1 : Disable (RS780) Enable (RX780)  
 0 : Enable (RS780) Disable (RX780)  
 PIN: RX780:NB\_TV\_C; RS740: RS740\_DFT\_GPIO5; RS780: VSYNC#



**DFT\_GPIO1:LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use Default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT

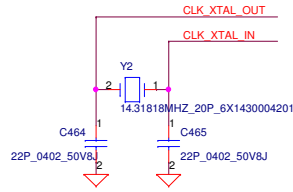
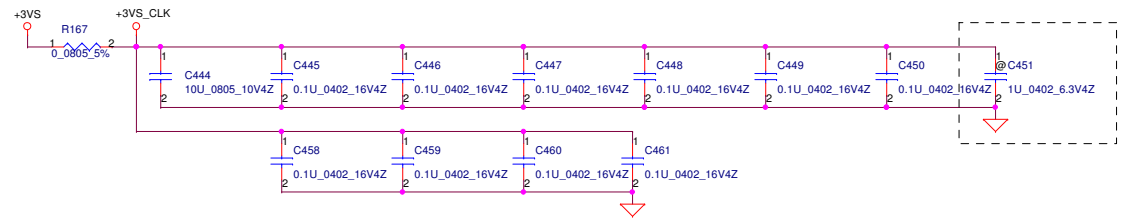
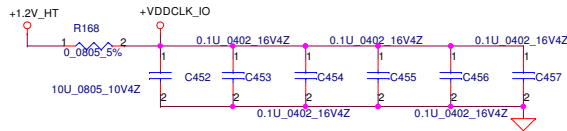


**DFT\_GPIO0:STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb**

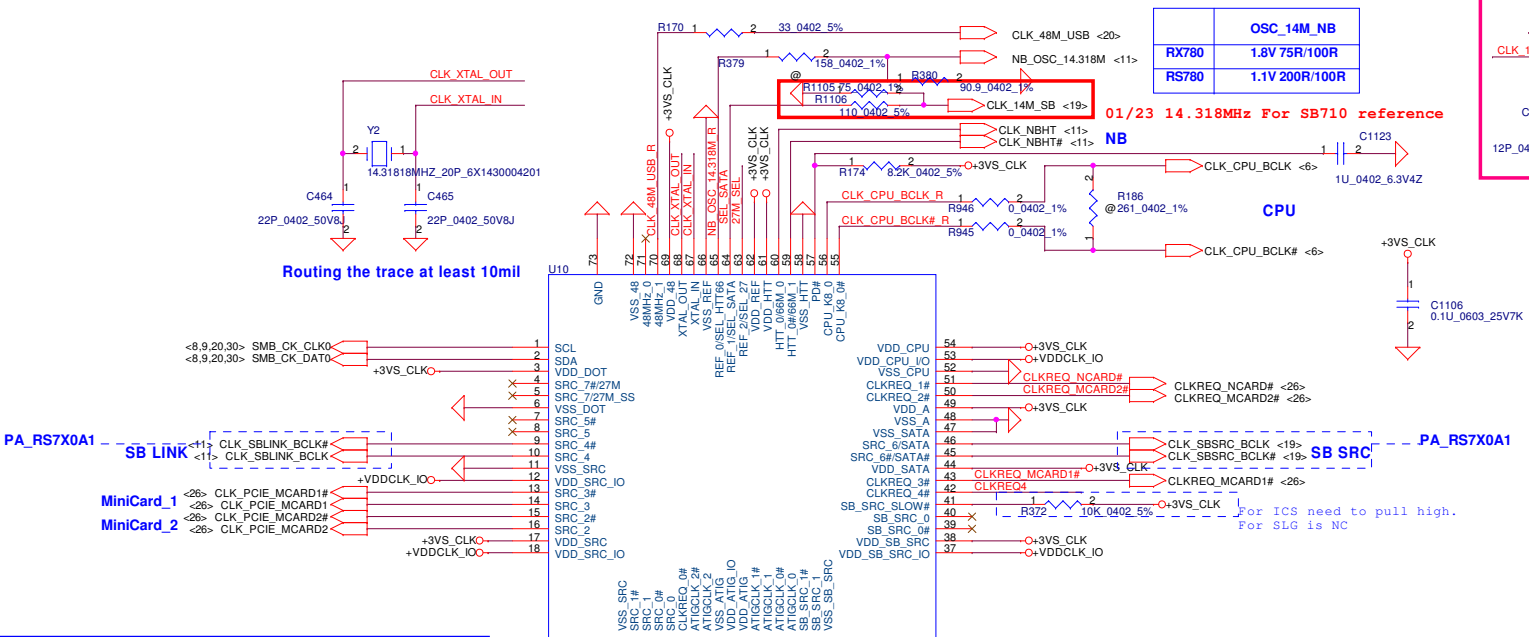
RX780: Enables the Test Debug Bus using PCIE bus  
 1 : Disable ( Can still be enabled using nbcfg register access )  
 0 : Enable

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)  
 1. Disable (RS740/RS780)  
 0 : Enable (RS740/RS780)

Security Classification	Compal Secret Data			Title		
Issued Date	2007/08/02	Deciphered Date	2008/08/02	RS880 STRAPS		
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				Custom	LA-4117P	0.3
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Routing the trace at least 10mil



PA\_RS7X0A1

SB LINK

MiniCard\_1

MiniCard\_2

PA\_RS7X0A1

SB SRC

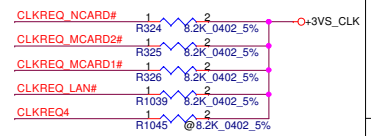
For ICS need to pull high.  
For SLG is NC

SEL_SATA	1	configure as SATA output
	0	configure as normal SRC(SRC_6) output
		* default

27M_SEL	1	configure as 27M and 27M_SS output
	0	configure as SRC_7 output
		* default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0	configure as differential 100MHz output
		* default



NB CLOCK INPUT TABLE

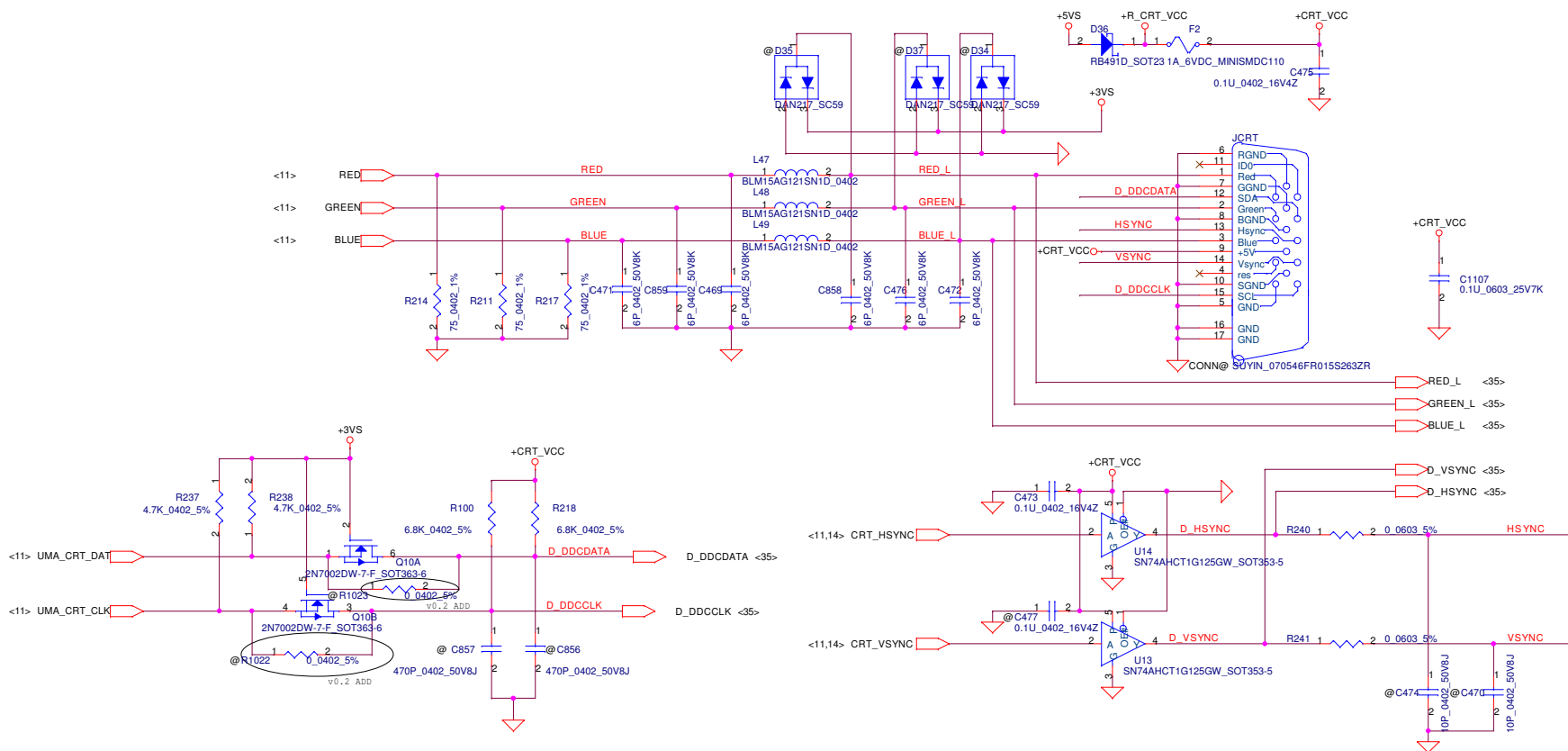
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P		vref
REFCLK_N	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)

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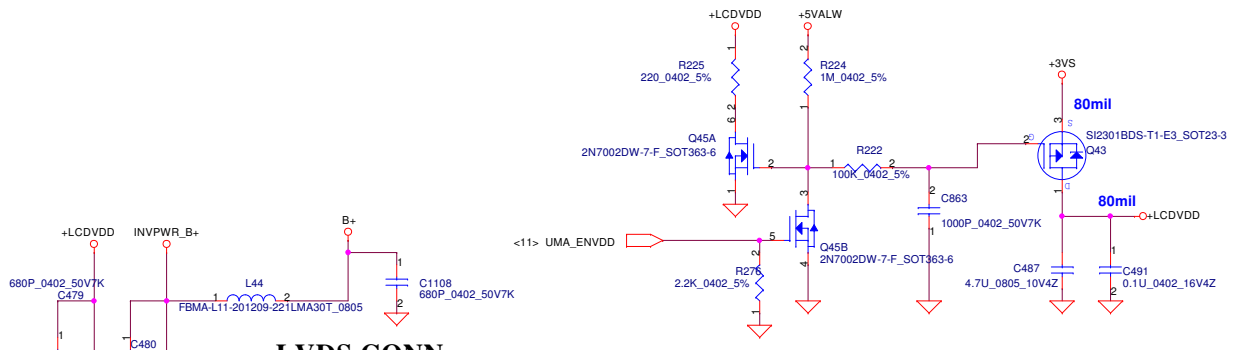
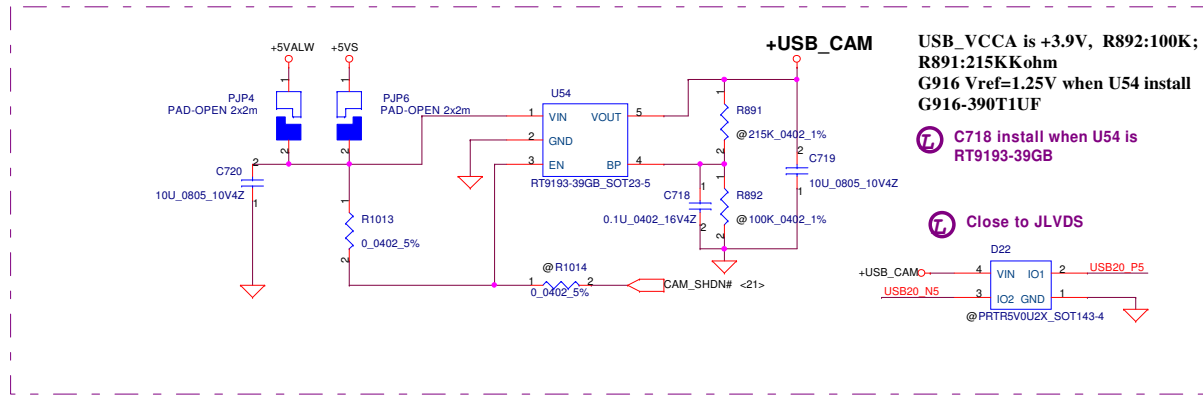
Compal Electronics, Inc.		
Clock generator		
Title		
Size	Document Number	Rev
Custom	LA-4117P	0.3
Date:	Monday, March 16, 2009	Sheet 15 of 56

# CRT CONNECTOR

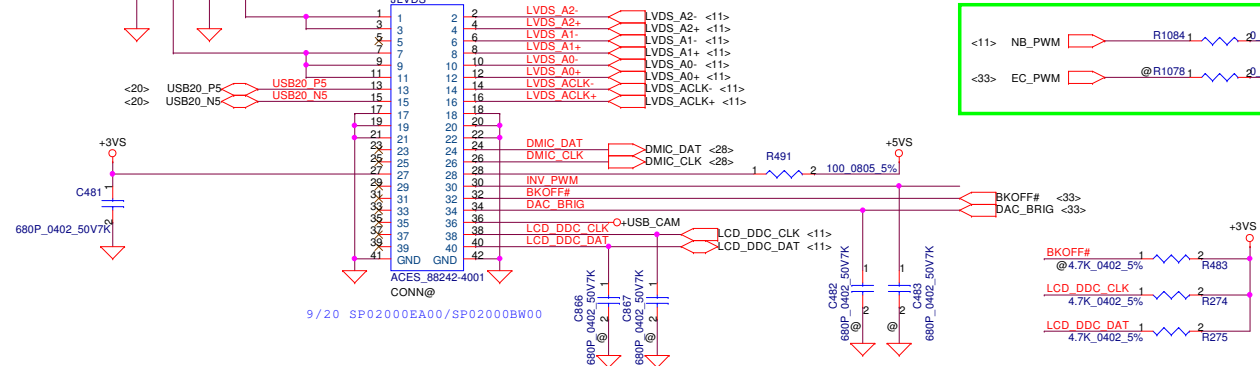
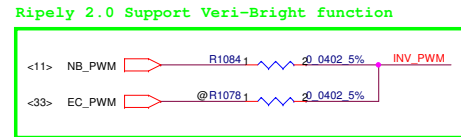


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2007/08/02	Deciphered Date	2008/08/02	<b>CRT Connector</b>		
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				Custom	<b>LA-4117P</b>	0.3
				Date:	Monday, March 16, 2009	Sheet 16 of 56

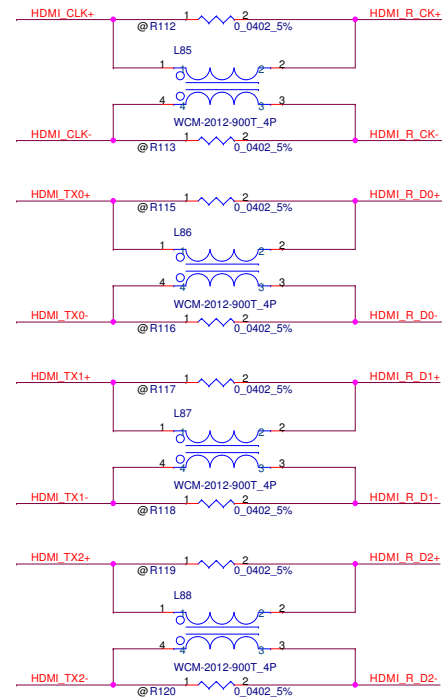
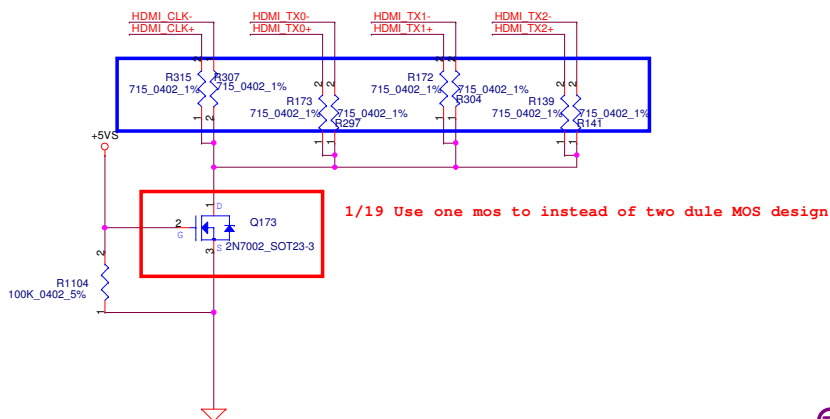
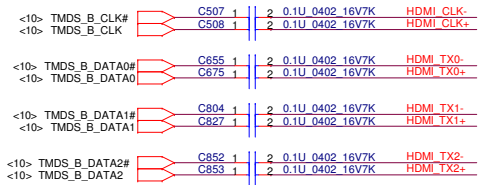
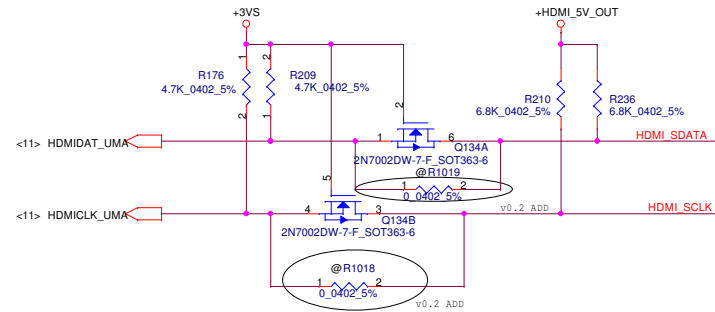
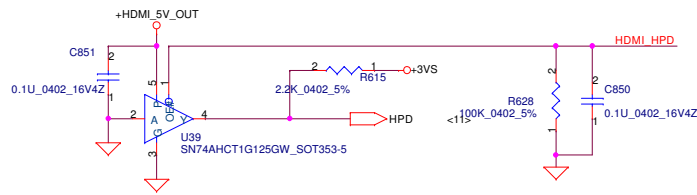




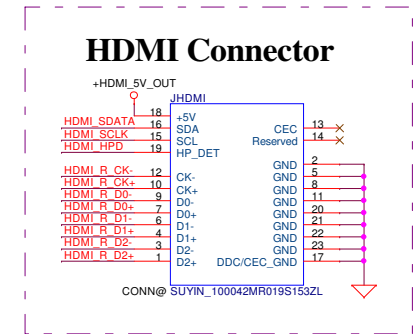
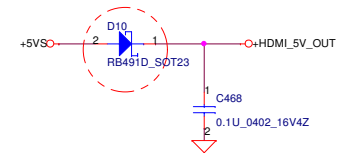
LVDS_A2-	C1056	1	2	@10P_0402_50V&J	LVDS_A2+
LVDS_A1-	C1057	1	2	@10P_0402_50V&J	LVDS_A1+
LVDS_A0-	C1058	1	2	@10P_0402_50V&J	LVDS_A0+
LVDS_ACLK-	C1059	1	2	@10P_0402_50V&J	LVDS_ACLK+



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Sheet 17 of 56				Rev 0.3



MP:Update D10 to meet HDMI.

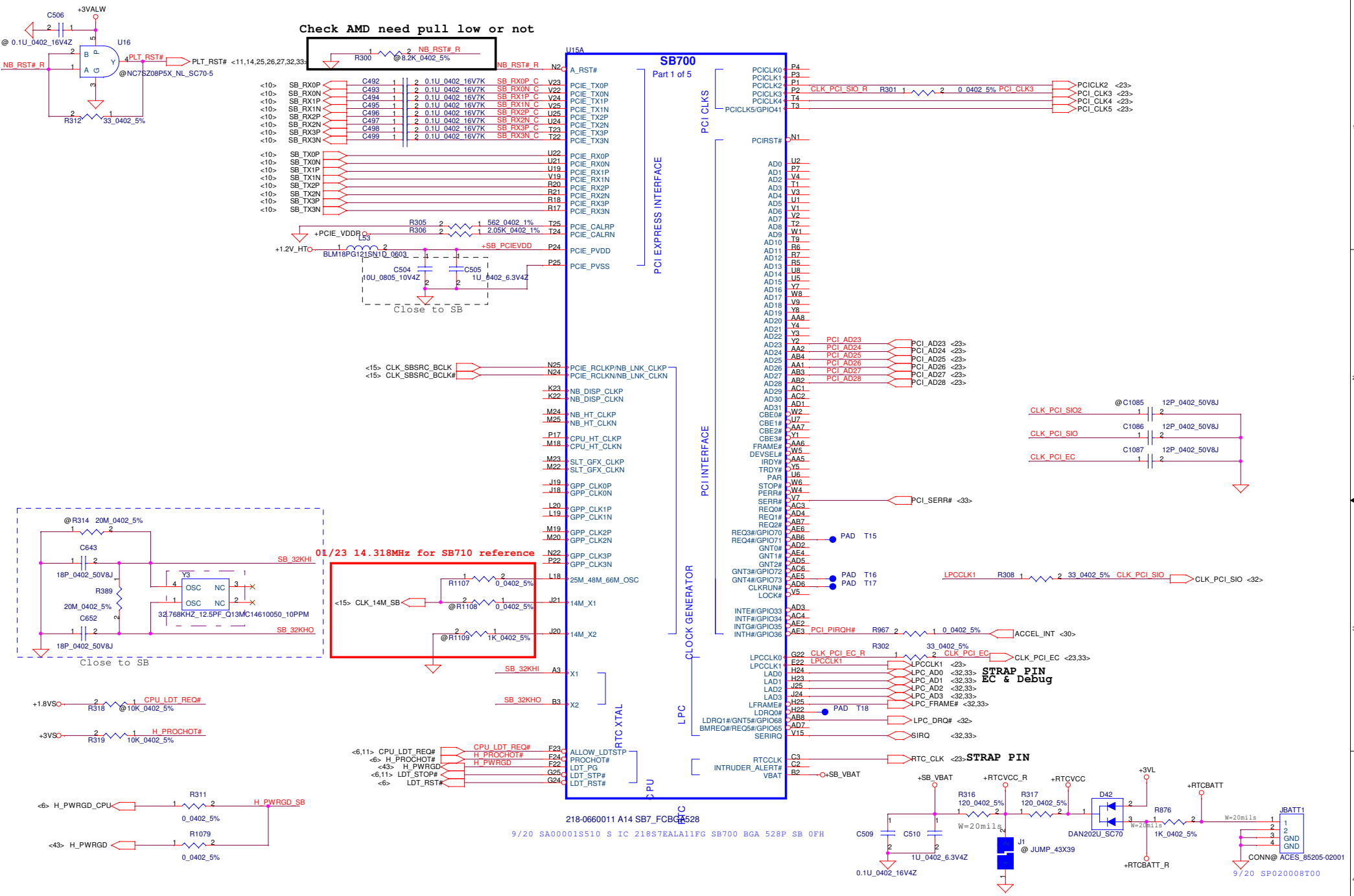


03/07 Chagnge R315, R307, R173, R297, R172, R304, R139, R141 from 750 ohm to 715 ohm.

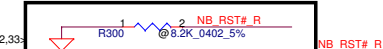
Change PCB Footprint from SW\_WCM2012F2S\_4P to KING\_WCM-2012-900T\_4P

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				HDMI	
Size	Document Number	Rev			
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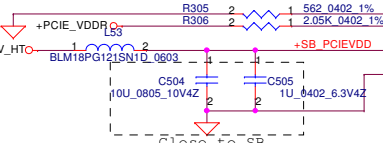


Check AMD need pull low or not



- <10> SB\_RX0P C492 1 2 0.1U 0402 16V7K SB\_RX0P C V23
- <10> SB\_RX0N C493 1 2 0.1U 0402 16V7K SB\_RX0N C V22
- <10> SB\_RX1P C494 1 2 0.1U 0402 16V7K SB\_RX1P C V24
- <10> SB\_RX1N C495 1 2 0.1U 0402 16V7K SB\_RX1N C V25
- <10> SB\_RX2P C496 1 2 0.1U 0402 16V7K SB\_RX2P C U25
- <10> SB\_RX2N C497 1 2 0.1U 0402 16V7K SB\_RX2N C U24
- <10> SB\_RX3P C498 1 2 0.1U 0402 16V7K SB\_RX3P C T23
- <10> SB\_RX3N C499 1 2 0.1U 0402 16V7K SB\_RX3N C T22

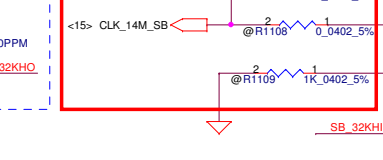
- <10> SB\_TX0P U22 PCI\_RX0P
- <10> SB\_TX0N U21 PCI\_RX0N
- <10> SB\_TX1P U19 PCI\_RX1P
- <10> SB\_TX1N U18 PCI\_RX1N
- <10> SB\_TX2P U25 PCI\_RX2P
- <10> SB\_TX2N U24 PCI\_RX2N
- <10> SB\_TX3P U23 PCI\_RX3P
- <10> SB\_TX3N U22 PCI\_RX3N



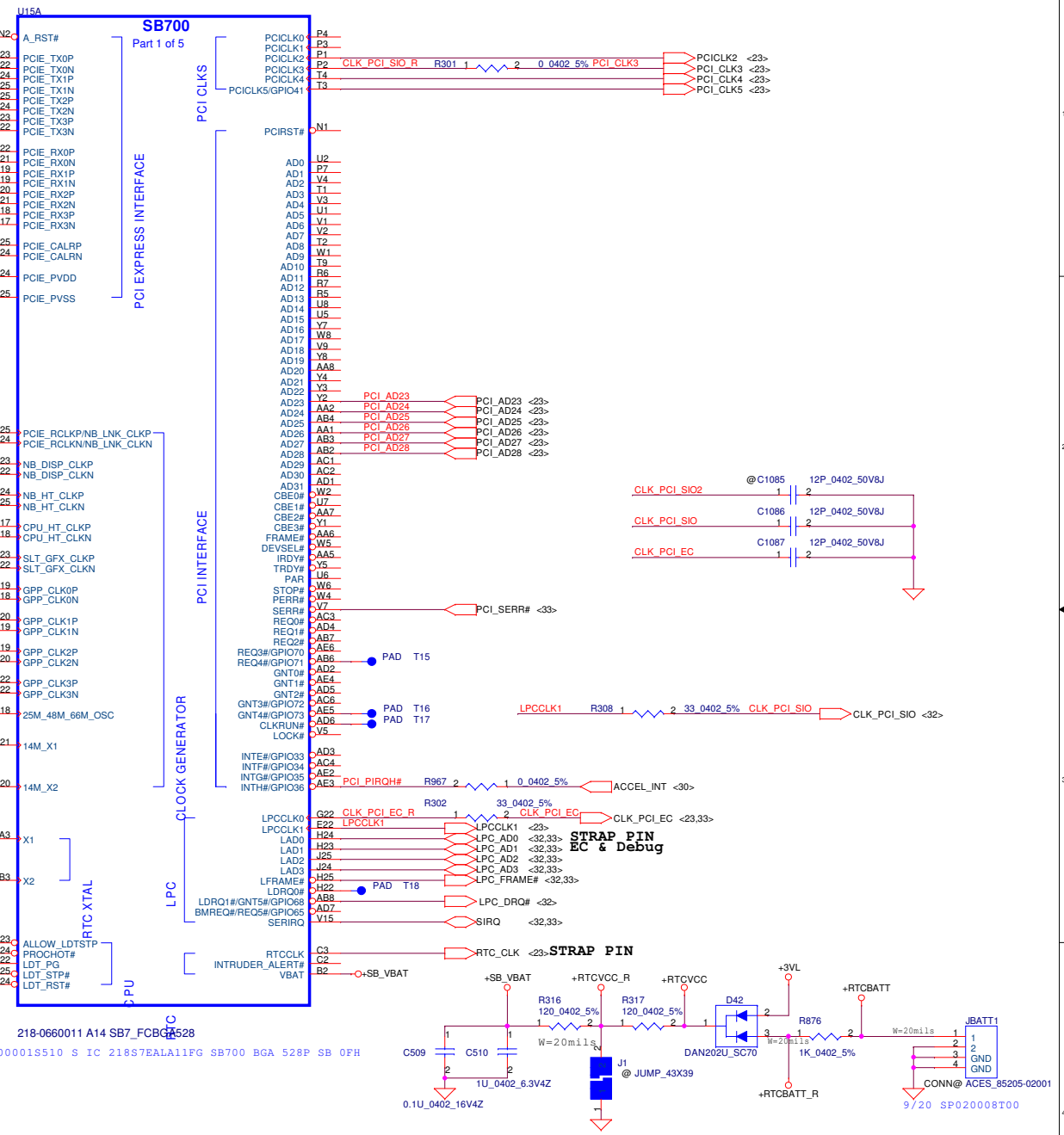
- <15> CLK\_SBSRC\_BCLK N25 PCI\_RCLKP/NB\_LNK\_CLKP
- <15> CLK\_SBSRC\_BCLK# N24 PCI\_RCLKN/NB\_LNK\_CLKN
- K23 NB\_DISP\_CLKP
- K22 NB\_DISP\_CLKN
- M24 NB\_HT\_CLKP
- M25 NB\_HT\_CLKN
- P17 CPU\_HT\_CLKP
- M18 CPU\_HT\_CLKN
- M23 SLT\_GFX\_CLKP
- M22 SLT\_GFX\_CLKN
- J19 GPP\_CLK0P
- J18 GPP\_CLK0N
- L20 GPP\_CLK1P
- L19 GPP\_CLK1N
- M19 GPP\_CLK2P
- M20 GPP\_CLK2N
- N22 GPP\_CLK3P
- N21 GPP\_CLK3N
- L18 25M\_48M\_66M\_OSC
- J21 14M\_X1
- J20 14M\_X2
- SB\_32KHI A3 X1
- SB\_32KHO B3 X2



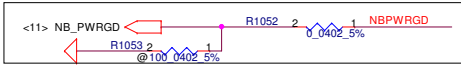
- <6> CPU\_LDT\_REQ# F23 CPU\_LDT\_REQ#
- <6> H\_PROCHOT# F24 H\_PROCHOT#
- <43> H\_PWRGD F22 H\_PWRGD
- <6,11> LDT\_STOP# G25 LDT\_STOP#
- <6> LDT\_RST# G24 LDT\_RST#
- <6,11> ALLOW\_LDTSTP F23 ALLOW\_LDTSTP
- <6> PROCHOT# F24 PROCHOT#
- <6> LDT\_PG F22 LDT\_PG
- <6,11> LDT\_STP# G25 LDT\_STP#
- <6> LDT\_RST# G24 LDT\_RST#
- RTC\_CLK C2 <23> STRAP PIN
- RTC\_ALERT# C2 RTC\_ALERT#
- VBAT B2 <+SB\_VBAT



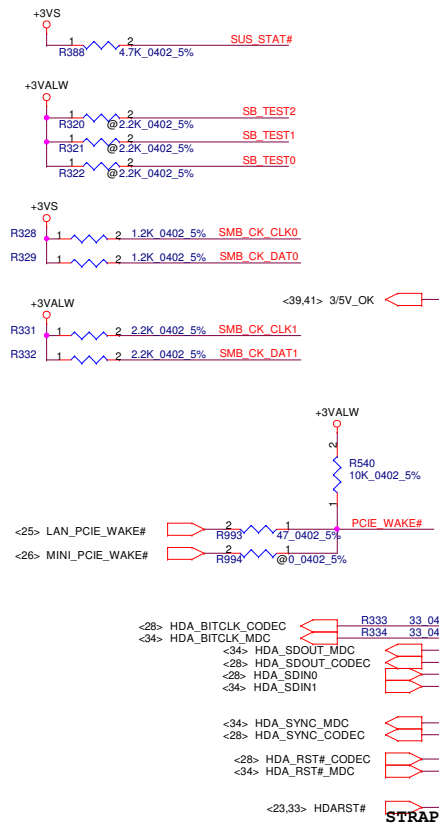
- LPC\_CLK1 G22 CLK\_PCI\_EC R
- LPC\_CLK1# G21 LPCCLK1
- LPC\_AD0 H24 LPC\_AD0 <32,33>
- LPC\_AD1 H23 LPC\_AD1 <32,33>
- LPC\_AD2 J25 LPC\_AD2 <32,33>
- LPC\_AD3 J24 LPC\_AD3 <32,33>
- LPC\_FRAME# H22 LPC\_FRAME# <32,33>
- LPC\_DRQ# H21 LPC\_DRQ# <32,33>
- SIRQ V15 <32,33>



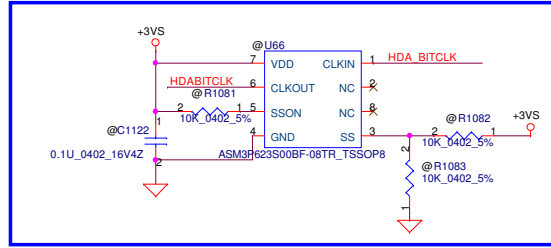
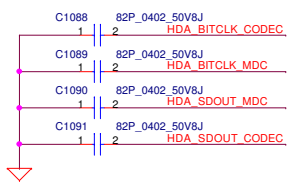
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	<b>SB710-PCIE/PCI/ACPI/LPC/RTC</b>	
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Size	Document Number	Rev	Date: Monday, March 16, 2009		
Custom	LA-4117P	0.3	Sheet	19	of 56



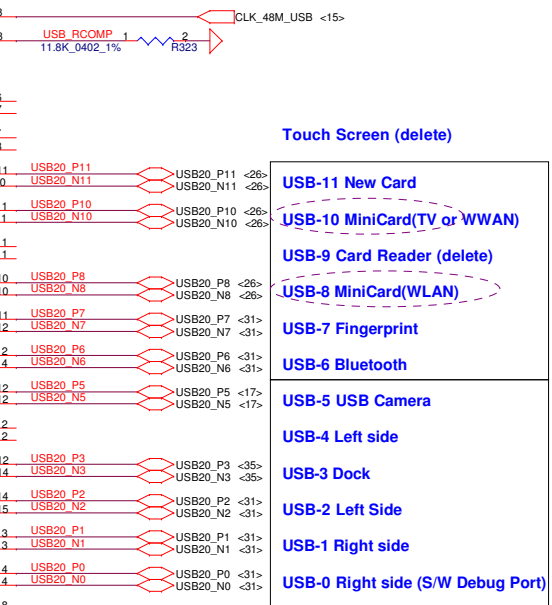
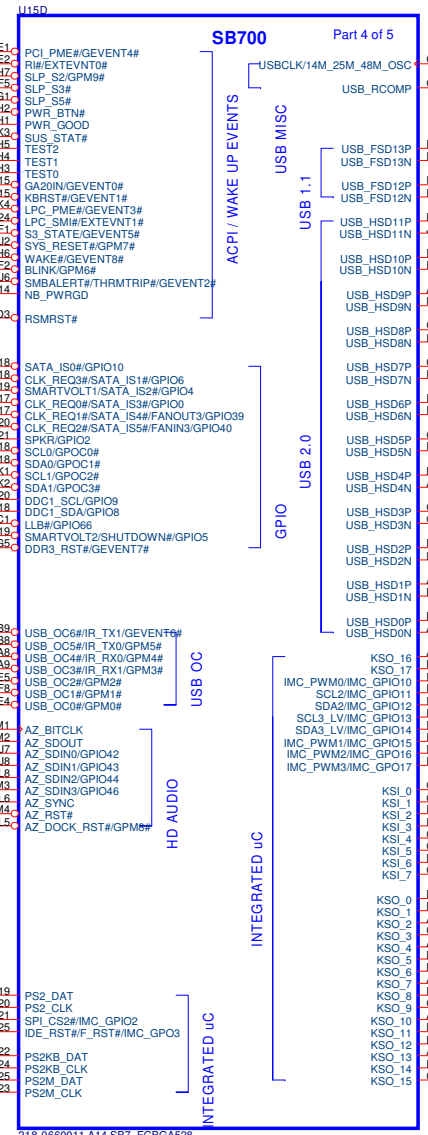
For SB700 All divider to 1.8V for RS & RX780



STRAP PIN



03/05 Add SSC circuit for HDA\_BITCLK.



Touch Screen (delete)

USB-11 New Card

USB-10 MiniCard(TV or WWAN)

USB-9 Card Reader (delete)

USB-8 MiniCard(WLAN)

USB-7 Fingerprint

USB-6 Bluetooth

USB-5 USB Camera

USB-4 Left side

USB-3 Dock

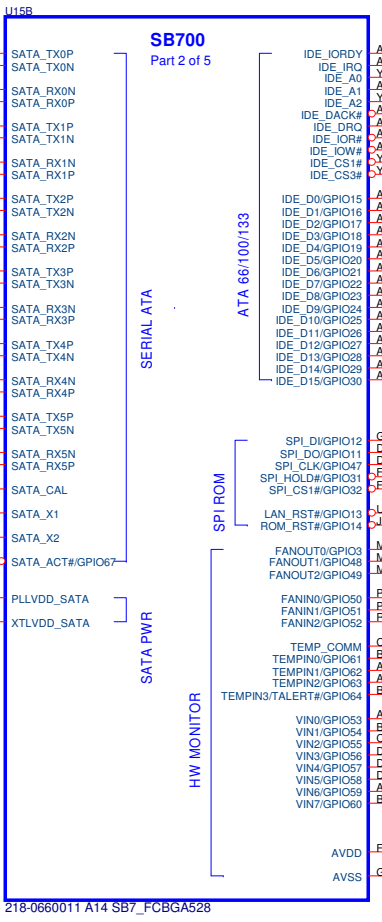
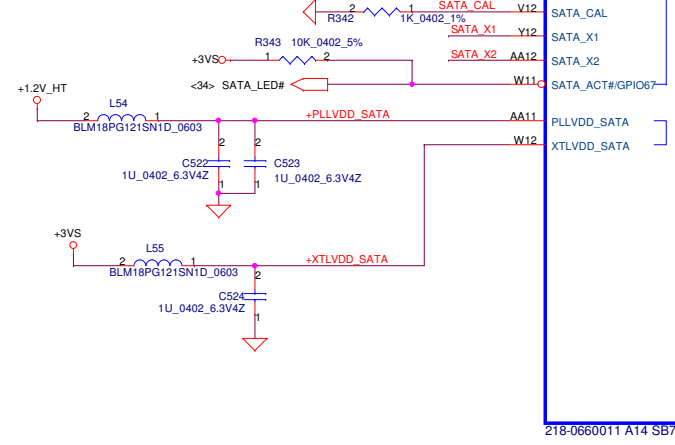
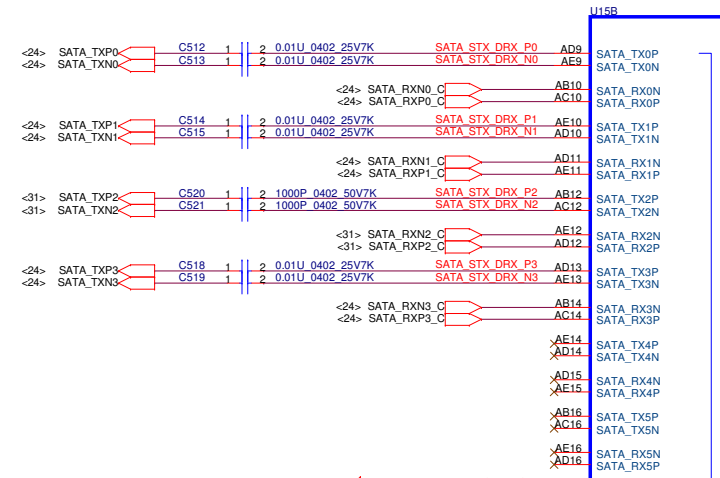
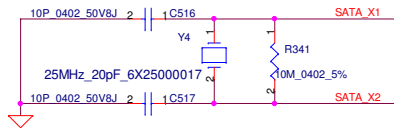
USB-2 Left Side

USB-1 Right side

USB-0 Right side (S/W Debug Port)

218-0660011 A14 SB7\_FCBGA528

Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	SB710 USB/AC97	
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Custom	LA-4117P	Rev	0.3		
Date	Monday, March 16, 2009	Sheet	20	of 56	

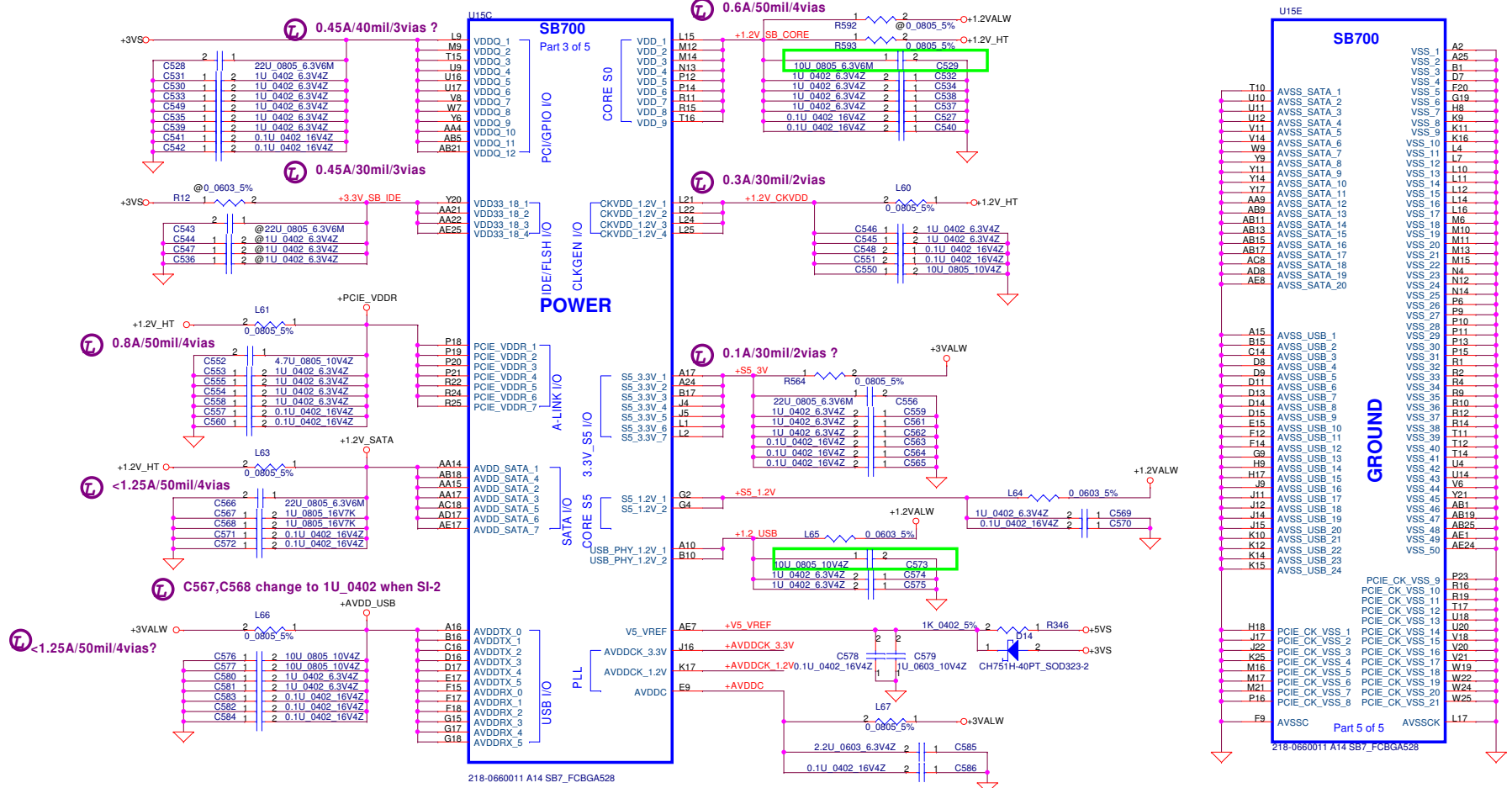


Local Frame Buffer Strapping List  
Copy from Becks.

	LFB_ID2	LFB_ID1	LFB_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

LFB\_ID0 to LFB\_ID2 got internal PU 10K to S5.

02/18 Add R1071 and D56 to connect to AC\_IN.



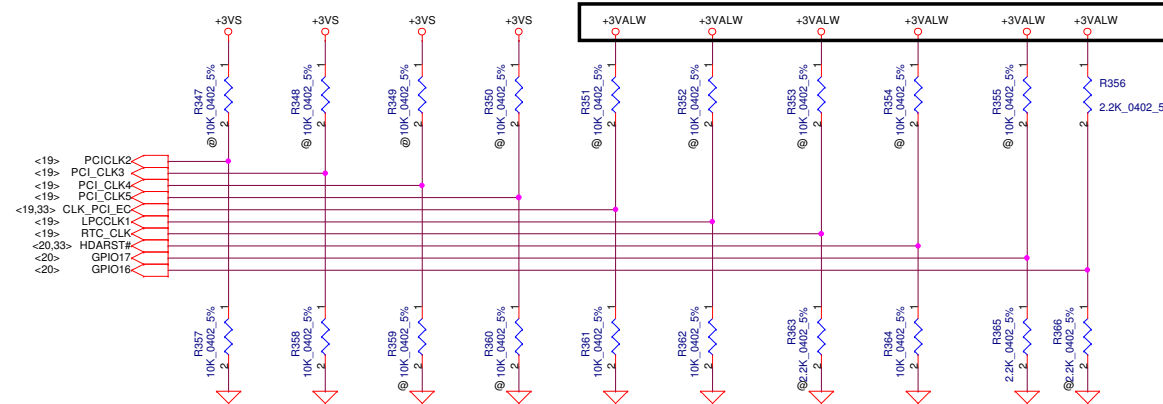
218-0660011 A14 SB7\_FCBGA528

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Sheet 22 of 56 Rev 0.3				

# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

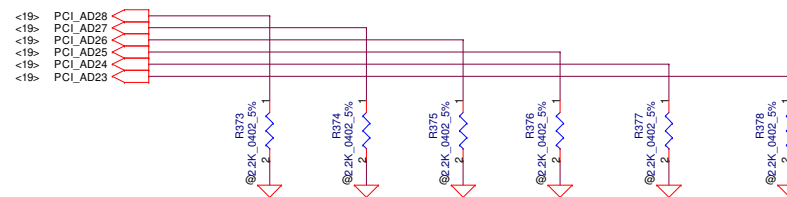
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved  H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FW ROM	



# DEBUG STRAPS

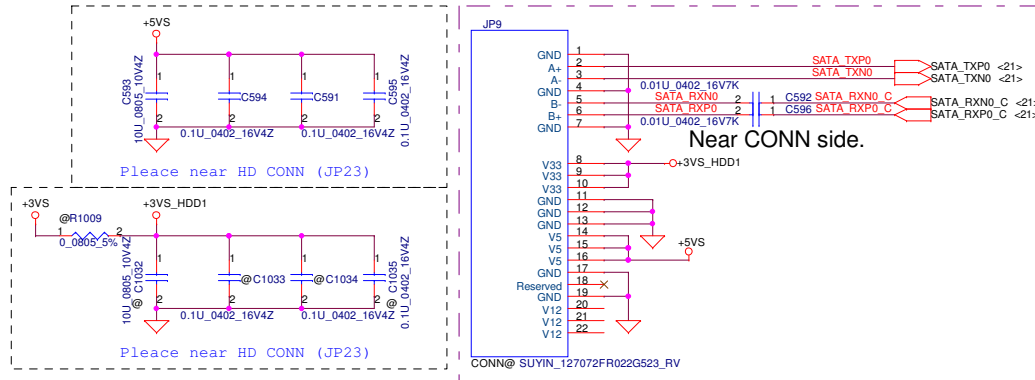
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

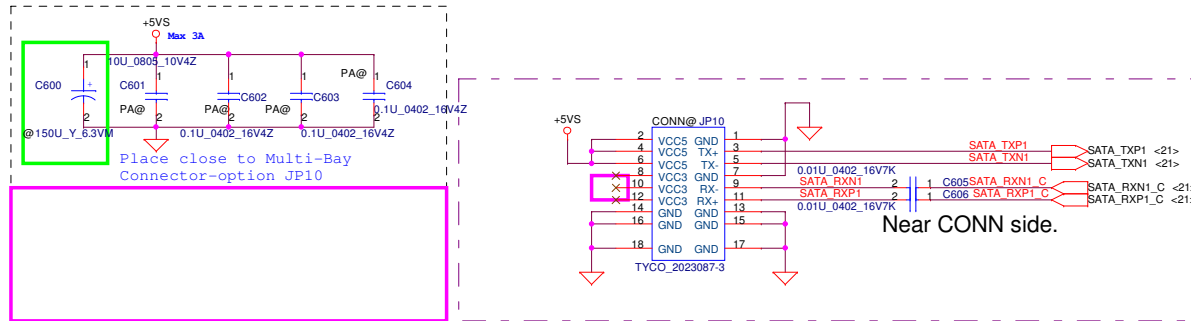


Security Classification	Compal Secret Data			Title <b>SB700 STRAPS</b>		
Issued Date	2007/08/02	Deciphered Date	2008/08/02			
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Date:	Monday, March 16, 2009	Sheet	23	of	56	

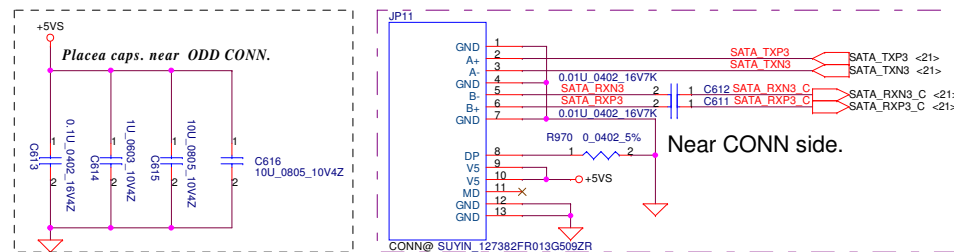
## HDD Connector



## Multi-Bay Connector-option

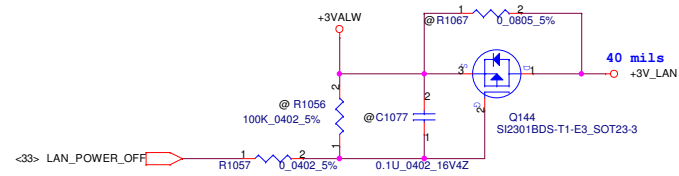
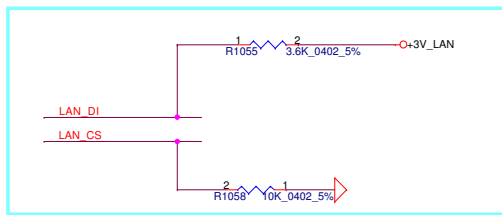


## CD-ROM Connector

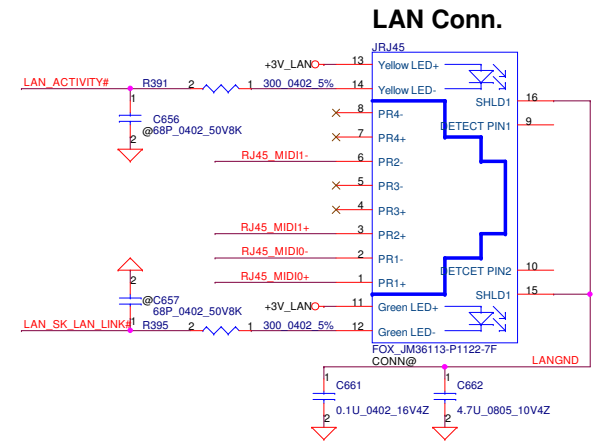
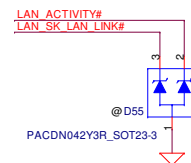
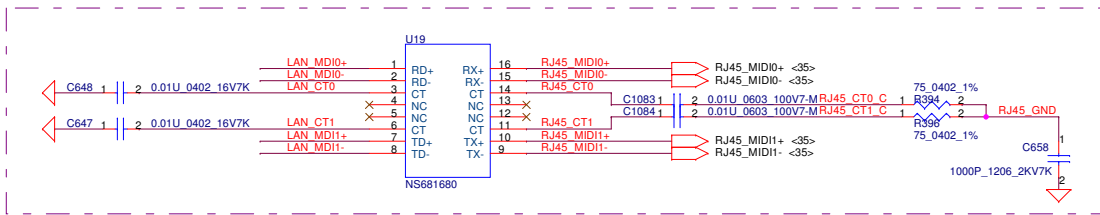
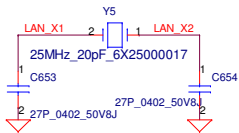
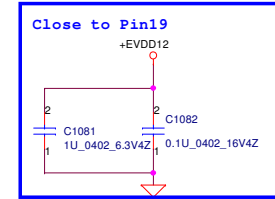
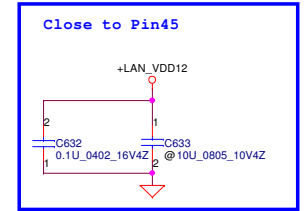
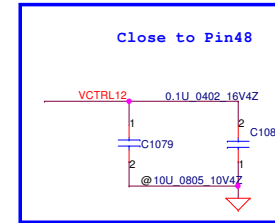
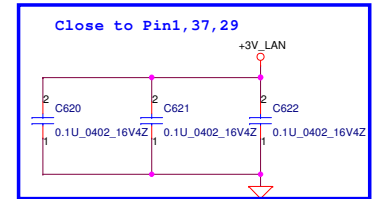
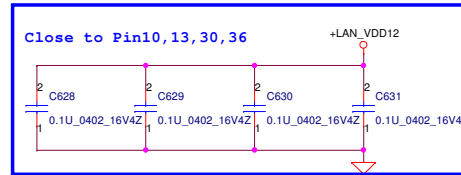
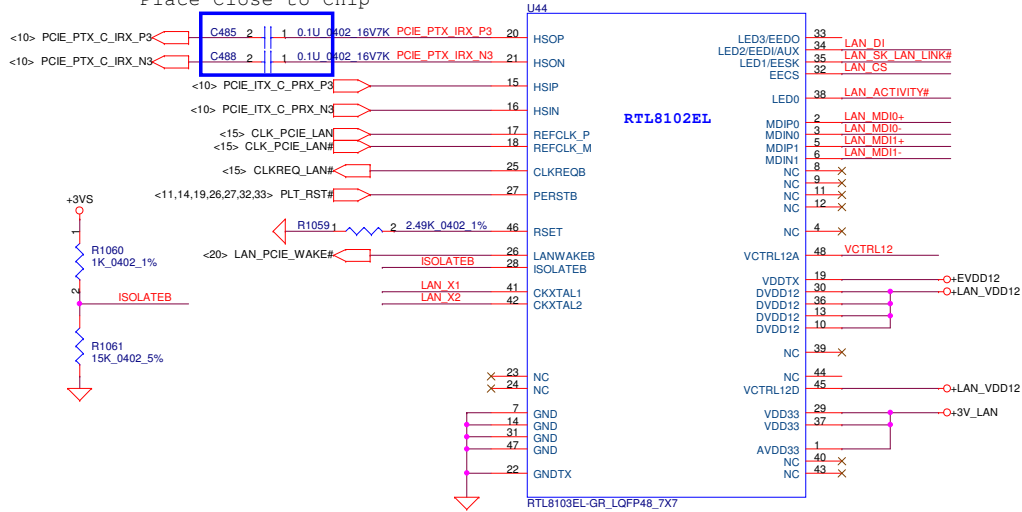


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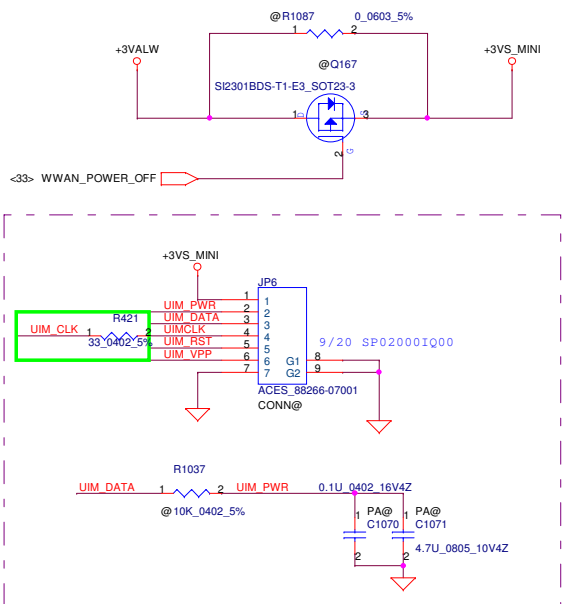
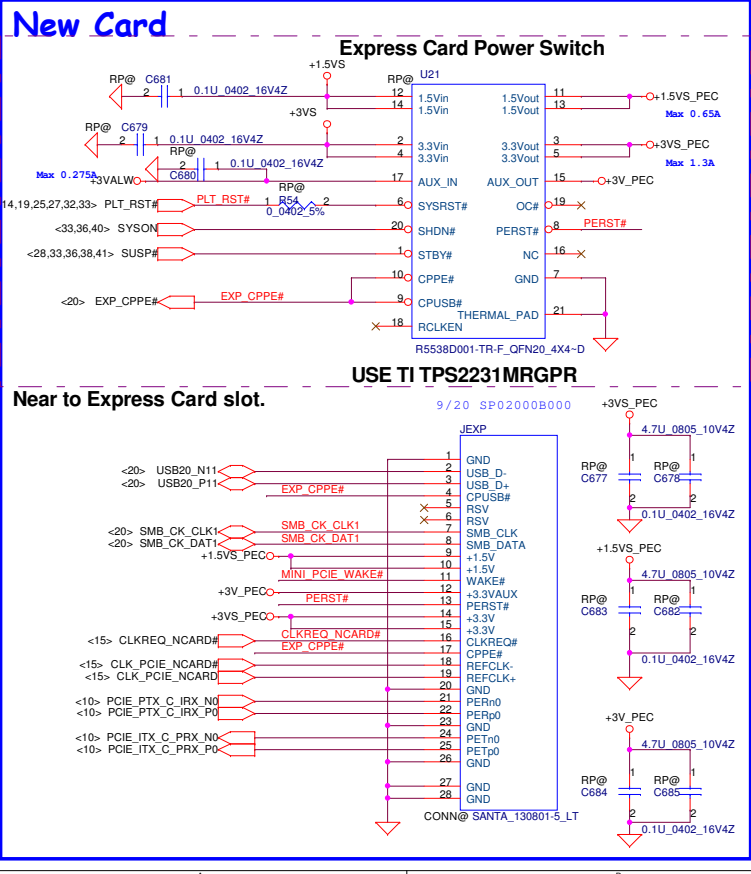
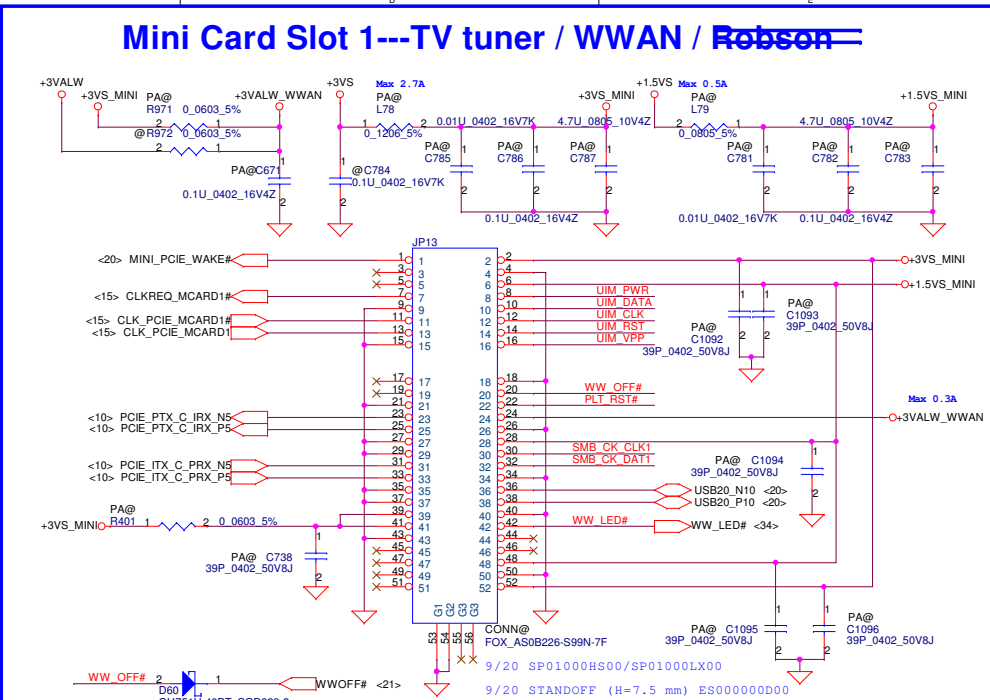
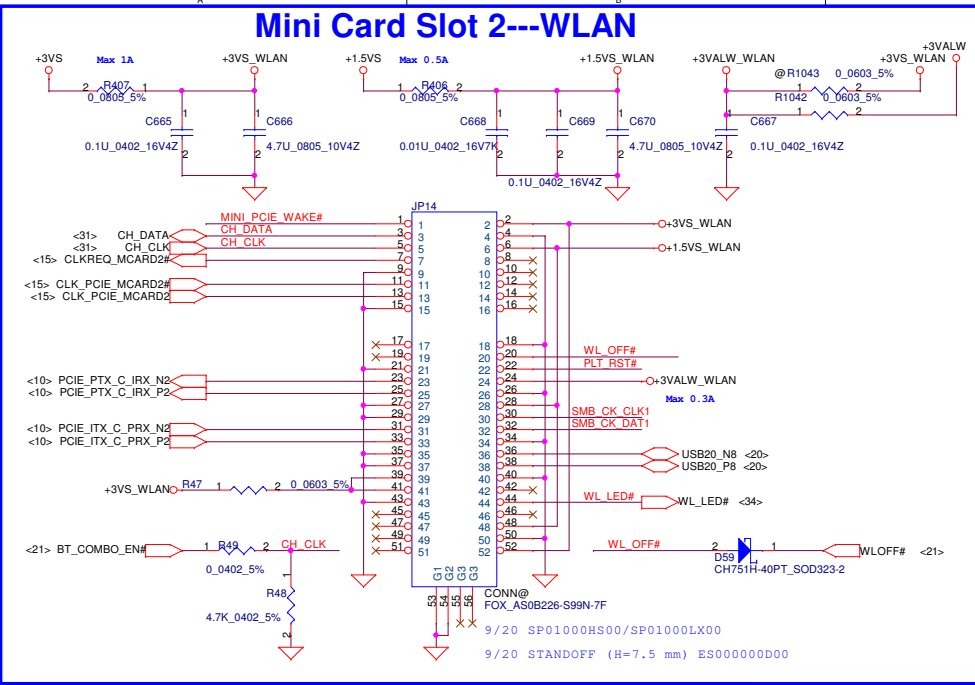




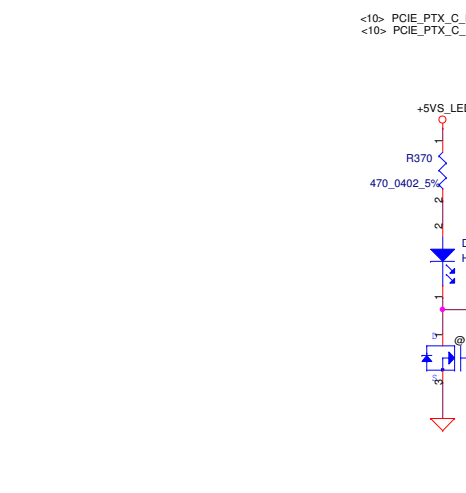
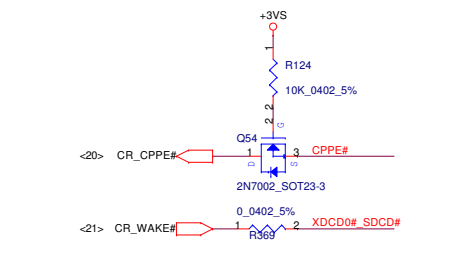
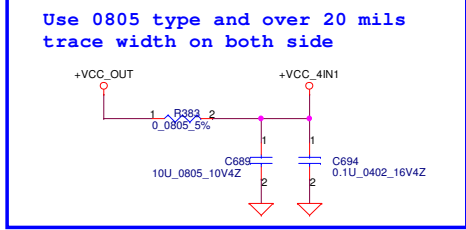
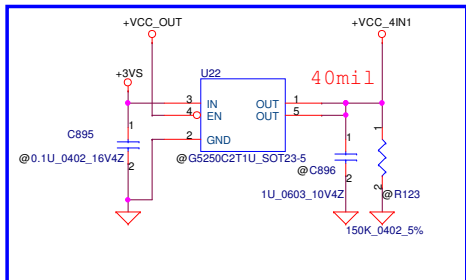
Place Close to Chip



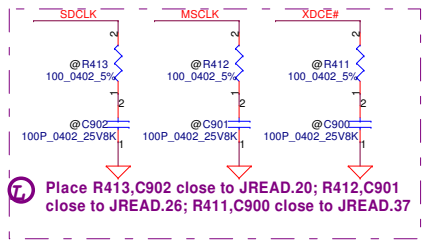
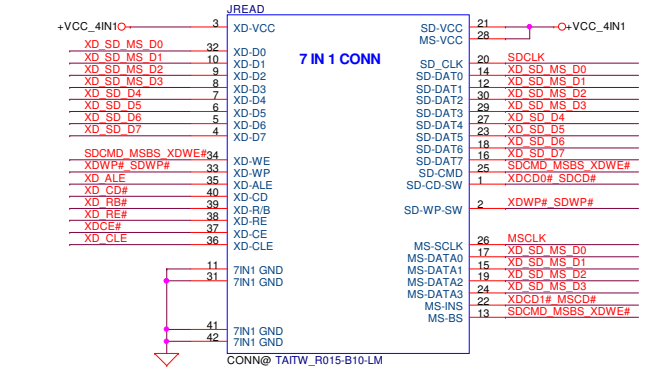
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	RTL8111C/8102E 10/100/1000 LAN	
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Size	Document Number	Rev	Date	
Custom	LA-4117P	0.3	Monday, March 16, 2009	
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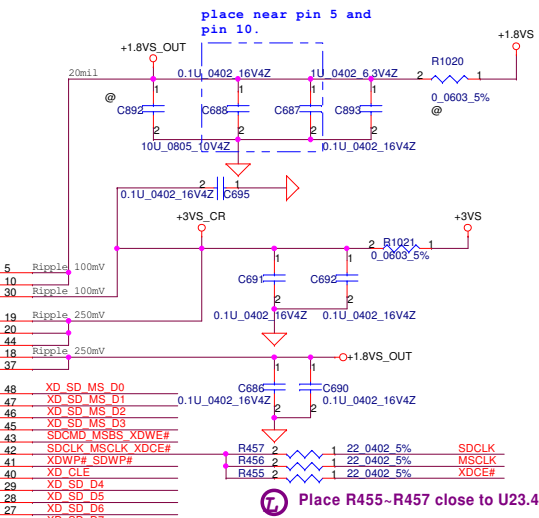
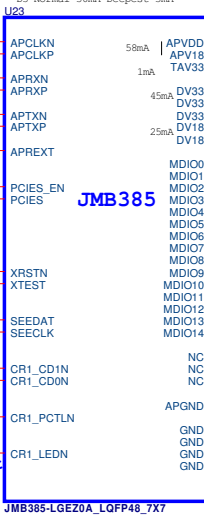


### Card Reader Connector



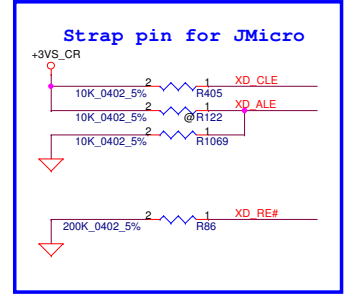
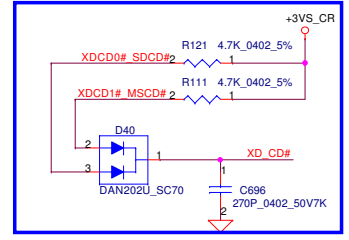
Place R413,C902 close to JREAD.20; R412,C901 close to JREAD.26; R411,C900 close to JREAD.37

### Power Circuit



Place R455-R457 close to U23.42

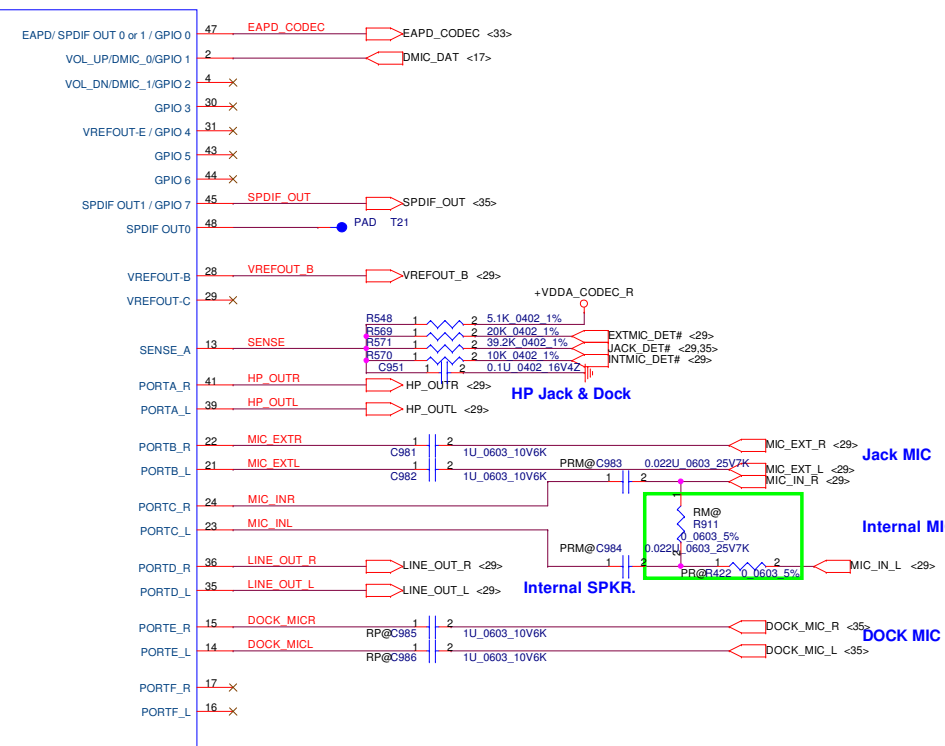
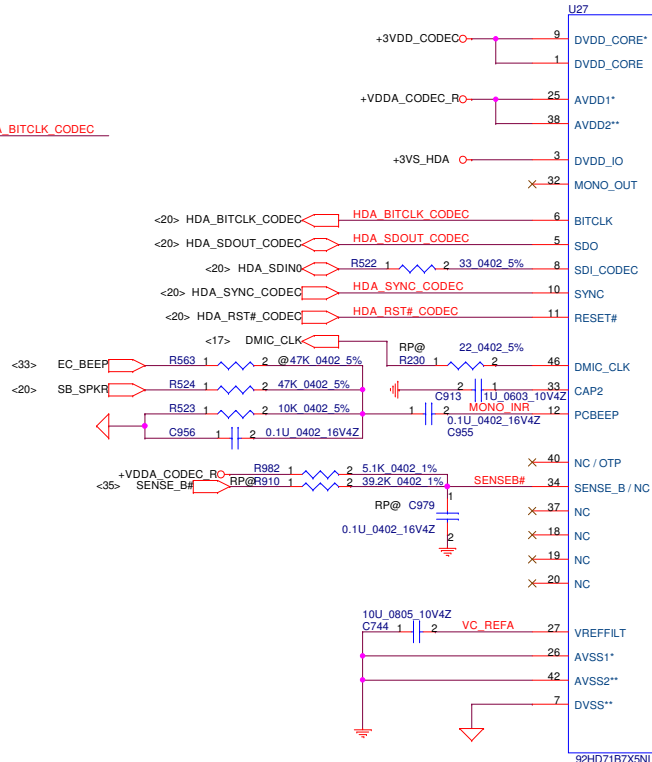
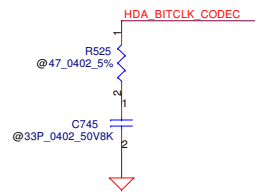
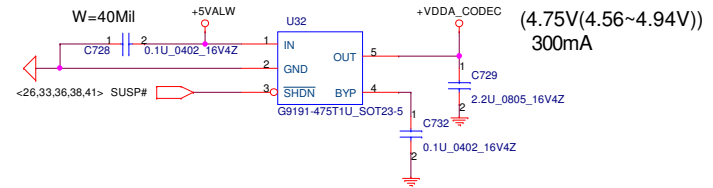
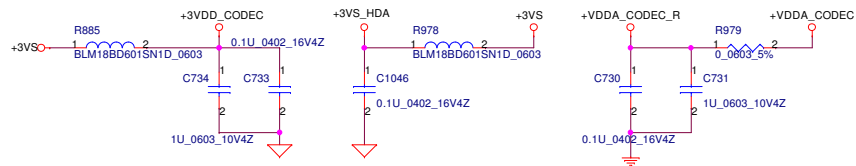
White LED: VF=3V, IF = 10mA, Res = 200 ohm



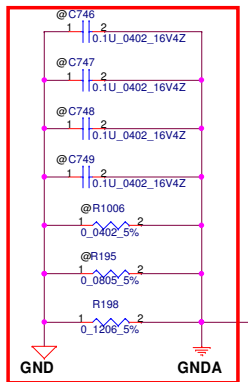
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Title <b>PCI-E I/F Card Reader-JM385</b>		
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# CODEC POWER

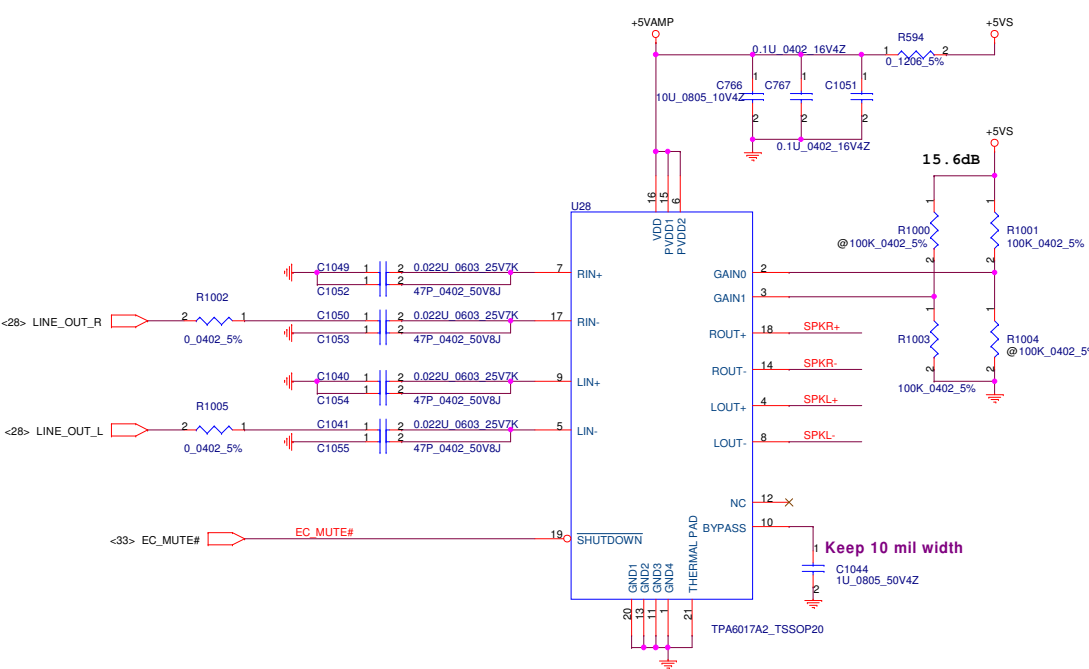


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

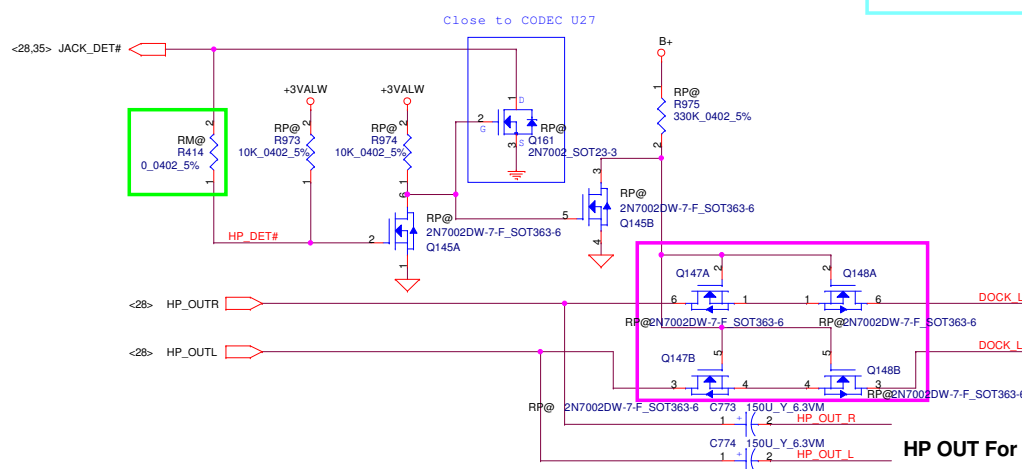
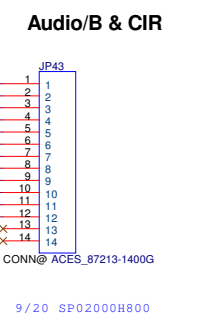
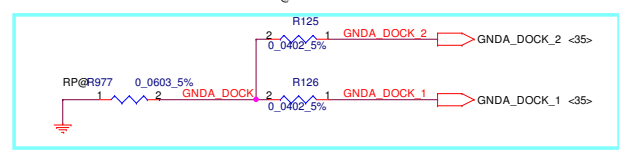
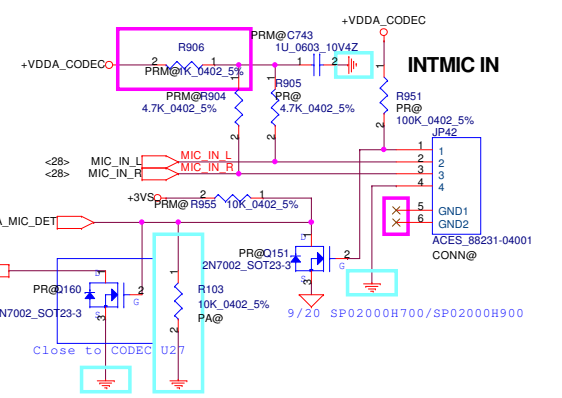
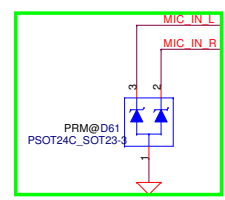
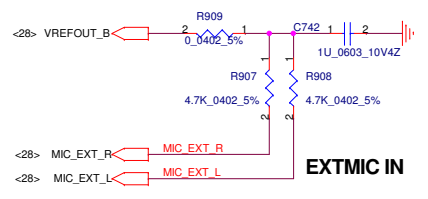
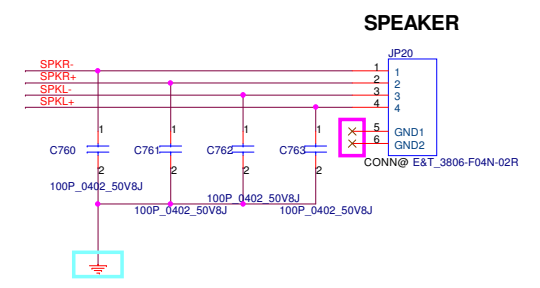


Use an 80mil to connection or place a 1206 resistor under CODEC with double vias.

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Size	Document Number	Rev		
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GAIN0	GAIN1	Av (inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

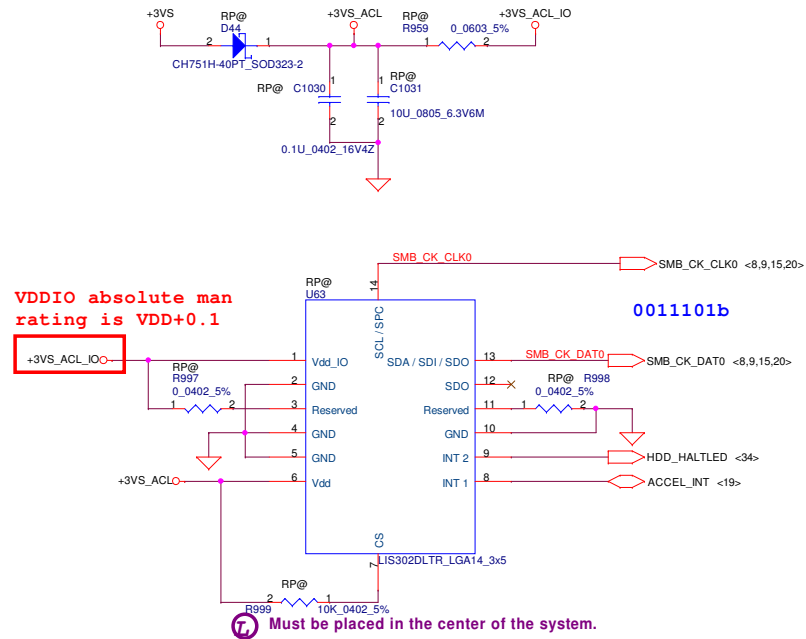


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		2008/08/02

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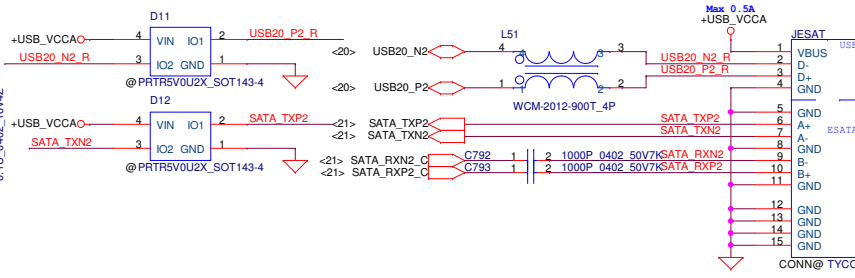
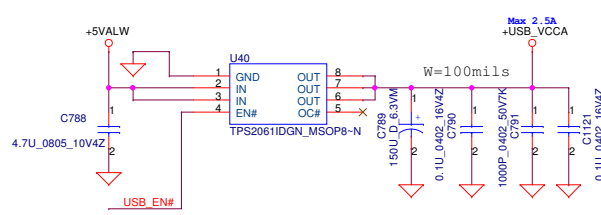
Title		
<b>Compal Electronics, Inc.</b>		
<b>AMP &amp; Audio Jack</b>		
Size	Document Number	Rev
Custom	LA-4117P	0.3
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# ACCELEROMETER

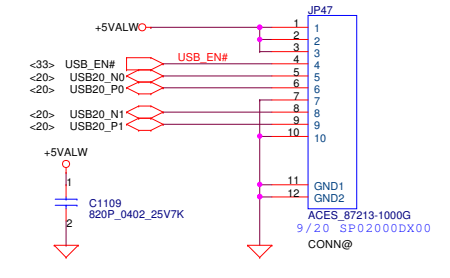


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Accelerometer	
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				Custom	LA-4117P
				Date:	Monday, March 16, 2009
				Sheet	30 of 56
				Rev	0.3

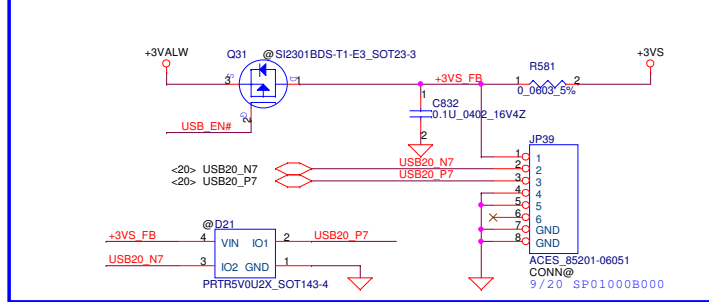
### Left side USB CONNECTOR



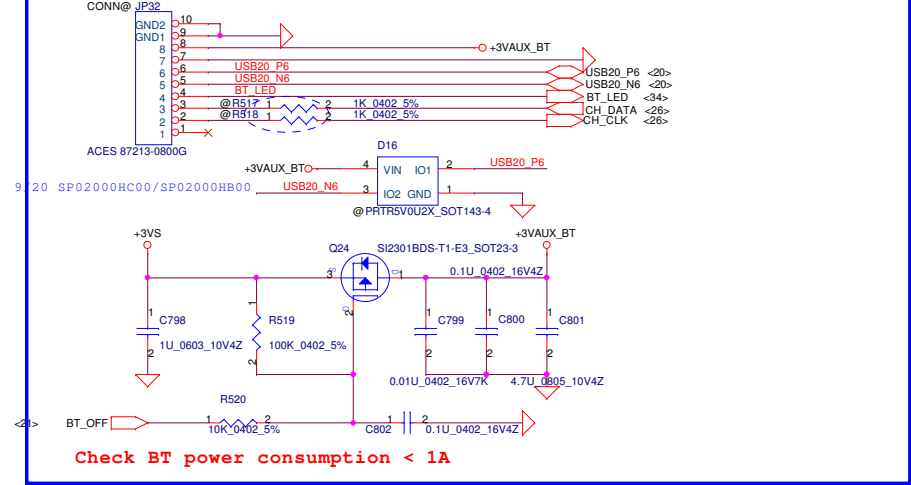
### Right side USB 0&1 Board Conn



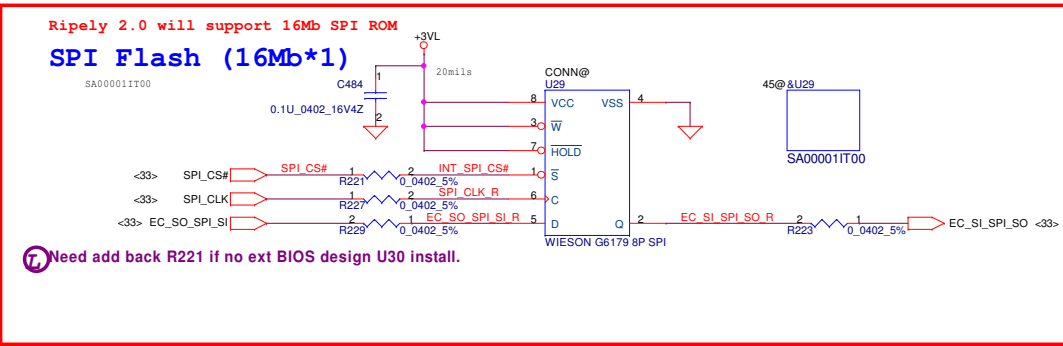
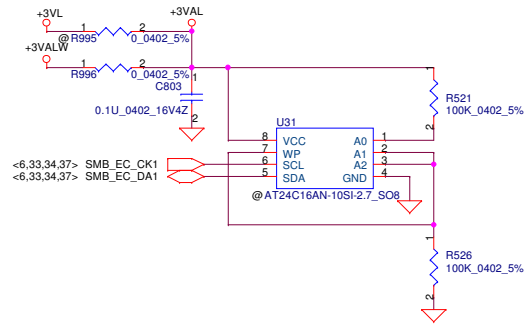
### Finger printer



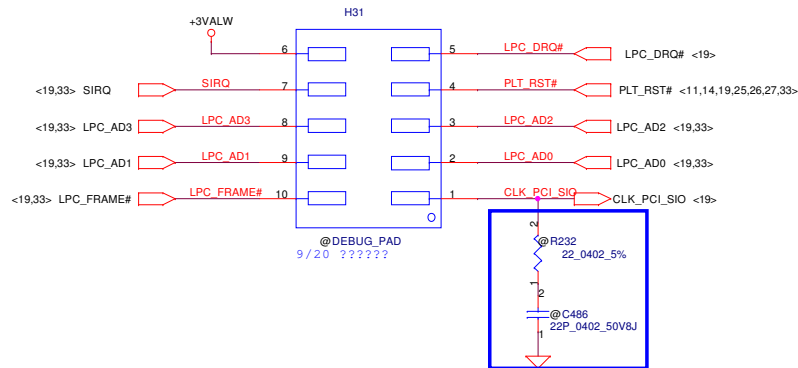
### BT Connector



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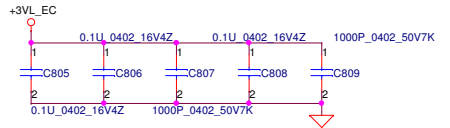


### LPC Debug Port

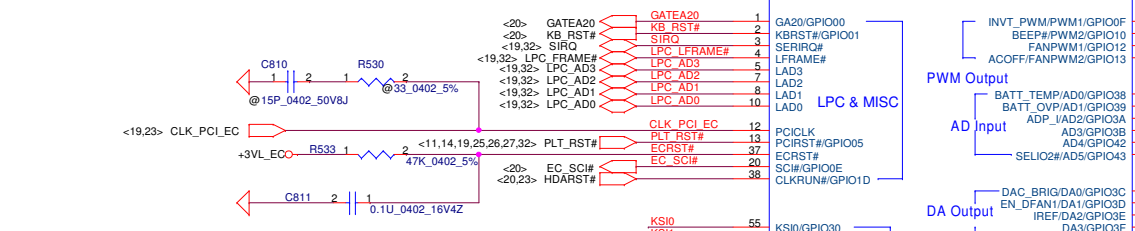


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				<b>BIOS ROM/Debug Tool</b>		
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				Custom	LA-4117P	0.3
Date:	Monday, March 16, 2009	Sheet	32	of	56	

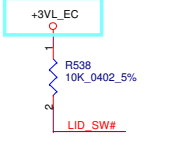




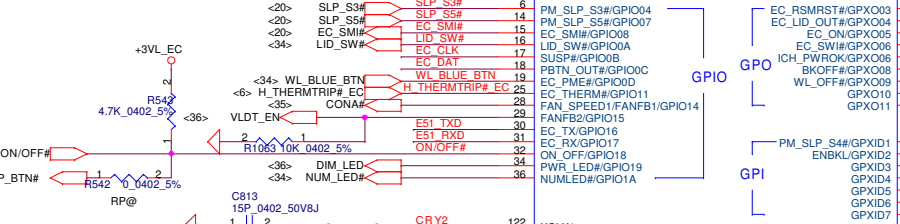
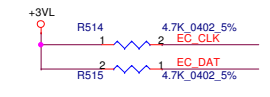
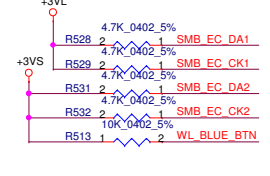
1/19 Change EC P/N to D3 version



02/22 Add R1076, C1104 and R1077 for EMI request.

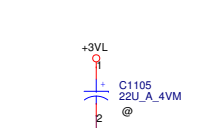
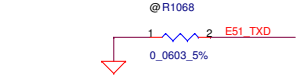


Please close to EC.

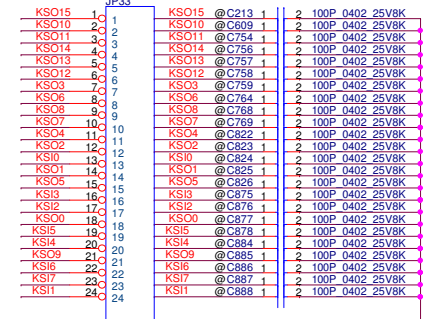


EC DEBUG port

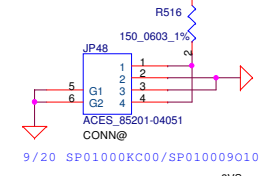
02/15 Remove JP34 and reserve R1068 for EC debug.



Keyboard Connector For EMI



KB Back Light Conn

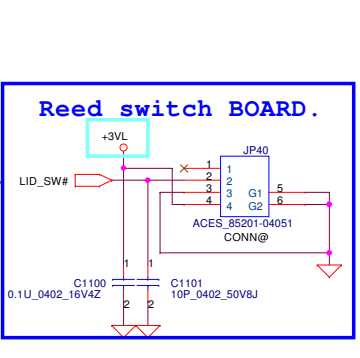
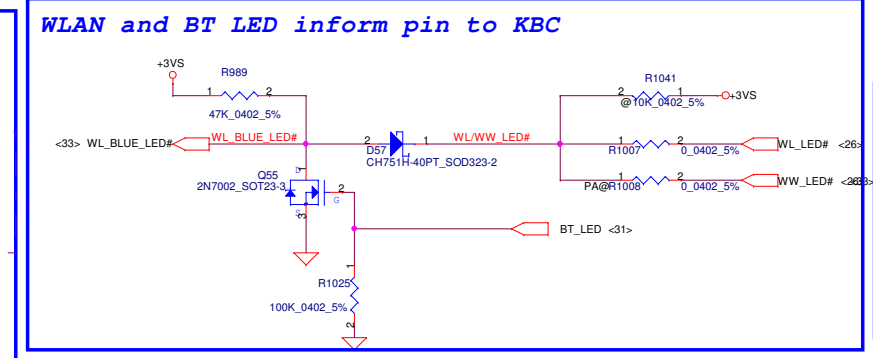
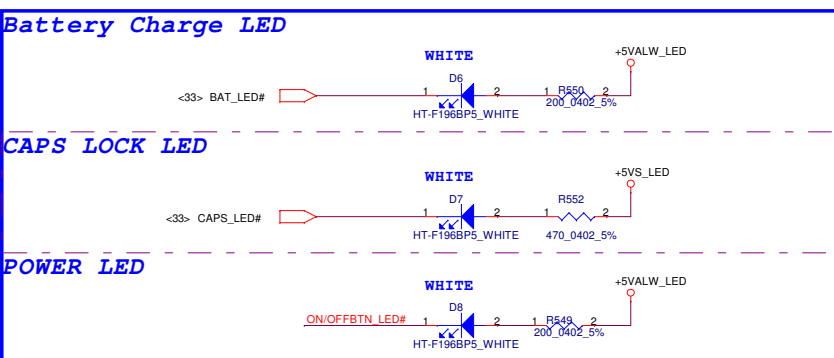
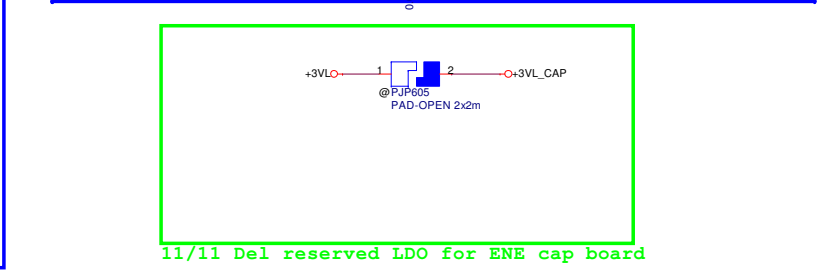
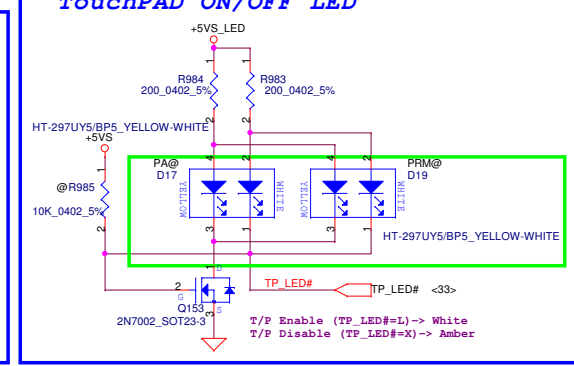
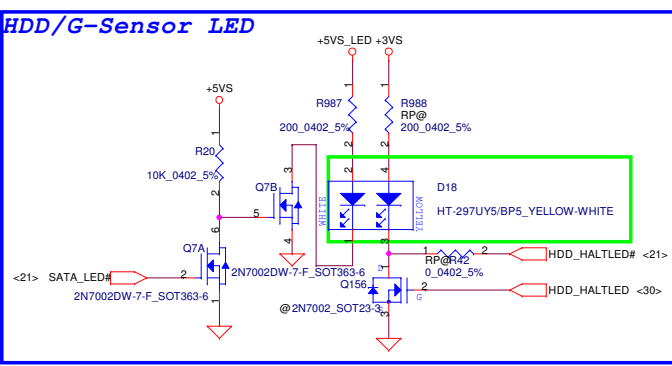
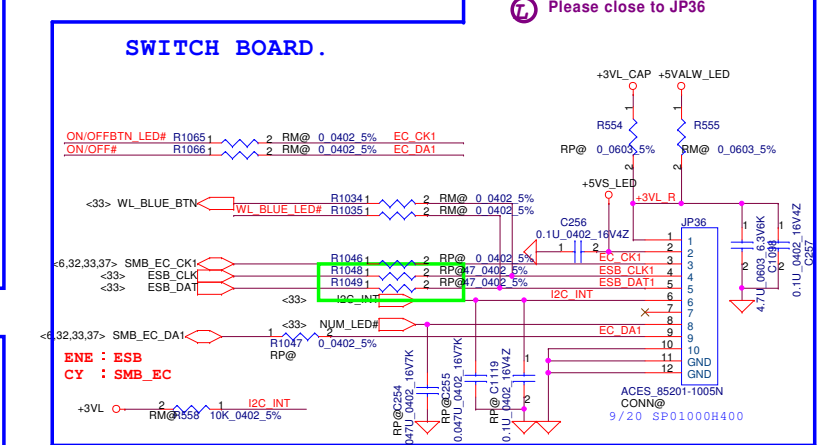
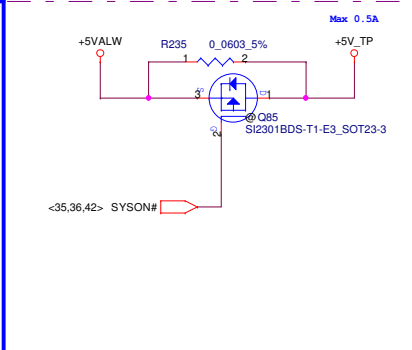
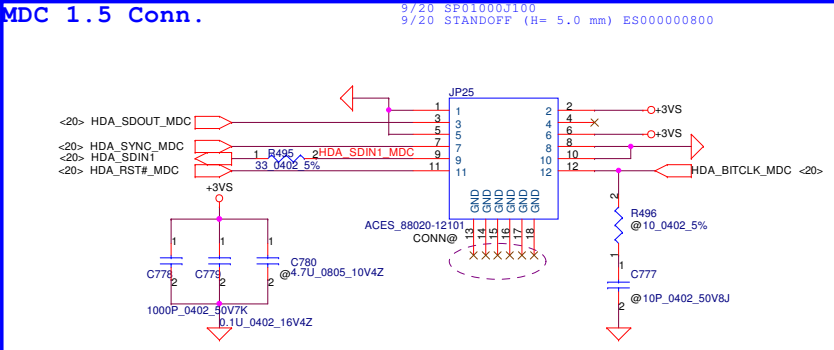
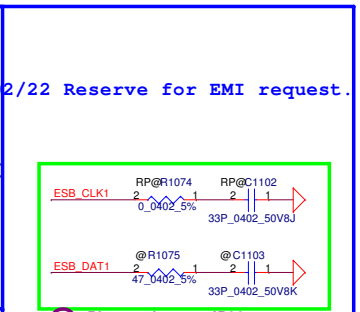
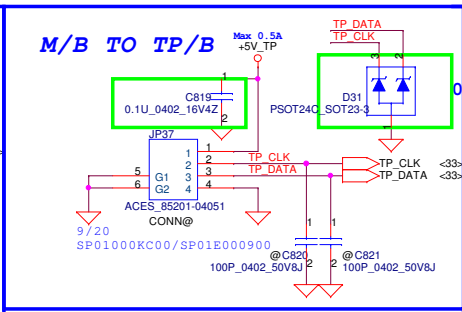
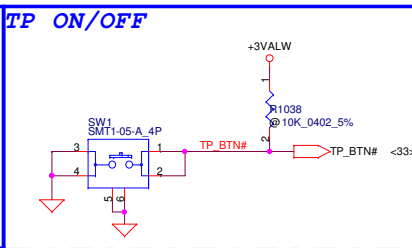
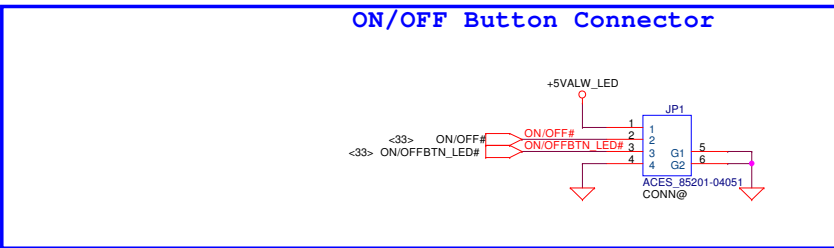


TP\_LED#=L, T/P disable  
TP\_LED#=float (GPO), T/P enable

Need 4.7uf for 926 C version

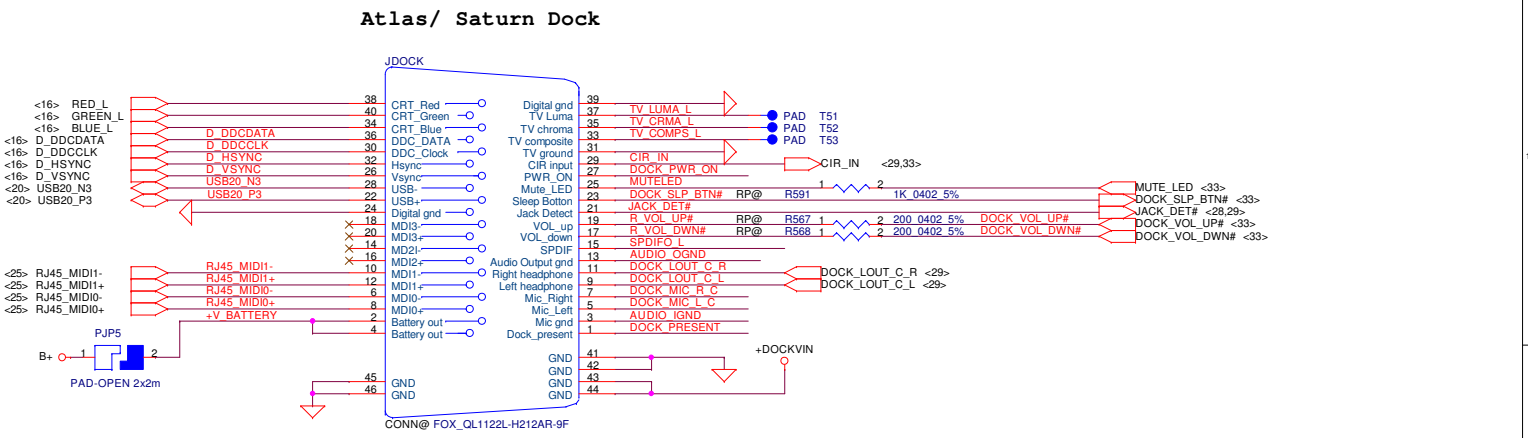
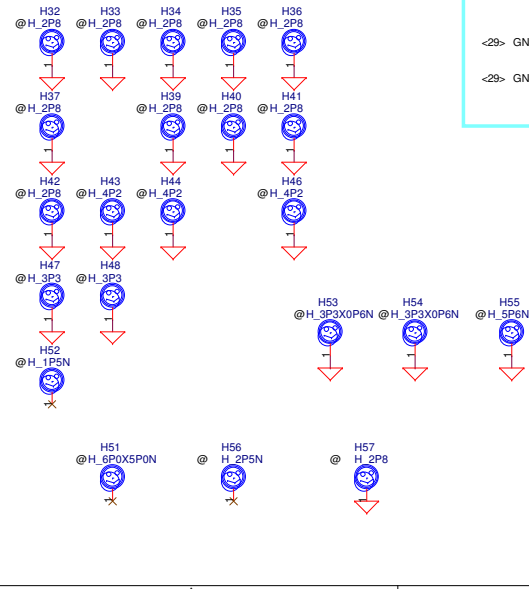
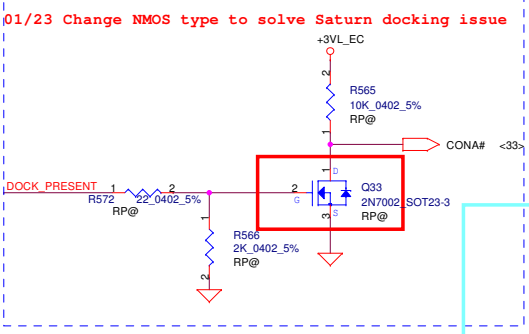
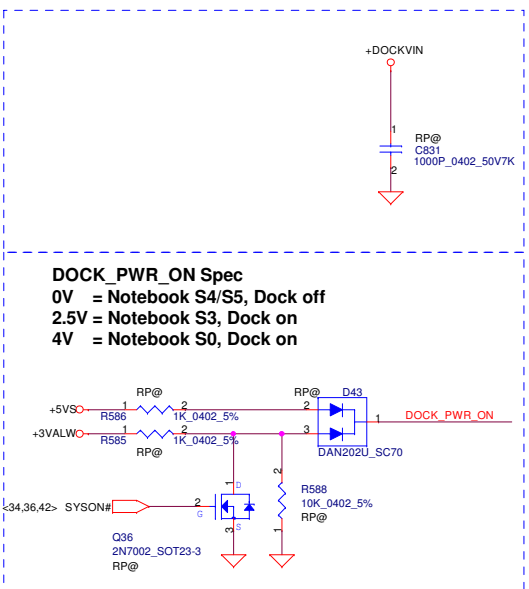
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Issued Date	2007/08/02	Deciphered Date
		2020/08/02
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Compal Electronics, Inc.		
EC KB926/KB conn		
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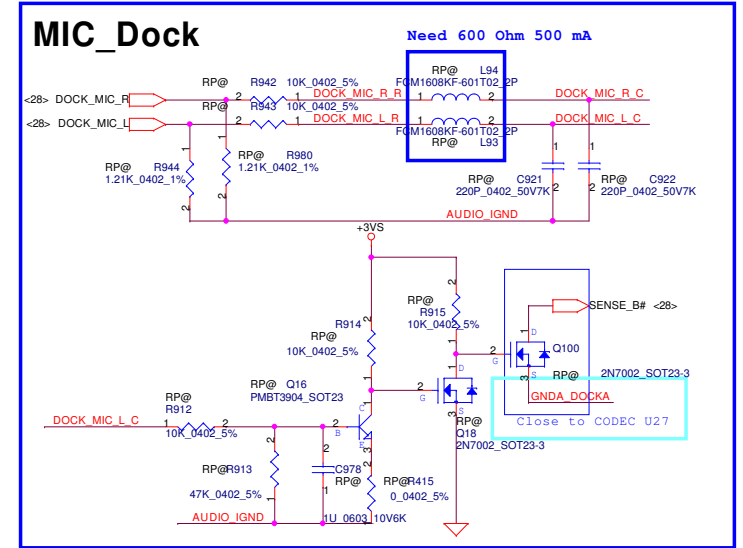
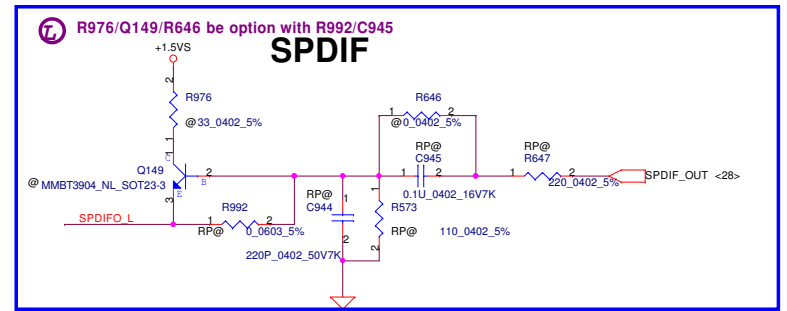
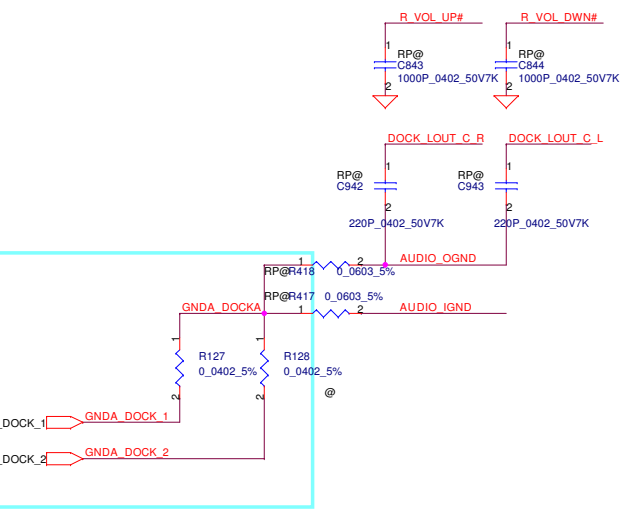


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				<b>TP,MDC,ON/OFF,S/W,LED,Reed</b>		
				Size	Document Number	Rev
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				Date	Monday, March 16, 2009	Sheet 34 of 56

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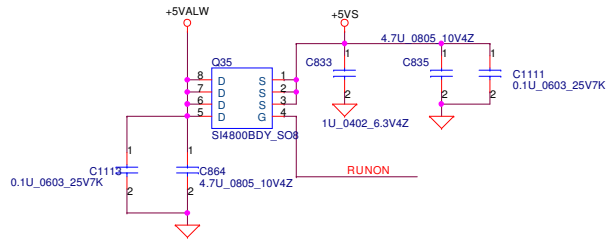


**03/03 Change JDOCK Footprint**

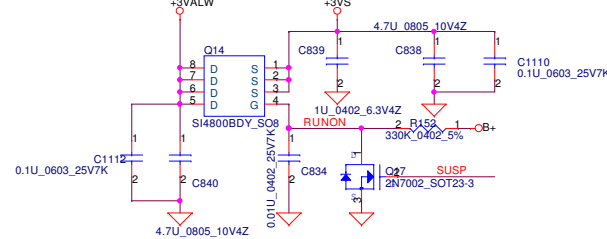


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	<b>DOCK CONN</b>	
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				Custom	<b>LA-4117P</b>
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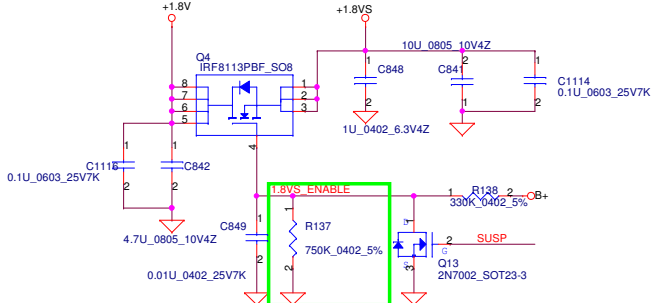
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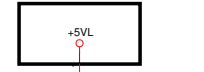
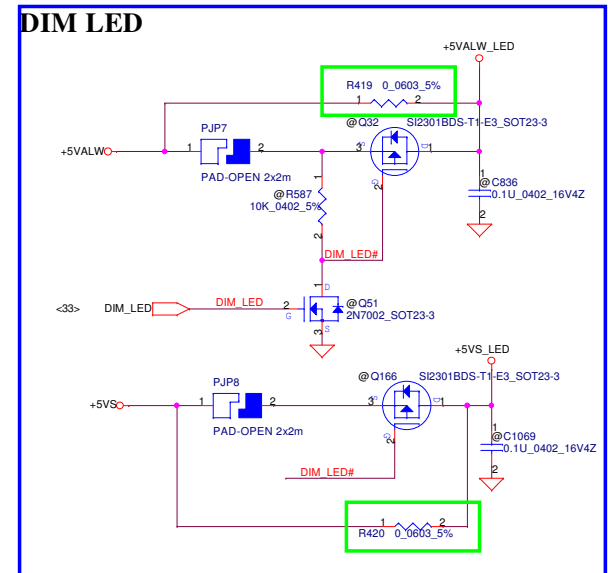
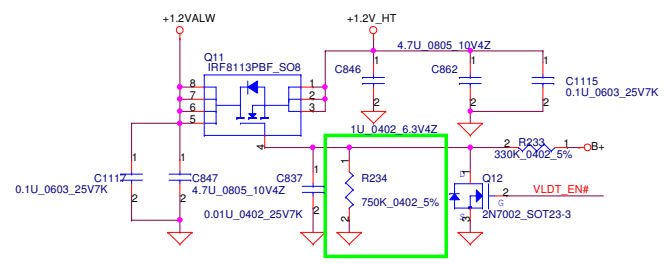
**+3VALW TO +3VS**



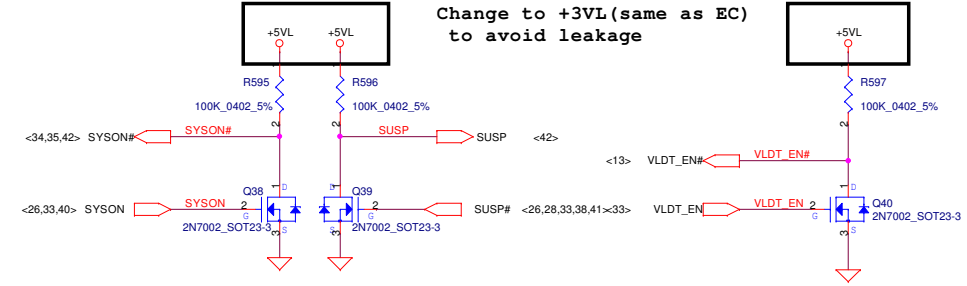
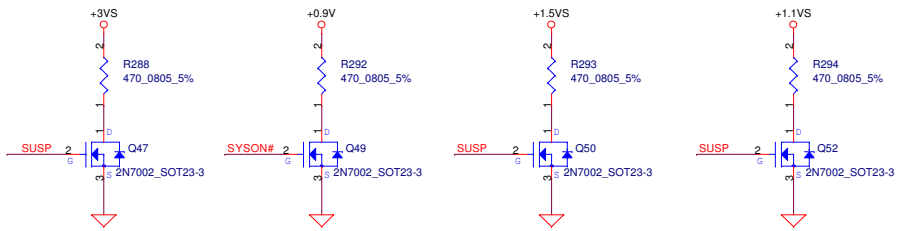
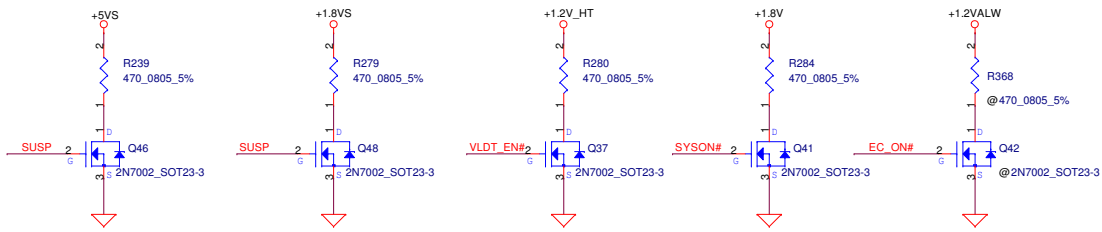
**+1.8V TO +1.8VS**



**+1.2VALW TO +1.2V\_HT**



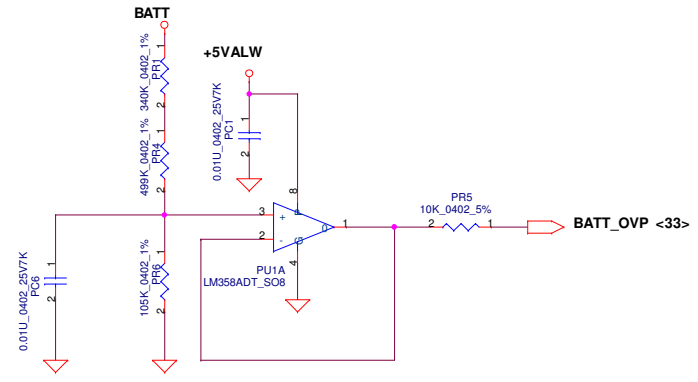
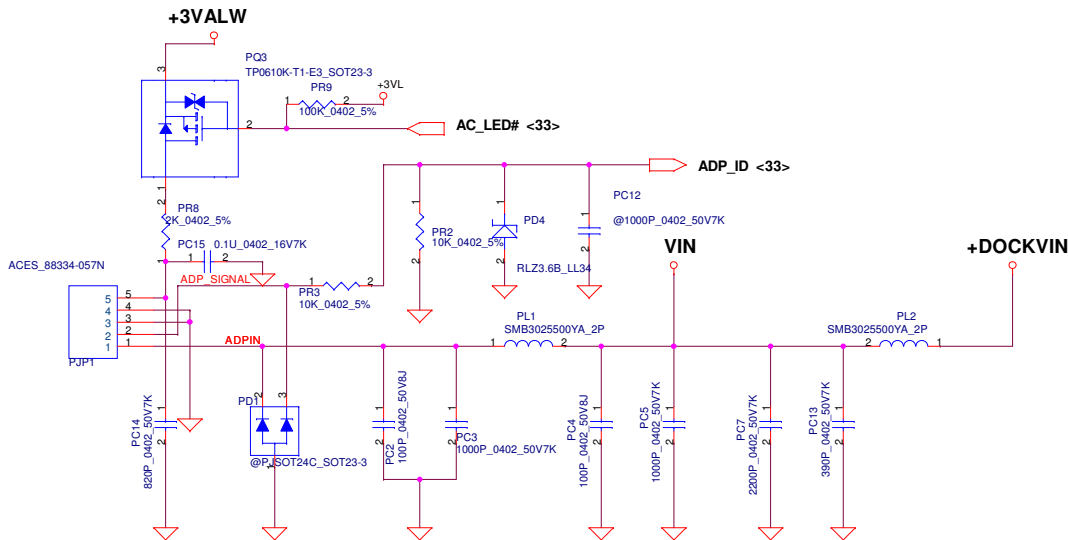
**Discharge circuit**



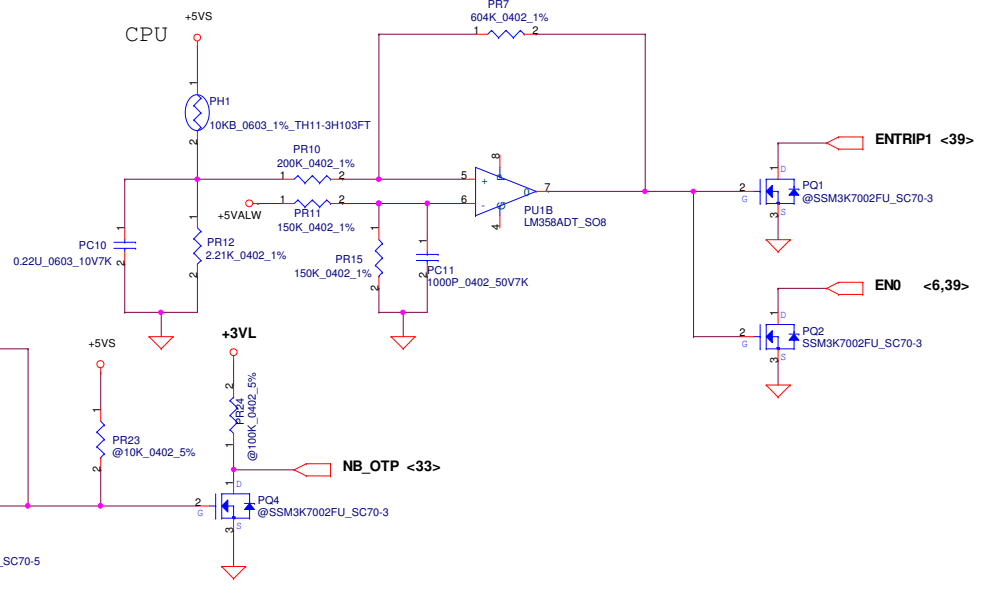
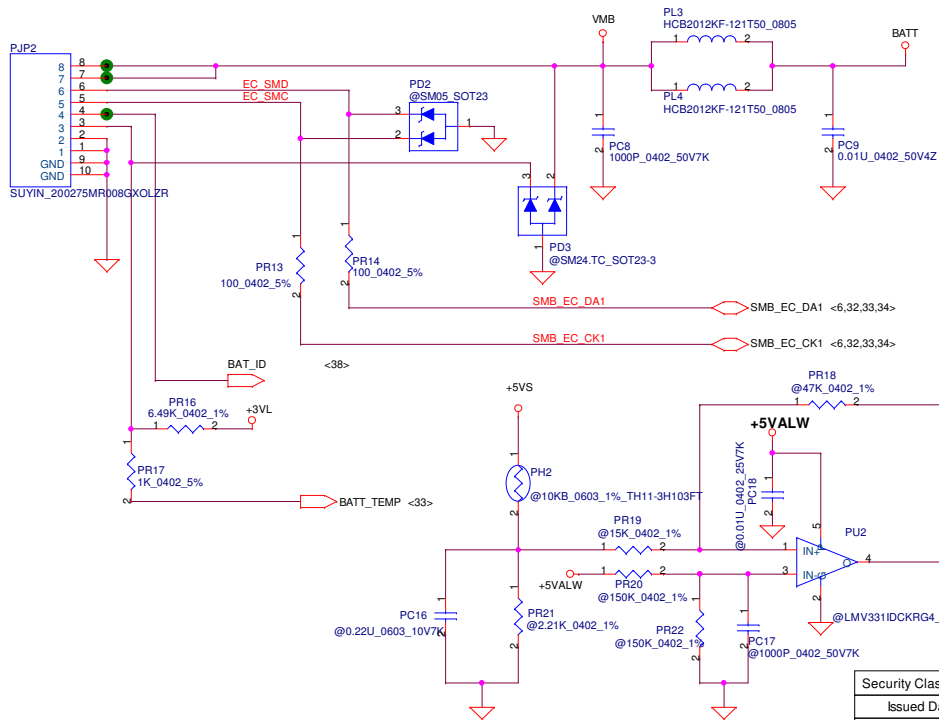
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	DC/DC Circuits	
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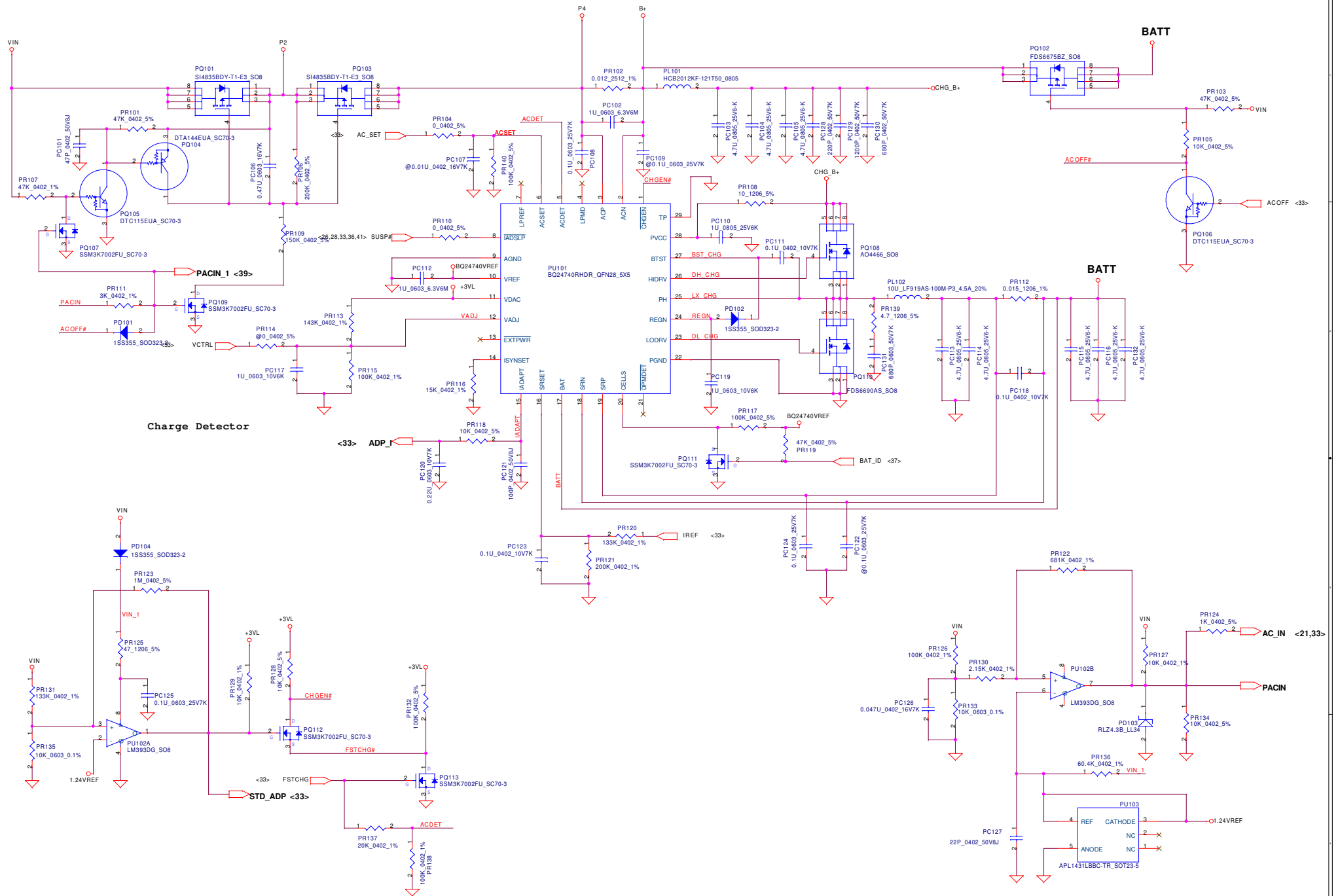
BATT1  
45@CR2032 RTC BATTERY



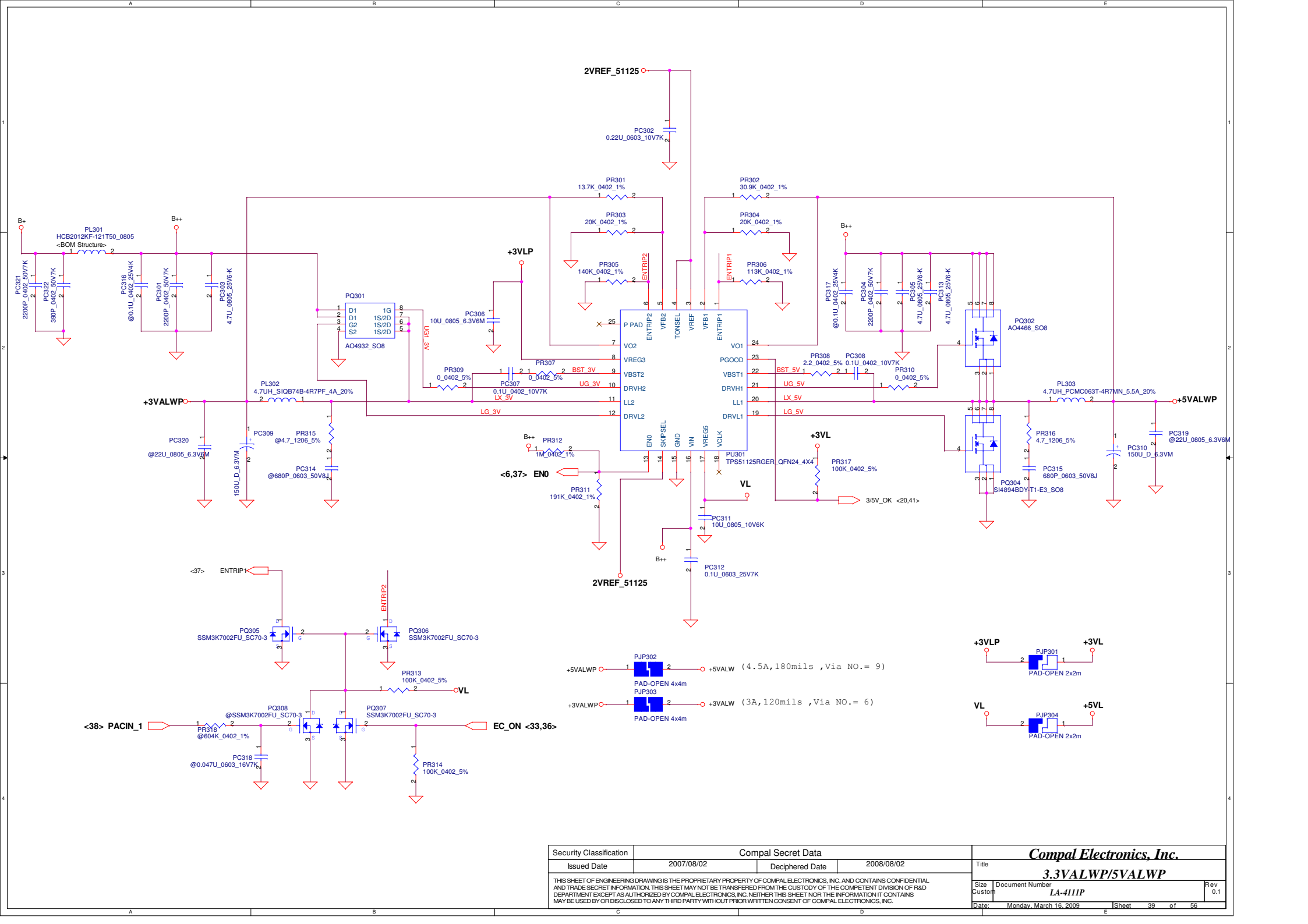
PH1 under CPU bottom side :  
CPU thermal protection at 95 +/-3 degree C



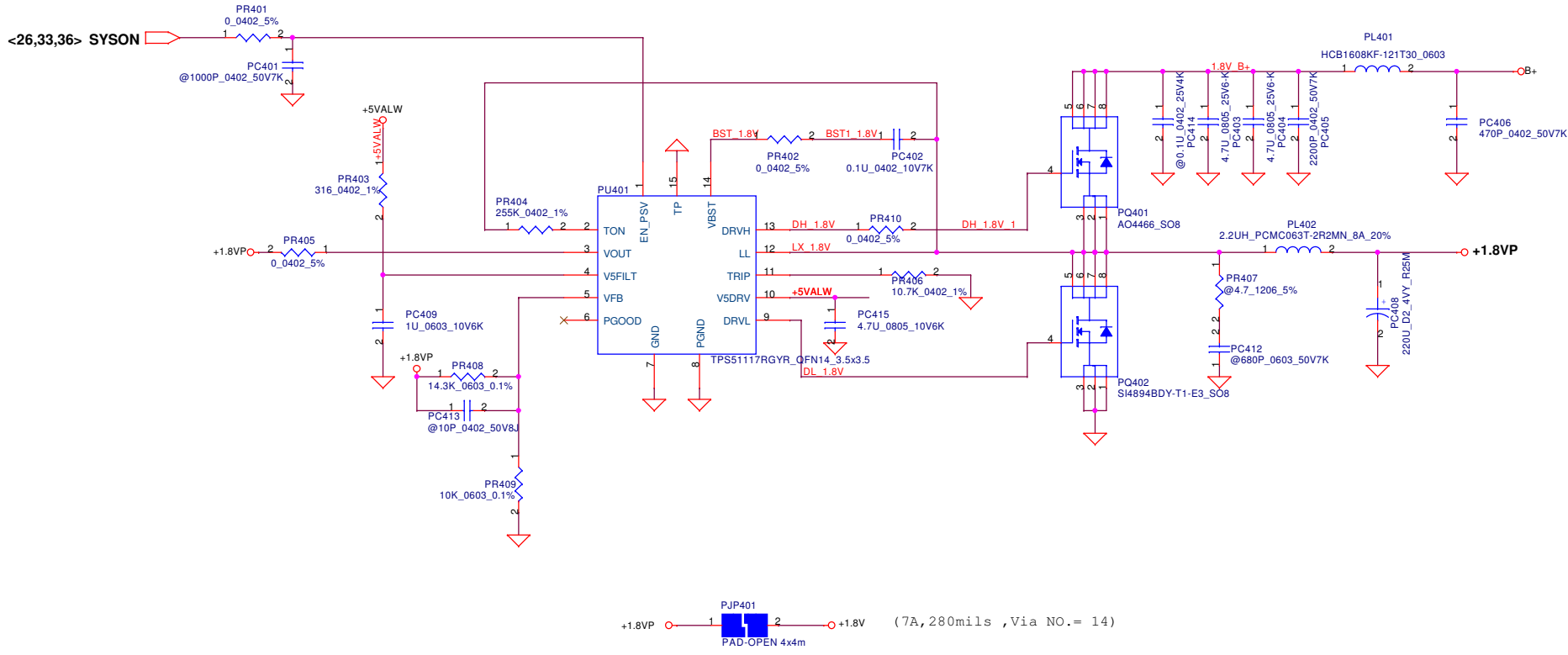
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.
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Size	Document Number	Rev		
Custom	LA-411P	0.1		
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Size	Document Number	Rev		Date	
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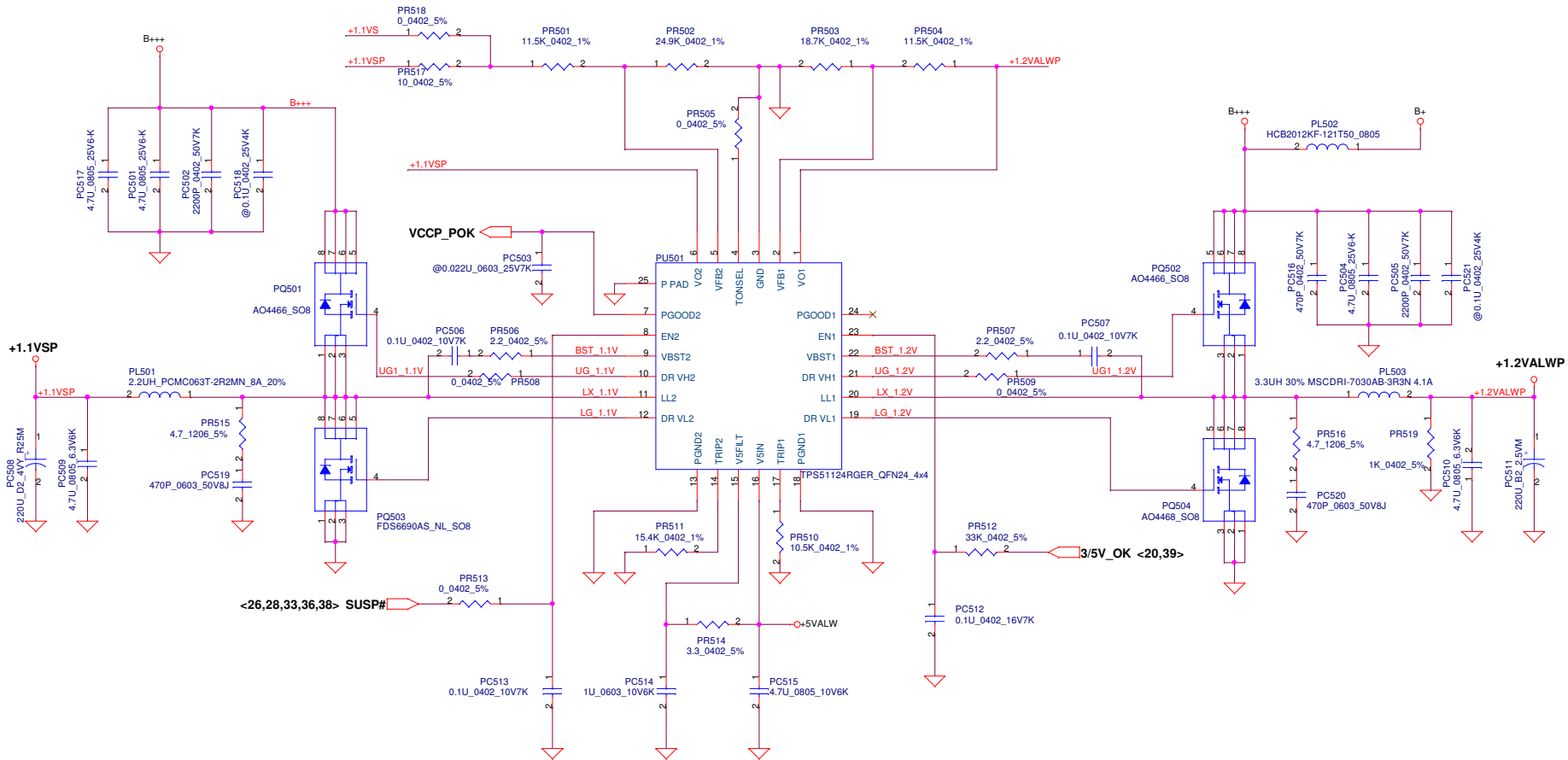
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	<b>3.3VALWP/5VALWP</b>
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Date: Monday, March 16, 2009				Document Number <b>LA-411P</b>
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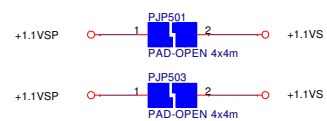
+1.8VP ○ 1 **PJP401** 2 ○ +1.8V (7A, 280mils, Via NO.= 14)  
 PAD-OPEN 4x4m

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				Date:	Monday, March 16, 2009
				Sheet	40 of 56
				Rev	0.1

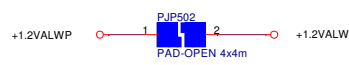




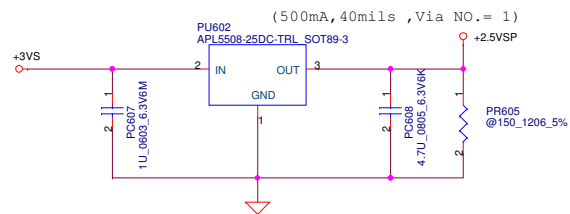
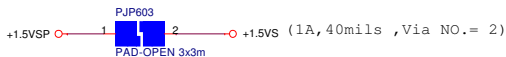
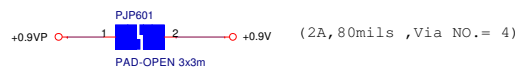
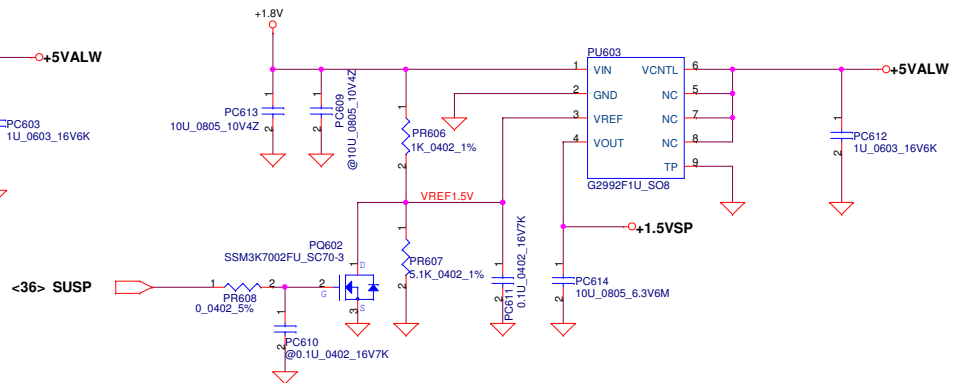
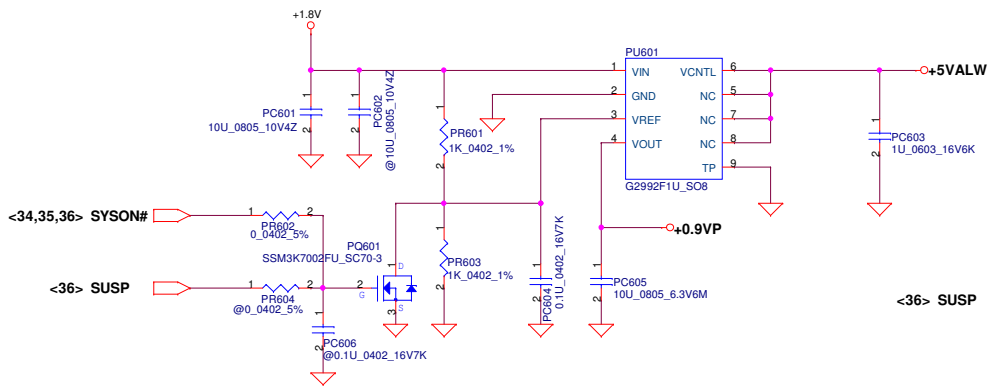
(6A, 240mils, Via NO.=12)



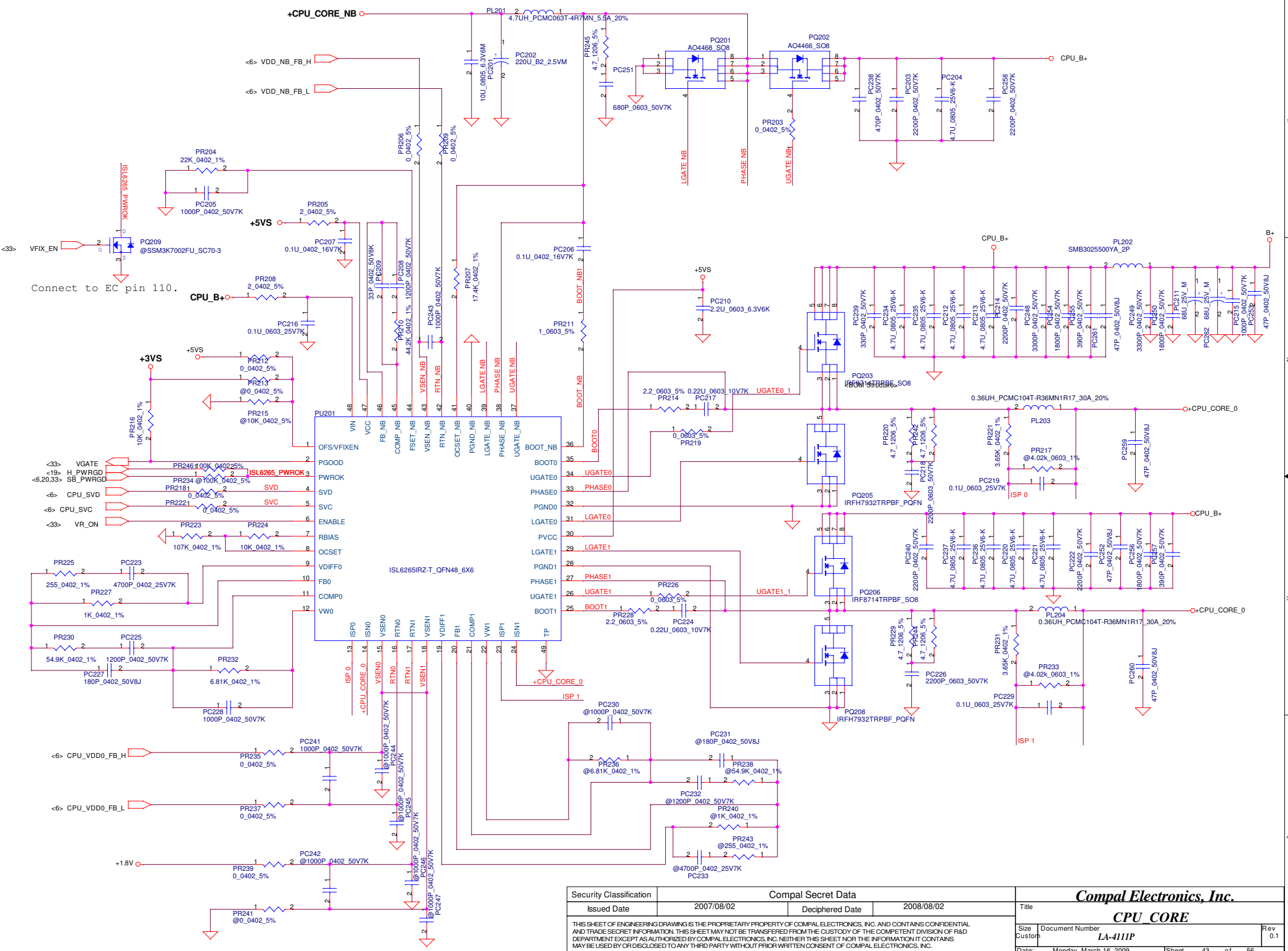
(4A, 160mils, Via NO.=8)



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Connect to EC pin 110.

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# Version Change List ( P. I. R. List ) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	9/29	Compal	for Layout	PL3 change the value from SMB3025500YA_2P to HCB2012KF-121T50_0805 and add PL4 the same of the value.	
2	41	1.1VSP/1.2VALWP	9/29	Compal	HW request	PC508 and PC511 change the value from 220U_6.3VM_R15 to 220U_D24VY_R25M	
3	41	1.1VSP/1.2VALWP	9/29	Compal	HW request	Add PJP503	
4	43	CPU_CORE	9/29	Compal	HW request	PC202 change the value from 220U_6.3VM_R15 to 220U_D24VY_R25M	
5	43	CPU_CORE	9/29	Compal	TI FAE suggested that after he review the layout.	Add PC241、PC242、PC243, and the value are 1000P_0402_50V7K. Reserve PC244、PC245、PC246、PC247, and the value are 1000P_0402_50V7K.	
6	43	CPU_CORE	9/29	Compal	TI FAE suggested that after he review the layout.	Add PJP201、PJP202	
7	38	Charger	9/29	Compal	the footprint is wrong	Change the footprint of PR102	
8	37	DC Connector /CPU_OTP	10/08	Compal	for Layout	These two choke are parallel ,it's not series.	
9	38	Charger	10/08	Compal	the footprint is wrong	Change the footprint of PR102	
10	40	1.8VP	10/08	Compal	PWR request	Delete PC410 and PC411	
11	41	1.1VSP/1.2VALWP	10/08	Compal	PWR request	Add PR517、PR518	
12	37	DC Connector /CPU_OTP	11/01	Compal	PWR request	Add PD4、PC12	
13	37	3.3VALWP/5VALWP	11/01	Compal	for Layout	change PQ301, Cencel PQ303	
14	43	CPU_CORE	11/02	Compal	EMI request	Add PC248, PC249, PC250	
15	37	3.3VALWP/5VALWP	11/12	Compal	for Layout	Change PC310, add PC319	
16	37	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
17	43	CPU_CORE	12/31	Compal	Vendor request	Change PR221 and PR231 to 16.6K_ohm Change PR217 and PR233 to 4.02K_ohm Change PR223 to 17.8K_ohm Change PR224 to 100K_ohm	

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# Version Change List ( P. I. R. List ) for Power Circuit

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18	38	Charger	01/08	Compal	EMI request	Add PC128 220pF	
19	37	DC Connector /CPU_OTP	01/09	Compal	AC LED change to KBC control	AC_LED# connect to KBC pin 97	
20	37	3.3VALWP/5VALWP	01/14	Compal	for layout	Change PC309 to D size and add PC320	
21	38	Charger	02/27	Compal	EMI request	CHG_B+ Add 1200pF and 330pF	
22	43	CPU_CORE	02/27	Compal	EMI request	CPU_B+ Add 1800pF*2 2200pF*1 and 390pF*2	
23	37	3.3VALWP/5VALWP	02/27	Compal	EMI request	B+ Add 2200pF and 390pF	
24	37	DC Connector /CPU_OTP	02/27	Compal	EMI request	VIN Add 2200pF and 390pF, ADPIN add 820pF	
25	37	3.3VALWP/5VALWP	02/27	Compal	Change OTC shun down pin.	Change OTC shun down pin to PU301 pin13.	
26	43	CPU_CORE	03/04	Compal	Change high-side MOS for WWAN issue	Change PQ203 and PQ206 to powerpak	
27	43	CPU_CORE	03/04	Compal	HW request	add H_PWRGD control net	
28	37	DC Connector /CPU_OTP	04/02	Compal	AC LED issue	Change AC_LED# pull high to +3VL	
29	43	CPU_CORE	04/24	Compal	acoustic noise	Add PC262	
30	37	DC Connector /CPU_OTP	04/24	Compal	HW CPU thermal protection change to 95 +-3 degree C	Change PR12 to 2.21K_ohm	
31	37	1.1VSP/1.2VALWP	05/23	Compal	+1.2VALW leakage	Add PR519	

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# Version Change List ( P. I. R. List ) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	25	LAN	10/29	HW	Change LAN Chip U20 from Marvell 88E8042 to Realtek RTL8102EL	Update the LAN Design page and support circuit	0.2
2	25	LAN	10/29	HPQ	Add POE(Power Over Ethernet) design	Update the LAN Design page and support circuit	0.2
3	16	CRT	10/29	HW	CRT can not display	Change the CRT Conn. signals connection first. Wait correct symbol for fix	0.2
4	29	Audio	10/30	HW	Speaker no sound	Add R973(10K_0402) to +3VALW on HP_DET#	0.2
5	4	FAN	11/01	HW	FAN Conn. not correct part	Change JP2 PCB Footprint from ACES_85204-02001_2P to ACES_88231-02001_2P	0.2
6	29	Speaker	11/01	HW	Speaker Conn. not correct part	Change JP20 PCB Footprint from ACES_85204-04001_4P to ACES_88231-04001_4P	0.2
7	34	MDC	11/01	HW	MDC Conn. not correct part	Change JP20 PCB Footprint from ACES_88018-124G_12P to ACES_88020-12101_12P	0.2
8	11,35	TV_OUT	11/05	HW	TV_OUT Function no support	Del R59,R60,R61,R115,R116,R117 and TV_OUT related design.	0.2
9	11,21	NB/SB Thermal	11/05	HW	NB Thermal Function no support (locate too far)	Cancel NB_THERMAL_DA/DC connection between NB and SB,del C500	0.2
10	21,31	SB SATA	11/05	HW	SB SATA Port 5 change to Port 2 for ATI Common Design	Change SB SATA port 5 to port 2	0.2
11	21	SB SATA	11/05	HW	SB SATA_ACT# Pull High become +3VS	Change R343.1 power rail from +5VS to +3VS. Install R343.	0.2
12	21	SB GPIO	11/05	HW	Change SB GPIO refer to JBX00 for common	1. Connect U15.C6 to GND by 0_0402. 2. Change WLOFF# from GPIO50 to GPIO61. 3. Change BT_COMBO_EN# from GPIO51 to GPIO62. 4. Change WWOFF# from GPIO52 to GPIO63.	0.2
13	31	SB SATA	11/05	HW	Vertical L51 1<->4 , 2<->3 for layout routing	Vertical L51 1<->4 , 2<->3 for layout routing	0.2
14	29	Audio HP OUT	11/05	HW	Add 150UF Caps for each DOCK_LOUT_R/L	Add 150UF Caps for each DOCK_LOUT_R/L	0.2
15	25	LAN Transformor	11/05	HW	Correct U19 LAN Transformor pin definition	Correct U19 LAN Transformor pin definition	0.2
16	21,24	SB SATA	11/06	HW	SB SATA Port 4 change to Port 3 for ATI Open Issue	Change SB SATA port 4 to port 3	0.2
17	36	DIM LED	11/06	HW	Reduce DIM LED unnecessary design	Del R1026 and Q167, add Net 'DIM_LED#' for connect. Change location from PJP604 to PJP8.	0.2
18	27	CardReader	11/06	HW	Change CardReader Socket for M/E new part and Chip for JMicron new version	Change JREAD to TAITW_R015-B10-LM. Reserve R413,C902 close to JREAD.20; R412,C901 close to JREAD.26; R411,C900 close to JREAD.37. Change R457 close to U23.42 Add R455,R456 close to U23.42 Del Q169,R1051. Change net CR_LED# become CR_LED connect U23.21 and Q53.2 Add R454 pull down to GND Change R405,R122 from 200K to 10K pull-high Remove C895,U22	0.2

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# Version Change List ( P. I. R. List ) for HW Circuit

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19	16	CRT	11/07	HW	Normalize CRT design for common	Change L83,L84 (10_0402) become R241,R240 (0_0603)	0.2
20	17	LCD	11/07	HW	Normalize LCD design for common	Change R491 from 200_0402 to 200_0805	0.2
21	18	LCD	11/07	CIC	CIC feedback RMA concern for common	Change Q43 from AOS3413 to SI2301	0.2
22	33	KBC	11/07	HW	Normalize KB926 Crystal part for common	Change Y7 from 9H03200413 small to 1TJS125DJ4A420P normal.	0.2
23	17	WebCam	11/09	HW	Change U54 WebCam power design and related	Change U54 from G916-390T1UF to RT9193-39GB. Remove R891,R892 if no use G916-390T1UF. Add C718 close to U54.4 for RT9193-39GB. Remove R1027~R1030 for JP7 no install. Change JP7 from 8pin to 6pin	0.2
24	18	HDMI	11/09	HW	Reduce HDMI Design	Remove R490(100K_0402)	0.2
25	19,32	SB-CLK-Debug	11/09	HW	Debug Card no function issue	Del R1031,add R303 close to R301 and U15.P2 Connect for CLK_PCI_SIO2 to JP41.15	0.2
26	25	LAN	11/09	HW	RJ45 LED Power correct back	Change JRJ45.13, JRJ45.11 from +3V_LAN_LED to +3V_LAN	0.2
27	18	HDMI	11/09	HW	Reduce HDMI Design	Remove R490(100K_0402)	0.2
28	6	CPU	11/09	HW	Add H_THERMTRIP# one more way	Add R16 close to Q3.1 for H_THERMTRIP#	0.2
29	33	KBC	11/09	HW	Update KBC Pin Definition for common	Add H_THERMTRIP# to U33.25	0.2
30	35	Holes	11/09	ME	Update for M/E Drawing	Del H49 H50 H38 H45 for M/E drawing change	0.2
31	26	Mini-Card	11/09	HW	Reduce Mini-Card design, change SIM Card design	Replace D17 and D47 become R52 and R53 Del R400 and R46, Change JP6 pin definition for common	0.2
32	33	KBC	11/09	HW	Reserve 0_0603 for KB Back Light	Add R516 (0_0603) between JP48.1/4 and +5VS_LED	0.2
33	27	CardReader	11/10	HW	Correct CardReader LED part	Change D5 from SC500004E00(AQUA_WHITE) to SC500004W00(WHITE)	0.2
34	34	LED Function	11/10	HW	Correct LED function for common	Change LED from D50,D30,D27 SC500004E00 (AQUA_WHITE) to D6,D7,D8 SC500004W00(WHITE) Change LED from D45,D46 SC500004B00 (AQUA_WHITE/AMBER) to D17,D18 SC500005M00 (YELLOW/WHITE); Add Q7,R20 and R42 close to D18	0.2
35	21	SB-GPIO	11/10	HW	Add one more way for GSENSOR LED# inform pin	Add HDD_HALTLED# connect from U15.P8	0.2
36	33	KBC-GPIO	11/11	HW	Add CIR_IN PH to +5VL Add ESB_CLK/DAT PH to +3VL	Add R46 10K_0402 PH to +5VL close to U33 Add R514,R515 10K_0402 PH to +3VL close to U33	0.2
37	6,31	CPU,FPR	11/13	HW	Reduce S3 power consumption	Change R15.2,R21.2,R36.2,R30.2 connection from +1.8V to +1.8VS; Remove R622, install R581	0.2
38	11	NB	11/13	HW	Reduce the level shift design for Chip A12.	Del Q6,R87; Q5,R84 and replace by 0ohm (add R67,R68) connect directly. Install R371 (10K ohm)	0.2
39	17	WebCam	11/13	HW	Update the WebCam+Digital Mic reserver conn.	Change JP7 from SP02000HC00(8pin)->SP020001L00(6pin)	0.2
40	6,33	CPU,KBC	11/13	HW	Update THERMTRIP# design to EC	Change R16.2 connection from THERMTRIP# to THERMTRIP#_EC for separate	0.2
41	18	HDMI	11/13	HW	Remove EMI solution become reserve for verify	Add R112,R113,R115~R120 close to each L85~L88 for co-lay	0.2

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42	19,32	SB,BIOS	11/13	HW	Reduce SB related design for Chip A12 and others	Del Q155,R986, and add R311 close to U15. Del R1011 become T18, Cancel R1012 and connect to H31 and JP41 directly	0.2
43	21,32	SB,BIOS	11/13	HW	BIOS Debug Tool reserve	Add SB_IN(T_FLASH_SEL and related (JP12,U30,R228,R226,C489 close to U29)	0.2
44	25	LAN	11/13	HW	Update LAN Chip Symbol link to CIS server	Update LAN Chip U20 Symbol link to CIS server	0.2
45	13	NB	11/13	HW	Add 0ohm_0603 to separate VDD18_MEM	Add R1051(0_0603) between +1.8VS & +1.8V_VDD_SP	0.2
46	18	HDMI	11/13	HW	Reduce HDMI related design for common	Del R490 (100K_0402)	0.2
47	20	SB	11/13	HW	Reduce SB related design for common and A12 chip	Remove R994 (0_0402) Change U15.F1 connection become test point Remove R1053, change R1052 become 0_0402	0.2
48	20,21,27	SB,Cardreader	11/13	HW	Reserve Cardreader D3E function (CR_WAKE# & CR_CPPE#)	Add R81 close to U15;Q54,R124 close to U23 for connect U15.F8 to U23.13 ;Add R369 close to U23 for connect U15.M5 to U23.16	0.2
49	21,33	SB,KBC	11/13	HW	Reduce SB related design for common	Del D51 and R1034, Change the net AC_IN become AC_IN_D	0.2
50	28,33	Codec,KBC	11/13	HPQ	EC_BEEP function for KBC add	Add R563 close to C955; Add R544 close to U33.31	0.2
51	33	KBC	11/13	HW	Reduce S5 Power Consumption	Change R1040.1 connection from +3VL_EC to +3VALW Del R546 PH to +3VL_EC, Del D26 replace by add R547 close to U33 for short	0.2
52	33	KBC	11/13	HW	Reduce KBC Design for common and Ver:C0 Chip Change from SA000019530 to SA000019540	Del R537 become Test Point, change R516 become 150_0603 Remove R1044, change R1040 from 10K to 100K Change R528.2 , R529.2 connection from +5VALW to +5VL	0.2
53	34	Switch Design	11/13	HW	Update CSD function board design for common	Install C814 (4.7u_0805) Change JP36.1 connection become +3VL;Change R1046.1 and R1047.1 connection become SMB_EC_CK1/DA1 Change JP36.7 connection from GND to +5VALW_LED by Change Q153 from 2N7002DW to 2N7002	0.2
54	34	LED	11/14	HW	Correct T/P On/Off LED design define Correct G-Sensor LED design define	Change R988.1 connection from +5VS_LED to +3VS	0.2
55	29	Audio-Dock	11/14	HPQ	For GS mark requirement	Add R968,R969 close to C775/C776.	0.2
56	29	Holes	11/14	ME	Update Holes to meet M/E Drawing	Add back H52 become H_1P5N; Del CF4	0.2
57	4,24	Multi-Bay	11/14	ME	Update Symbol to meet M/E Drawing	Update JP2,JP9,JP10,JP11,JP20,JP40,JPDMI,JPESAT,JPCT,JPDOCK Symbol	0.2
58	33	Holes	11/14	ME	Update Holes to meet M/E Drawing	Add back H52 become H_1P5N; Del CF4	0.2
59	20	SB	11/16	ATI	Reserve to fix the OTS325055 Issue	Reserve R83 PH to +3VS	0.2
60	33	KBC	11/16	EC	Change design for EC team debug	Change JP34.1 from +5VALW to +5VL	0.2
61	35	DOCK	11/16	EMC	Connect DOCK guide pin to GND	Add JDOCK.45/46 to GND	0.2
62	33	K/B	11/16	HW	Fix KB matrix issue	Del KS16 and KSO9 out of page net connect	0.2
63	28,29	AUDIO	11/18	HPQ	Make some Audio related design change	Change C983,C984 from 1uF to 0.022uF. Change C1049,C1050,C1040,C1041 from 0.47uF to 0.022uF. Change R1002,R1005 from 20K to 0 ohm. Change C1044 from 10uF to 4.7uF. Remove R1000,R1004; Install R1001,R1003.	0.2
64	29	AUDIO	11/19	HPQ	Make some Audio related design change	Change R968,R969 from 40.2_0402 to 47_0603	0.2

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65	13	NB	11/20	ATI	Design Change for NB A12 Version chip	Remove U64,C1064,C1065,C1066,C1067,R1015,R1016,Q163,R1017. Install L19, remove L95	0.2
66	22	SB	11/20	ATI	Design Change for SB A12 Version chip	Install R593, remove R592	0.2
67	22	SB	11/20	HW	Reduce SB Power Design-No IDE support	Remove R12,C543,C544,C547,C536	0.2
68	33,34	Function Board	11/20	HW	Reserve for Rachman UMA selective	Reserve R555 for +5V <sub>ALW_LED</sub> , add R554 for +3V <sub>L</sub> close to JP36.1 Reserve R1034 close to JP36.4,R1035 close JP36.5,Remove R1036 Add R513 PH to +3V <sub>S</sub> close to U33.19	0.2
69	23	SB	11/20	HW	Make the SB Strap Seeting for common	Install R356 (10K_0402)	0.2
70	31	BlueTooth	11/20	HW	Update BT design for common	Change R520 from 47K_0402 to 10K_0402	0.2
71	34	Power On Switch	11/22	HW	Cancel one reserved power on switch	Del SW3	0.2
72	33	KBC	11/22	HW	Modify SMB_EC_DA1/CK1 PH for common	Change R528,R529 pin 2 connection from +5V <sub>L</sub> to +3V <sub>L</sub>	0.2
73	6	CPU	11/22	HW	Link PROCHOT# between CPU and NB	Add R59 close to Q2	0.2
74	19	SB	11/22	HW	Reserve LPCLK1 for debug card function	Add R308 22_0402 for U15.E22 close to R362.1, remove R301	0.2
75	26	Express Card	11/22	HW	To avoid New Card Switch leakage issue	Add R54(0_0402) close to U21.6	0.2
76	28	Audio Codec	11/22	HW	Reserve SPDIF OUT1 test point for verify	Add T21 close to U27.45	0.2
77	10~13	NB,	11/23	HW	BOM correct for SI-1 SMT build	update U3(SA00001ZG00-->SA00001ZG20);U10(SA00001Z300-->SA00001Z310);U15(SA00001S510-->SA00001S560)	0.2
78	19	SB	11/23	HW	Change Crystal Res. size for layout space	Change R389 from 0603 to 0402	0.2
79	22	SB	11/26	HW	Reduce SB SATA Power Caps (Confirm with ATI FAE)	Change C567,C568 from 10U_0805 to 1U_0805	0.2
80	28	Codec	11/26	HW	SPDIF0 --> 1 design change to follow Vader	Change U27.48/45 pin connection	0.2
81	34	T/P	11/28	HW	Change T/P Power for reduce S4/S5 power consumption	Remove R235; Add Q85, R645, Q34	0.2
82	14	HDMI	11/28	ATI	Fix HDMI no function issue	Remove R102; Add R101	0.2
83	15	CLK Gen.	11/28	HW	Change design for new version CLK Gen.	Remove R1045	0.2
84	28	Codec	11/28	HW	Change EC_BEEP function become reserve	Remove R563	0.2
85	20,27	SB,CardReader	11/28	HW	Disconnect D3E support for A version to avoid risk	Remove R81,R369	0.2
86	32	BIOS	11/28	HW	Use Ext. BIOS as default	Remove R221	0.2
87	34	LED	11/28	HW	Cancel WLAN/WWAN ext pull high	Remove R1041	0.2
88	19	SB	11/30	HW	Fix PA M/E Interfere issue for SI-1	change Y3 from SJ100001U00 to SJ100006600 with 10PPM	0.2
89	06,19,23	SB	11/30	ATI	ATI recommend for update	Change R312 from 0_0402 to 33_0402; Change R356 from 10K_0402 to 2.2K_0402; Install C23 as 0.1UF_0402	0.2
90	33	KBC	11/30	HW	Change 32.768KHz Main Source Vendor become EPSON	Change Y7 from SJ100001V00 to SJ132P7K220	0.2
91	32	BIOS	12/03	HW	Cancel Ext. BIOS reflash design because of +3V <sub>L</sub> erroe	Add R221; Remove U30,R226,R228,C489	0.2
92	34	LED	12/03	HW	Cancel G-Sensor INT2 LED function	Remove Q156	0.2

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# Version Change List ( P. I. R. List ) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	19	SB	12/26	HW		Remove R303 from PCICLK3 and add R301 as 0 ohm.	0.3
02	19	SB	12/26	HW		Add R303 and connect to CLK_PCI_ISO2.	0.3
03	23	SB	12/26	HW		Change net name to PCI_CLK3.	0.3
04	29	Amplifier	12/26	HW		Change value from 4.7uF to 1uF.	0.3
05	23	Speaker	12/26	HW	Speaker right and left channel reverse.	Reverse JP20 pin define.	0.3
06	31	Finger Printer	12/26	HW		Delete R622	0.3
07	32	BIOS ROM	12/26	HW		Reserve R221	0.3
08	32	BIOS ROM	12/26	HW		Stuff U30, R228, R226, C489. Change power from +3VALW to +3VL	0.3
09	33	EC	12/26	HW		Add pull down resistor R1063.	0.3
11	34	T/P ON/OFF LED	12/26	EC	Common design.	Reverse TP on/off LED	0.3
12	35	Docking	12/26	HW		Change R572 to 22 ohm and R566 to 2K ohm	0.3
13	35	MDC	12/26	ME	ME change stand off.	Change PCB Footprint from 3P3 to 4P0	0.3
15	34	Switch board	01/03	HW	Useless	Delete R556, R557.	0.3
16	34	Switch board	01/03	HW	Useless	R1036	0.3
17	34	Switch board	01/03	HW	Option Cypress and ENE Cap. board.	Connect R1046 to JP36.3 and connect R1047 to JP36.9	0.3
18	33	EC	01/07	Power		Connect VFIX_EN to EC pin 110.	0.3
19	14	SB	01/08	HW		Add pull high resistor R1064.	0.3
20	17	Webcam and Digital MIC	01/08	HW		Remove reserve circuit for Webcam and Digital MIC.	0.3
21	22	SB	01/08	HW		Change L61, L63, L66, L60, L67, L68, L69 to 0 ohm resistor. Change C528, C543, C566, C504 to MLCC type. Change C552 from 22uE to 4.7uF.	0.3
22	25	LAN	01/08	Realtek		Change part number from SA000026Q00 to SA000026Q10	0.3
23	31	USB port	01/08	Layout		Swap D11, D12, L51 pin define per layout request.	0.3
24	19	SB	01/09	EMI		Add reserve cap. C1085~C1087.	0.3
25	19	SB	01/09	EMI		Fine-tune R302, R303, R308 from 22 ohm to 33 ohm.	0.3
26	20	SB	01/09	EMI		Add reserve cap. C1088~C1091	0.3
27	21	SB	01/09	DFB		Y4 Change Footprint to the same as Y2.	0.3
28	25	LAN	01/09	DFB		Change Y5 Footprint to the same as Y2.	0.3
29	26	WWAN	01/09	EMI		Add C738, C739, C740, C750, C751 as 39pF	0.3
30	33	EC	01/09	HW		Connect AC_LED# to PQ3	0.3
31	35	M/B	01/09	ME		Add screw hole.	0.3
32	36	DC-DC	01/09	HW		Remove +1.2V and +3V circuit.	0.3
33	34	Switch board	01/10	HW		Add R1065 and R1066 for OPP power button board	0.3
34	33	Keyboard connector	01/10	DFB		Change Keyboard connector same as JBK00.	0.3
35	34	Lid switch connector	01/10	DFB		Change Lid switch connector type.	0.3
36	34	Switch board	01/10	EMI		Change R1048 and R1049 from 0 ohm to bead.	0.3
36	06	HDT debug port	01/14	AMD		Stuff R26, R28 and R41.	0.3

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37	25	LAN	01/14	HW	8102E (10/100M 48 pin) can not support DSM function.	Reserve Q1056, Q1057, C1077 and Q144. Change PJP605 to R1067.	0.3
38	33	EC	01/14	HW	8102E (10/100M 48 pin) can not support DSM function.	Reserve R544	0.3
39	11	NB	01/15	HW	No support daul channel panel.	Remove LVDS signal of Channel B.	0.3
40	17	LVDS	01/15	HW	No support daul channel panel.	Remove LVDS signal of Channel B (remove C1061~C1063)	0.3
41	15	Clock GEN.	01/15	HW	To slove noise issue.	Chagne C1074~C1076 to 12pF	0.3
42	15	Clock GEN.	01/15	Vendor	Clock Gen. spec. update	Change R379 to 158 ohm and R380 to 90.9 ohm.	0.3

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# Version Change List ( P. I. R. List ) for HW Circuit

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01	25	LAN	02/12	HW	For ESD protect.	Reserve D55.	0.4
02	34	S/W board connector	02/12	HW	To avoid cap. sensor board abnormal.	Reserve R558.	0.4
03	06	CPU	02/12	HW		Reserve R59.	0.4
04	06	CPU	02/15	HW	Follow Trinity design.	Change CPU SM BUS from EC2 to EC1.	0.4
05	06	CPU	02/15	HW		Reserve C16.	0.4
06	06	CPU	02/15	HW	Follow Trinity design.	Change R18 and R19 from 330 to 2.2K ohm.	0.4
07	07	CPU	02/15	HW		Reserve C54.	0.4
08	12	NB	02/15	HW		Remove L96.	0.4
09	12	NB	02/15	HW		Change L12, L13 from bead to 0 ohm.	0.4
10	13	NB	02/15	HW		Change L16, L18, L19, L22 from bead to 0 ohm.	0.4
11	13	NB	02/15	HW		Remove L95.	0.4
12	24	Multibay connector	02/15	ME		Change JP10 Footprint.	0.4
13	27	Card Reader	02/15	HW	Change Card Reader LED active status.	Reserve Q53 and R454, add R1070.	0.4
14	27	Card Reader	02/15	HW	Change Card Reader LED active status.	Reserve R112 and add pull low resistor R1069.	0.4
15	31	BT	02/15	ME		Change JP32 Footprint and reverse pin define.	0.4
16	31	BT	02/15	HW	Saving Power consumption.	Change BT power source from +3VALW to +3VS.	0.4
17	33	EC	02/15	HW		Remove JP34 and reserve R1068 for EC debug.	0.4
18	33	EC	02/15	HW	To solve can't power on when first plug in AC adapter.	Change R1040 from 100K to 10K ohm and connect to +3VL_EC.	0.4
19	34	Debug SW	02/15	HW		Remove SW2.	0.4
20	34	TP LED	02/15	ME		Add D19 for PR sku.	0.4
21	11	NB	02/18	HW		Change R371 from 10K to 300 ohm.	0.4
22	11	NB	02/18	HW		Add pull low resistor R1072.	0.4
23	19	SB	02/18	HW		Reserve C1085 and R303.	0.4
24	21	SB	02/18	HW	To solve can't power on when first plug in AC adapter.	Add R1071 and D56 to connect to AC_IN.	0.4
25	32	SPI BIOS	02/18	HW		Remove U30, C489, R226, and R228. Stuff R221.	0.4
26	34	WL/BT LED control	02/18	HW		Modify circuit WLAN/WWAN/BT LED control.	0.4
27	33	EC	02/18	HW	Follow Trinity design.	Change R514 and R515 from 10K to 4.7K ohm.	0.4
28	35	Screw hole	02/19	ME	To slove TP on/off button feeling no good when press.	Add H57.	0.4
29	34	S/W board connector	02/19	ENE	For ENE cap. board.	Add LDO circuit (U65, R1073, C1097,C1099, J2).	0.4
30	34	S/W board connector	02/19	ENE	For ENE cap. board.	Change R554 pin 1 power plan from +3VL to +3VL_CAP.	0.4
31	34	S/W board connector	02/22	HW	For cap. board.	Add C1098.	0.4
32	11	NB	02/22	HW	To splve CRT rising/falling fail issue.	Reserve R62, R63, R64.	0.4
33	16	CRT connector	02/22	HW	To splve CRT rising/falling fail issue.	Change R211, R214 and R217 from 150 ohm to 75 ohm	0.4
34	16	CRT connector	02/22	HW	To splve CRT rising/falling fail issue.	Change C472, C476, C858 from 22pF to 6pF.	0.4
35	34	Lid switch connector	02/22	HW	To solve short issue for lid switch board.	Move C1100 and C1101 from lid swtich board to M/B	0.4

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36	25	LAN	02/22	DFB	To solve kink pin to interfere with PCB.	Update JRJ45 PCB Footprint.	0.4
37	35	Screw hole	02/22	DFB		Change H53 and H54 from non PTH to PTH hole.	0.4
38	34	S/W board connector	02/22	EMI	To solve EMI issue for ENE cap. board.	Change R1048 and R1049 from bead to 0 ohm.	0.4
39	34	S/W board connector	02/22	EMI	To solve EMI issue for ENE cap. board.	Reserve R1074/C1102 for ESB_CLK1 and R1075/C1103 for ESB_DAT1.	0.4
40	33	EC	02/22	EMI	To solve EMI issue for ENE cap. board.	Add R1076, C1104 and R1077.	0.4
41	33	EC	02/22	EMI		Add C1105.	0.4
42	36	DC/DC	02/25	EMI	For EMI request.	Add C1110~C1117.	0.4
43	31	USB connector	02/25	EMI	For EMI request.	Add C1109.	0.4
44	15	Clock GEN.	02/25	EMI	For EMI request.	Add C1106.	0.4
45	16	CRT Connector	02/25	EMI	For EMI request.	Add C1107.	0.4
46	17	LCD Connector	02/25	EMI	For EMI request.	Add C1108.	0.4
47	32	Debug connector	02/26	EMI	For EMI request.	Add C1118.	0.4
48	17	WEBCam LDO	02/26	HW	To reduce power consumption in S3 mode.	Add PJP6 to connect to +5VS. Stuff R1013 and reserve R1014.	0.4
49	34	Lid switch connector	02/26	HW		Connect JP40 pin 4 to +3VALW.	0.4
50	06	CPU	02/27	POWER		Change net name ENTRIP2 to EN0.	0.4
51	34	S/W board connector	03/03	EMI	For EMI request.	Change R558 to C1119 (0.1uF)	0.4
52	11	NB	03/03	EMI	For EMI request.	Change C1120 (0.1uF)	0.4
53	31	USB connector	03/03	EMI	For EMI request.	Change C1121 (0.1uF)	0.4
<del>54</del>	<del>22</del>	<del>SB</del>	<del>03/03</del>	<del>HW</del>		<del>Change L60, L61, L63, L66, L67, L68, L69 from 0 ohm to bead.</del>	<del>0.4</del>
55	13	NB	03/03	HW		Remove L20, L21 and use PJP604 to replace.	0.4
56	35	Docking connector	03/03	DFB		Change JDOCK connector Footprint.	0.4
57	11	NB	03/03	AMD	To support VariBright feature.	Add D58 and connect to INV_PWM.	0.4
58	11	NB	03/03	AMD	To support VariBright feature.	Change backlight inform signal (R70, R1072) from LVDS_BLON to LVDS_ENA_BL.	0.4
59	33	EC	03/03	AMD	To support VariBright feature.	Change JDOCK connector Footprint.	0.4
60	06	CPU	03/04	AMD		Reserve R175, R814, C939, Q127 and Q129.	0.4
61	19	SB	03/04	AMD	To solve can not power on when use single core CPU.	Change net name from H_PWRGD to H_PWRGD_SB.	0.4
62	20	SB	03/05	EMI	For EMI request	Add SSC circuit (U66, R1080, R1081, R1082, R1083, C1122) for HDA_BITCLK.	0.4
63	21	SB	03/06	AMD	For eSATA GEN1 fail issue.	Change C520 and C521 from 0.01uF to 1000pF.	0.4
64	21	SB	03/06	AMD	For eSATA GEN1 fail issue.	Change C520 and C521 from 0.01uF to 1000pF.	0.4
65	31	eSATA connector	03/06	AMD	For eSATA GEN1 fail issue.	Change C792 and C793 from 0.01uF to 1000pF.	0.4
66	17	LCDVCC circuit	03/06	HW	To solve LCD power up sequence fail.	Change R225 from 470 ohm to 220 ohm.	0.4
67	15	Clock GEN.	03/06	HW	For IDT CLOCK GEN.	Add C1123.	0.4
68	20	SB	03/06	HW	To avoid CMOS data lose when shutdown suddenly.	Add D58 and connect to 3/5V_OK.	0.4
67	15	WWAN connector	03/06	HW	To support wake on WWAN feature.	Add power on/off control circuit (Q167, R1087).	0.4
67	15	WWAN/WLAN	03/06	HW	To avoid leakage power from SB.	Add D59 and D60.	0.4

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68	20	SB	03/06	HW	To solve can not power on if use CPU with single core	Stuff R83.	0.4
69	11	NB	03/06	HW	To support VariBright feature.	Add R1085 and R1086.	0.4
70	25	LAN	03/06	HW	To reduce power consumption in S3 mode.	Stuff Q144, R1056, R1057, C1077 and reserve R1067.	0.4
71	33	LAN	03/06	HW	To reduce power consumption in S3 mode.	Stuff R544.	0.4
72	18	HDMI	03/07	HW	To pass HDMI test.	Chagne R315, R307, R173, R297, R172, R304, R139, R141 from 750 ohm to 715 ohm.	0.4
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68	20	SB	03/06	HW	To solve can not power on if use CPU with single core	Stuff R83.	0.4
69	11	NB	03/06	HW	To support VariBright feature.	Add R1085 and R1086.	0.4
70	25	LAN	03/06	HW	To reduce power consumption in S3 mode.	Stuff Q144, R1056, R1057, C1077 and reserve R1067.	0.4
71	33	LAN	03/06	HW	To reduce power consumption in S3 mode.	Stuff R544.	0.4
72	18	HDMI	03/07	HW	To pass HDMI test.	Chagnge R315, R307, R173, R297, R172, R304, R139, R141 from 750 ohm to 715 ohm.	0.4
73	33	EC	09/10	HW	Avoid DOCK_VOL_UP# and DOCK_VOL_down# folating	R589 R590 use 10k ohm pull high	1.0
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