

Jan. 21 '05

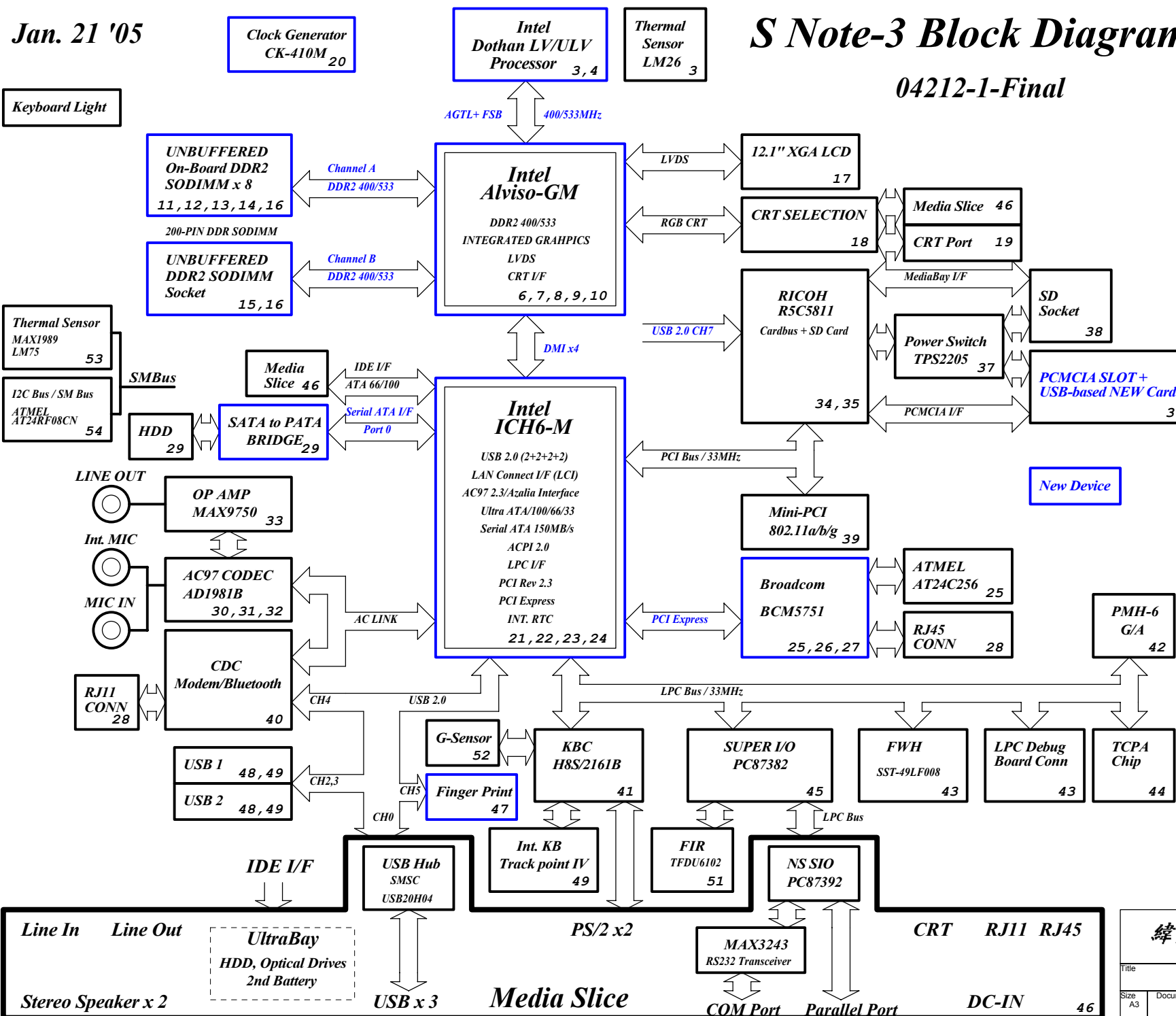
# S Note-3 Block Diagram

04212-1-Final

## PCB Layer Stackup

- L1: Component
- L2: GND
- L3: Signal 1
- L4: VCC
- L5: Signal 2
- L6: Signal 3
- L7: GND
- L8: Component

| System DC/DC             |            |
|--------------------------|------------|
| MAXI1977                 | 64         |
| INPUTS                   | OUTPUTS    |
| VINT16                   | VCC5M      |
|                          | VCC3M      |
| Battery Charger/Selector |            |
| MAXI870                  | 58         |
| CV16                     | M-BAT-PWR  |
|                          | S-BAT-PWR  |
| VCC1R8M                  |            |
| MAXI1993                 | 67         |
| VINT16                   | VCC1R8M    |
| CPU DC/DC                |            |
| MAXI1907                 | 65         |
| VINT16                   | VCCCPUCORE |
| VCC1R05B/VCC1R5M         |            |
| MAXI1540                 | 68         |
| VINT16                   | VCC1R5M    |
|                          | VCC1R5B    |
| VCC0R9B/DDR2_VREF        |            |
| LP2997MRX                | 69         |
| VCC1R8A                  | VCC0R9B    |
|                          | DDR2_VREF  |



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Title: **Block Diagram**

Size: A3 Document Number: **S Note-3** Rev: -1

Date: Tuesday, June 21, 2005 Sheet 1 of 75

### RESISTOR

| Symbol name | Value    | Tolerance<br>(J: 5%, F: 1%, D: 0.5%, B: 0.1 %) | Rating<br>0402=> 1/16W, 25V<br>0603 => 1/16W, 75V<br>0805 => 1/10W, 100V | Size<br>2=>0402, 3=>0603, 5=>0805,<br>6=>1206, 0=>1210 |
|-------------|----------|--|--|--|
| 10KR3       | 10K Ohm  | If no letter, it means J: 5%                   | 1/16W, 75V   | 0603   |
| 33D3R5      | 33.3 Ohm | If no letter, it means J: 5%                   | 1/10W, 100V  | 0805   |
| 1KR3F       | 1K Ohm   | F: 1%  | 1/16W, 75V   | 0603   |

The naming rule is value + R + size + tolerance  
 For the value, it can be read by the number before R. (R means resistor)  
 For the tolerance, it can be read from the last letter.  
 For the rating, we don't show on the symbol name.  
 For the size, R2=>0402, R3=>0603, R5=>0805,....

### PCI TABLE

| DEVICE                                   | IDSEL | IRQ (Default) | REQ# / GNT#   |
|--|-------|---------------|---------------|
| MINIPCI SLOT                             | AD18  | F, G          | REQ# 3/ GNT#3 |
| CARDBUS R5C811                           | AD16  | SERIRQ        | REQ#0 / GNT#0 |
| USB UHCI                                 | AD29  | A, C, D       |               |
| USB 2.0 EHCI                             | AD29  | H             |               |
| DMI-to-PCI/<br>AC97 Modem/<br>AC97 Audio | AD30  | B<br>B        |               |
| LPC Bridge<br>IDE<br>SATA<br>SMBus       | AD31  | C<br>C<br>B   |               |
| PCI Express                              | AD28  | A, B, C, D    |               |

### CAPACITOR

| Symbol name   | Value | Tolerance<br>(M: +/-20, K: +/-10, Z: +80/-20) | Rating | Size<br>2=>0402, 3=>0603, 5=>0805,<br>6=>1206, 0=>1210 |
|---------------|-------|---|--------|--|
| SCD1U10V2MX-1 | 0.1uF | M/X5R   | 10V    | 0402   |
| SC10U6D3V5MX  | 10uF  | M/X5R   | 6.3V   | 0805   |
| SC2D2U16V5ZY  | 2.2uF | Z/Y5V   | 16V    | 0805   |

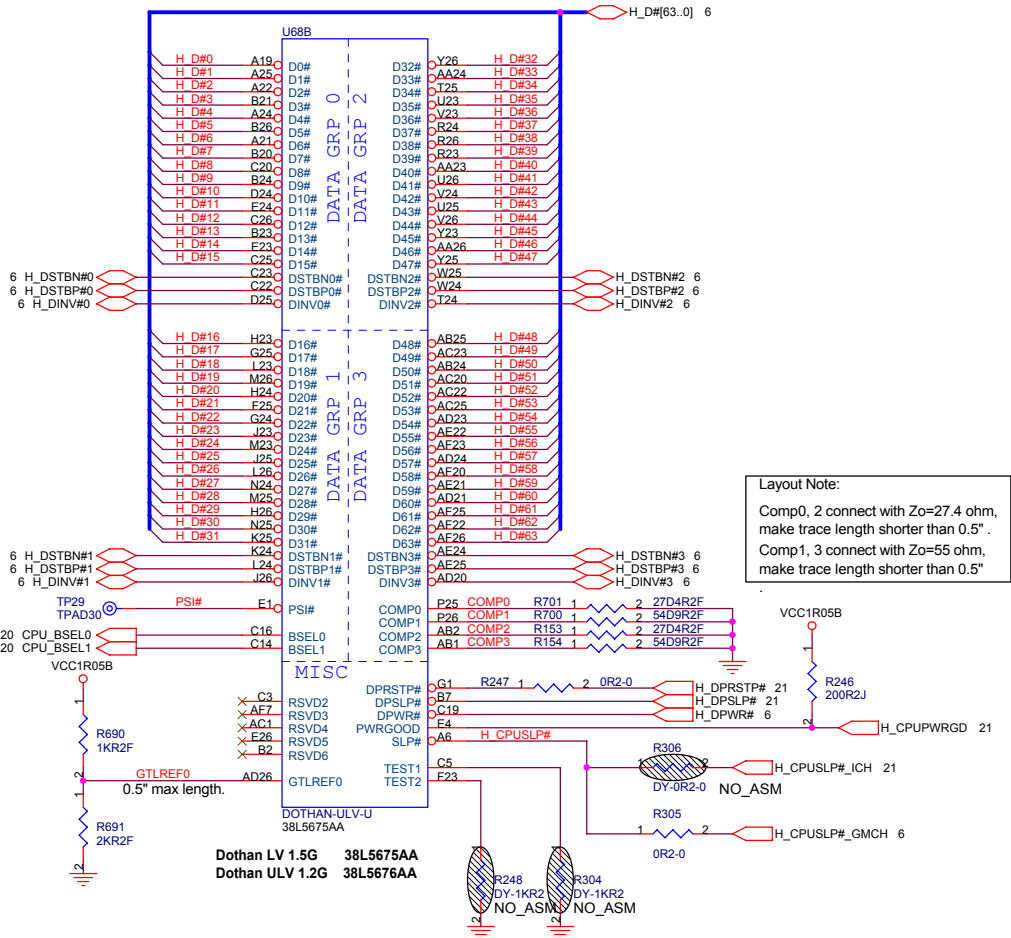
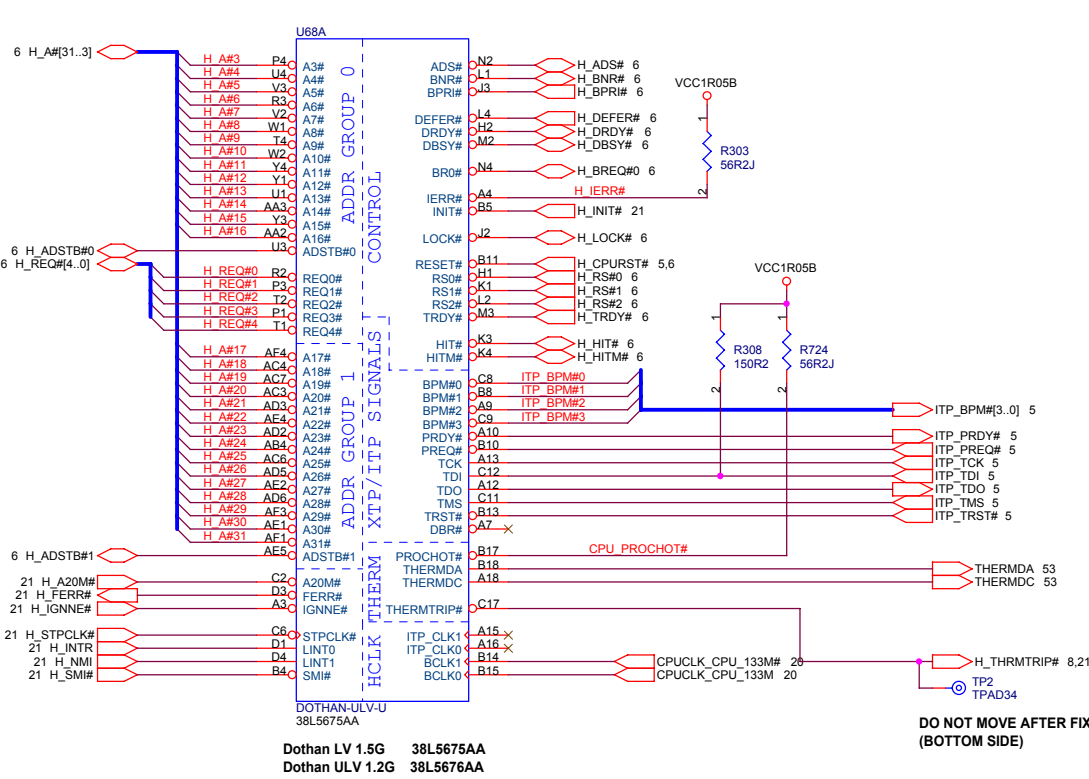
The naming rule is  
 Capacitor type + value + rating + size + tolerance + material  
 SCD1U10V2MX-1  
 SC=> SMT Ceramic, TC=> POS cap or SP cap  
 D1U => 0.1uF  
 10V => the voltage rating is 10V  
 2=> 0402, 3=>0603, 5=>0805  
 M=>tolerance M, K, Z  
 X=> X7R/X5R, Y=> Y5V  
 -1 => symbol version, nonsense to EE characteristic

### PLANAR\_ID[3..0]

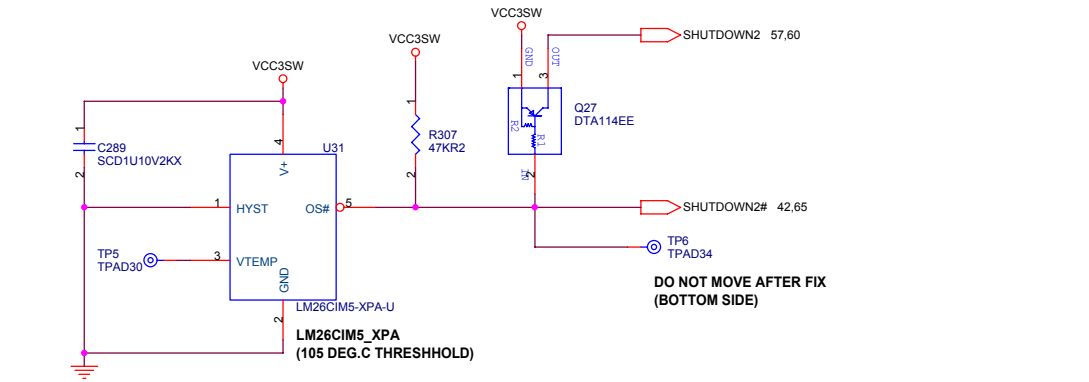
| ICH4-M GPIOn | 31 | 30 | 29 | 26 | Planar ID Version | Planar PCB Version |
|--------------|----|----|----|----|-------------------|--------------------|
| PLANAR_IDn   | 3  | 2  | 1  | 0  |                   |                    |
|              | 0  | 0  | 0  | 0  | SDV               | 04212-SA           |
|              | 0  | 0  | 0  | 1  | SIV               | 04212-SB           |
|              | 0  | 0  | 1  | 0  | SIT               | 04212-SC           |
|              | 0  | 0  | 1  | 1  | SVT               | 04212-1            |
|              | 0  | 1  | 0  | 0  |                   |                    |
|              | 0  | 1  | 0  | 1  |                   |                    |
|              | 0  | 1  | 1  | 0  |                   |                    |
|              | 0  | 1  | 1  | 1  |                   |                    |

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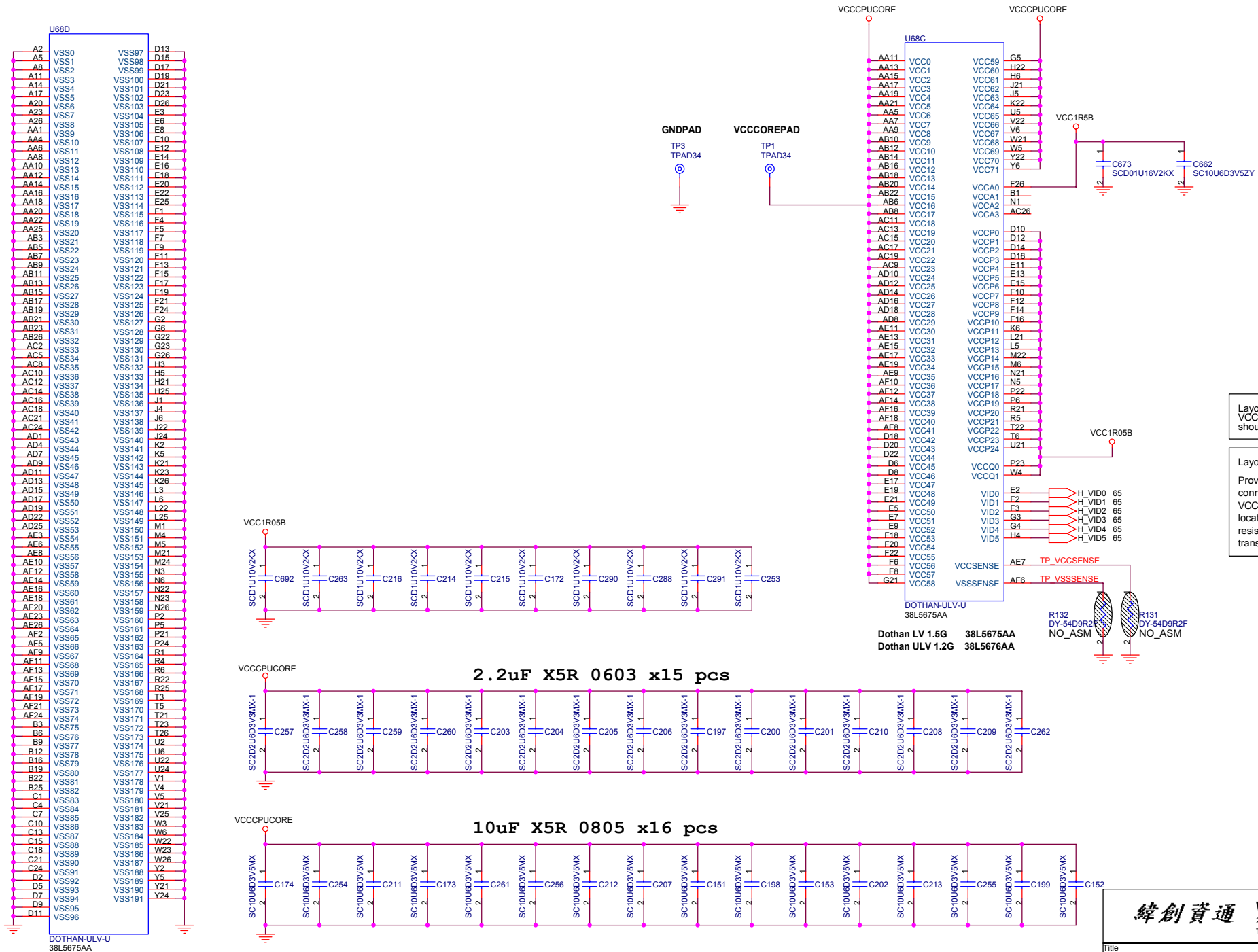
|                              |                 |                  |           |
|------------------------------|-----------------|------------------|-----------|
| Title                        |                 | <b>Reference</b> |           |
| Size<br>A3                   | Document Number | <b>S Note-3</b>  |           |
| Date: Tuesday, June 21, 2005 |                 |                  | Rev<br>-1 |



**Layout Note:**  
 Comp0, 2 connect with  $Z_0=27.4$  ohm, make trace length shorter than 0.5".  
 Comp1, 3 connect with  $Z_0=55$  ohm, make trace length shorter than 0.5".



|  |                 |
|--|-----------------|
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| <b>Dothan CPU(1/2)</b>   |                 |
| Title  | Rev             |
| Size A3  | Document Number |
| <b>S Note-3</b>  |                 |
| Date: Tuesday, June 21, 2005   | Sheet 3 of 75   |



Dothan LV 1.5G 38L5675AA  
 Dothan ULV 1.2G 38L5676AA

Dothan LV 1.5G 38L5675AA  
 Dothan ULV 1.2G 38L5676AA

Layout Note:  
 VCCSENSE and VSSSENSE lines should be of equal length.

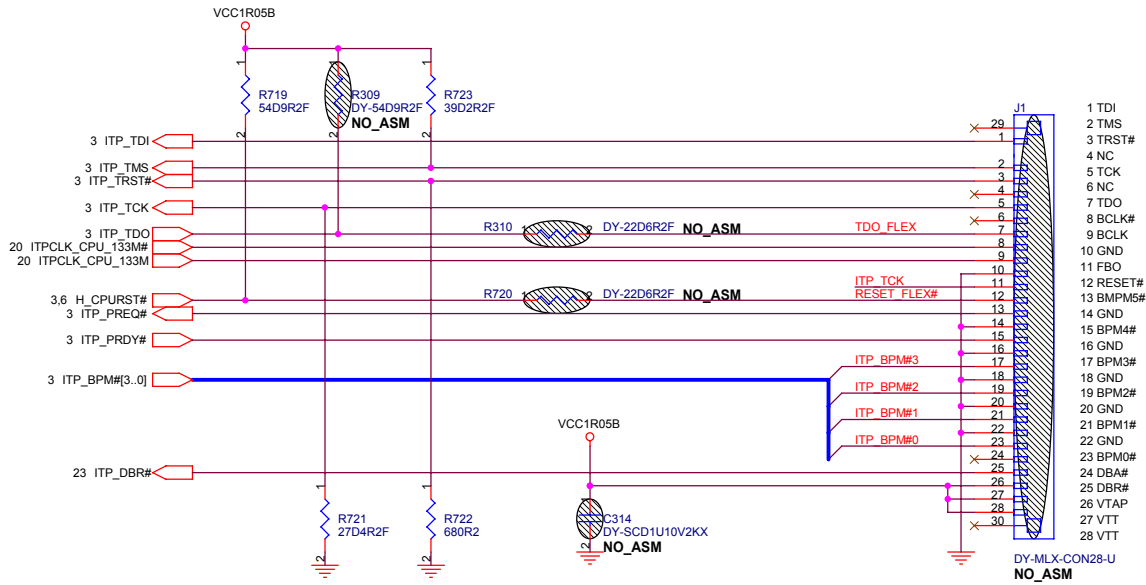
Layout Note:  
 Provide a test point (withno stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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Title: **Dothan CPU(2/2)**

Size A3 Document Number **S Note-3** Rev **-1**

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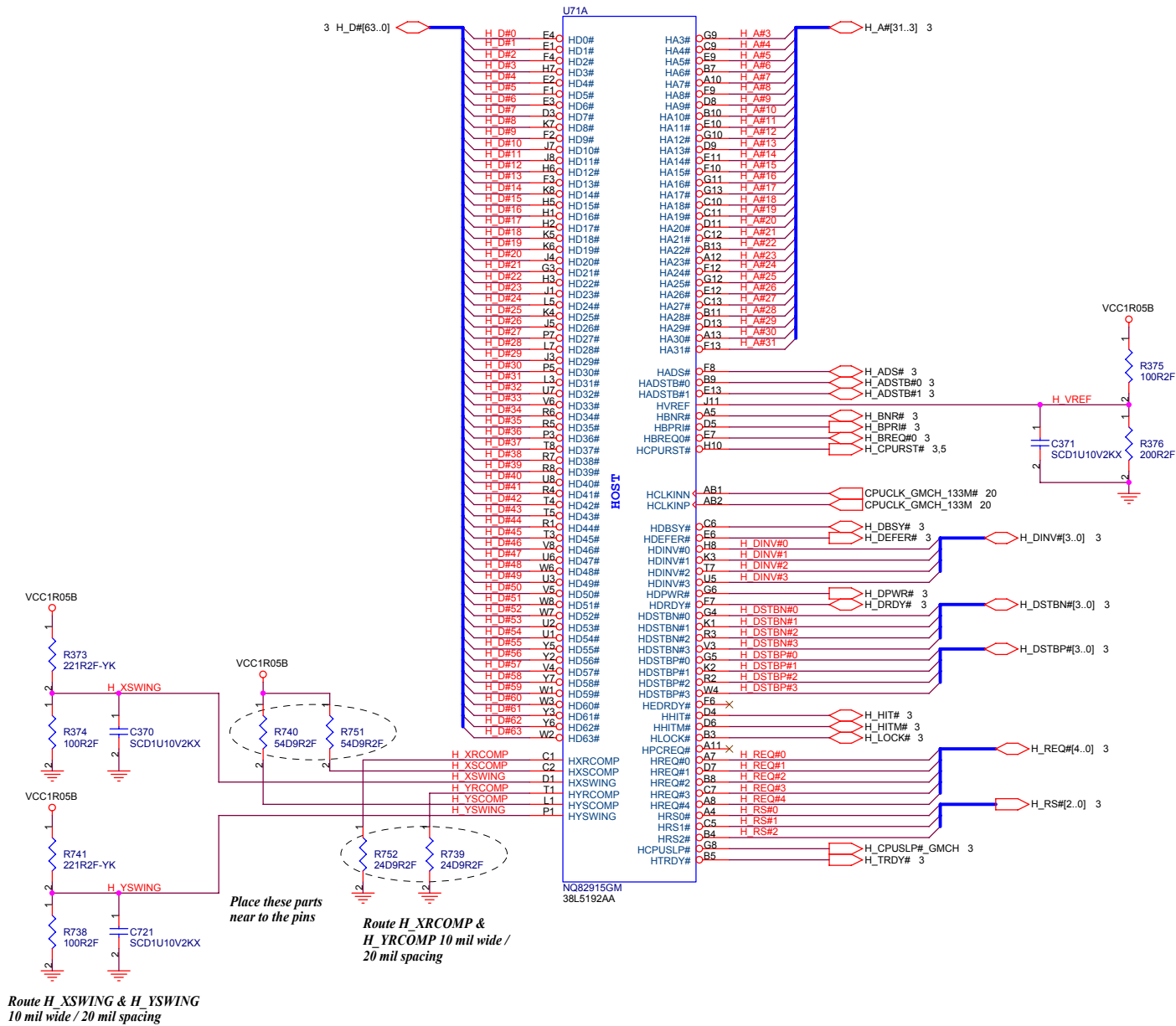


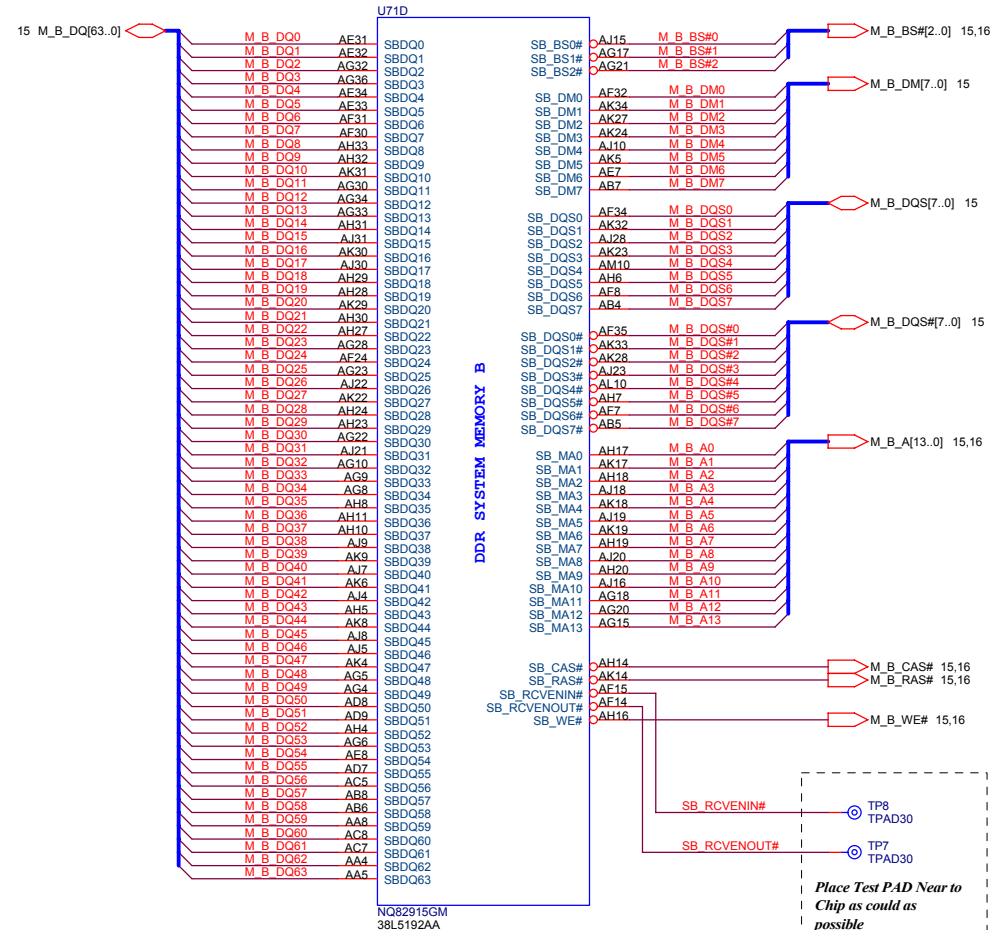
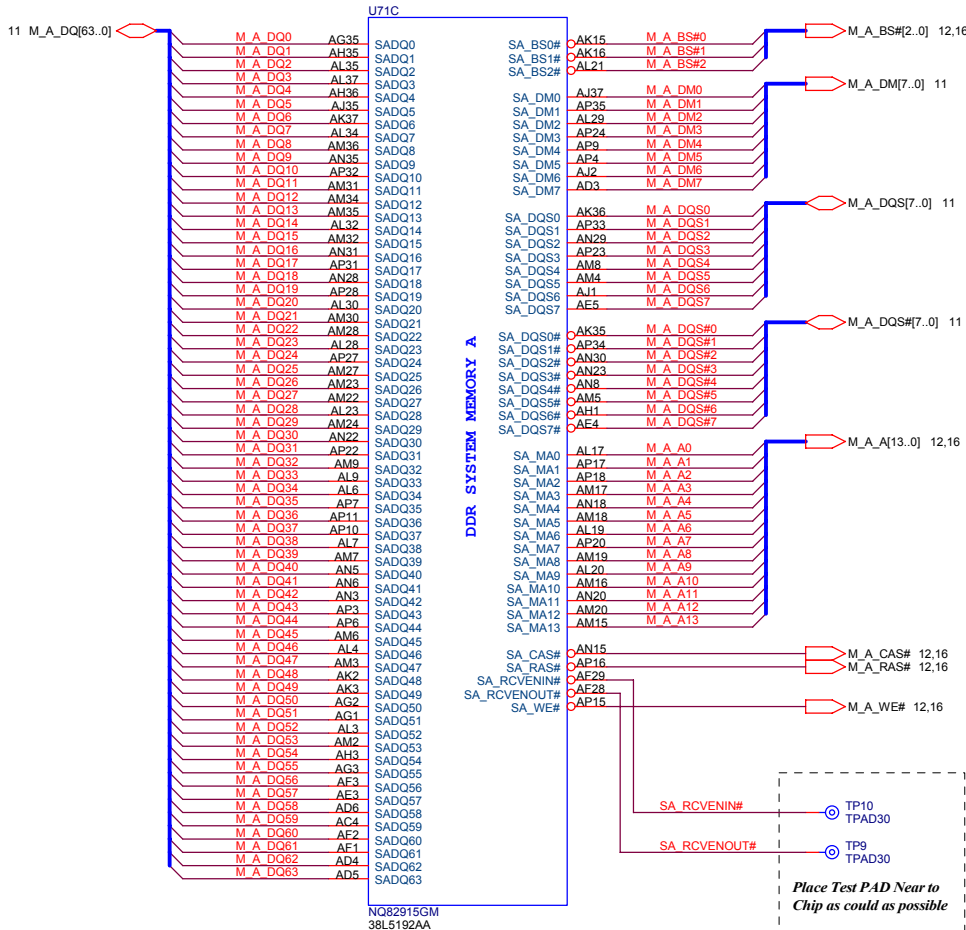
(\*1) TCK SIGNAL IS BRANCHED AT DOTHAN PIN

(\*2) CPURST# SIGNAL IS BRANCHED AT ALVISO PIN

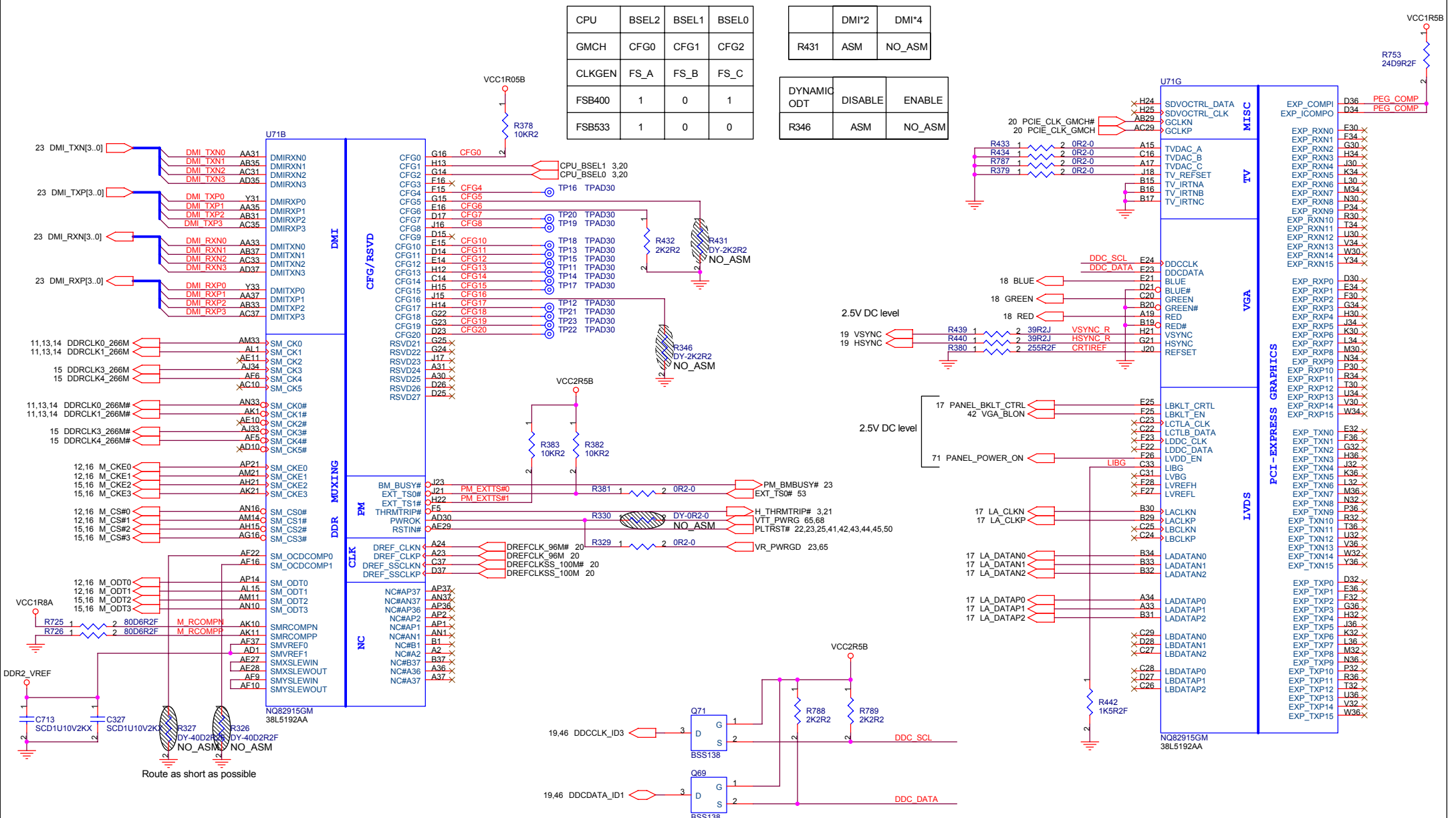
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|                              |                 |     |                       |   |       |
|------------------------------|-----------------|-----|-----------------------|---|-------|
| Title                        |                 |     | <b>ITP CCONNECTOR</b> |   |       |
| Size                         | Document Number | Rev |                       |   |       |
| A3                           |                 | -1  | <b>S Note-3</b>       |   |       |
| Date: Tuesday, June 21, 2005 |                 |     | Sheet                 | 5 | of 75 |









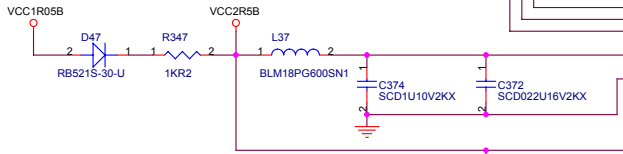
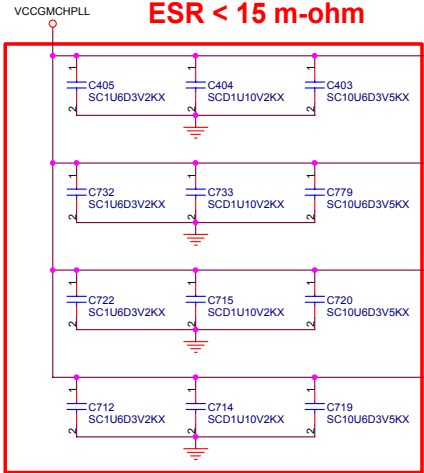
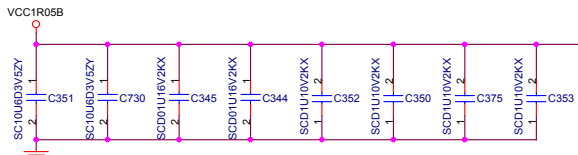
| CPU    | BSEL2 | BSEL1 | BSEL0 |
|--------|-------|-------|-------|
| GMCH   | CFG0  | CFG1  | CFG2  |
| CLKGEN | FS_A  | FS_B  | FS_C  |
| FSB400 | 1     | 0     | 1     |
| FSB533 | 1     | 0     | 0     |

|      | DMI*2 | DMI*4  |
|------|-------|--------|
| R431 | ASM   | NO_ASM |

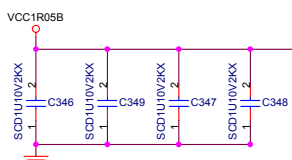
| DYNAMIC ODT | DISABLE | ENABLE |
|-------------|---------|--------|
| R346        | ASM     | NO_ASM |

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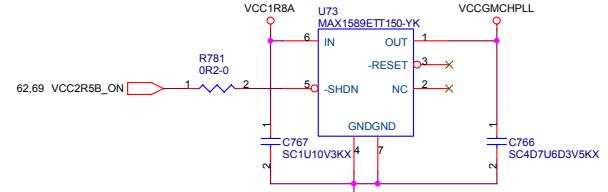
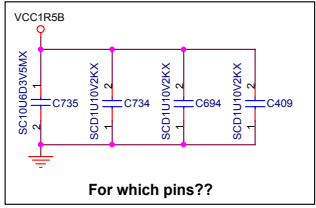
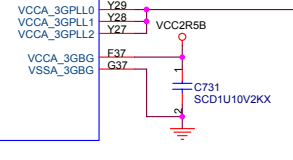
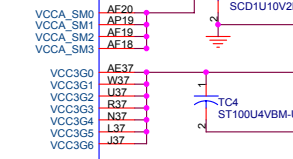
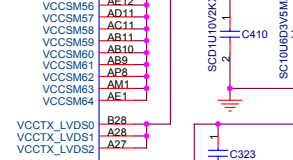
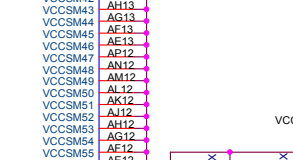
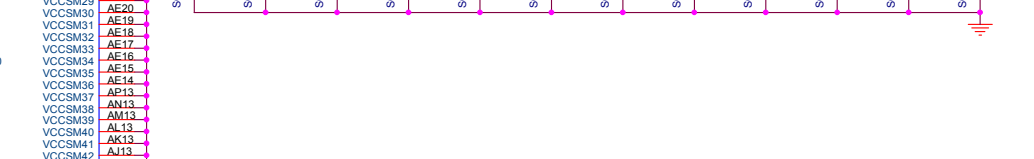
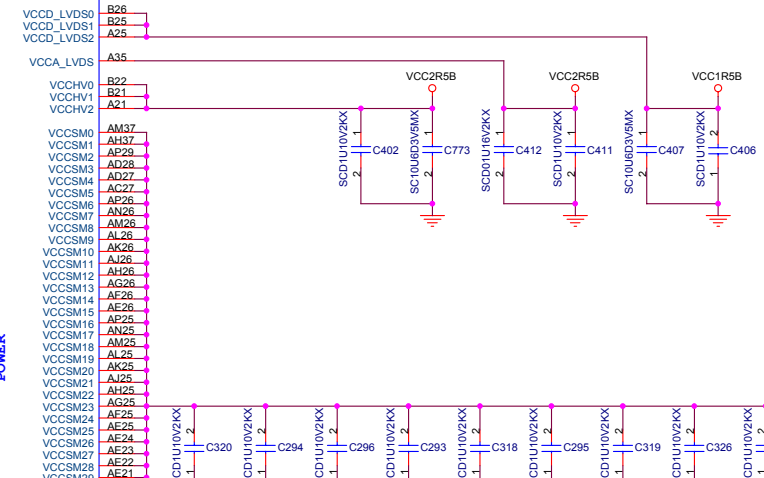
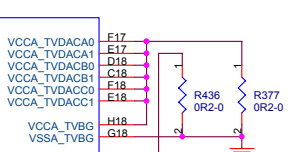




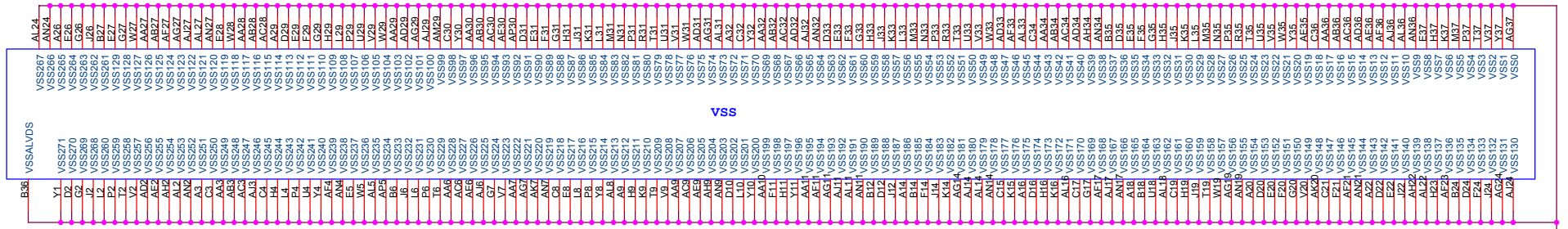
Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the GND plane



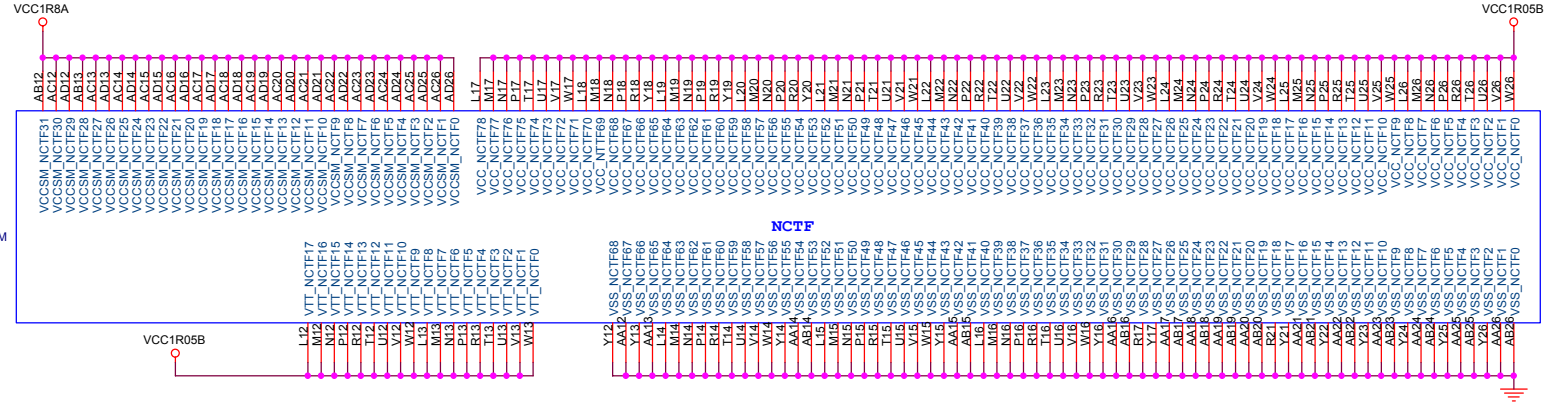
- POWER**
- T29 VCC0
  - R29 VCC1
  - N29 VCC2
  - M29 VCC3
  - K29 VCC4
  - V28 VCC5
  - U28 VCC6
  - T28 VCC7
  - R28 VCC8
  - P28 VCC9
  - N28 VCC10
  - M28 VCC11
  - L28 VCC12
  - K28 VCC13
  - J28 VCC14
  - H28 VCC15
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U71F  
NQ82915GM  
38L5192AA



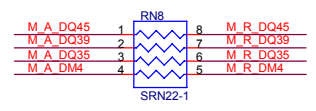
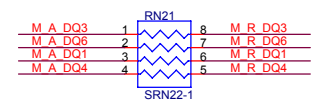
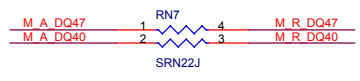
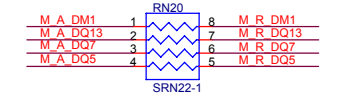
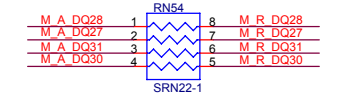
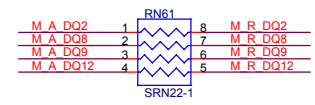
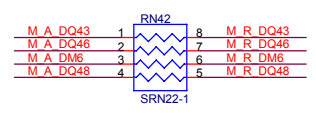
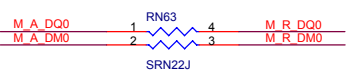
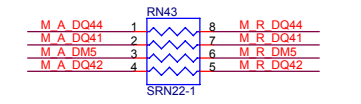
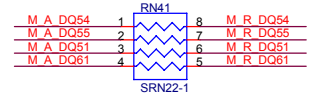
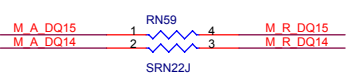
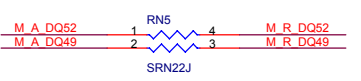
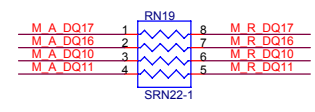
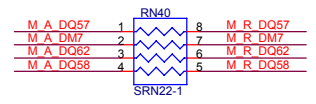
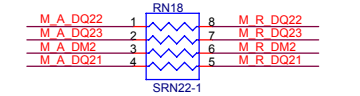
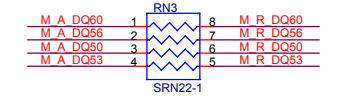
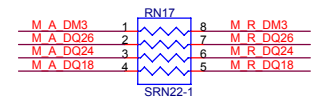
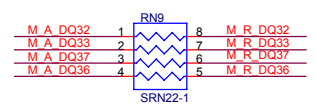
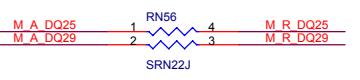
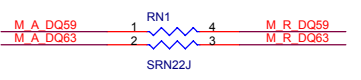
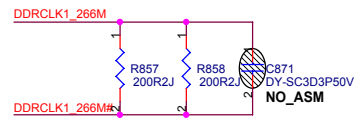
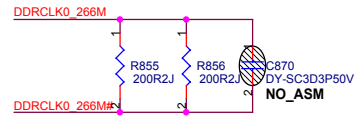
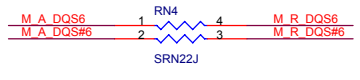
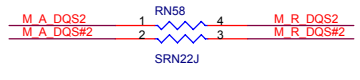
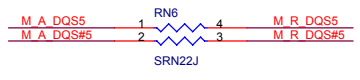
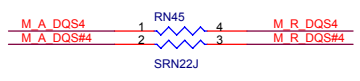
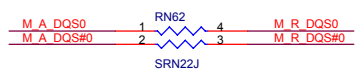
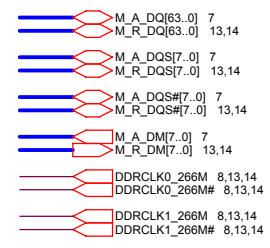
U71H  
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38L5192AA



VSS

NCTF

|   |                |
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|   |                |
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| <b>GMCH (5/5) : GND</b>   |                |
| Title   | Rev            |
| Size A3   | -1             |
| <b>S Note-3</b>   |                |
| Date: Tuesday, June 21, 2005  | Sheet 10 of 75 |

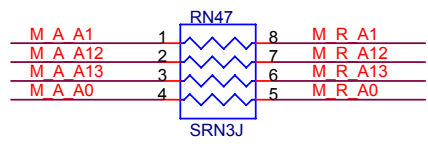
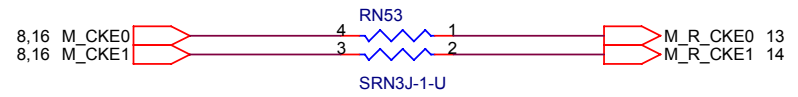
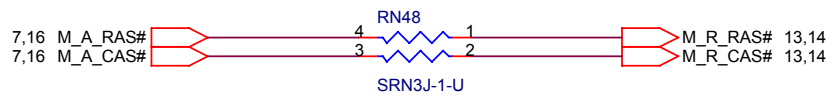
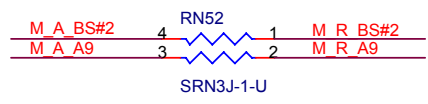
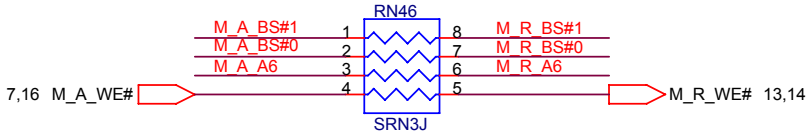
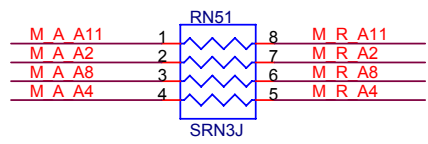
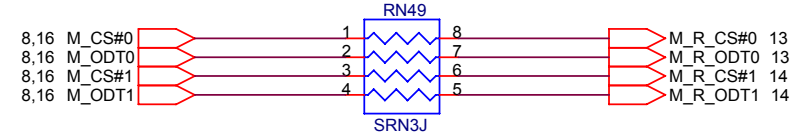
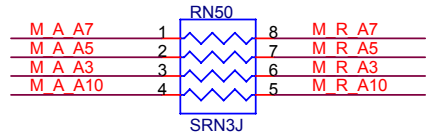


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 Taipei Hsien 221, Taiwan, R.O.C.

Title  
**MEMORY RESISTORS (1/2)**

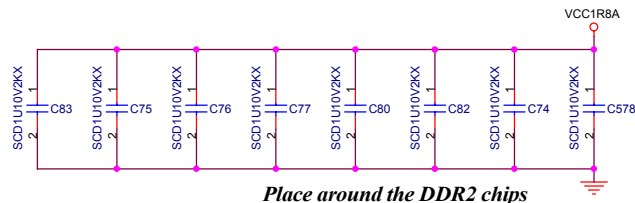
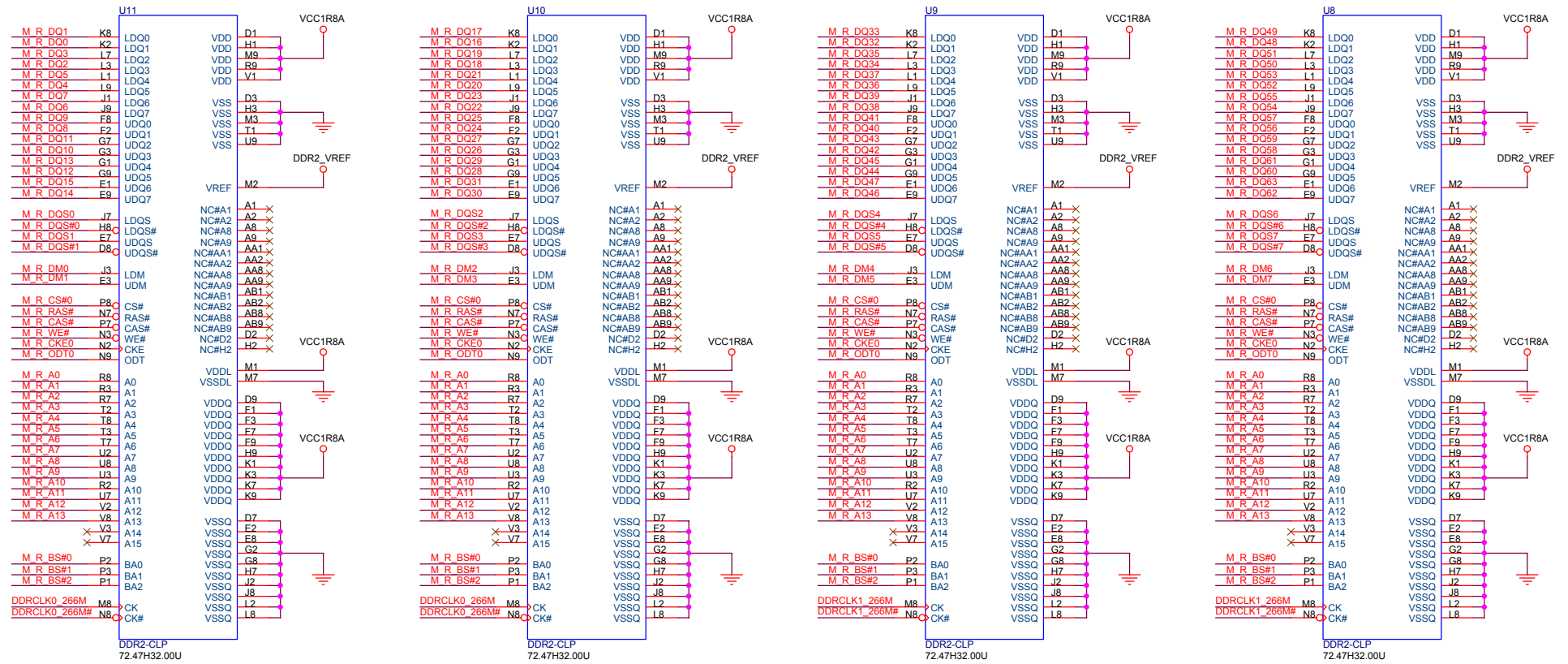
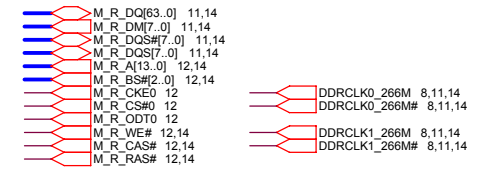
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| Size<br>A3 | Document Number | Rev<br>-1 |
|------------|-----------------|-----------|

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|                               |                 |   |                |
|-------------------------------|-----------------|---|----------------|
|                               |                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                |
| <b>MEMORY RESISTORS (1/2)</b> |                 |   |                |
| Title                         |                 | Rev   |                |
| <b>S Note-3</b>               |                 | <b>-1</b>   |                |
| Size A4                       | Document Number | Date: Tuesday, June 21, 2005  | Sheet 12 of 75 |

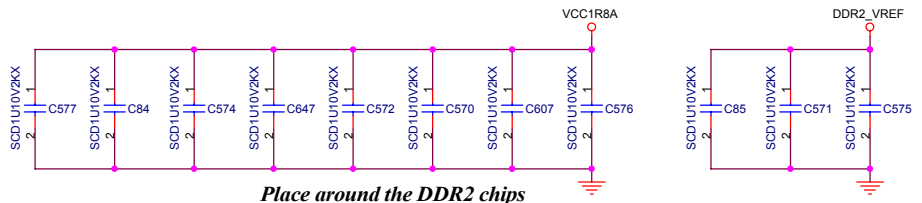
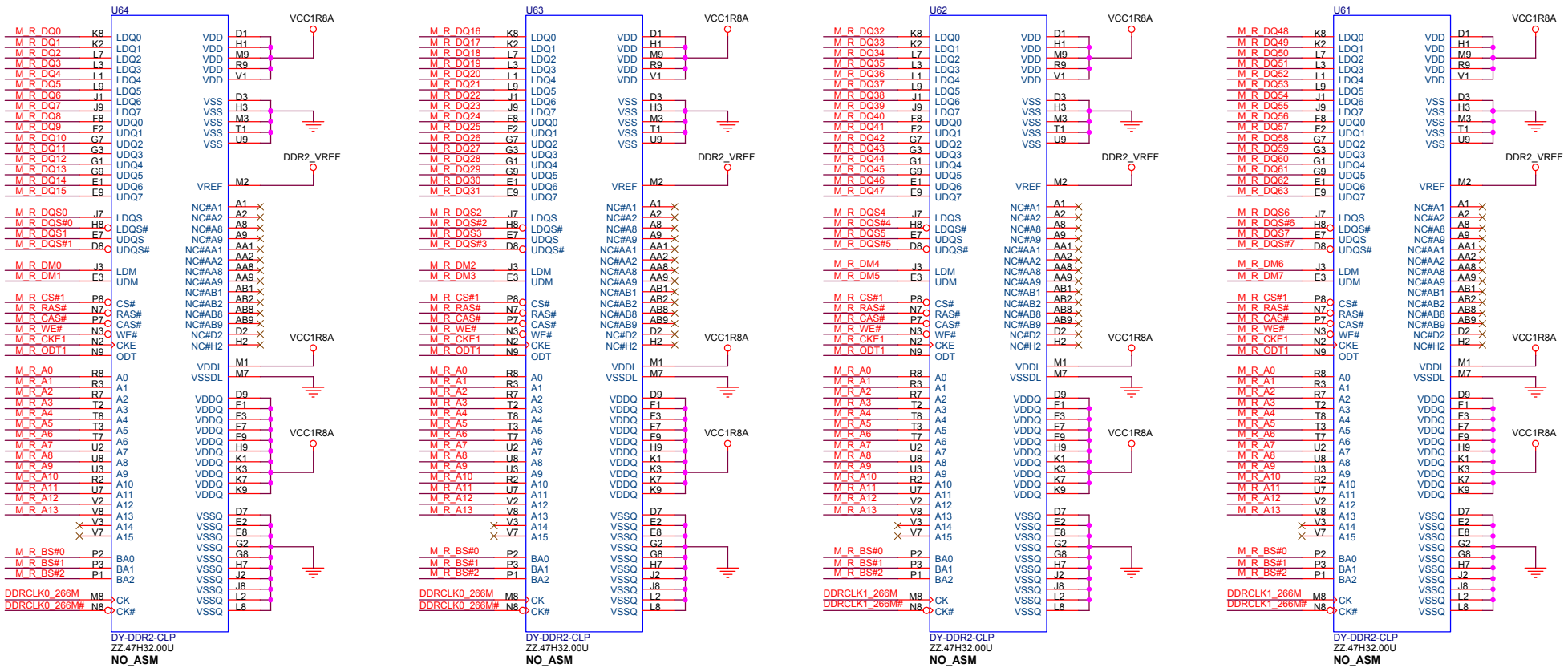
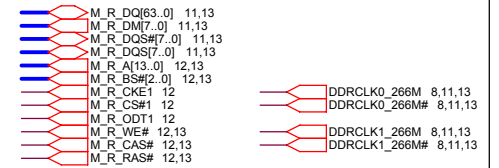
# On-board DDR2 Memory



Place around the DDR2 chips

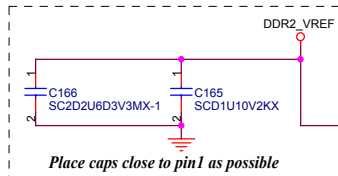
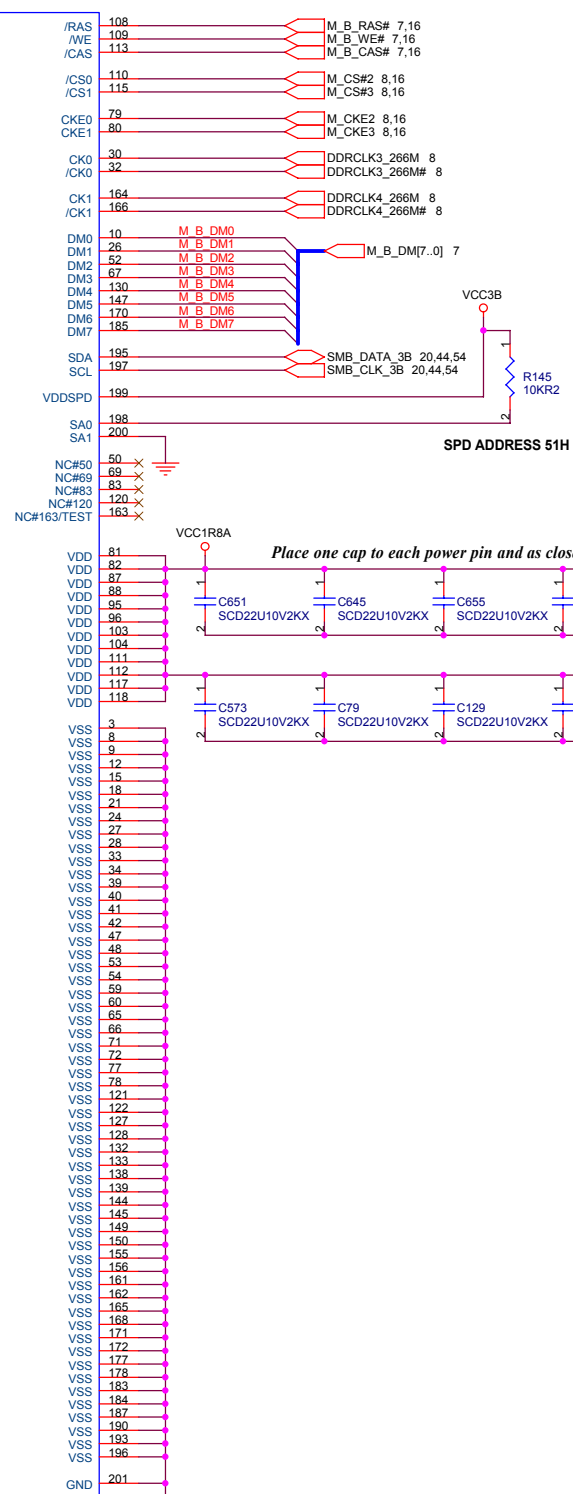
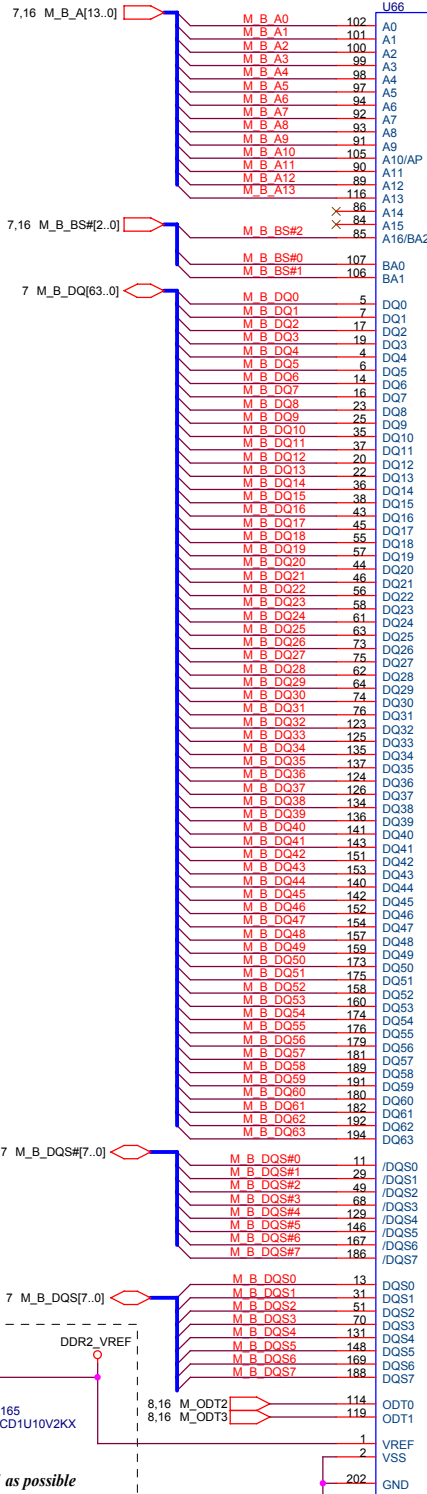
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| <b>緯創資通 Wistron Corporation</b>   |                          |           |
| 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                          |           |
| <b>BASE MEMORY BANK0</b>  |                          |           |
| Title   | <b>BASE MEMORY BANK0</b> |           |
| Size  | Document Number          | Rev       |
| A3  | <b>S Note-3</b>          | <b>-1</b> |
| Date: Tuesday, June 21, 2005  | Sheet 13 of              | 75        |

# On-board DDR2 Memory



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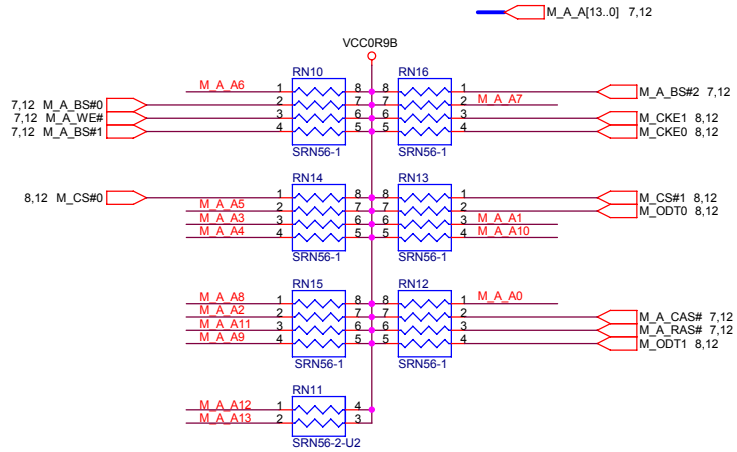
Title: **BASE MEMORY BANK1**  
 Size A3 Document Number **S Note-3** Rev -1  
 Date: Tuesday, June 21, 2005 Sheet 14 of 75



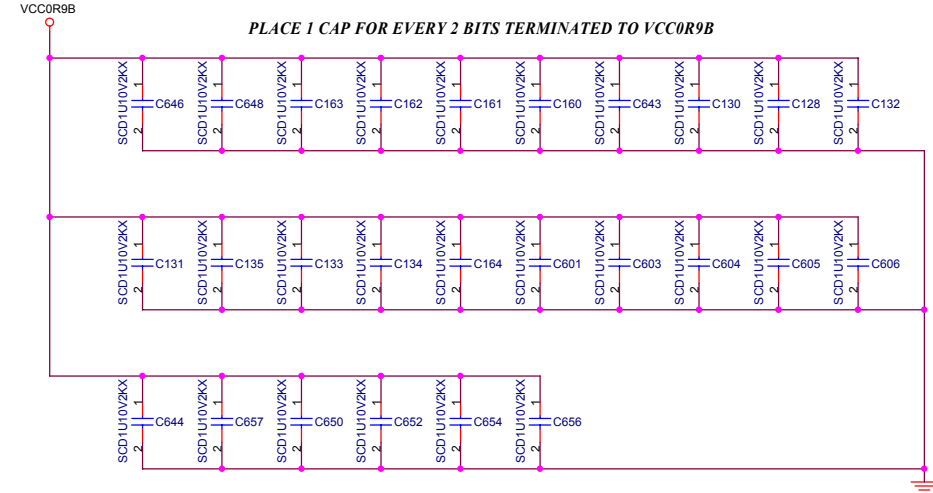
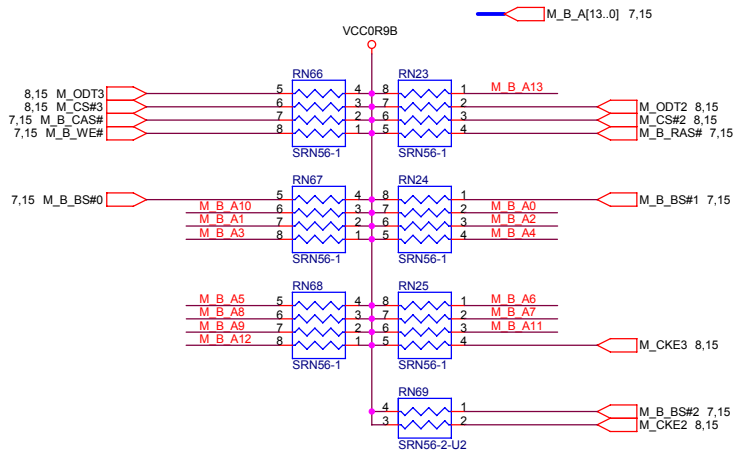
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| <b>緯創資通 Wistron Corporation</b>  |                                 |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                                 |
| Title <b>DDR-2 SO-DIMM</b>   |                                 |
| Size A3  | Document Number <b>S Note-3</b> |
| Date: Tuesday, June 21, 2005   | Sheet 15 of 75                  |



## CHANNEL A PARALLEL TERMINATION

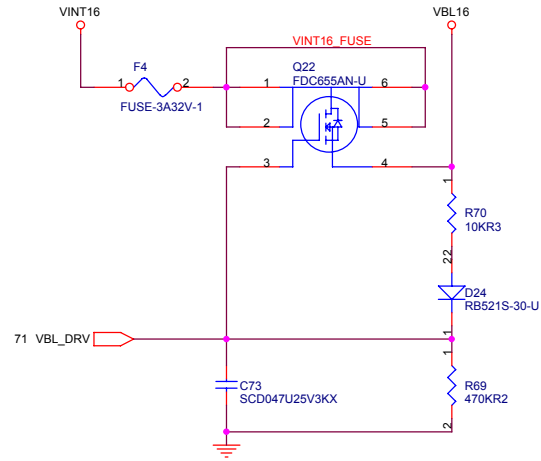
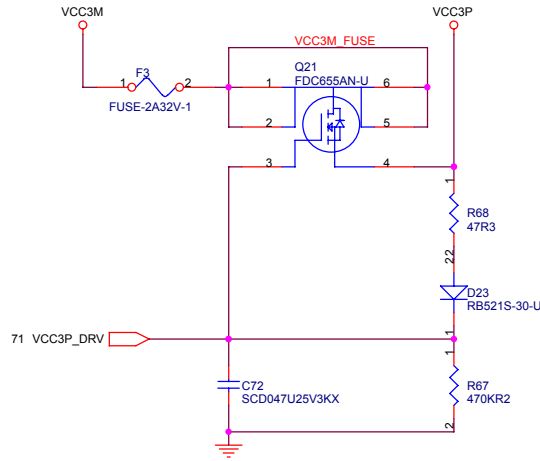
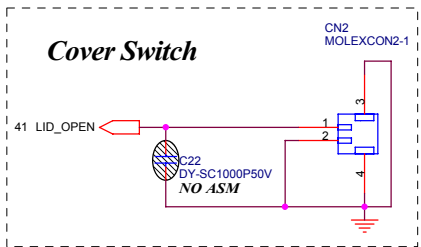
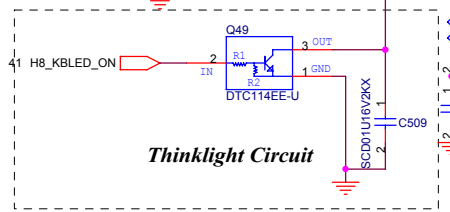
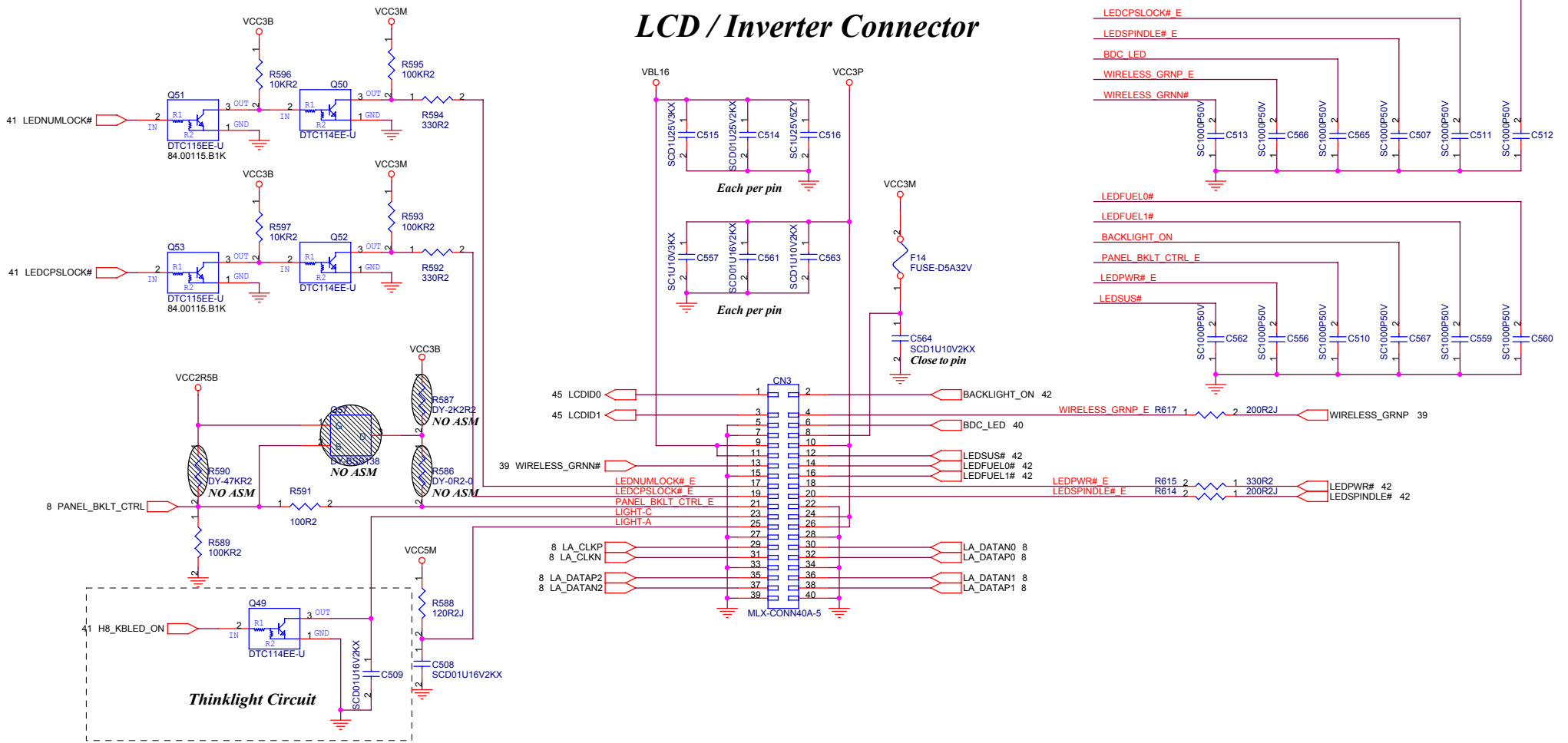


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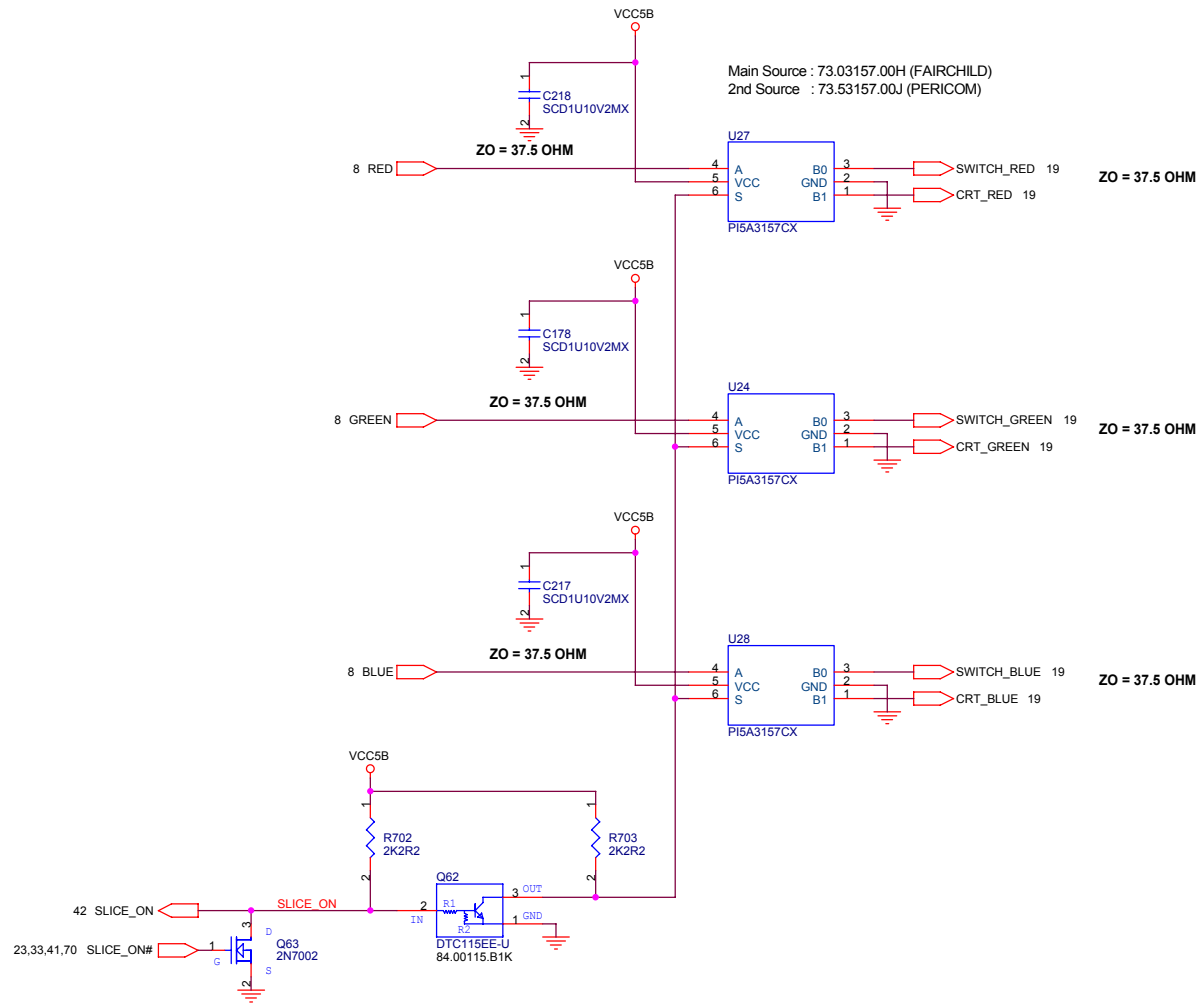


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| Title  |                 |
| <b>DDR-2 TERMINATION</b>   |                 |
| Size   | Document Number |
| A3   | <b>S Note-3</b> |
| Date:  | Rev             |
| Tuesday, June 21, 2005   | -1              |
| Sheet  | of              |
| 16   | 75              |

# LCD / Inverter Connector

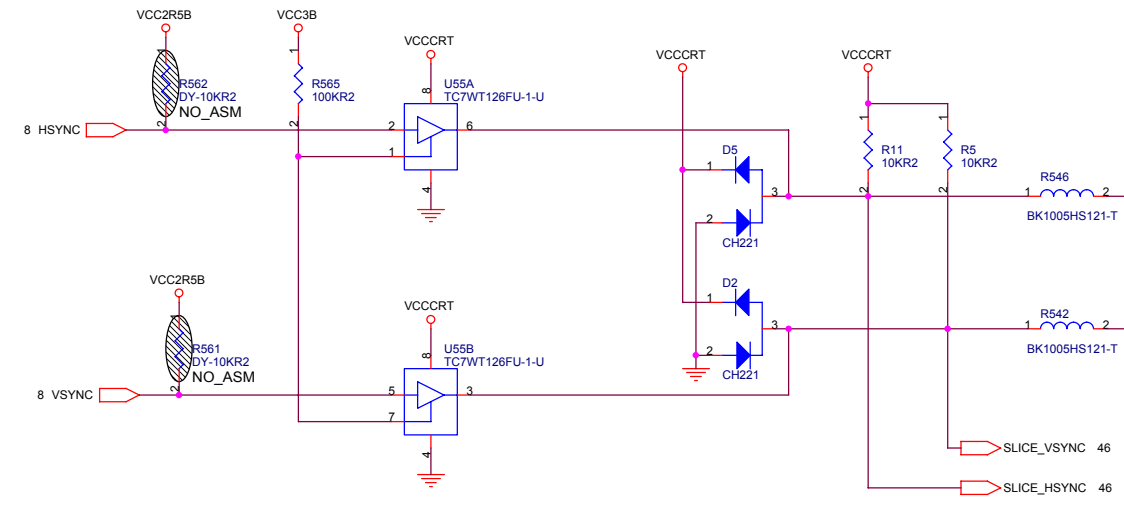
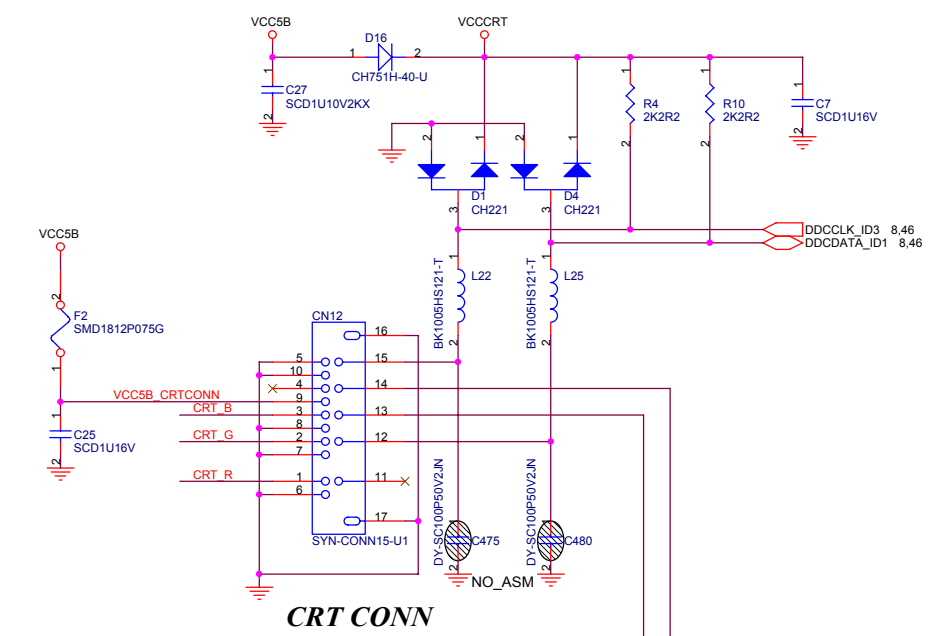
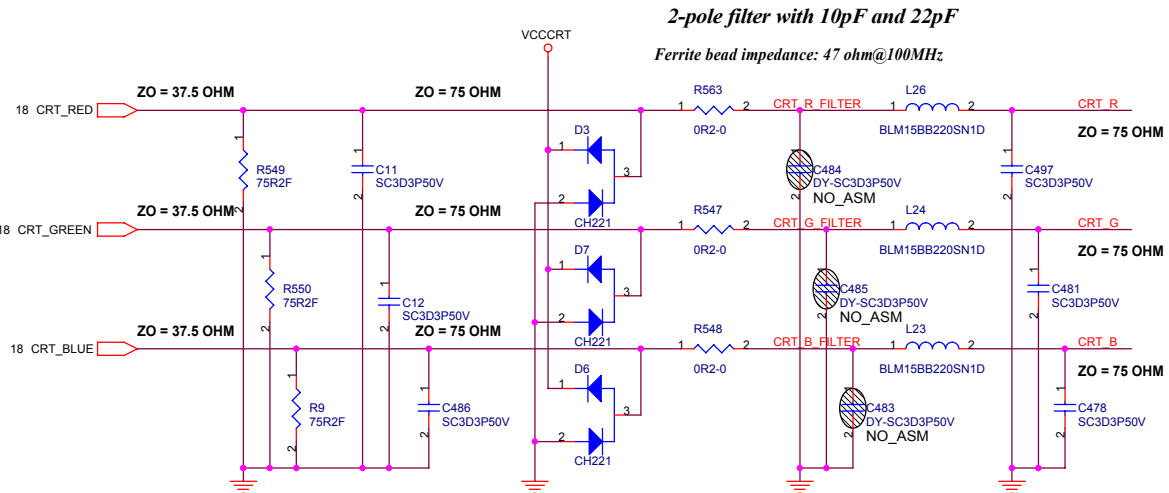
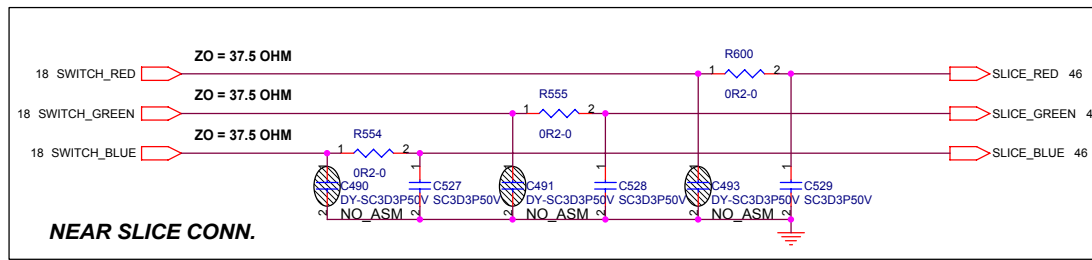


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| <b>LCD CONNECTOR</b>   |                 |        |
| Title  | <b>S Note-3</b> |        |
| Size A3  | Document Number | Rev -1 |
| Date: Tuesday, June 21, 2005   | Sheet 17 of     | 75     |

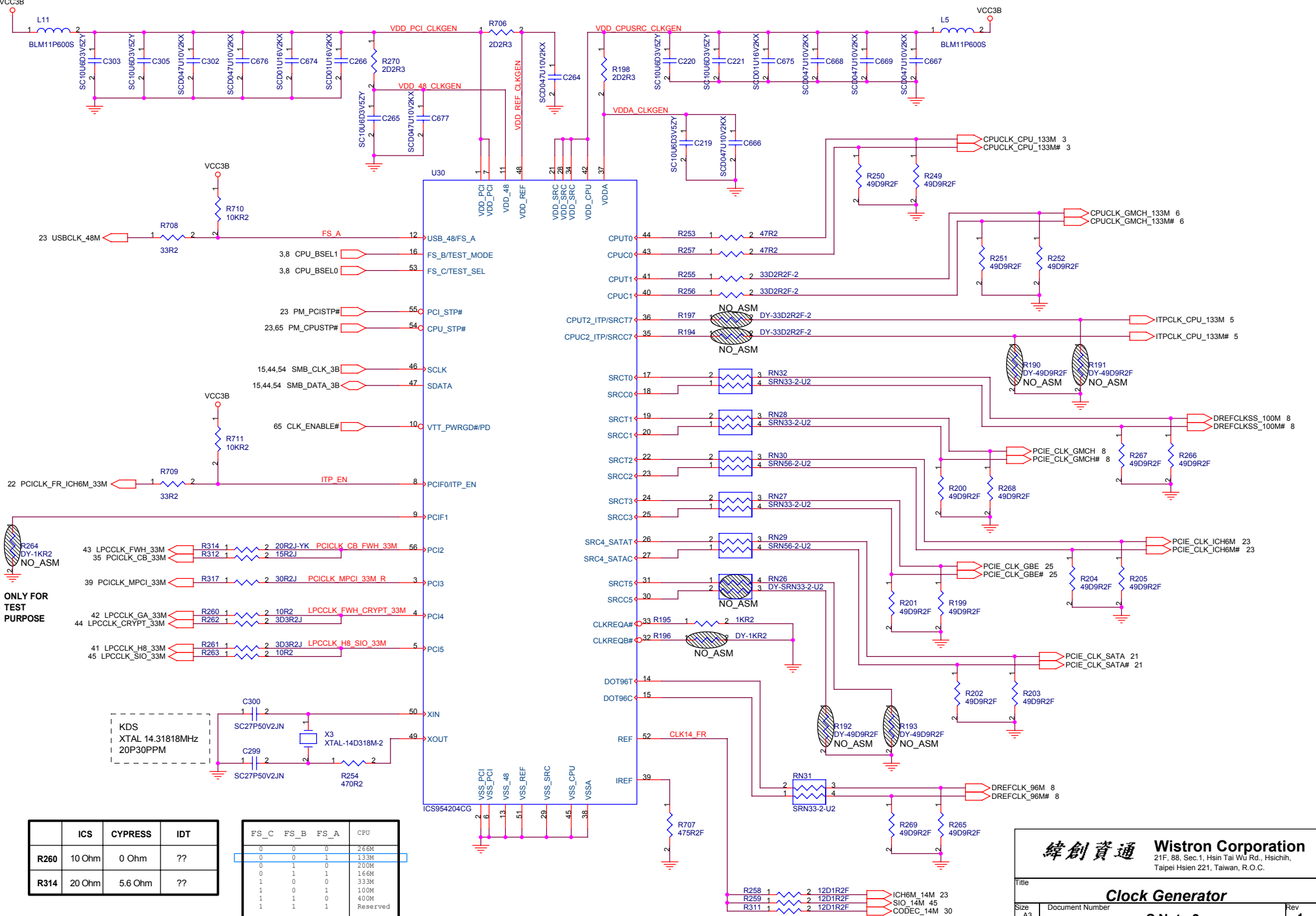


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|       |                        |       |                      |    |     |
|-------|------------------------|-------|----------------------|----|-----|
| Title |                        |       | <b>CRT SELECTION</b> |    |     |
| Size  | Document Number        |       |                      |    | Rev |
| A3    | <b>S Note-3</b>        |       |                      |    | -1  |
| Date: | Tuesday, June 21, 2005 | Sheet | 18                   | of | 75  |



|  |                 |    |     |
|--|-----------------|----|-----|
| <b>緯創資通 Wistron Corporation</b>  |                 |    |     |
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| <b>EXT CRT CONNECTOR</b>   |                 |    |     |
| Title  | Document Number |    | Rev |
| Size A3  | <b>S Note-3</b> |    | -1  |
| Date: Tuesday, June 21, 2005   | Sheet 19        | of | 75  |



ONLY FOR TEST PURPOSE

|      | ICS    | CYPRESS | IDT |
|------|--------|---------|-----|
| R260 | 10 Ohm | 0 Ohm   | ??  |
| R314 | 20 Ohm | 5.6 Ohm | ??  |

| FS_C | FS_B | FS_A | CPU      |
|------|------|------|----------|
| 0    | 0    | 0    | 266M     |
| 0    | 0    | 1    | 133M     |
| 0    | 1    | 0    | 200M     |
| 0    | 1    | 1    | 166M     |
| 1    | 0    | 0    | 333M     |
| 1    | 0    | 1    | 100M     |
| 1    | 1    | 0    | 400M     |
| 1    | 1    | 1    | Reserved |

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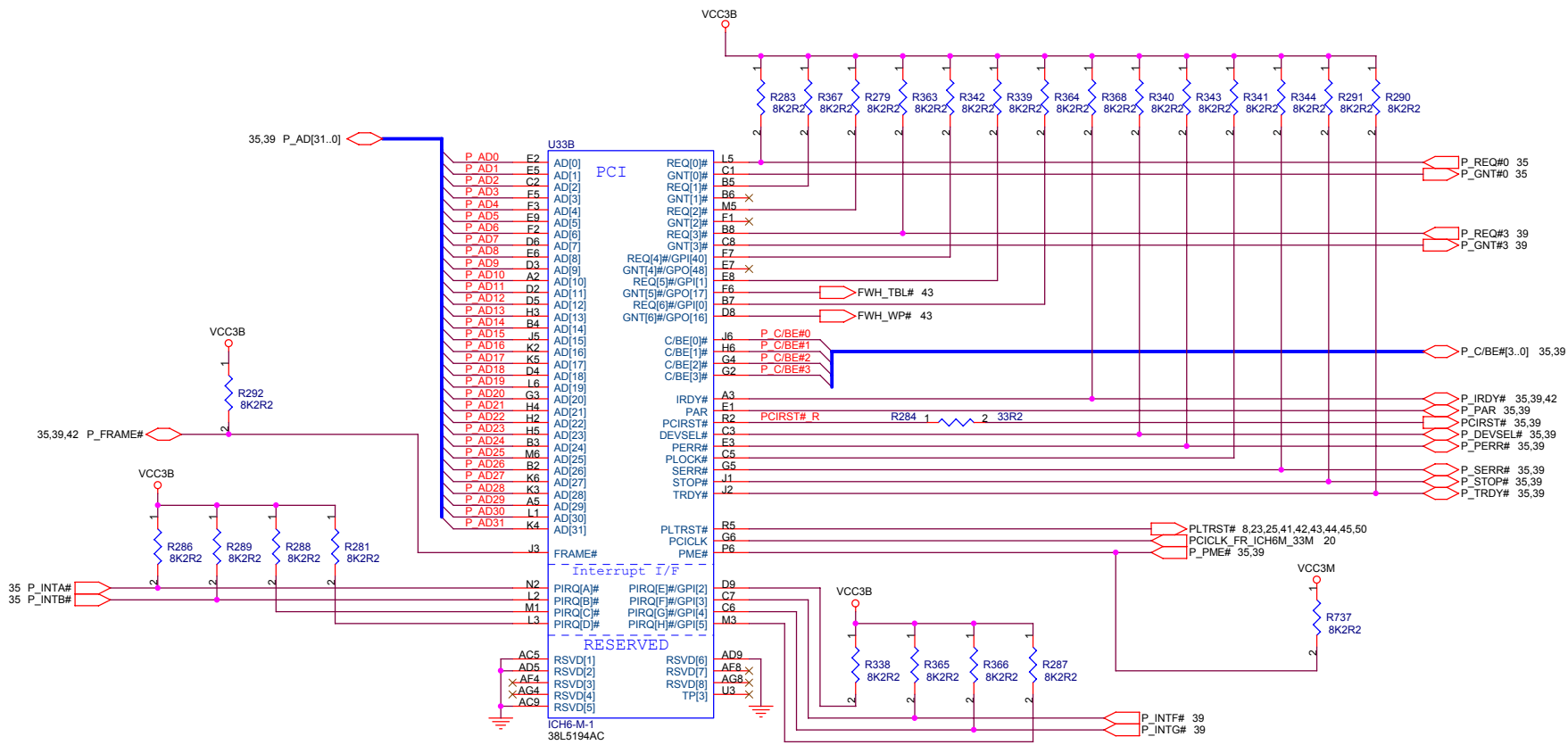
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Title: **Clock Generator**

Size A3 Document Number: **S Note-3** Rev: **-1**

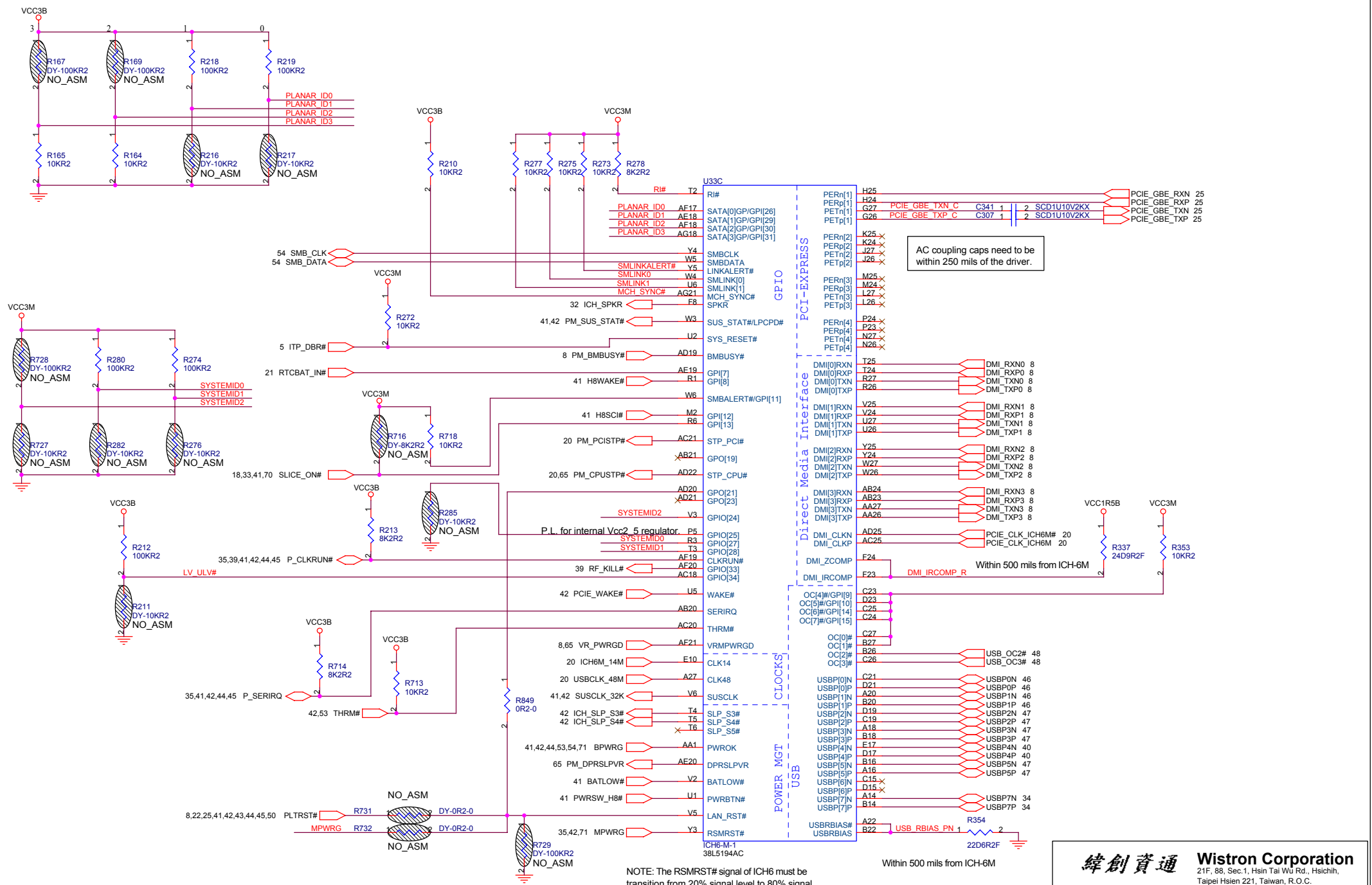
Date: Tuesday, June 21, 2005 Sheet 20 of 75





AC5: SATA1RXN  
 AD5: SATA1RXP  
 AC9: SATA3RXN  
 AD5: SATA3RXP





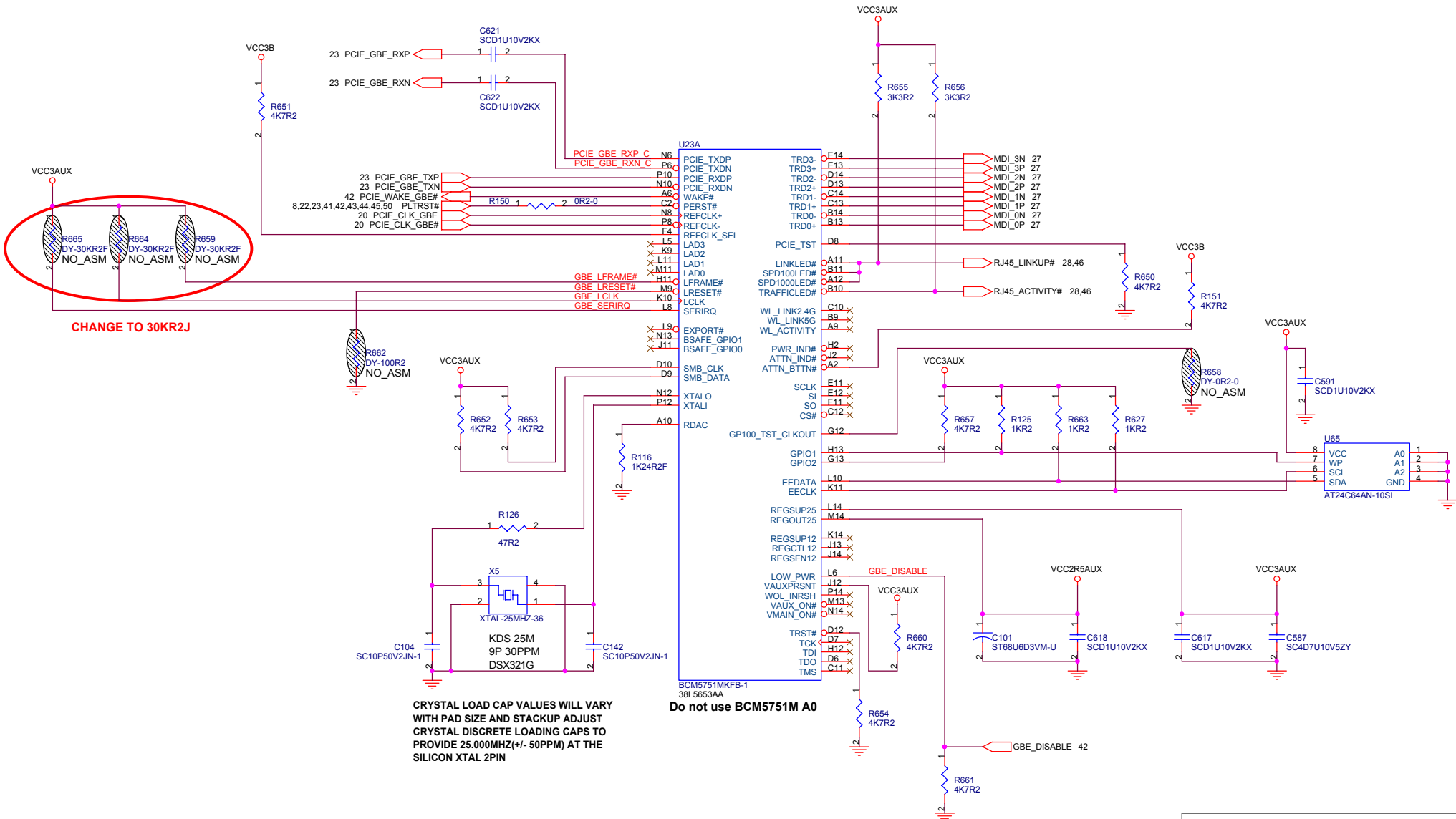
AC coupling caps need to be within 250 mils of the driver.

Within 500 mils from ICH6-M

Within 500 mils from ICH6-M

|  |                 |    |
|--|-----------------|----|
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| <b>ICH6-M (3/4)</b>  |                 |    |
| Title  | Rev             |    |
| Size   | Document Number | -1 |
| <b>S Note-3</b>  |                 |    |
| Date: Tuesday, June 21, 2005   | Sheet 23 of     | 75 |





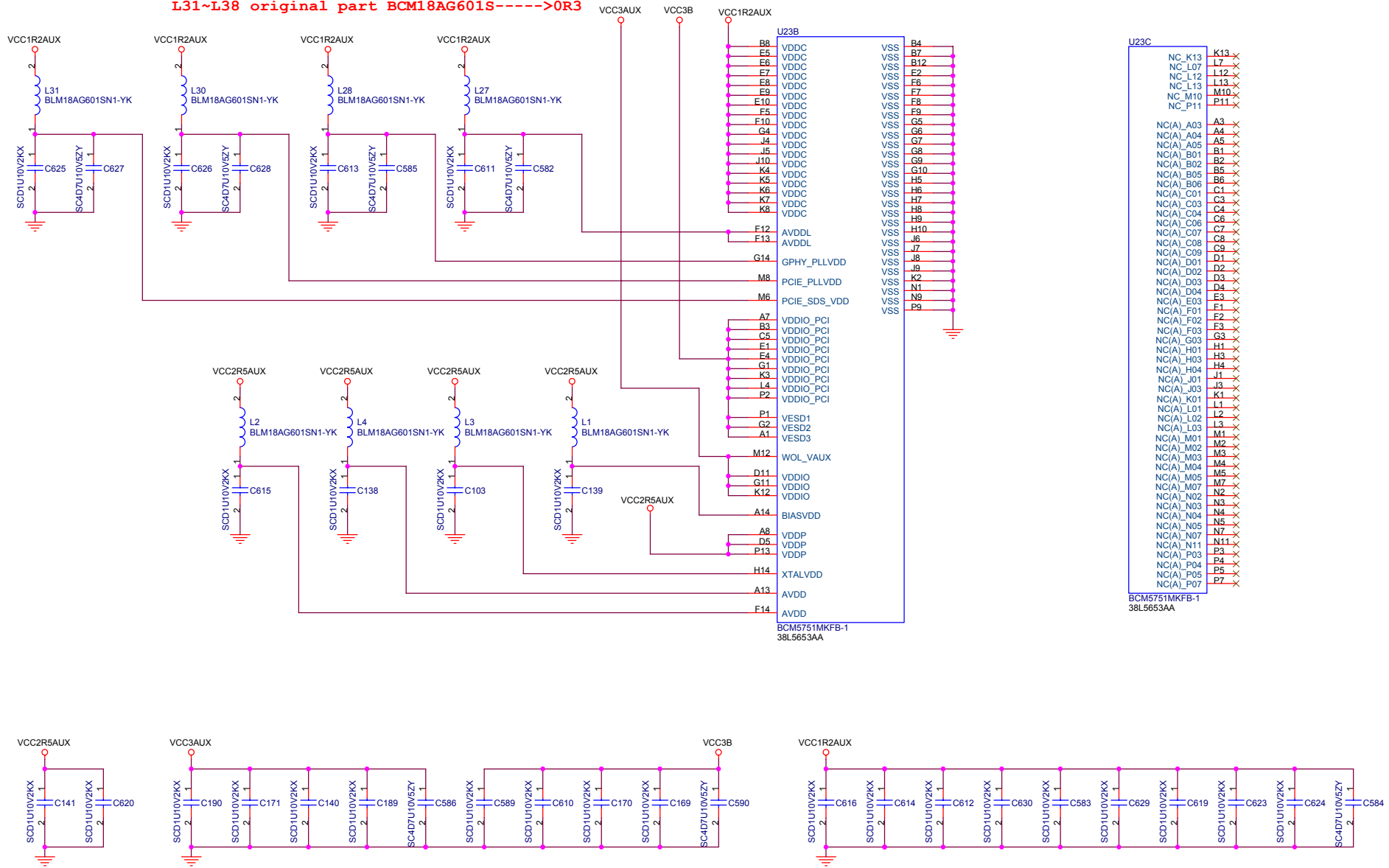
CHANGE TO 30KR2J

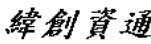
CRYSTAL LOAD CAP VALUES WILL VARY WITH PAD SIZE AND STACKUP ADJUST CRYSTAL DISCRETE LOADING CAPS TO PROVIDE 25.000MHZ(+/- 50PPM) AT THE SILICON XTAL 2PIN

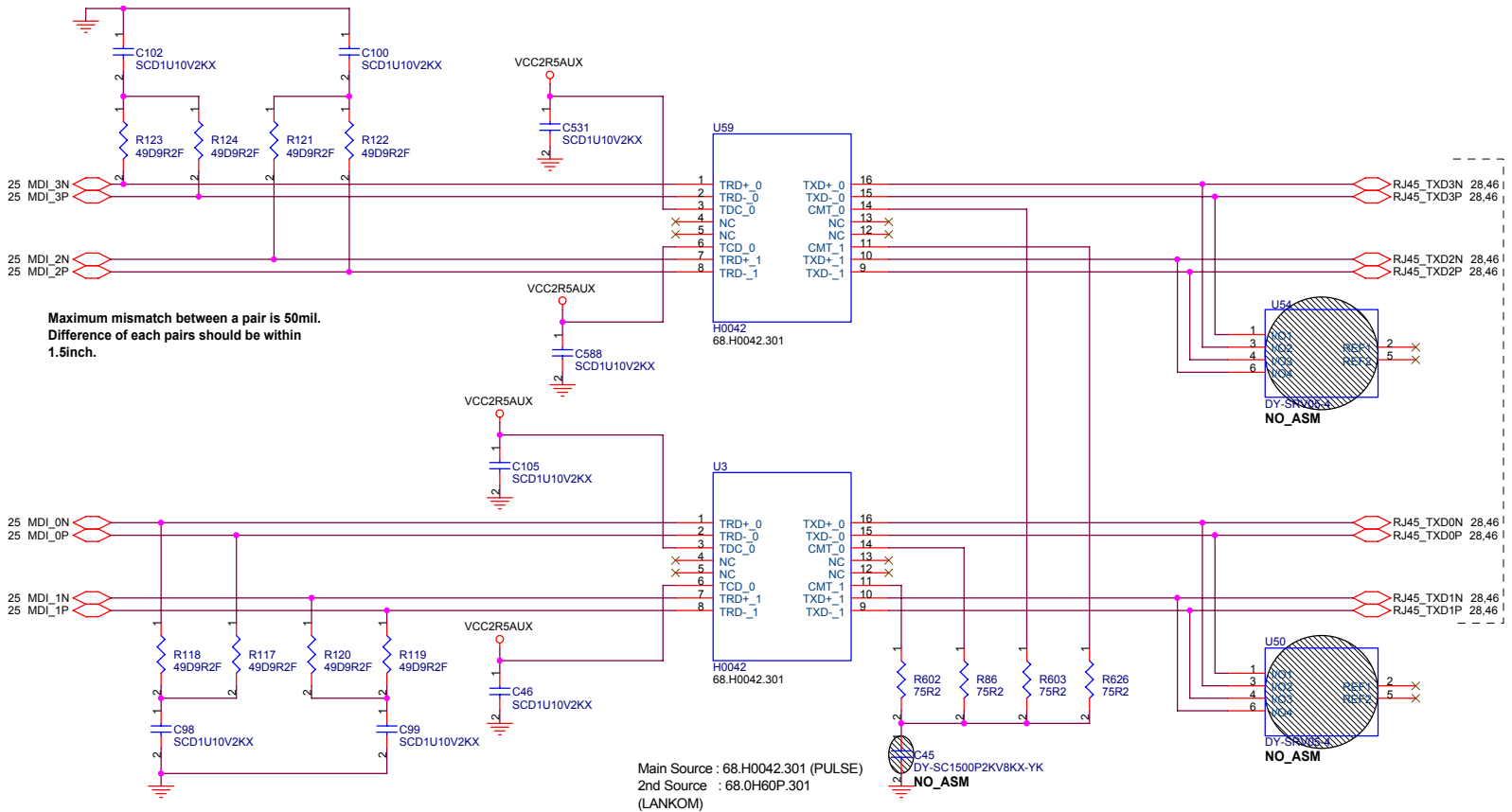
Do not use BCM5751M A0

|                              |                 |  |    |
|------------------------------|-----------------|--|----|
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| Title                        |                 |  |    |
| <b>GBE BCM5751 (1/2)</b>     |                 |  |    |
| Size                         | Document Number | Rev  |    |
| A3                           |                 | <b>S Note-3</b>  |    |
| Date: Tuesday, June 21, 2005 |                 | Sheet  | of |
|                              |                 | 25   | 75 |

L31~L38 original part BCM18AG601S----->OR3



|  |           |
|--|-----------|
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| <b>GBE BCM5751M (2/2) : POWER</b>  |           |
| Title<br>Document Number   | Rev<br>-1 |
| <b>S Note-3</b>  |           |
| Date: Tuesday, June 21, 2005      Sheet 26 of 75   |           |

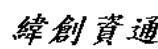


Maximum mismatch between a pair is 50mil.  
Difference of each pairs should be within 1.5inch.

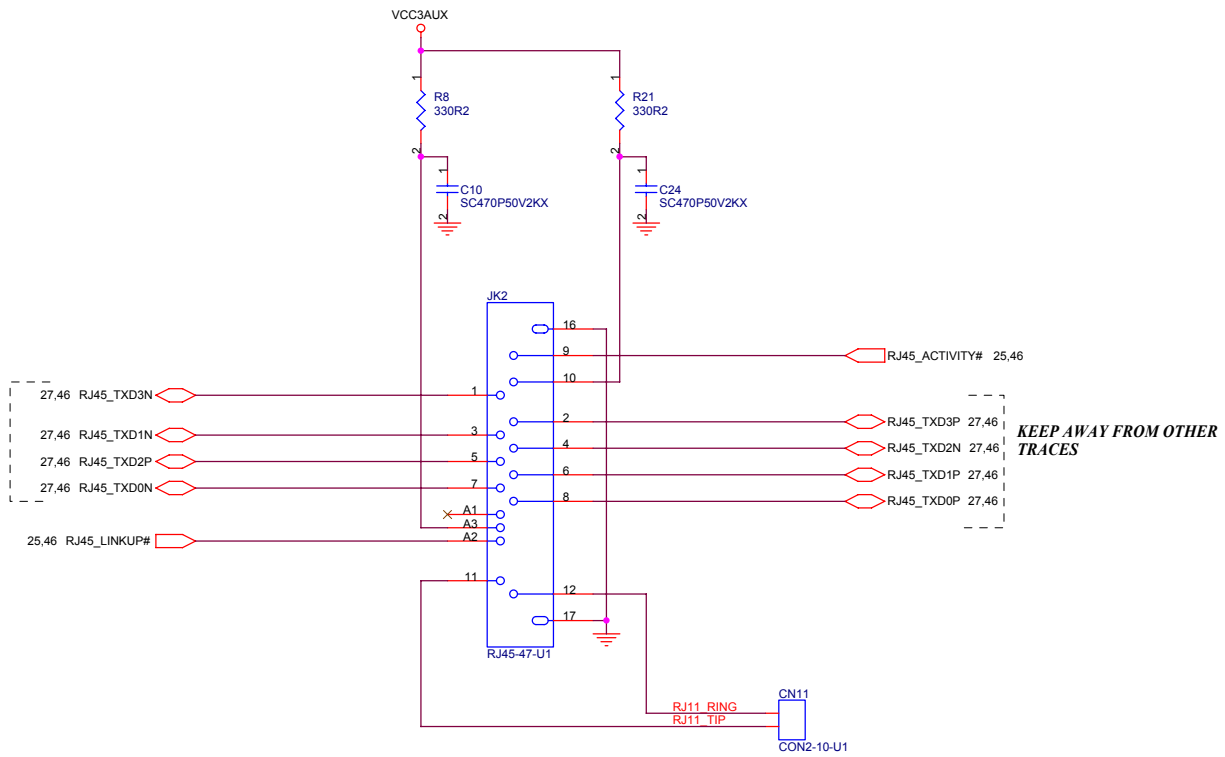
Be careful wiring.  
- Need more 40mil spacing from other signals in case of routing on top/bottom(surface) side.  
- Need more 20mil spacing from other signals in case of routing on internal layers.

Maximum mismatch between a pair is 50mil.  
Difference of each pairs should be within 1.5inch.

Main Source : 68.H0042.301 (PULSE)  
2nd Source : 68.OH60P.301 (LANKOM)

|  |                 |
|--|-----------------|
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| <b>GBE MAGNETICS</b>   |                 |
| Title  |                 |
| Size   | Document Number |
| A3   | S Note-3        |
| Date: Tuesday, June 21, 2005   | Sheet 27 of 75  |
| Rev -1   |                 |

KEEP AWAY FROM OTHER TRACES



KEEP AWAY FROM OTHER TRACES

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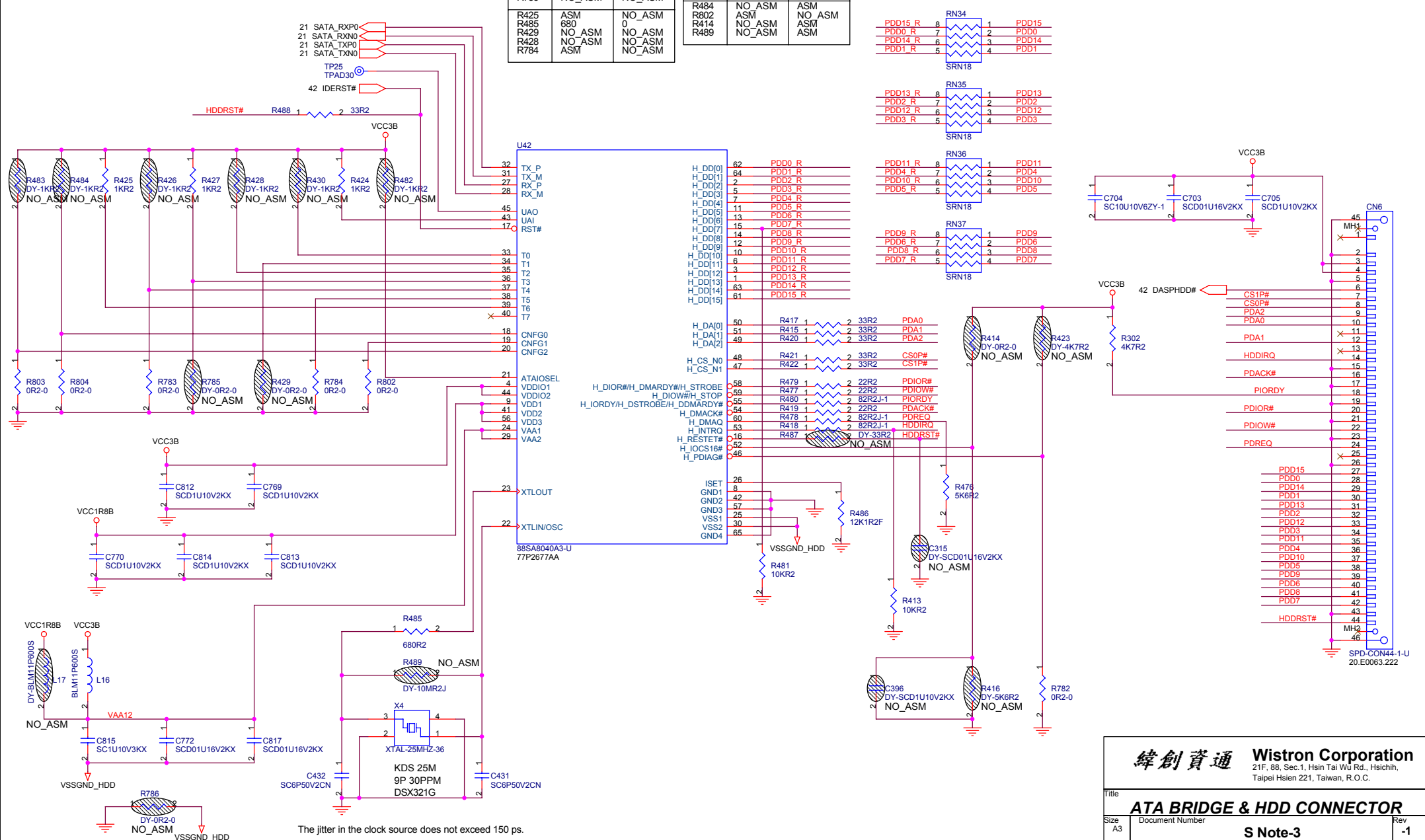
|                              |                 |                       |           |
|------------------------------|-----------------|-----------------------|-----------|
| Title                        |                 | <b>RJ11/RJ45 CONN</b> |           |
| Size<br>A3                   | Document Number | <b>S Note-3</b>       | Rev<br>-1 |
| Date: Tuesday, June 21, 2005 | Sheet           | 28                    | of 75     |

S-ATA TABLE 1/2

| U42                                  | 88SA8040                                    | SII3811                                     |
|--------------------------------------|---|---|
| C396<br>C431<br>C432                 | NO_ASM<br>10PF<br>10PF                      | ASM<br>10PF<br>10PF                         |
| L17<br>L16                           | NO_ASM<br>ASM                               | ASM<br>NO_ASM                               |
| R786<br>R426<br>R783<br>R427<br>R785 | NO_ASM<br>NO_ASM<br>ASM<br>NO_ASM<br>NO_ASM | ASM<br>NO_ASM<br>NO_ASM<br>NO_ASM<br>NO_ASM |
| R425<br>R485<br>R429<br>R428<br>R784 | ASM<br>680<br>NO_ASM<br>NO_ASM<br>ASM       | NO_ASM<br>0<br>NO_ASM<br>NO_ASM<br>NO_ASM   |

S-ATA TABLE 2/2

| U42                                  | 88SA8040                                  | SII3811                                    |
|--------------------------------------|---|--|
| R430<br>R424<br>R482<br>R486<br>R416 | NO_ASM<br>ASM<br>NO_ASM<br>12TK<br>NO_ASM | NO_ASM<br>NO_ASM<br>NO_ASM<br>1K<br>NO_ASM |
| R423<br>R782<br>R803<br>R804<br>R483 | NO_ASM<br>ASM<br>ASM<br>ASM<br>NO_ASM     | NO_ASM<br>ASM<br>NO_ASM<br>NO_ASM<br>ASM   |
| R484<br>R802<br>R414<br>R489         | NO_ASM<br>ASM<br>NO_ASM<br>NO_ASM         | ASM<br>NO_ASM<br>ASM<br>ASM                |



The jitter in the clock source does not exceed 150 ps.

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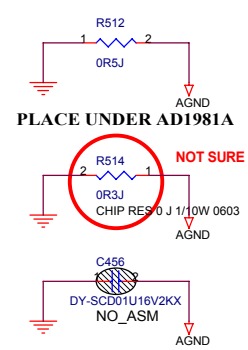
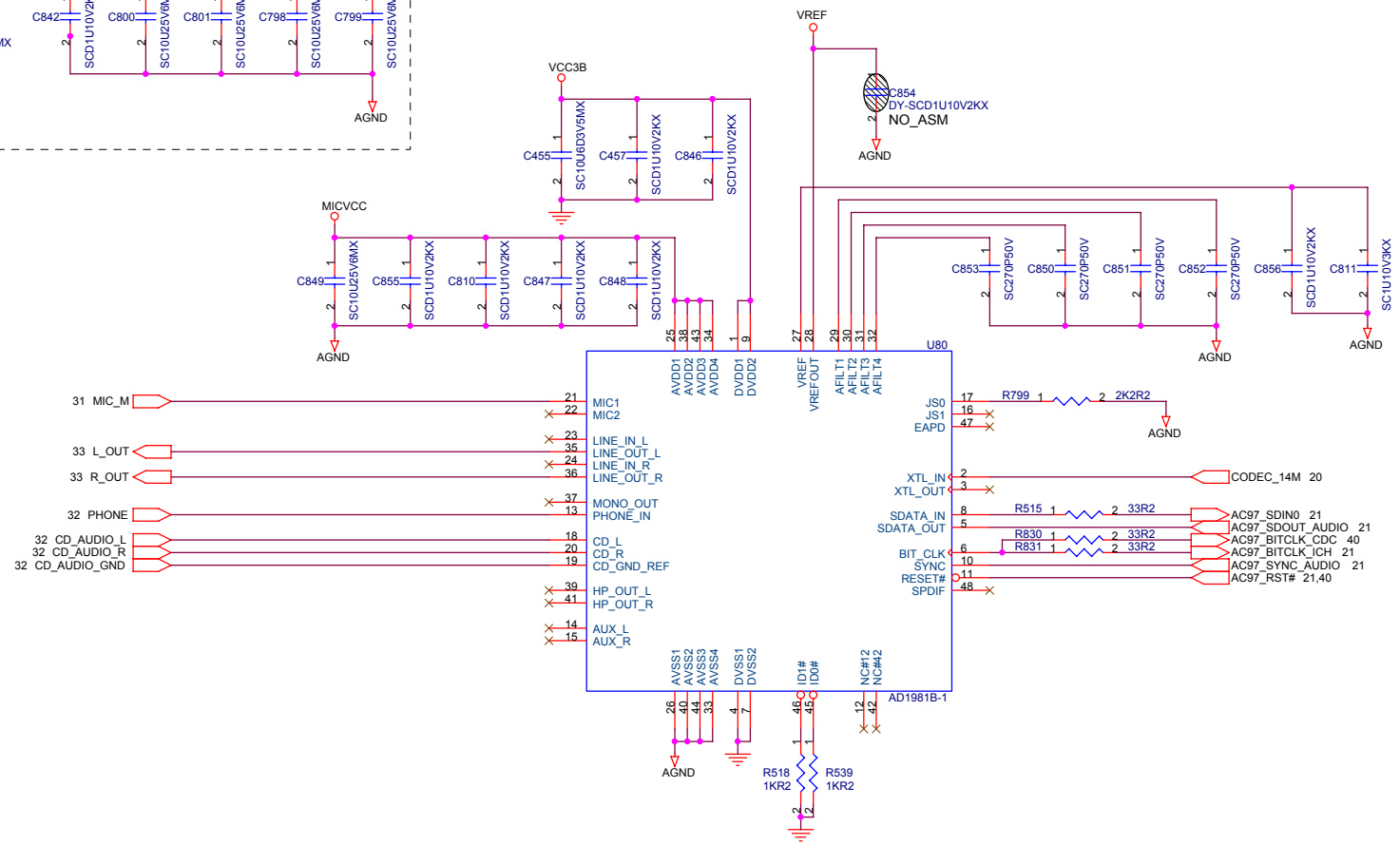
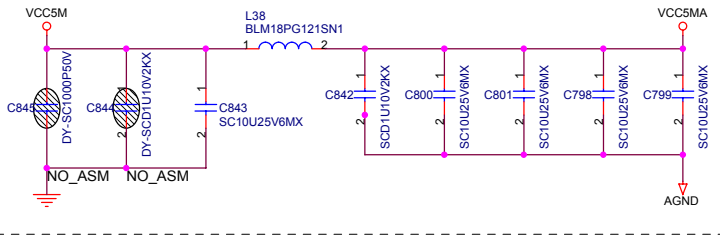
Title: **ATA BRIDGE & HDD CONNECTOR**

Size A3 Document Number: **S Note-3** Rev: **-1**

Date: Tuesday, June 21, 2005 Sheet 29 of 75

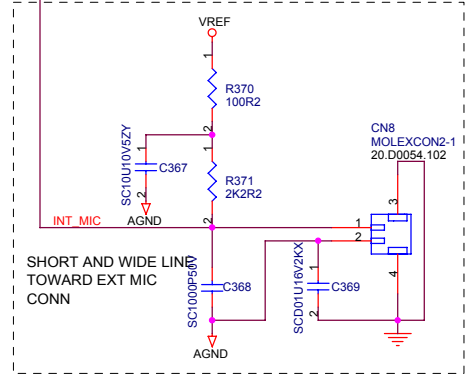
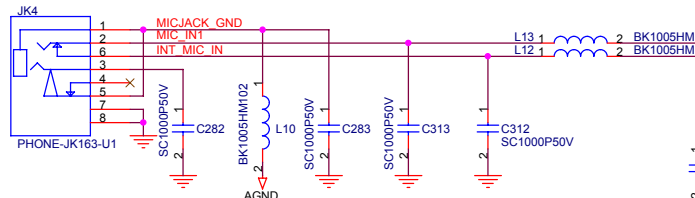


# VCC5MA



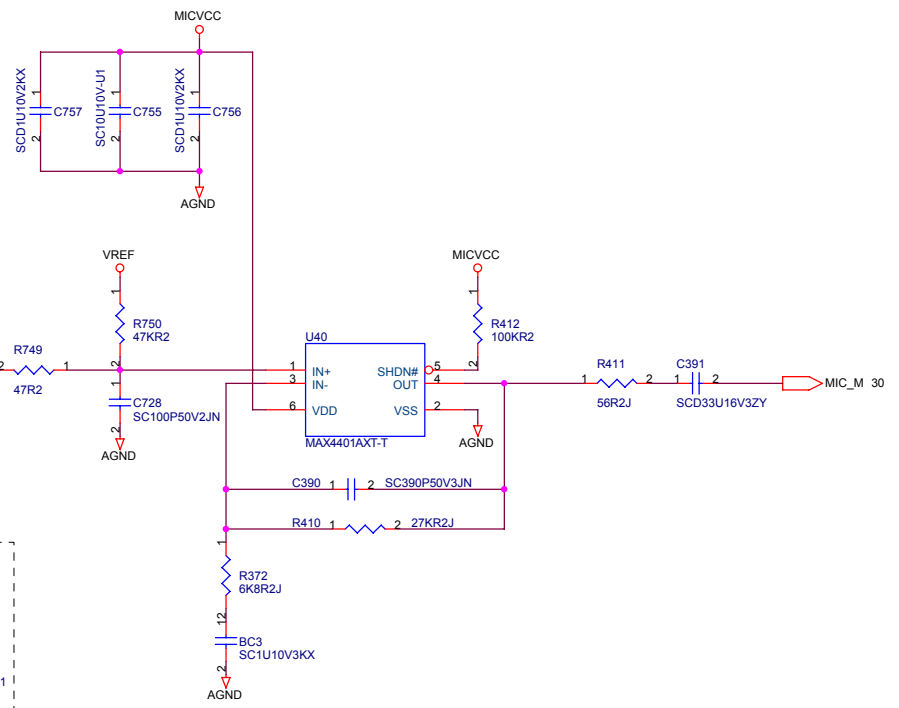
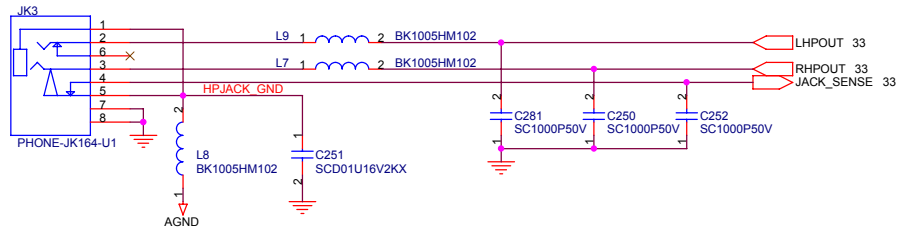
|  |                 |
|--|-----------------|
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| <b>AUDIO 1981B</b>   |                 |
| Title  |                 |
| Size A3  | Document Number |
| <b>S Note-3</b>  |                 |
| Date: Tuesday, June 21, 2005   | Sheet 30 of 75  |
| Rev -1   |                 |

### EXT MIC CONN

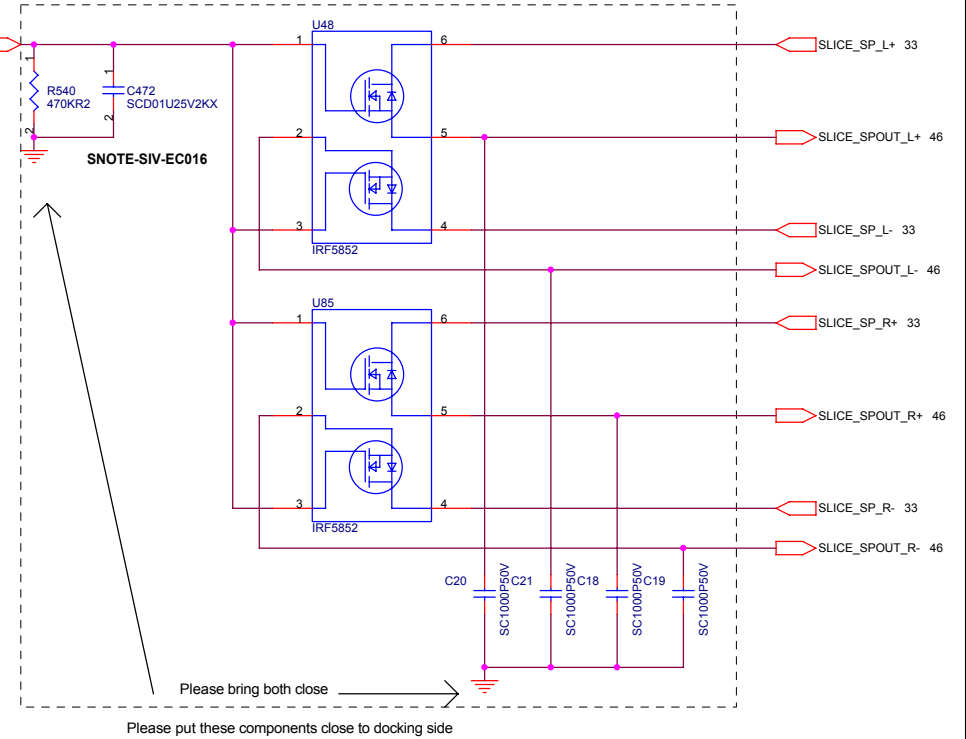
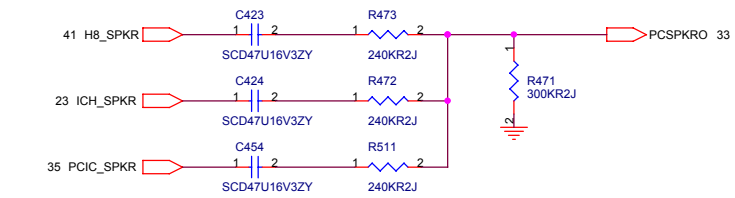
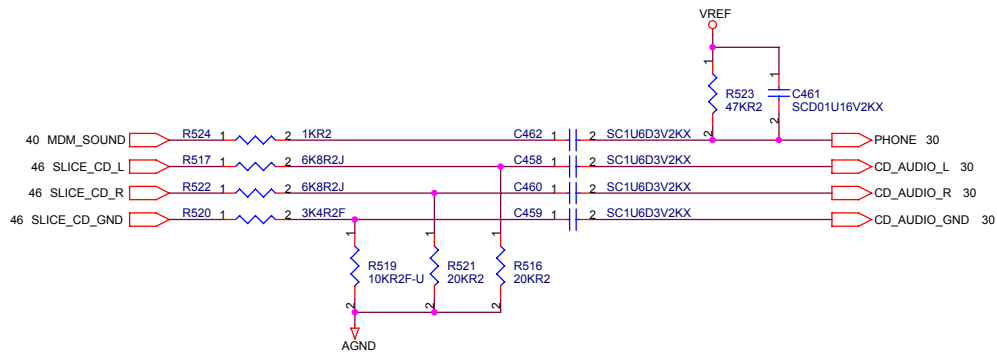
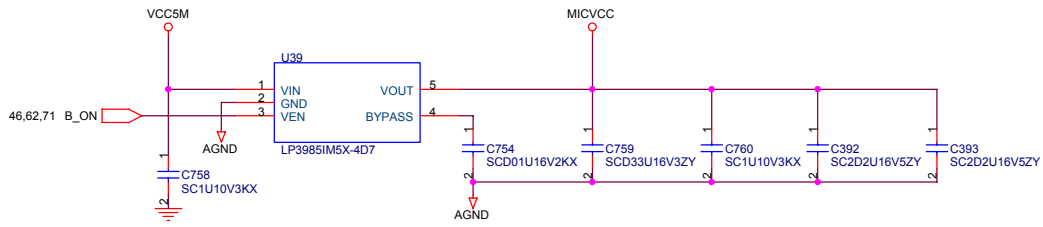


ALL PARTS MUST BE PLACED NEAR TO INTERNAL MICROPHONE

### HEADPHONE CONN



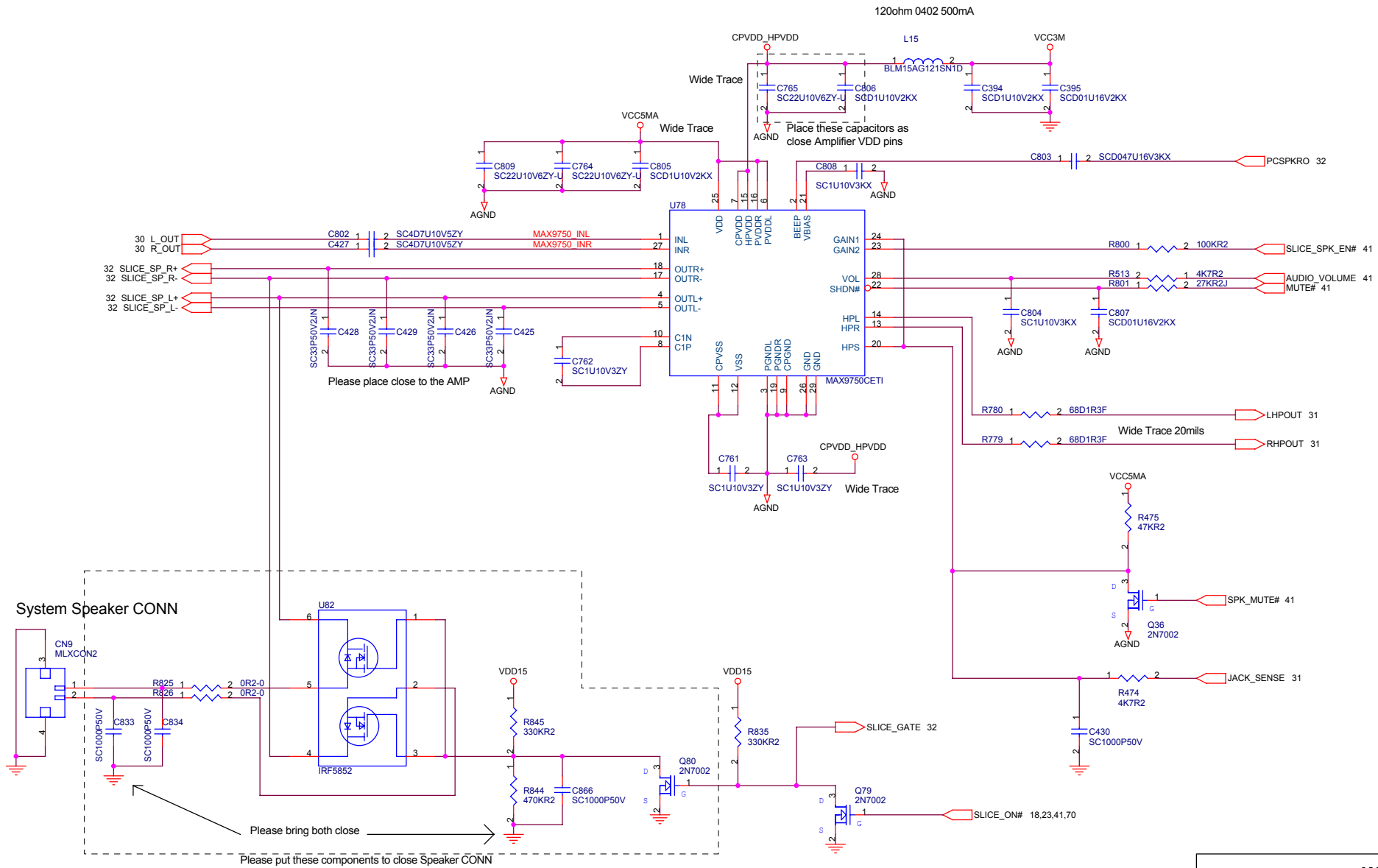
|                              |                 |  |  |
|------------------------------|-----------------|--|--|
| <b>緯創資通</b>                  |                 | <b>Wistron Corporation</b>   |  |
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| Title                        |                 |  |  |
| <b>AUDIO MIC &amp; CONN</b>  |                 |  |  |
| Size                         | Document Number | Rev  |  |
| A3                           |                 | -1   |  |
| <b>S Note-3</b>              |                 |  |  |
| Date: Tuesday, June 21, 2005 |                 | Sheet 31 of 75   |  |



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|                              |                 |          |                |  |    |
|------------------------------|-----------------|----------|----------------|--|----|
| Title                        |                 |          | AUDIO MISC     |  |    |
| Size                         | Document Number | Rev      |                |  |    |
| A3                           |                 | S Note-3 |                |  | -1 |
| Date: Tuesday, June 21, 2005 |                 |          | Sheet 32 of 75 |  |    |

| SPEAKER MODE GAIN (dB) |                        |                        |                        | HEADPHONE MODE GAIN (dB) |                        |
|------------------------|------------------------|------------------------|------------------------|--------------------------|------------------------|
| GAIN1 = 0<br>GAIN2 = 0 | GAIN1 = 1<br>GAIN2 = 0 | GAIN1 = 0<br>GAIN2 = 1 | GAIN1 = 1<br>GAIN2 = 1 | GAIN1 = X<br>GAIN2 = 0   | GAIN1 = X<br>GAIN2 = 1 |
| 6                      | 7.5                    | 9                      | 10.5                   | 0                        | 3                      |

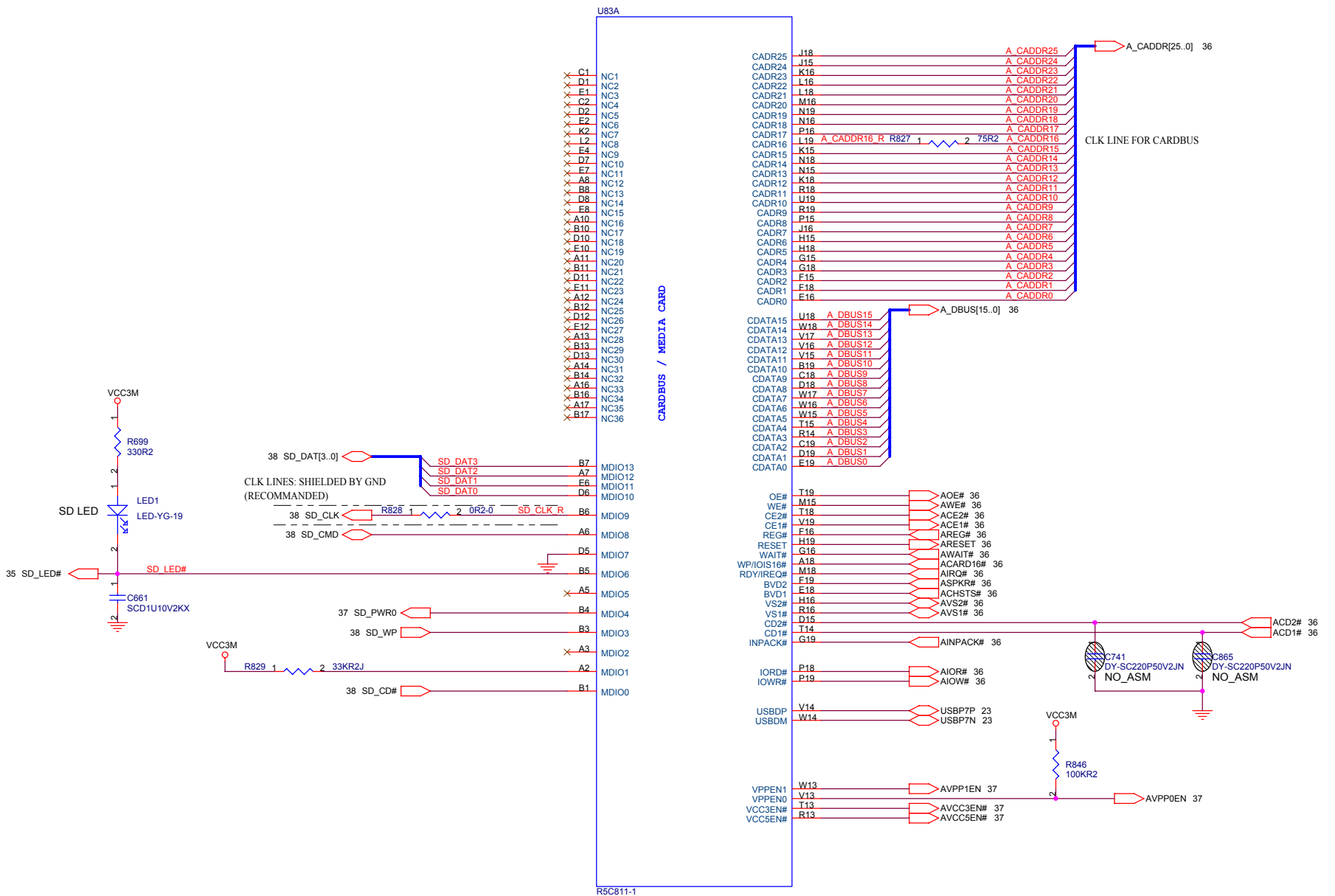


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Title: **AUDIO AMP MAX9750**

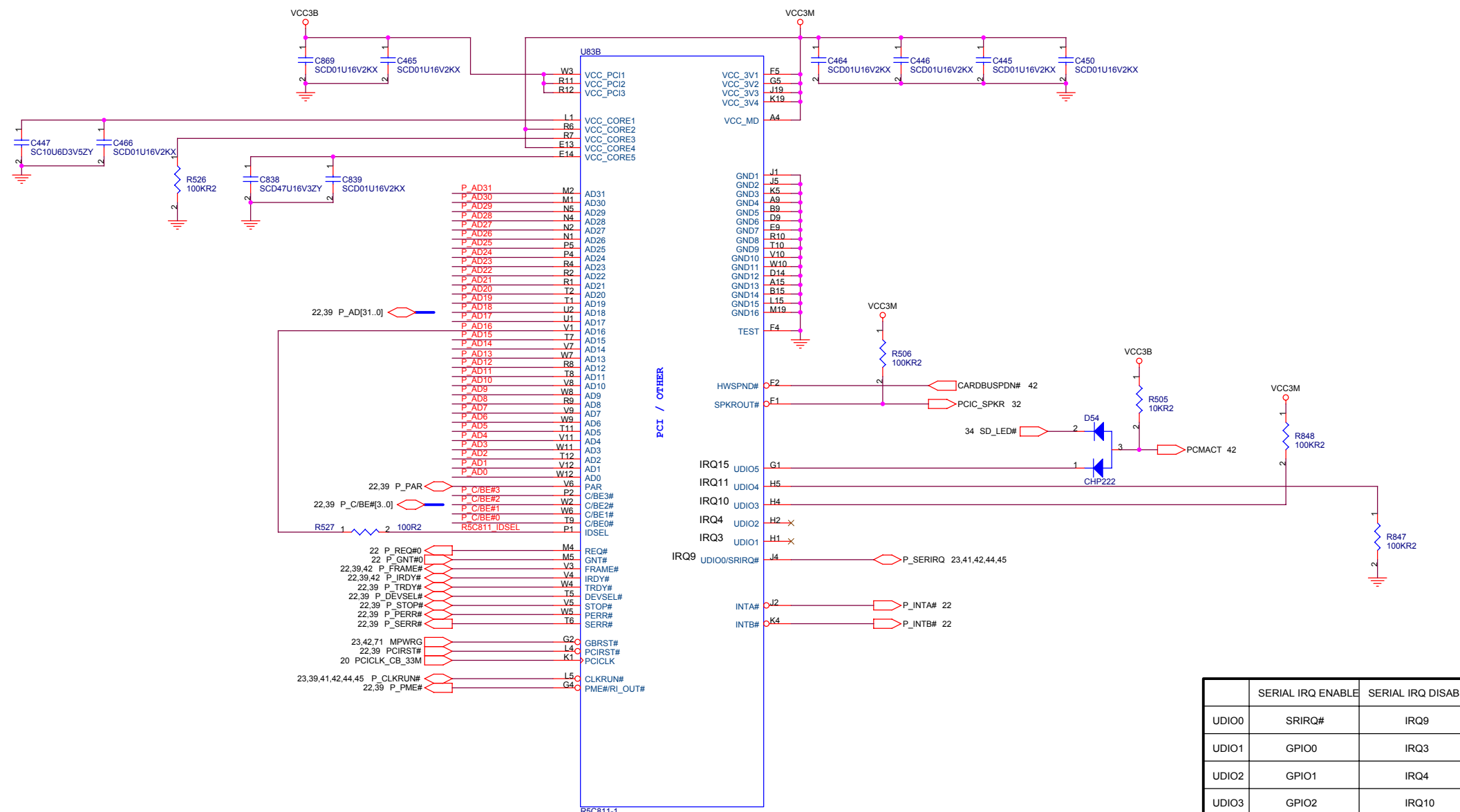
Size: A3 Document Number: **S Note-3** Rev: -1

Date: Tuesday, June 21, 2005 Sheet: 33 of 75



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|                              |                 |                      |  |
|------------------------------|-----------------|----------------------|--|
| Title                        |                 | <b>CARD BUS(1/2)</b> |  |
| Size                         | Document Number | <b>S Note-3</b>      |  |
| A3                           |                 | Rev -1               |  |
| Date: Tuesday, June 21, 2005 |                 | Sheet 34 of 75       |  |



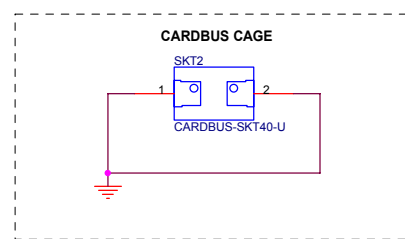
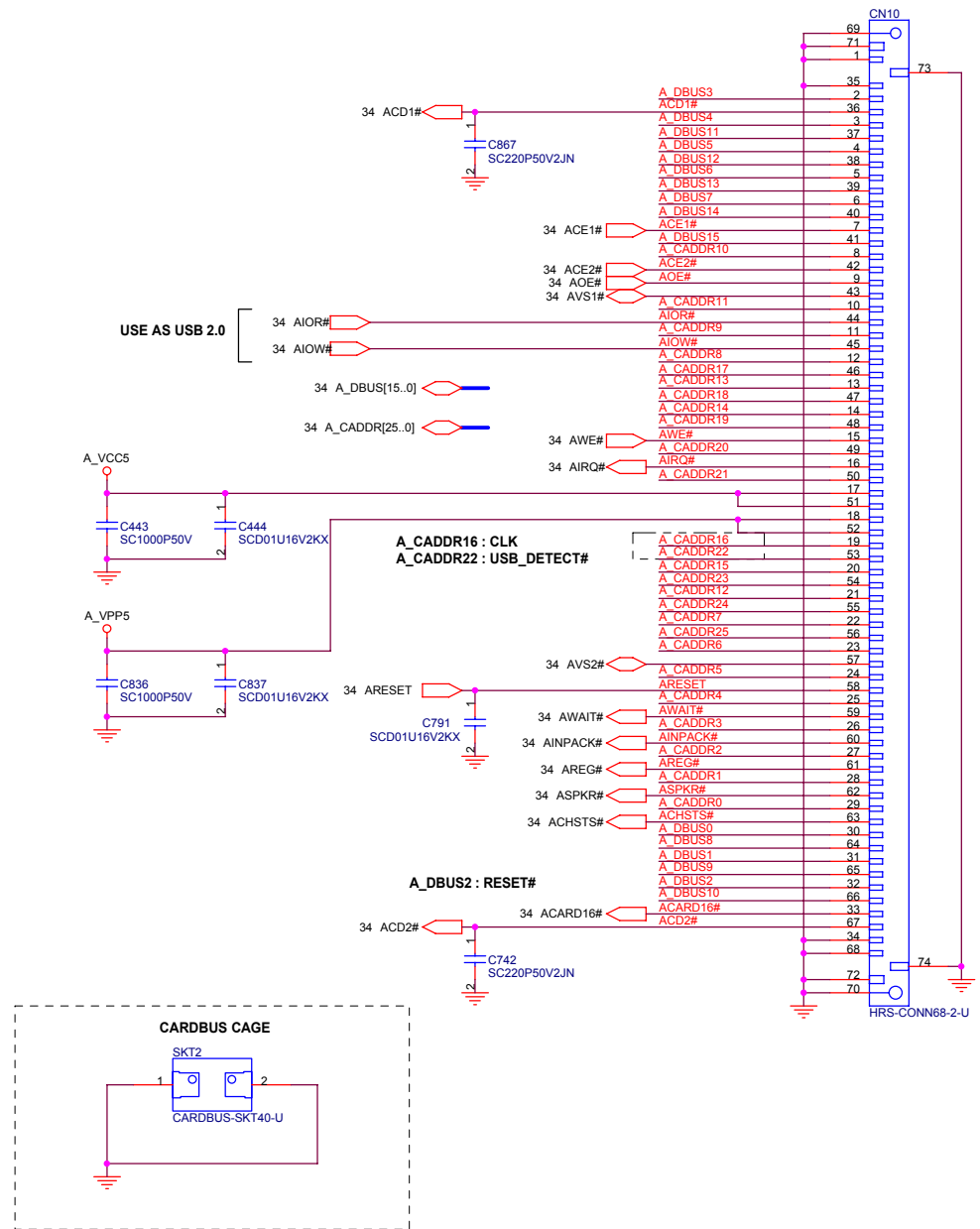
|       | SERIAL IRQ ENABLE | SERIAL IRQ DISABLE |
|-------|-------------------|--------------------|
| UDIO0 | SRIQ#             | IRQ9               |
| UDIO1 | GPIO0             | IRQ3               |
| UDIO2 | GPIO1             | IRQ4               |
| UDIO3 | GPIO2             | IRQ10              |
| UDIO4 | GPIO3             | IRQ11              |
| UDIO5 | LED0#             | IRQ15              |

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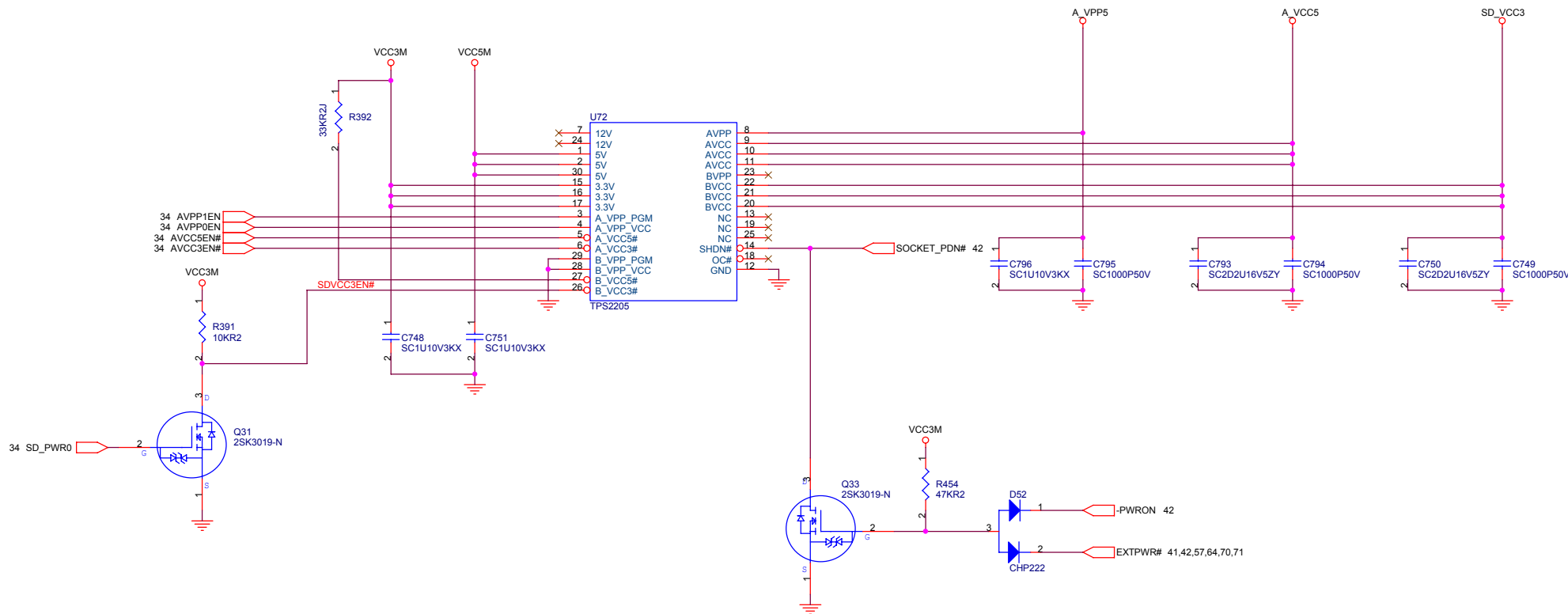
Title: **CARD BUS(2/2)**

Size: A3 Document Number: **S Note-3** Rev: -1

Date: Tuesday, June 21, 2005 Sheet: 35 of 75



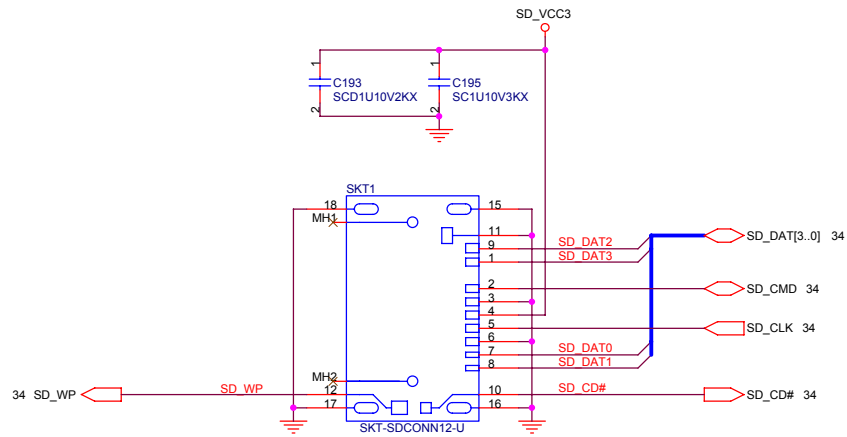




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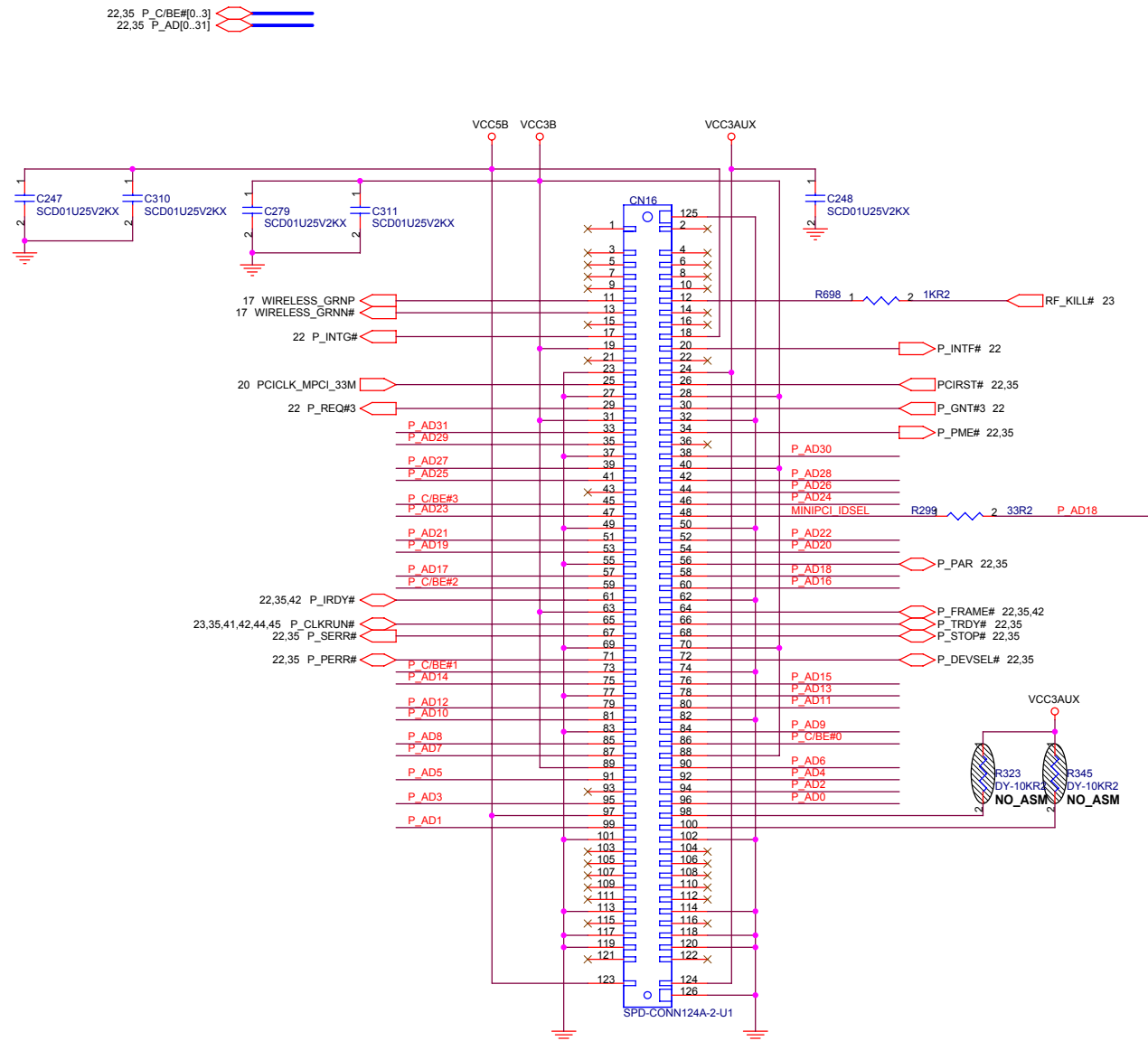
|                               |                 |                |
|-------------------------------|-----------------|----------------|
| Title                         |                 |                |
| <b>CARD BUS POWER CONTROL</b> |                 |                |
| Size                          | Document Number | Rev            |
| A3                            |                 | -1             |
| Date: Tuesday, June 21, 2005  |                 | Sheet 37 of 75 |

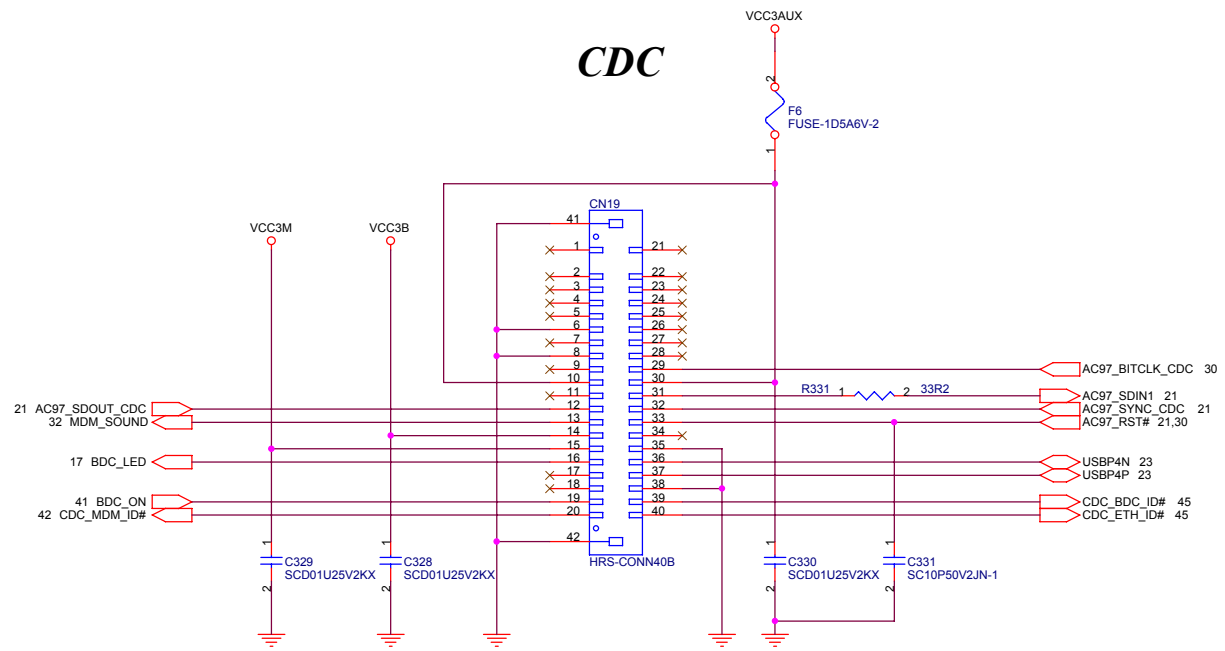
# SD Slot



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|                              |                 |     |
|------------------------------|-----------------|-----|
| Title                        |                 |     |
| <b>SD SLOT</b>               |                 |     |
| Size                         | Document Number | Rev |
| A3                           | <b>S Note-3</b> | -1  |
| Date: Tuesday, June 21, 2005 |                 |     |
| Sheet 38 of 75               |                 |     |









MEM\_BASE\_ID[4..0]

| FWH GPIn     | 4 | 3 | 2 | 1 | 0        | Base Memory    | Memory   | Memory Bank     |  |
|--------------|---|---|---|---|----------|----------------|----------|-----------------|--|
| BASE_MEM_IDn | 4 | 3 | 2 | 1 | 0        | Total Capacity | Capacity | ( Device Q'ty ) |  |
|              | 0 | 0 | 0 | x | x        | 128MB          | 256Mbit  | 1 ( 4pcs )      | Reserved                                     |
|              | 0 | 0 | 1 | x | x        | 256MB          | 256Mbit  | 2 ( 8pcs )      | Reserved                                     |
|              | 0 | 1 | 0 | 0 | 0        | 256MB          | 512Mbit  | 1 ( 4pcs )      | Elpida / Hynix / Infineon / Micron / Samsung |
|              |   |   | 0 | 1 | Reserved |                |          |                 |  |
|              |   |   | 1 | 0 | Reserved |                |          |                 |  |
|              |   |   | 1 | 1 | Reserved |                |          |                 |  |
|              | 0 | 1 | 1 | 0 | 0        | 512MB          | 512Mbit  | 2 ( 8pcs )      | Elpida / Hynix / Infineon / Micron / Samsung |
|              |   |   | 0 | 1 | Reserved |                |          |                 |  |
|              |   |   | 1 | 0 | Reserved |                |          |                 |  |
|              |   |   | 1 | 1 | Reserved |                |          |                 |  |
|              | 1 | 0 | 0 | x | x        | 512MB          | 1Gbit    | 1 ( 4pcs )      | Reserved                                     |
|              | 1 | 0 | 1 | x | x        | 1GB            | 1Gbit    | 2 ( 8pcs )      | Reserved                                     |

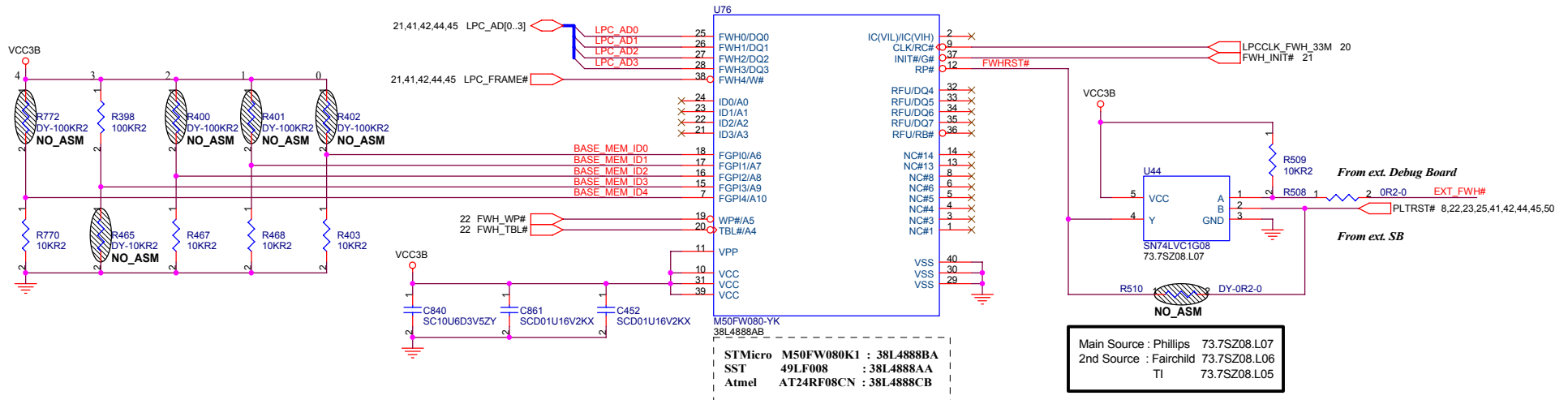
MEM\_BASE\_ID[4..0]

Bit 4-3 : Memory Capacity ID[1:0]  
 00 = 256Mbit  
 01 = 512Mbit  
 10 = 1Gbit  
 11 = Reserved

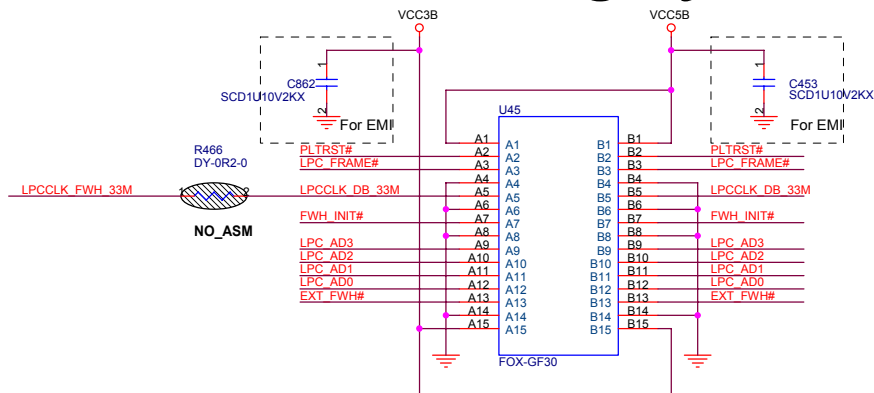
Bit 2 : Memory Bank ID  
 0 = 1 Rank ( 4pcs )  
 1 = 2 Rank ( 8pcs )

Bit 1-0 : Memory Vendor ID[1:0]  
 00 = Default  
 01 = Reserved ( for Specific Memory Vendor )  
 10 = Reserved ( for Specific Memory Vendor )  
 11 = Reserved ( for Specific Memory Vendor )

x : don't care  
 11000b ~ 11111b : reserved



# Golden Finger for Debug Board



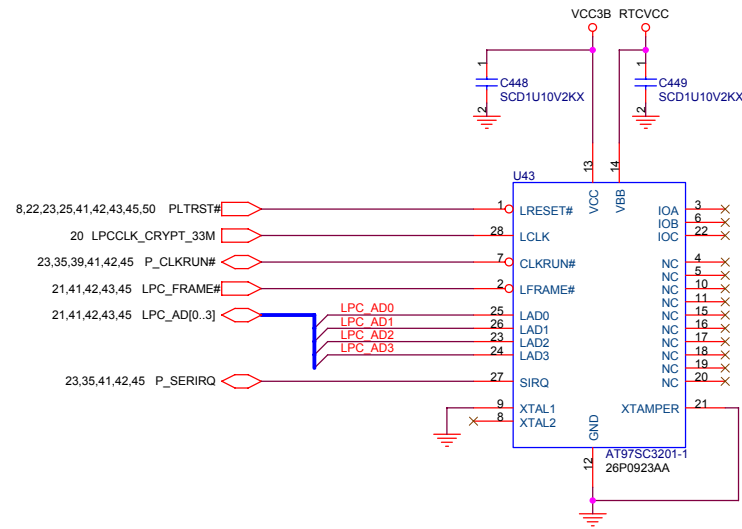
TOP VIEW

- A15 (B1)
- A14 (B2)
- ...
- A2 (B14)
- A1 (B15)

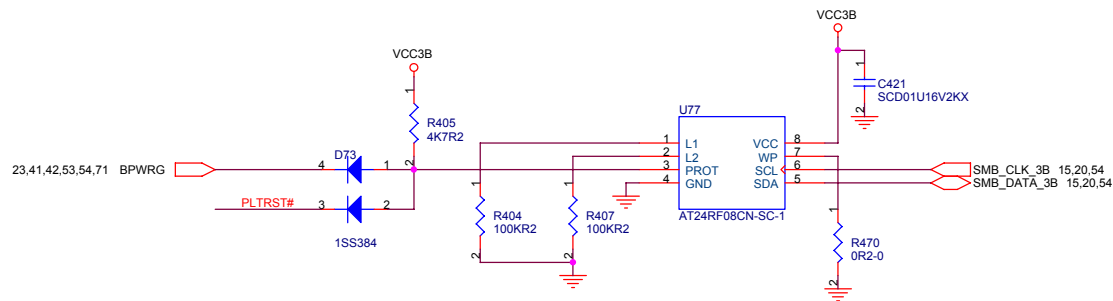
(BOTTOM VIEW)

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# TCPA



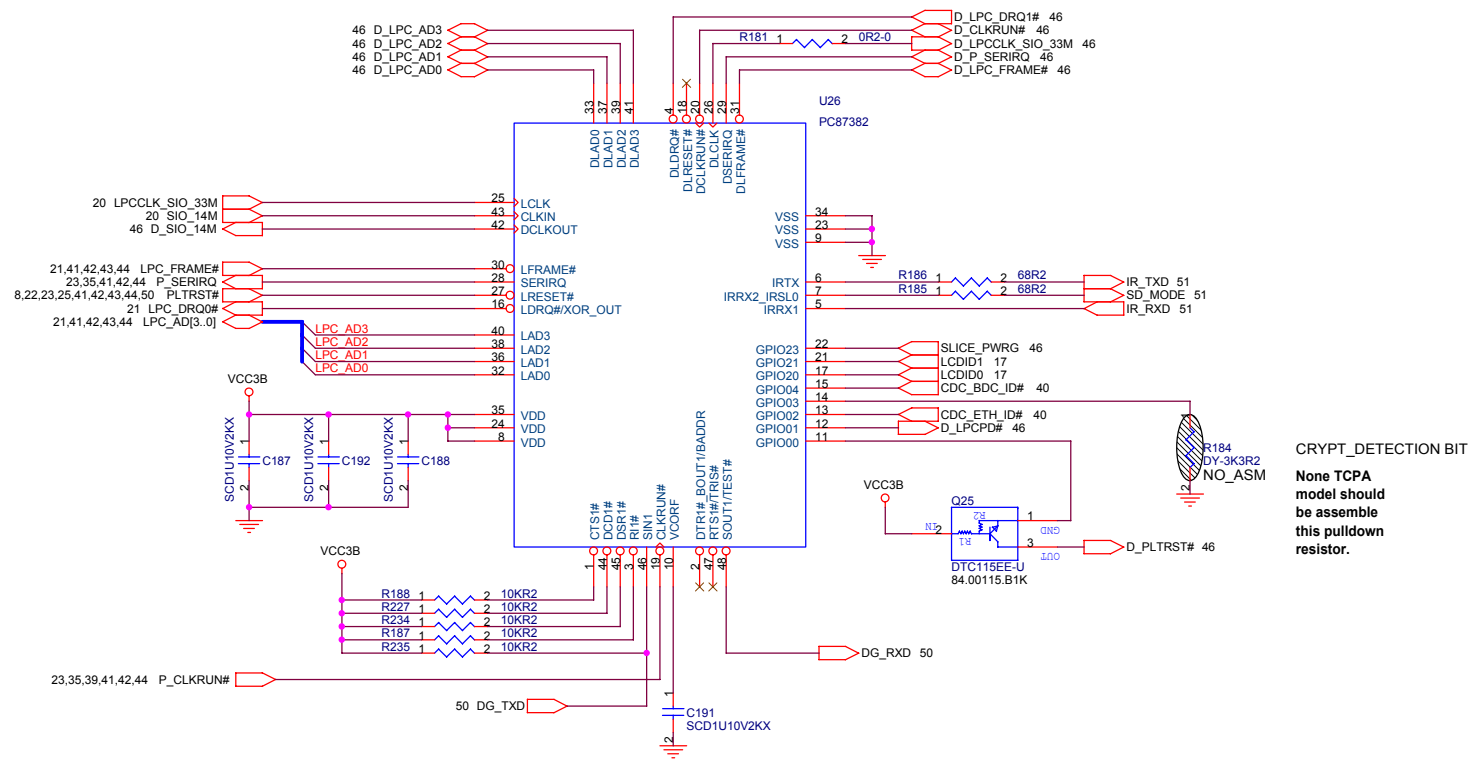
# EEPROM



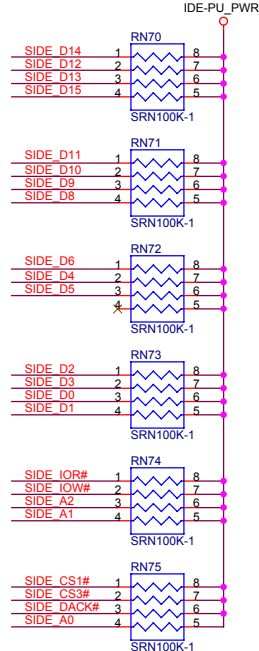
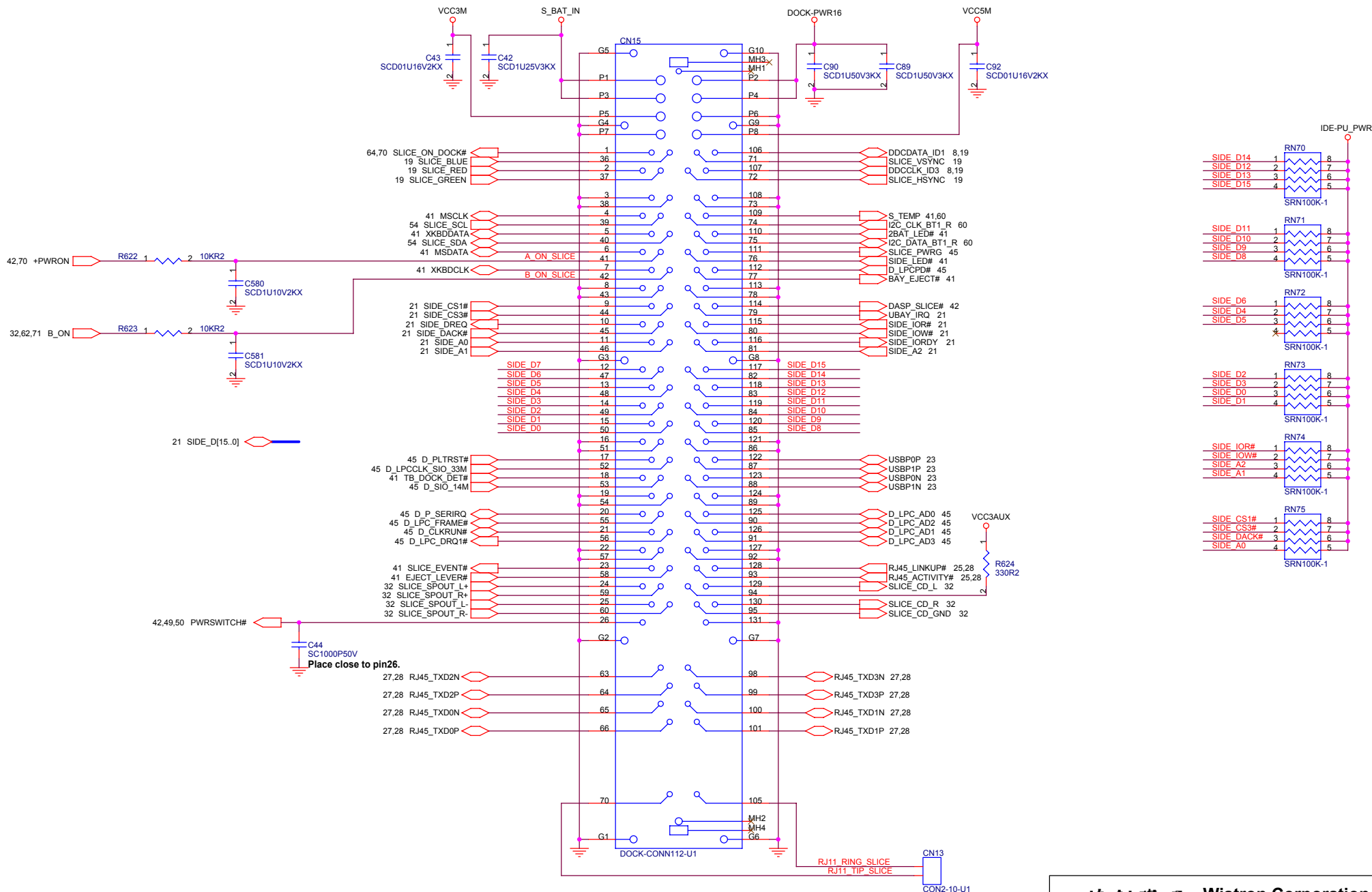
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|                              |                 |                |
|------------------------------|-----------------|----------------|
| Title                        |                 |                |
| <b>EEPROM / TPM</b>          |                 |                |
| Size                         | Document Number | Rev            |
| A3                           | <b>S Note-3</b> | -1             |
| Date: Tuesday, June 21, 2005 |                 | Sheet 44 of 75 |



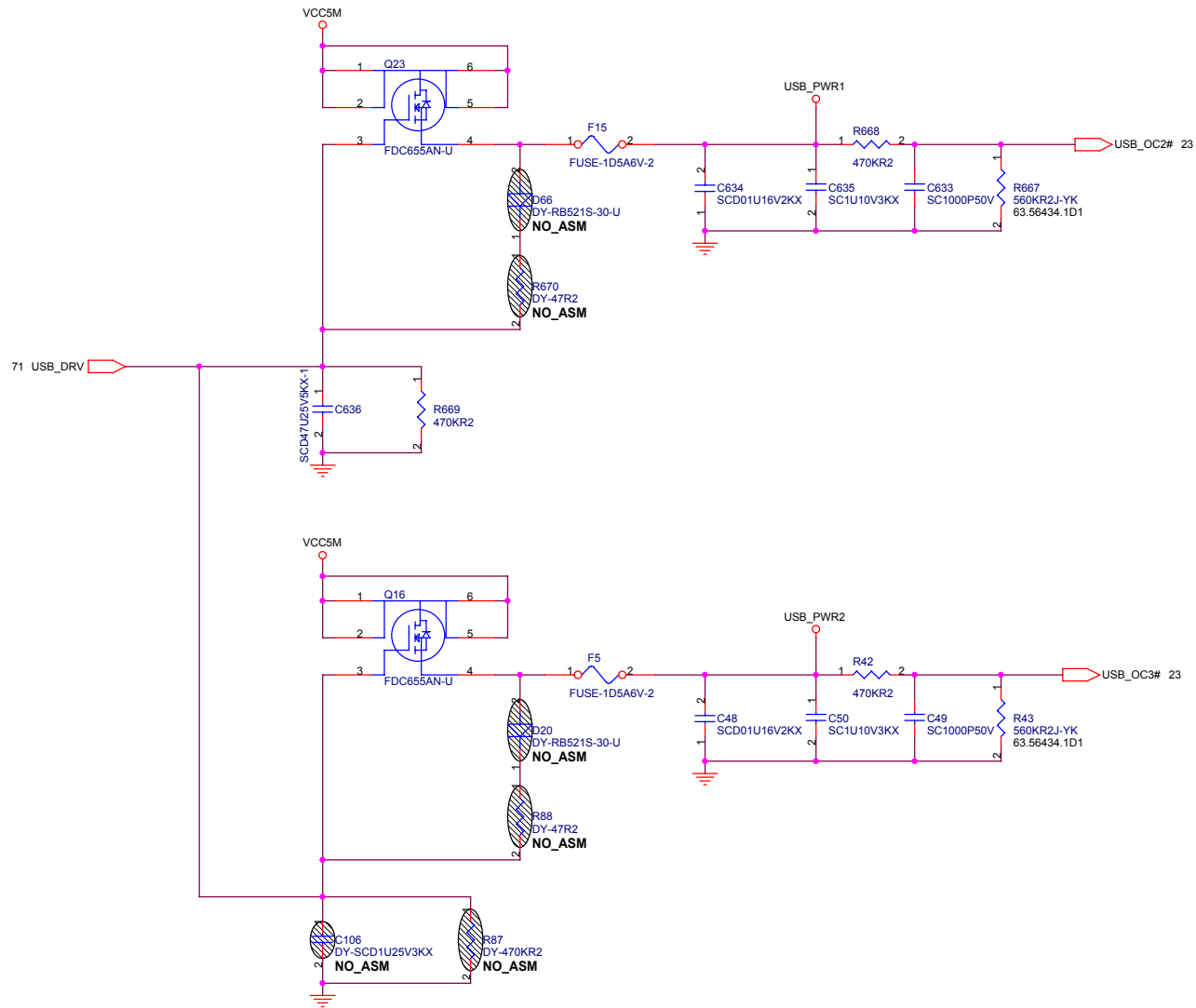


CRYPT\_DETECTION BIT  
None TCPA model should be assemble this pulldown resistor.



|                              |                 |  |     |
|------------------------------|-----------------|--|-----|
| <b>緯創資通</b>                  |                 | <b>Wistron Corporation</b>   |     |
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| Title                        |                 |  |     |
| <b>SLICE CONNECTOR</b>       |                 |  |     |
| Size                         | Document Number | Sheet  | Rev |
| A3                           |                 | 46   | -1  |
| <b>S Note-3</b>              |                 |  |     |
| Date: Tuesday, June 21, 2005 |                 | Sheet 46 of 75   |     |

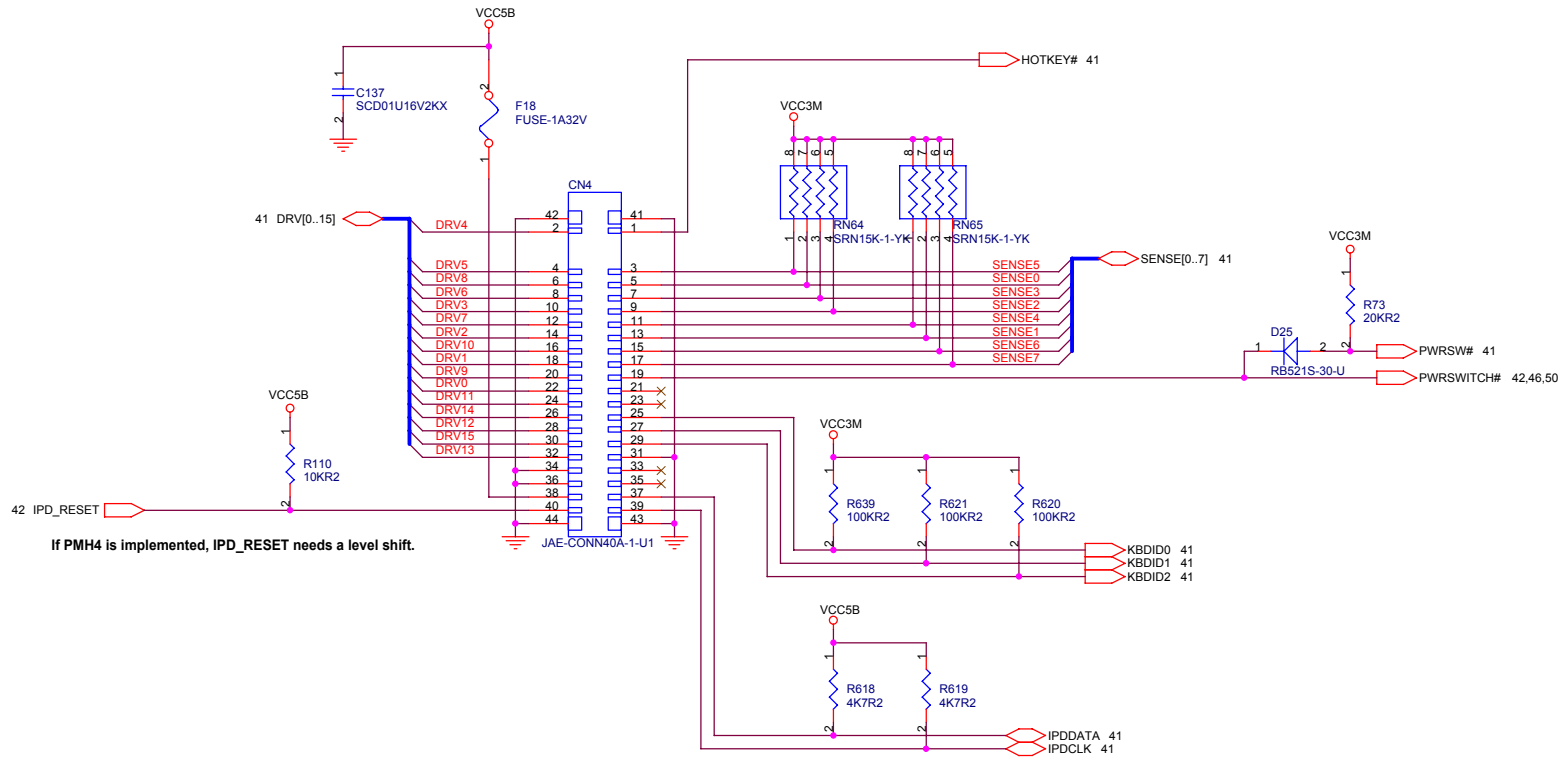




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|                              |                                    |                  |
|------------------------------|------------------------------------|------------------|
| Title                        |                                    |                  |
| <b>USB POWER</b>             |                                    |                  |
| Size<br>A3                   | Document Number<br><b>S Note-3</b> | Rev<br><b>-1</b> |
| Date: Tuesday, June 21, 2005 | Sheet 48 of                        | 75               |

# Keyboard Connector

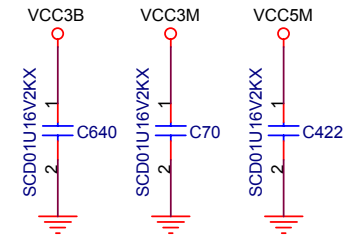
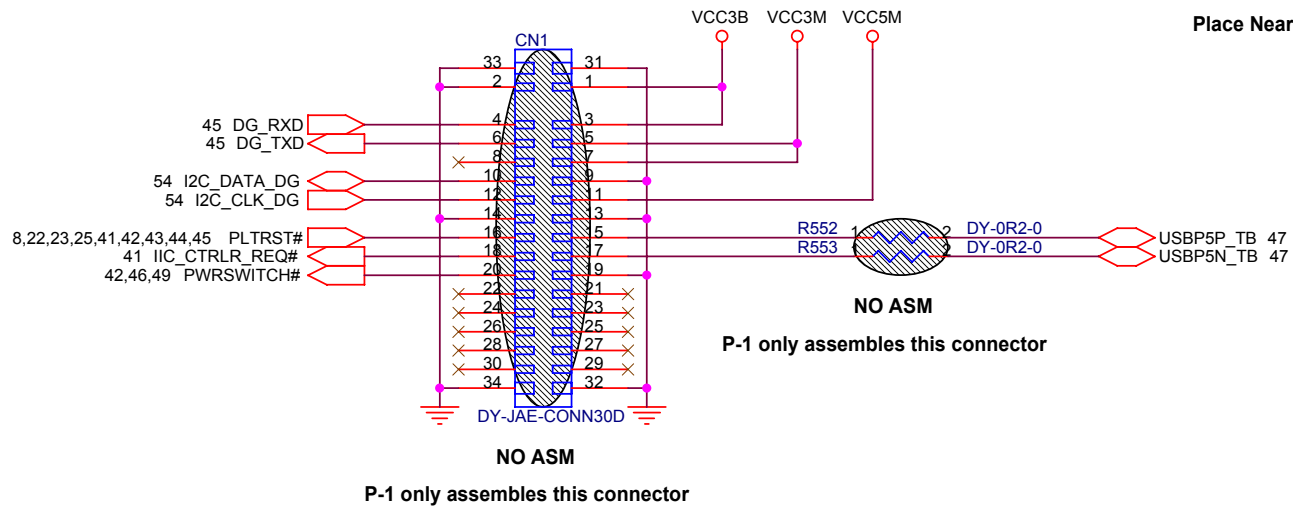


If PMH4 is implemented, IPD\_RESET needs a level shift.



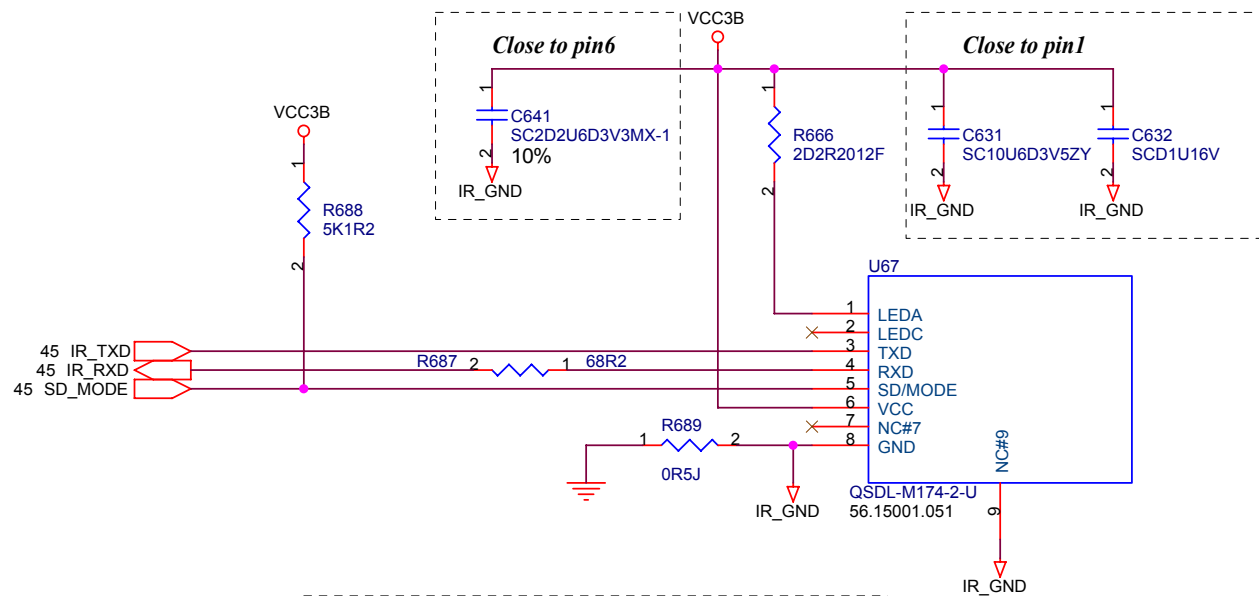
Keyboard Connector Top View

|  |                        |  |          |
|--|------------------------|--|----------|
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| Title  |                        |  |          |
| <b>KEYBOARD CONN</b>   |                        |  |          |
| Size   | Document Number        | S Note-3   | Rev      |
| A3   |                        |  | -1       |
| Date:  | Tuesday, June 21, 2005 | Sheet  | 49 of 75 |

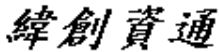


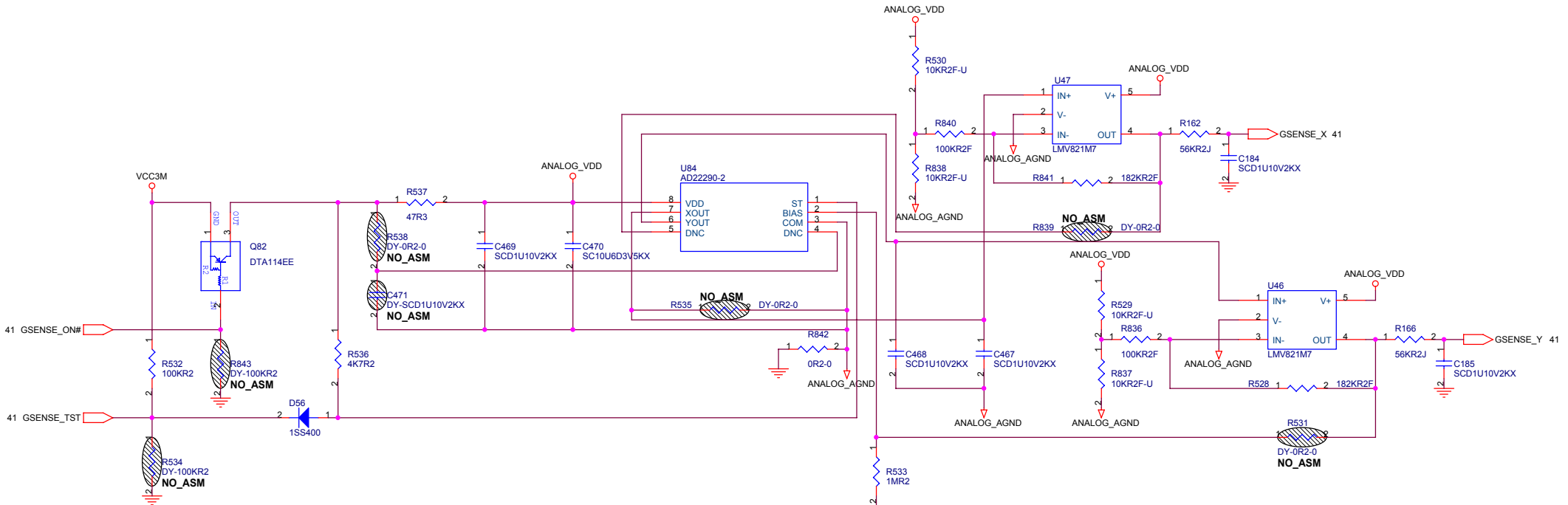
Place Near to CONN

|   |                 |   |    |
|---|-----------------|---|----|
|   |                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |    |
| Title<br><h2 style="margin: 0;">DG CONNECTOR</h2> |                 |   |    |
| Size<br>A4  | Document Number | <h3 style="margin: 0;">S Note-3</h3>  |    |
| Date: Tuesday, June 21, 2005                      | Sheet 50        | of  | 75 |
|   |                 | Rev   | -1 |



SHOULD QUALIFY BELOW PARTS  
 PRIMATY ALIGENT QSDL-M174-1 : 74.00174.001  
 SECOND VISHAY TFDU6102 : 56.15001.051

|   |                                    |                  |
|---|------------------------------------|------------------|
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| <b>IR MODULE</b>  |                                    |                  |
| Size<br>A4  | Document Number<br><b>S Note-3</b> | Rev<br><b>-1</b> |
| Date: Tuesday, June 21, 2005  |                                    | Sheet 51 of 75   |



**Accelerometer Parts List**

| Page | Usage Code           | AD22290 | MEMSIC    | NO ACC. |
|------|----------------------|---------|-----------|---------|
| 52   | R843 (100K 5%)       | NO_ASM  | NO_ASM    | ASM     |
| 52   | R534 (100K 5%)       | NO_ASM  | ASM       | ASM     |
| 52   | U47 (MAX4400AXK-T-1) | ASM     | NO_ASM    | NO_ASM  |
| 52   | U84 (AD22290-2)      | ASM     | MXA2500GL | NO_ASM  |
| 52   | U46 (MAX4400AXK-T-1) | ASM     | NO_ASM    | NO_ASM  |
| 52   | Q82 (DTA114EE)       | ASM     | ASM       | NO_ASM  |
| 52   | D56 (1SS400)         | ASM     | NO_ASM    | NO_ASM  |
| 52   | R537(47ohm 5%)       | 47 ohm  | 10 ohm    | NO_ASM  |
| 52   | R530(10K 1%)         | ASM     | NO_ASM    | NO_ASM  |
| 52   | R840(100K 1%)        | ASM     | NO_ASM    | NO_ASM  |
| 52   | R612(56K 5%)         | ASM     | 8.2K 5%   | NO_ASM  |
| 52   | R838(10K 1%)         | ASM     | NO_ASM    | NO_ASM  |
| 52   | R841(182K 1%)        | ASM     | NO_ASM    | NO_ASM  |
| 52   | R536(4.7K 5%)        | ASM     | NO_ASM    | NO_ASM  |
| 52   | R529(10K 1%)         | ASM     | NO_ASM    | NO_ASM  |
| 52   | R836(100K 1%)        | ASM     | NO_ASM    | NO_ASM  |
| 52   | R116(56K 5%)         | ASM     | 8.2K 5%   | NO_ASM  |
| 52   | R842(0ohm 5%)        | ASM     | ASM       | NO_ASM  |

| Page | Usage Code          | AD22290 | MEMSIC | NO ACC. |
|------|---------------------|---------|--------|---------|
| 52   | R532(100K 5%)       | ASM     | NO_ASM | NO_ASM  |
| 52   | R837(10K 1%)        | ASM     | NO_ASM | NO_ASM  |
| 52   | R528(182K 1%)       | ASM     | NO_ASM | NO_ASM  |
| 52   | R533(1M 5%)         | ASM     | NO_ASM | NO_ASM  |
| 52   | C184 (0.1u 10%10V)  | ASM     | ASM    | NO_ASM  |
| 52   | C469 (0.1u 10%10V)  | ASM     | ASM    | NO_ASM  |
| 52   | C468 (0.1u 10%10V)  | ASM     | NO_ASM | NO_ASM  |
| 52   | C467 (0.1u 10%10V)  | ASM     | NO_ASM | NO_ASM  |
| 52   | C185 (0.1u 10%10V)  | ASM     | ASM    | NO_ASM  |
| 52   | R538(0ohm 5%)       | NO_ASM  | ASM    | NO_ASM  |
| 52   | R839(0ohm 5%)       | NO_ASM  | ASM    | NO_ASM  |
| 52   | R535(0ohm 5%)       | NO_ASM  | ASM    | NO_ASM  |
| 52   | R531(0ohm 5%)       | NO_ASM  | ASM    | NO_ASM  |
| 52   | C741 (0.1u 10%10V)  | NO_ASM  | ASM    | NO_ASM  |
| 52   | C470 (10u 10% 6.3V) | ASM     | NO_ASM | NO_ASM  |

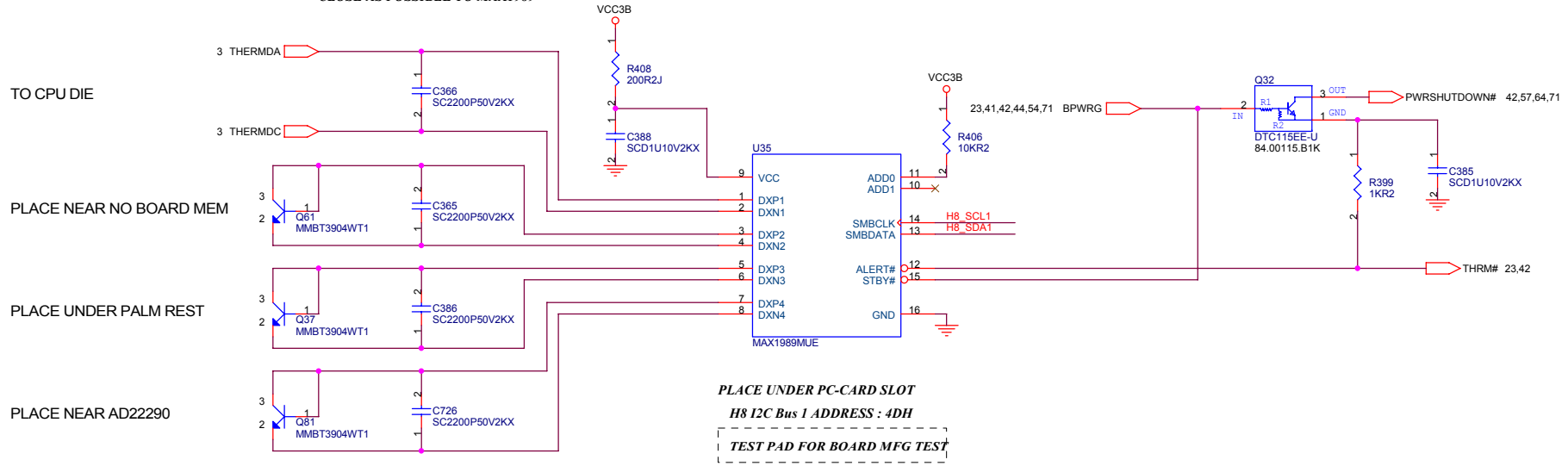
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**G-SENSOR**  
**S Note-3**

Title: \_\_\_\_\_  
 Size: A3 Document Number: \_\_\_\_\_ Rev: -1  
 Date: Tuesday, June 21, 2005 Sheet: 52 of 75



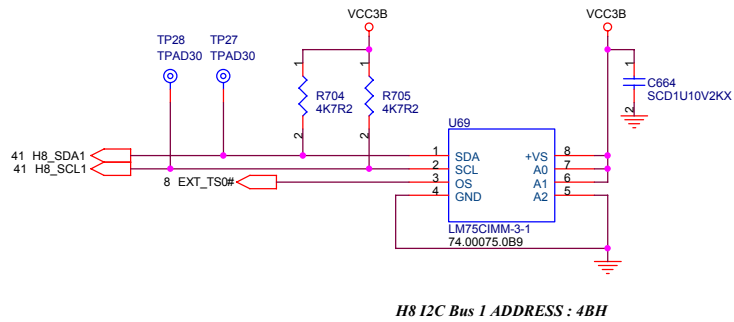
THESE CAPS MUST BE PLACED AS  
CLOSE AS POSSIBLE TO MAX1989



## Thermal Sensor LM75 for DDR module

(For DDR throttling implementation)

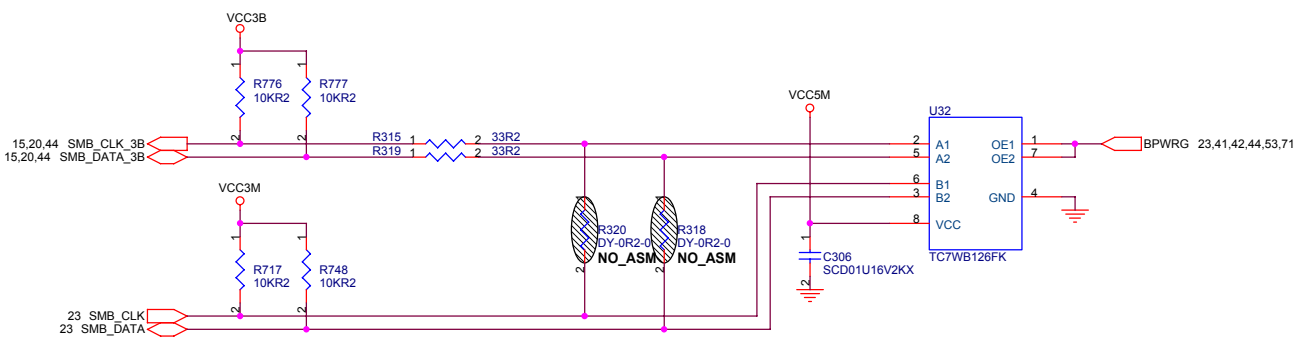
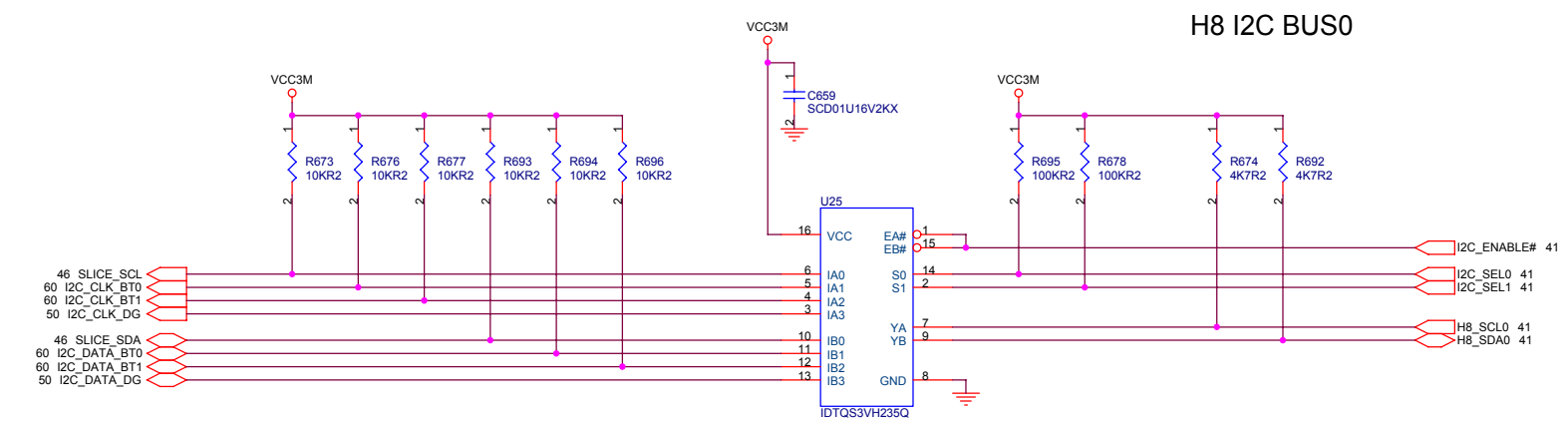
PLACE UNDER DIMM



Main Source : 74.00075.0B9 (NS)  
2nd Source : 74.00075.AB9 (MAXIM)  
74.07416.0B9 (ADI)

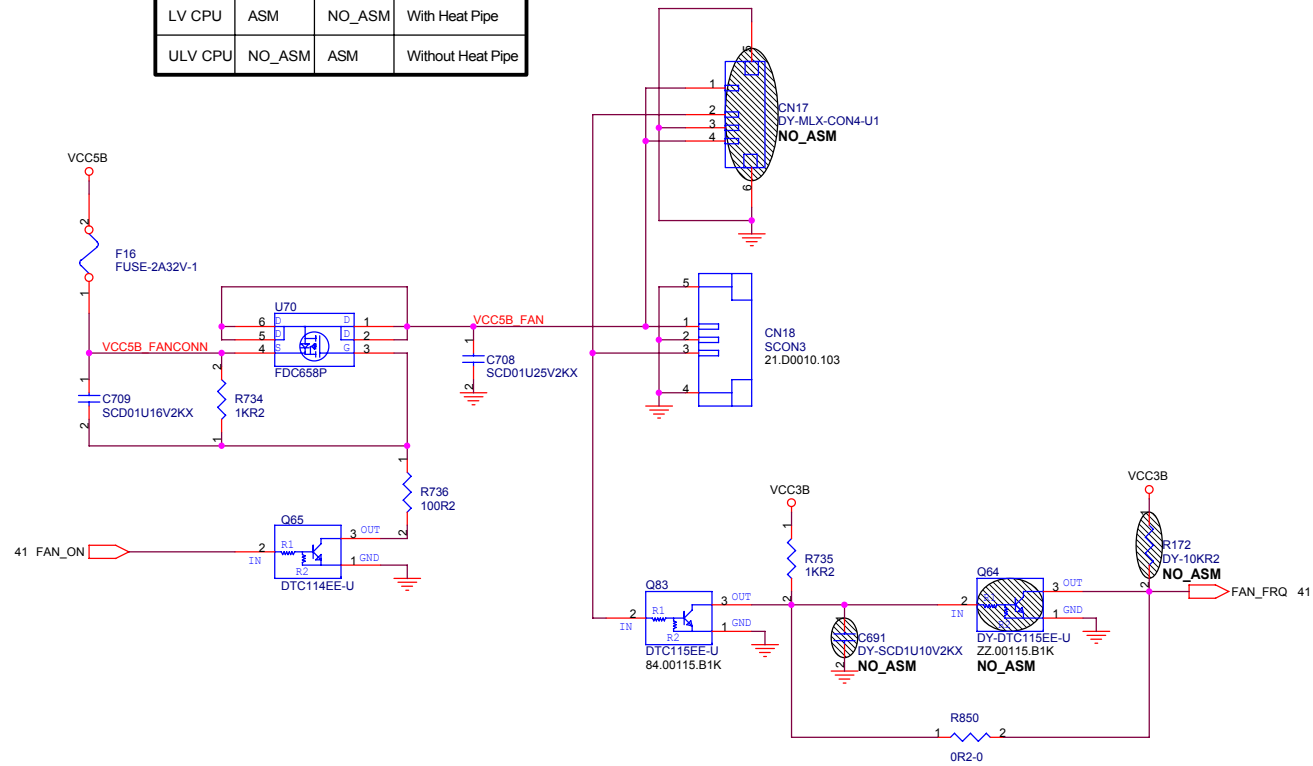
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|                       |                        |                |
|-----------------------|------------------------|----------------|
| Title                 |                        |                |
| <b>THERMAL SENSOR</b> |                        |                |
| Size                  | Document Number        | Rev            |
| A3                    | <b>S Note-3</b>        | -1             |
| Date:                 | Tuesday, June 21, 2005 | Sheet 53 of 75 |



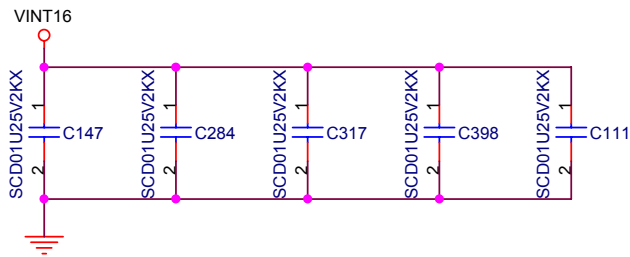
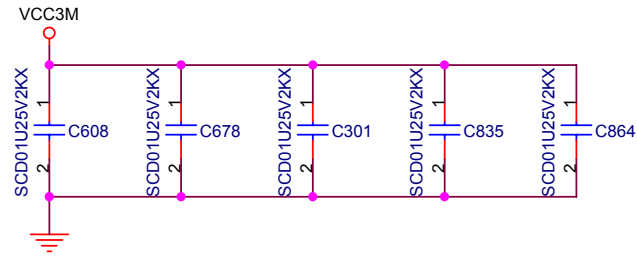
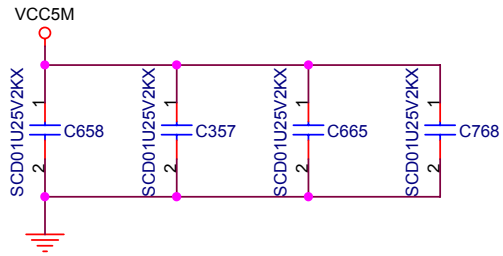
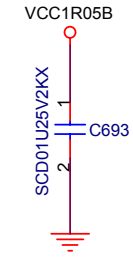
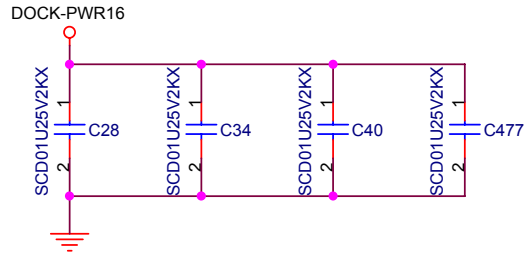
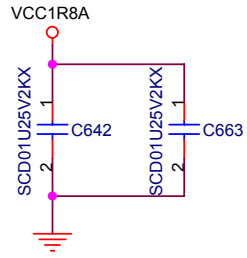
## Fan Power Control

|         | CN18   | CN17   | FAN Module        |
|---------|--------|--------|-------------------|
| LV CPU  | ASM    | NO_ASM | With Heat Pipe    |
| ULV CPU | NO_ASM | ASM    | Without Heat Pipe |



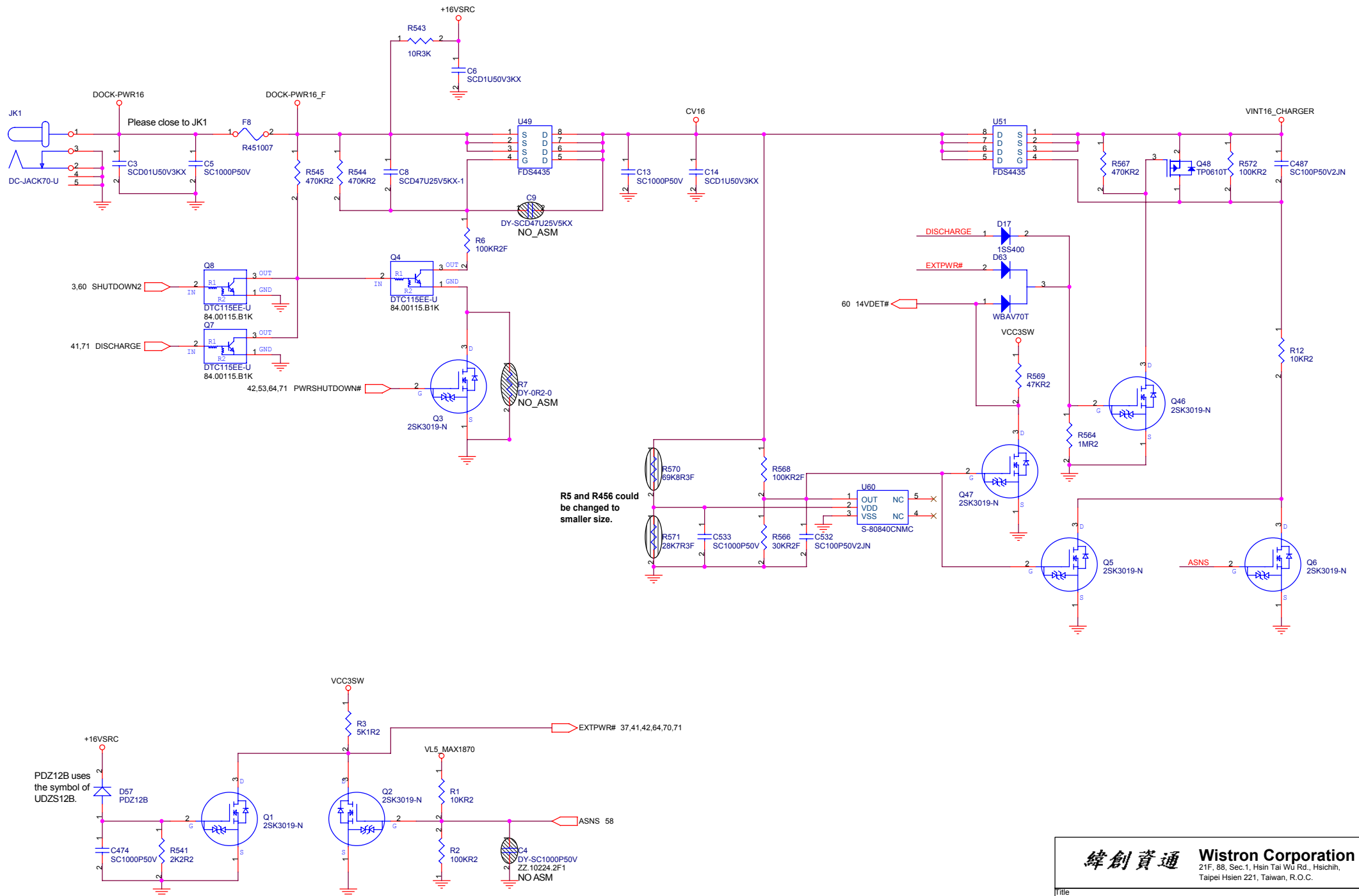
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|                              |                 |                |
|------------------------------|-----------------|----------------|
| Title                        |                 |                |
| <b>FAN CONTROL</b>           |                 |                |
| Size<br>A3                   | Document Number | Rev<br>-1      |
| <b>S Note-3</b>              |                 |                |
| Date: Tuesday, June 21, 2005 |                 | Sheet 55 of 75 |

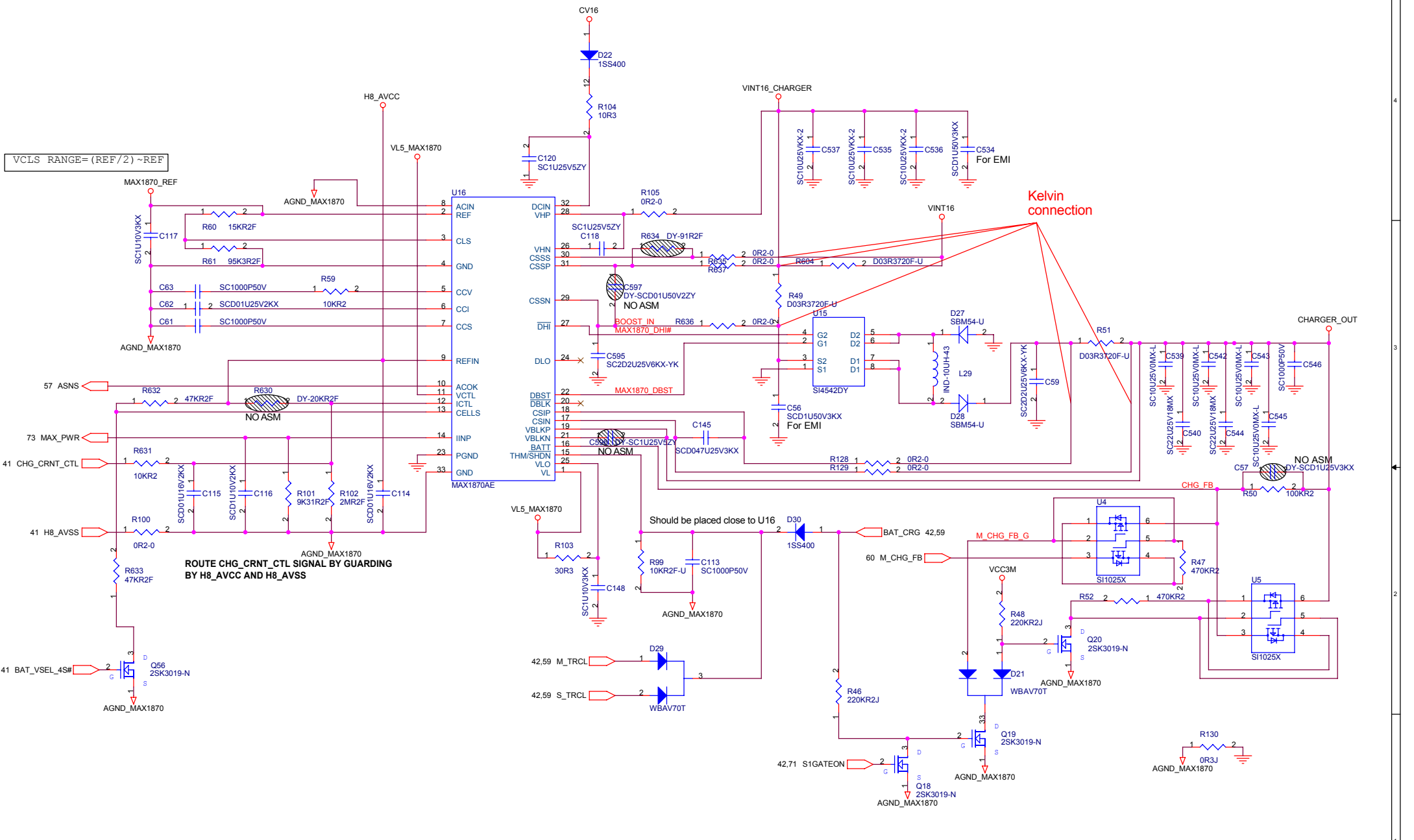


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|                              |                                    |                  |
|------------------------------|------------------------------------|------------------|
| Title                        |                                    |                  |
| <b>EMC DECOUPLING</b>        |                                    |                  |
| Size<br>A4                   | Document Number<br><b>S Note-3</b> | Rev<br><b>-1</b> |
| Date: Tuesday, June 21, 2005 | Sheet 56 of 75                     |                  |

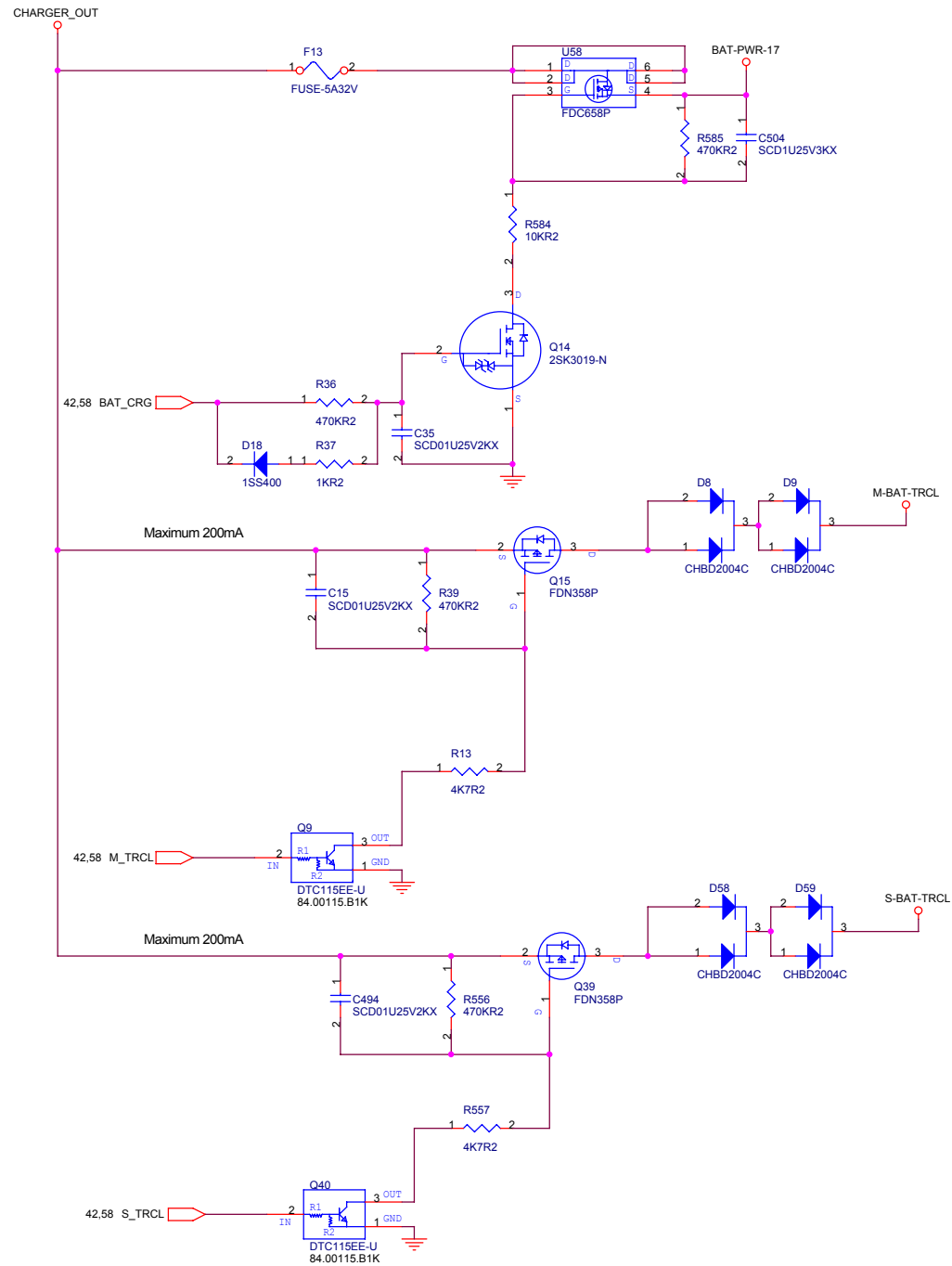


$$VCLS\_RANGE = (REF/2) \sim REF$$



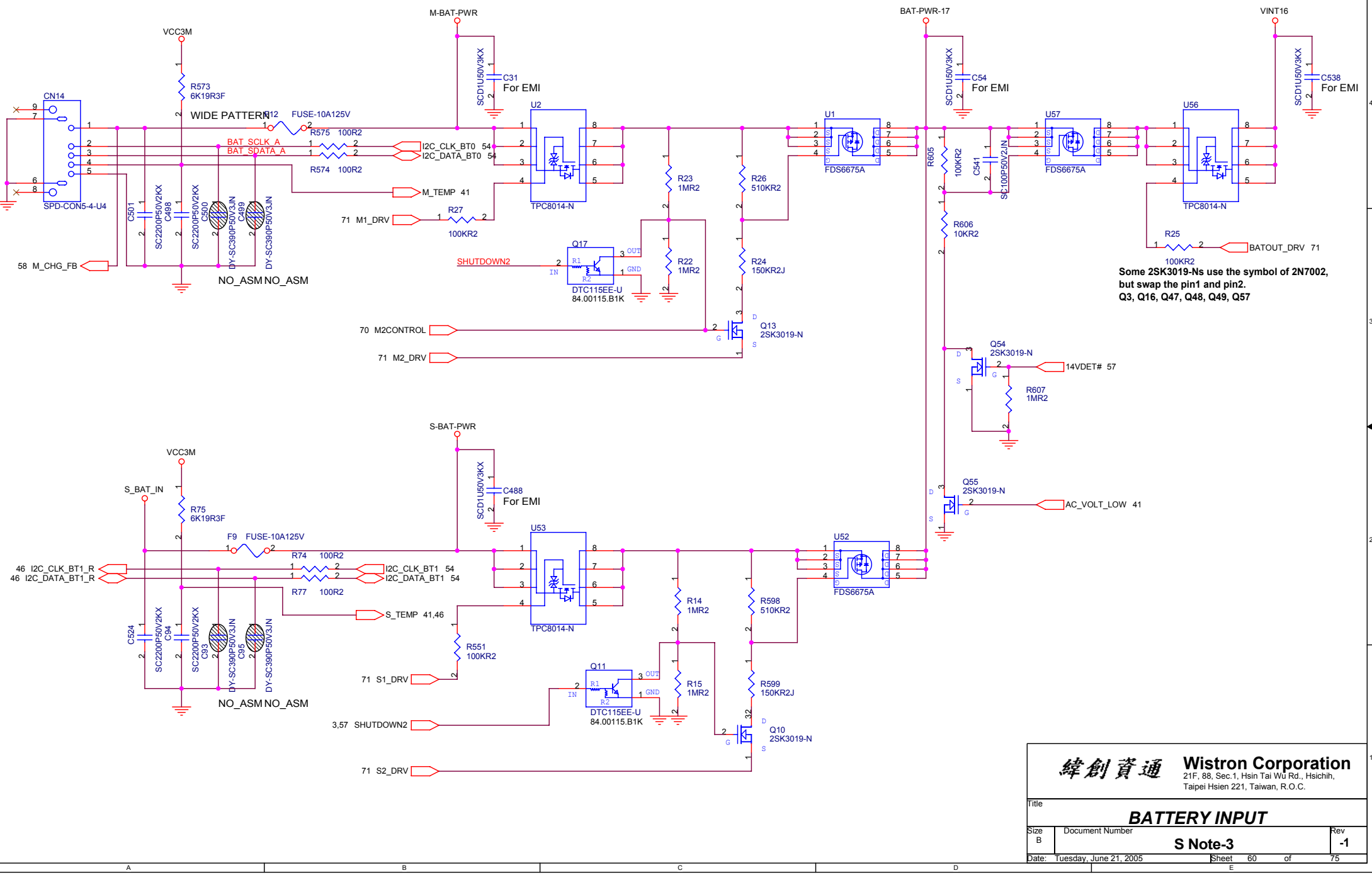
Some 2SK3019-Ns use the symbol of 2N7002, but swap the pin1 and pin2. Q55, Q56, Q83, Q84

|  |                 |
|--|-----------------|
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| <b>CHARGER MAX1870</b>   |                 |
| Title  |                 |
| Size A3  | Document Number |
| <b>S Note-3</b>  |                 |
| Date: Tuesday, June 21, 2005   | Sheet 58 of 75  |
|  | Rev -1          |



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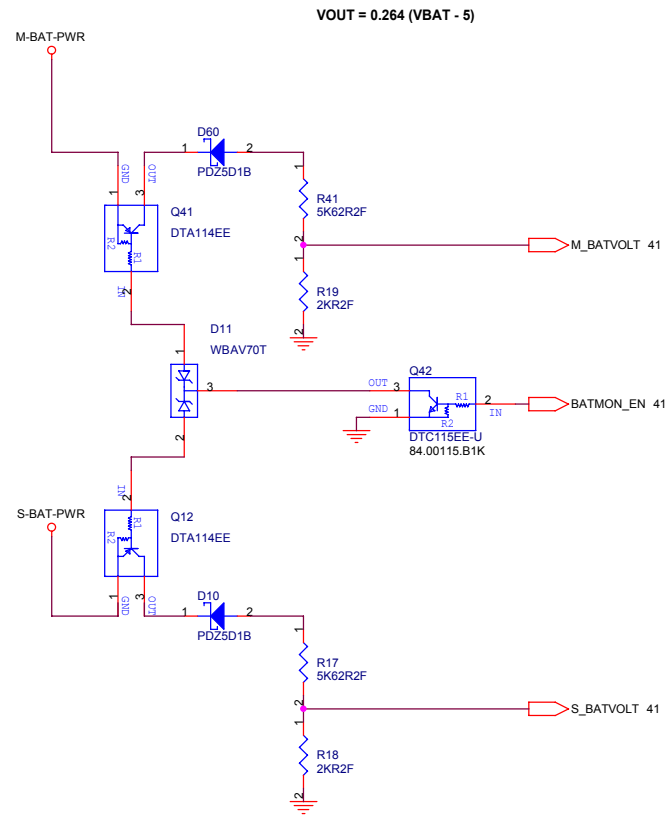
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|------------------------------|-----------------|--|-----------------------|--|----|
| Title                        |                 |  | <b>CHARGER SELECT</b> |  |    |
| Size                         | Document Number |  | Rev                   |  |    |
| A3                           |                 |  | <b>S Note-3</b>       |  | -1 |
| Date: Tuesday, June 21, 2005 |                 |  | Sheet 59 of 75        |  |    |



Some 2SK3019-Ns use the symbol of 2N7002, but swap the pin1 and pin2. Q3, Q16, Q47, Q48, Q49, Q57

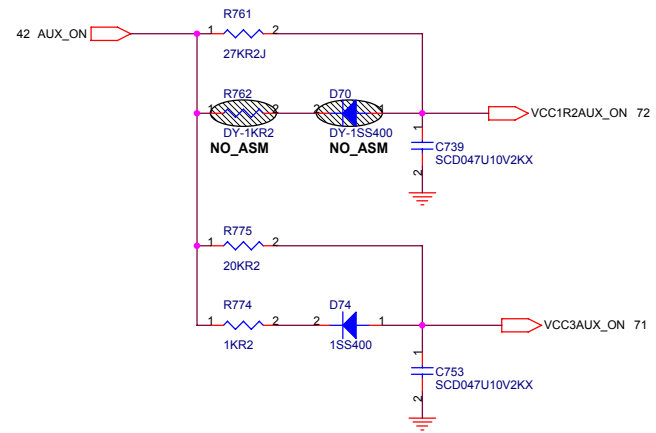
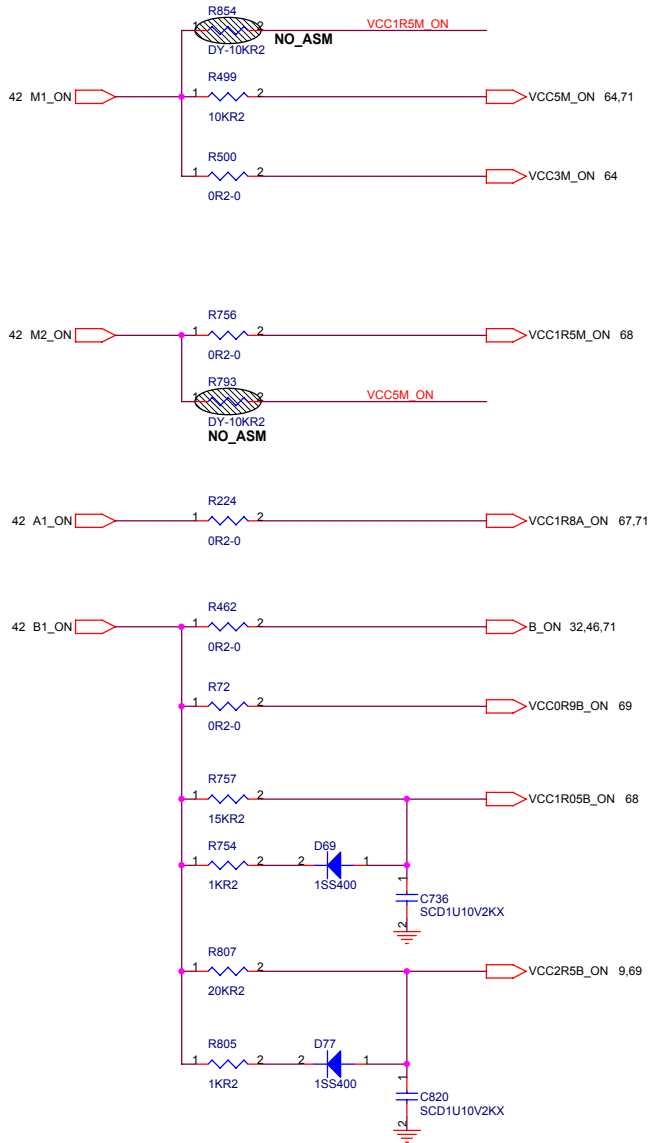
|   |  |
|---|--|
|   |  |
| <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |  |
| <b>BATTERY INPUT</b>  |  |
| Title<br>Size B<br>Date: Tuesday, June 21, 2005   | Document Number<br><b>S Note-3</b><br>Sheet 60 of 75 |
| Rev<br><b>-1</b>  |  |





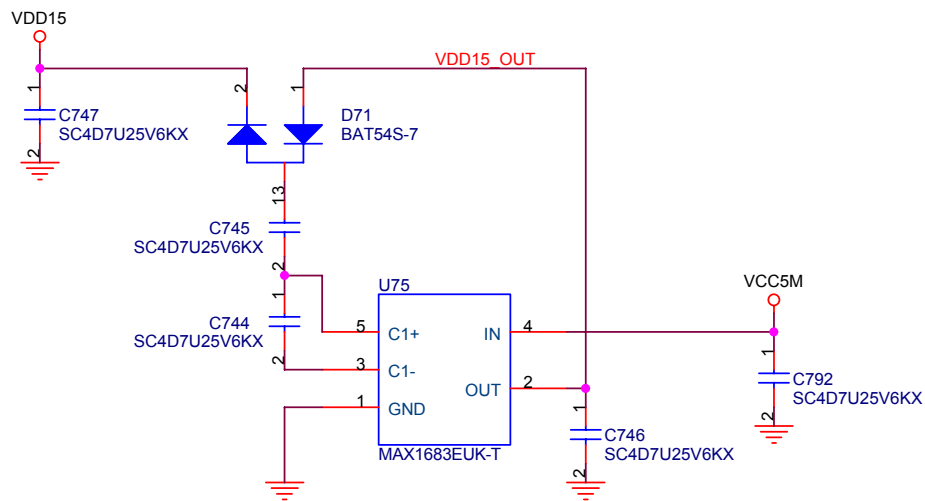
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|                              |                 |  |                        |  |    |
|------------------------------|-----------------|--|------------------------|--|----|
| Title                        |                 |  | <b>BATTERY MONITOR</b> |  |    |
| Size                         | Document Number |  | Rev                    |  |    |
| A3                           |                 |  | S Note-3               |  | -1 |
| Date: Tuesday, June 21, 2005 |                 |  | Sheet 61 of 75         |  |    |



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|                              |                 |       |                       |    |    |
|------------------------------|-----------------|-------|-----------------------|----|----|
| Title                        |                 |       | <b>POWER SEQUENCE</b> |    |    |
| Size                         | Document Number | Rev   |                       |    |    |
| A3                           |                 | -1    | <b>S Note-3</b>       |    |    |
| Date: Tuesday, June 21, 2005 |                 | Sheet | 62                    | of | 75 |




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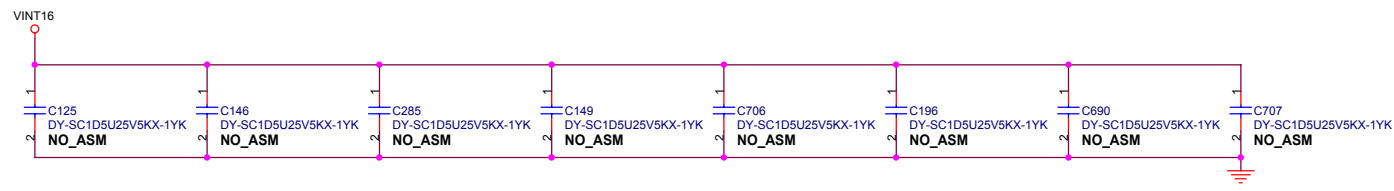
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|--------------------|------------------------|----------------|
| Title              |                        |                |
| <b>DC-DC VDD15</b> |                        |                |
| Size               | Document Number        | Rev            |
| A4                 | <b>S Note-3</b>        | <b>-1</b>      |
| Date:              | Tuesday, June 21, 2005 | Sheet 63 of 75 |





**ALL CAPS ON THIS PAGE ARE NO-ASM FOR VCCCPUCORE.**

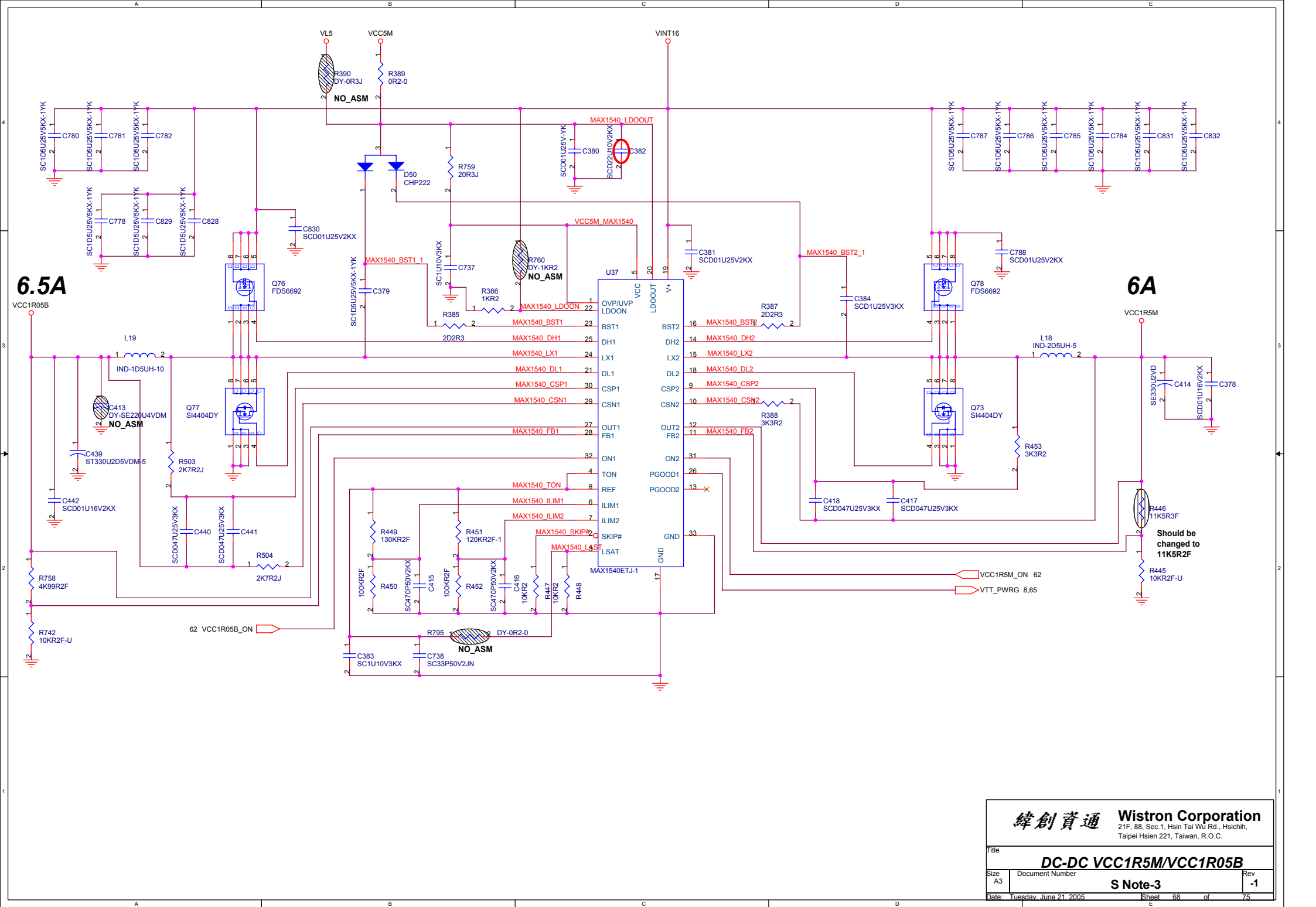
**X8 PCS**



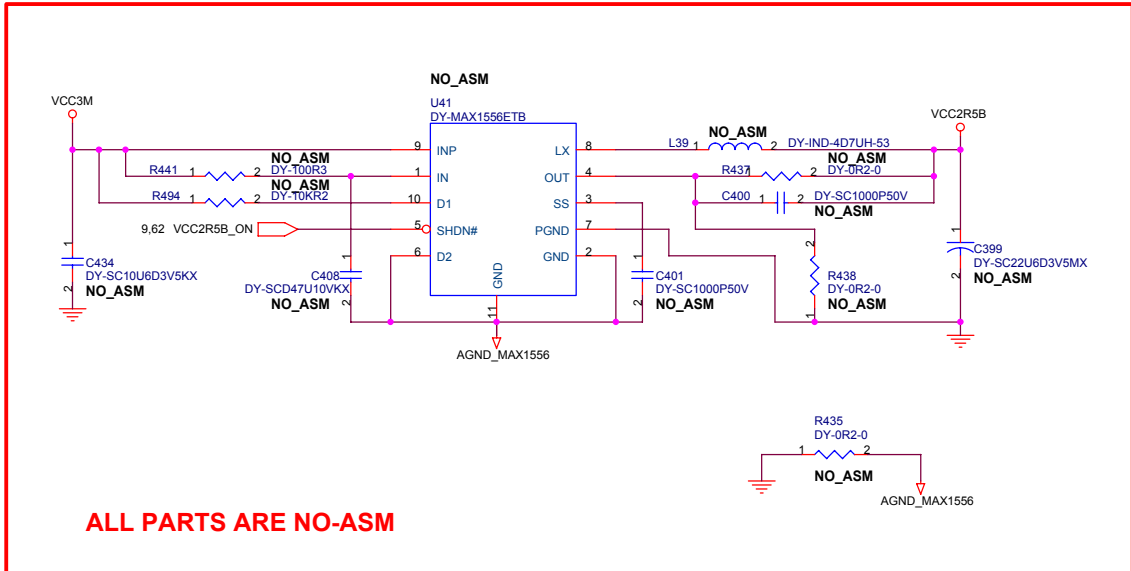
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|                              |                 |     |
|------------------------------|-----------------|-----|
| Title                        |                 |     |
| <b>DC-DC VCORE INPUT CAP</b> |                 |     |
| Size                         | Document Number | Rev |
| A3                           | <b>S Note-3</b> | -1  |
| Date: Tuesday, June 21, 2005 |                 |     |
| Sheet 66 of 75               |                 |     |

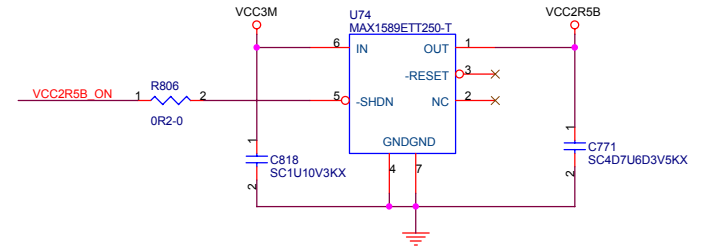




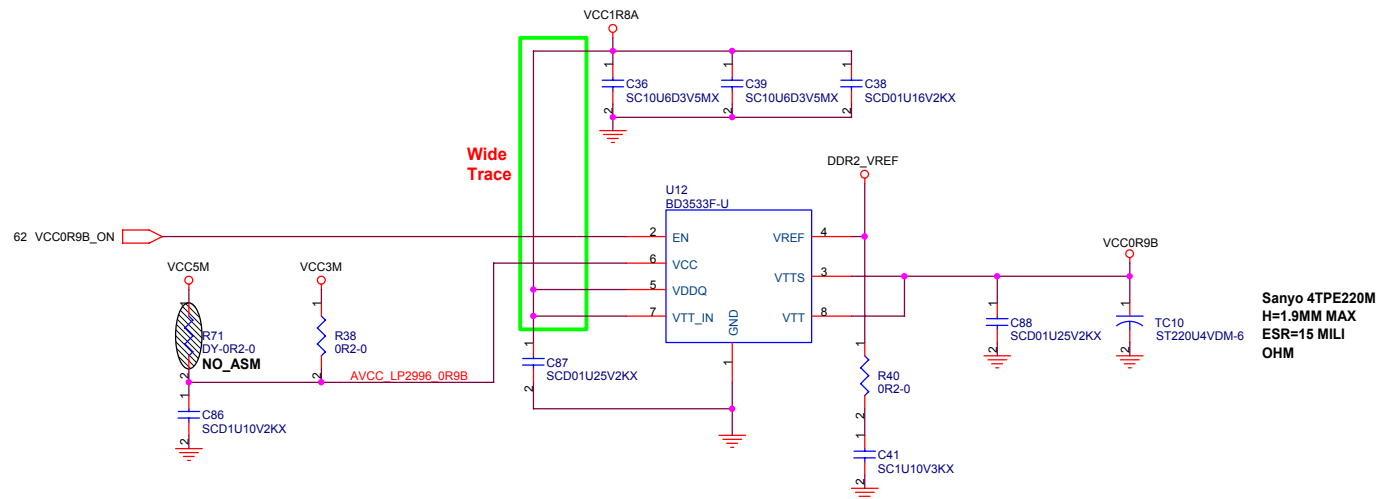




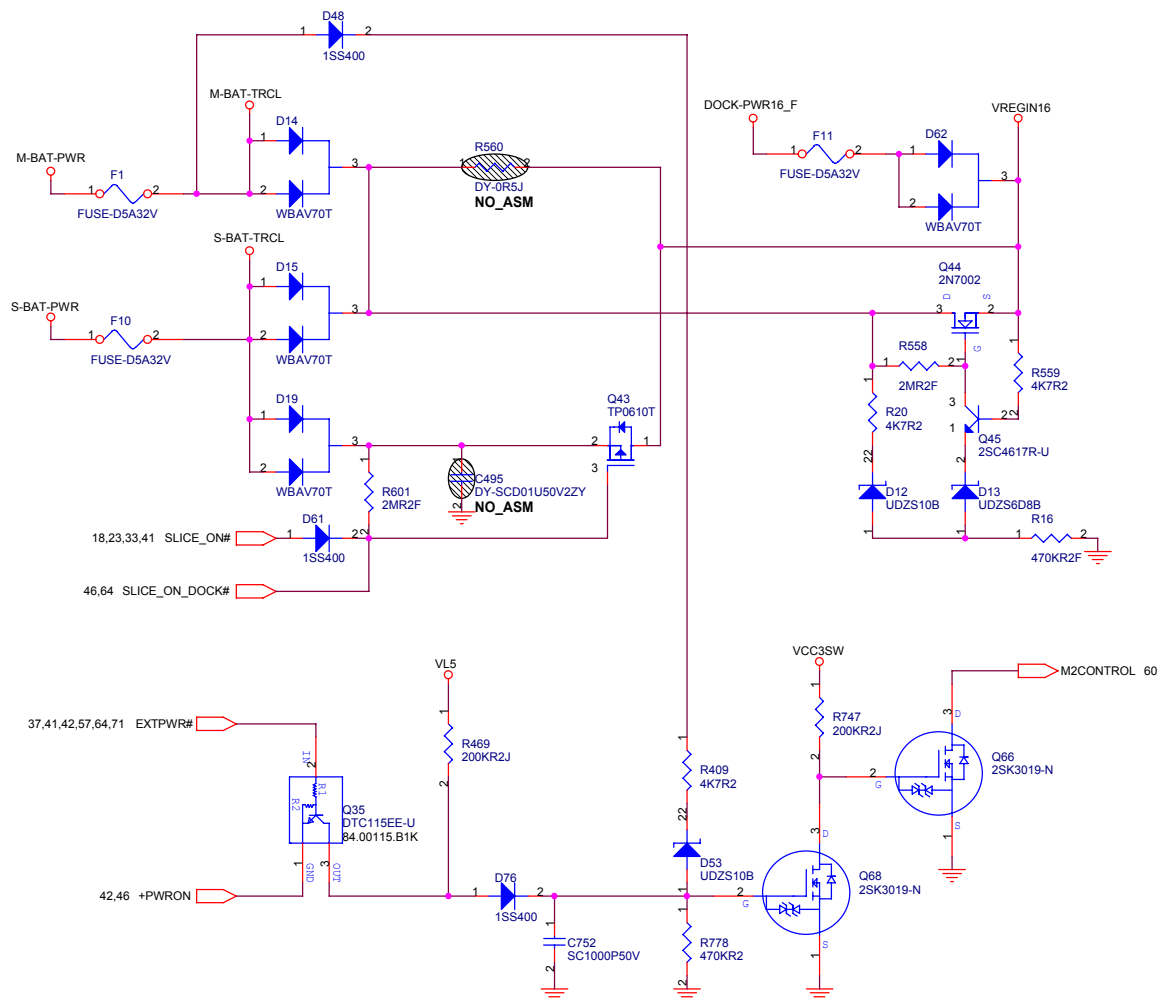
### VCC2R5B



### VCC0R9B & DDR2\_VREF



|   |                 |                            |       |
|---|-----------------|----------------------------|-------|
| <b>緯創資通</b>   |                 | <b>Wistron Corporation</b> |       |
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| <b>DC-DC VCC2R5B/VCC0R9B</b>  |                 |                            |       |
| Title   | Document Number |                            | Rev   |
| Size<br>A3  | <b>S Note-3</b> |                            | -1    |
| Date: Tuesday, June 21, 2005  | Sheet           | 69                         | of 75 |

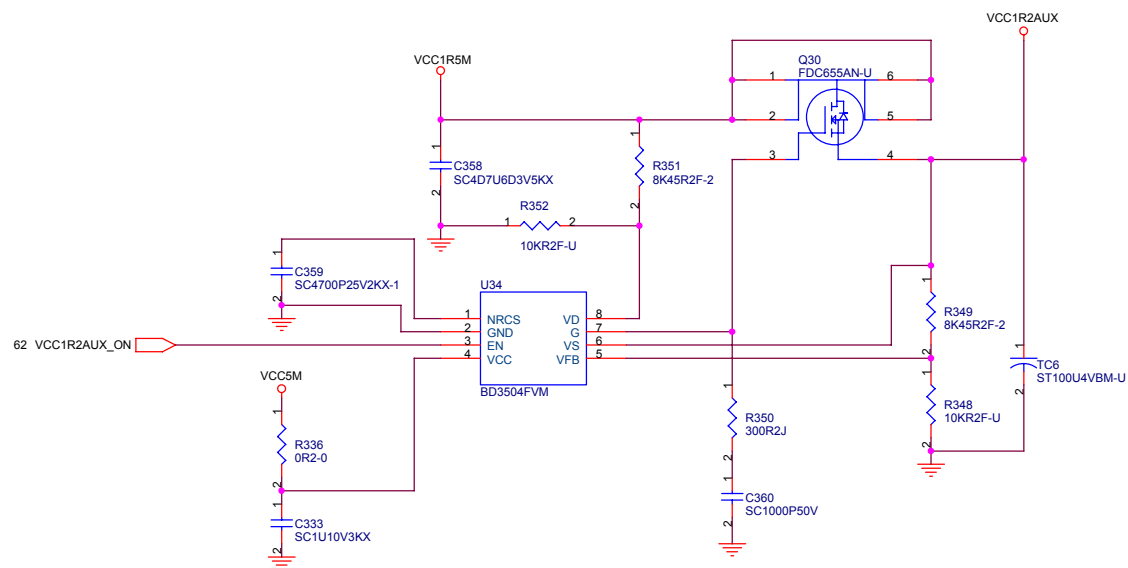


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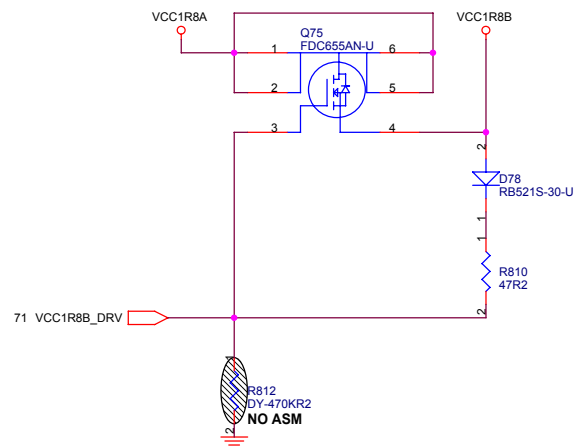
|                              |                 |  |                |    |  |
|------------------------------|-----------------|--|----------------|----|--|
| Title                        |                 |  | DC-DC VREGIN16 |    |  |
| Size                         | Document Number |  | Rev            |    |  |
| A3                           |                 |  | S Note-3       | -1 |  |
| Date: Tuesday, June 21, 2005 |                 |  | Sheet 70 of 75 |    |  |



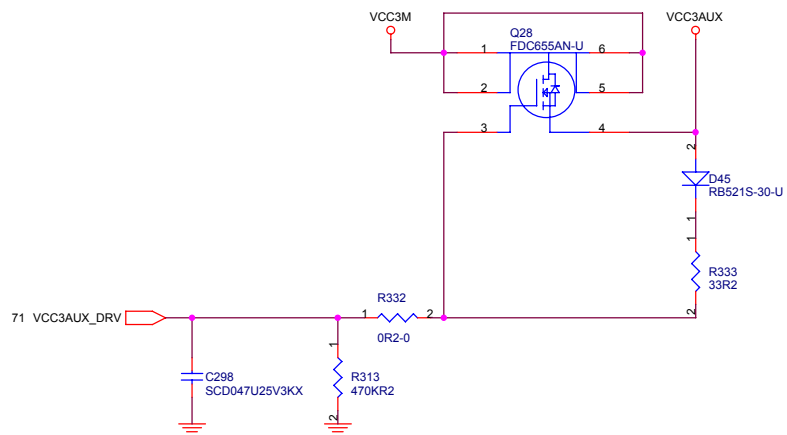
# VCC1R2AUX



# VCC1R8B

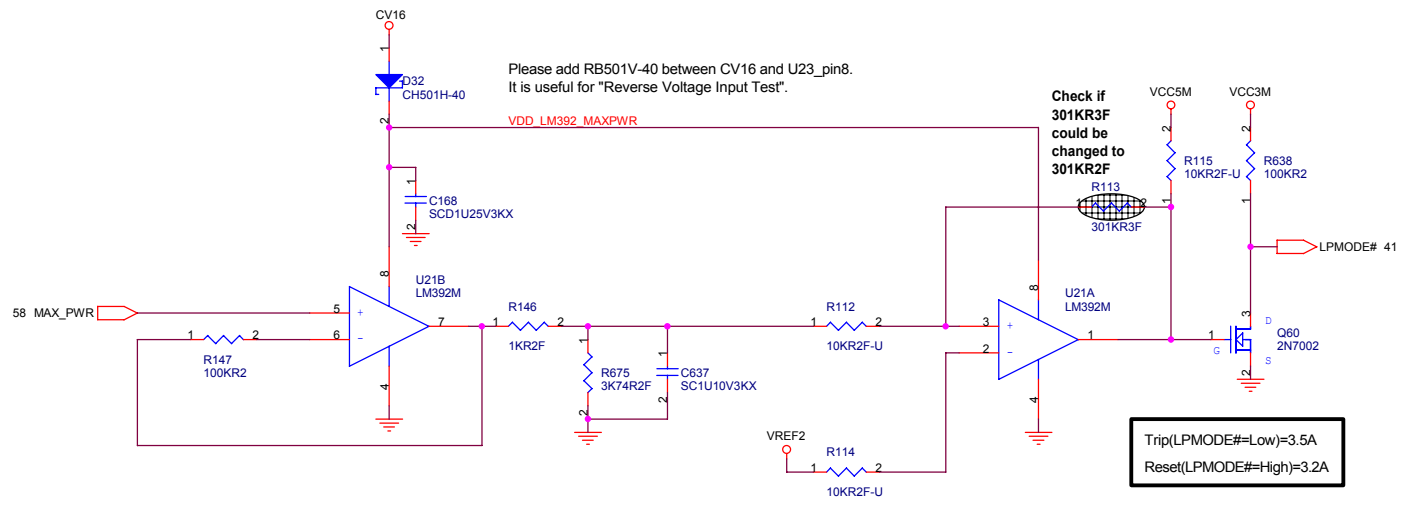


# VCC3AUX



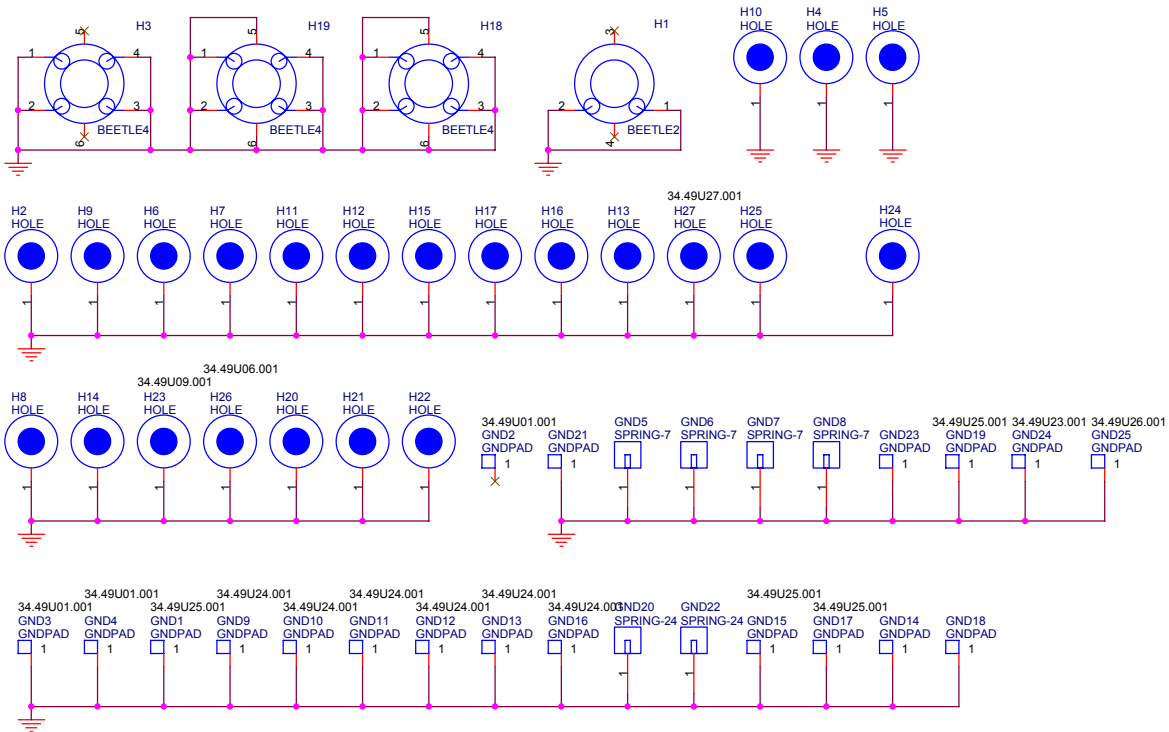
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|                              |                                    |                  |
|------------------------------|------------------------------------|------------------|
| Title                        |                                    |                  |
| <b>LOAD SW</b>               |                                    |                  |
| Size<br>A3                   | Document Number<br><b>S Note-3</b> | Rev<br><b>-1</b> |
| Date: Tuesday, June 21, 2005 | Sheet                              | 72 of 75         |

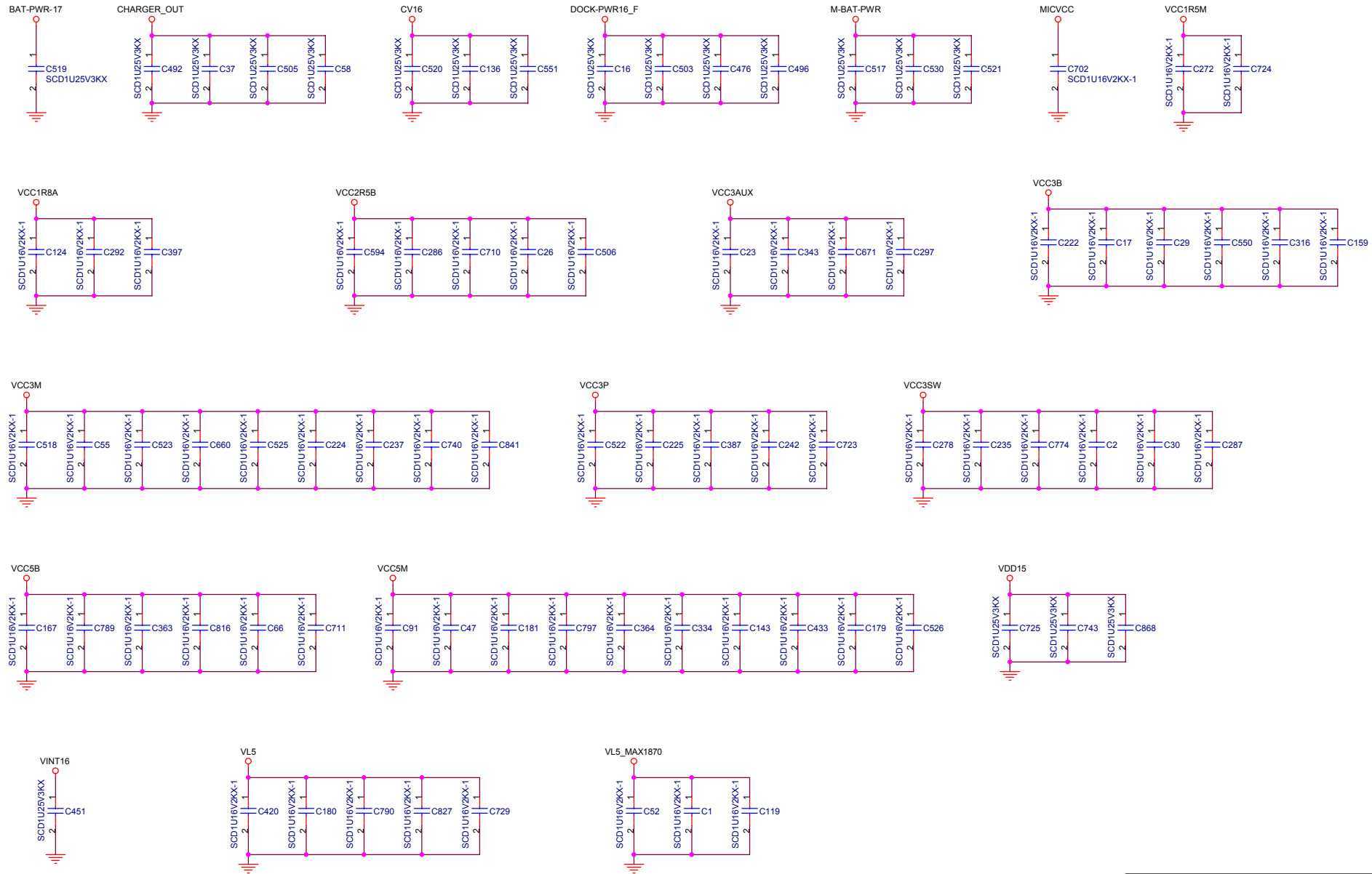


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|                              |                 |  |                   |    |  |
|------------------------------|-----------------|--|-------------------|----|--|
| Title                        |                 |  | MAX POWER CONTROL |    |  |
| Size                         | Document Number |  | Rev               |    |  |
| A3                           |                 |  | S Note-3          | -1 |  |
| Date: Tuesday, June 21, 2005 |                 |  | Sheet 73 of 75    |    |  |



|  |                                    |
|--|------------------------------------|
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| <b>HOLES/GND PADS</b>  |                                    |
| Title<br>Size<br>A3  | Document Number<br><b>S Note-3</b> |
| Date: Tuesday, June 21, 2005   | Rev<br><b>-1</b>                   |
| Sheet 74 of 75   |                                    |



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|                    |                        |                |
|--------------------|------------------------|----------------|
| Title              |                        |                |
| <b>WISTRON EMI</b> |                        |                |
| Size               | Document Number        | Rev            |
| A3                 |                        | -1             |
| <b>S Note-3</b>    |                        |                |
| Date:              | Tuesday, June 21, 2005 | Sheet 75 of 75 |