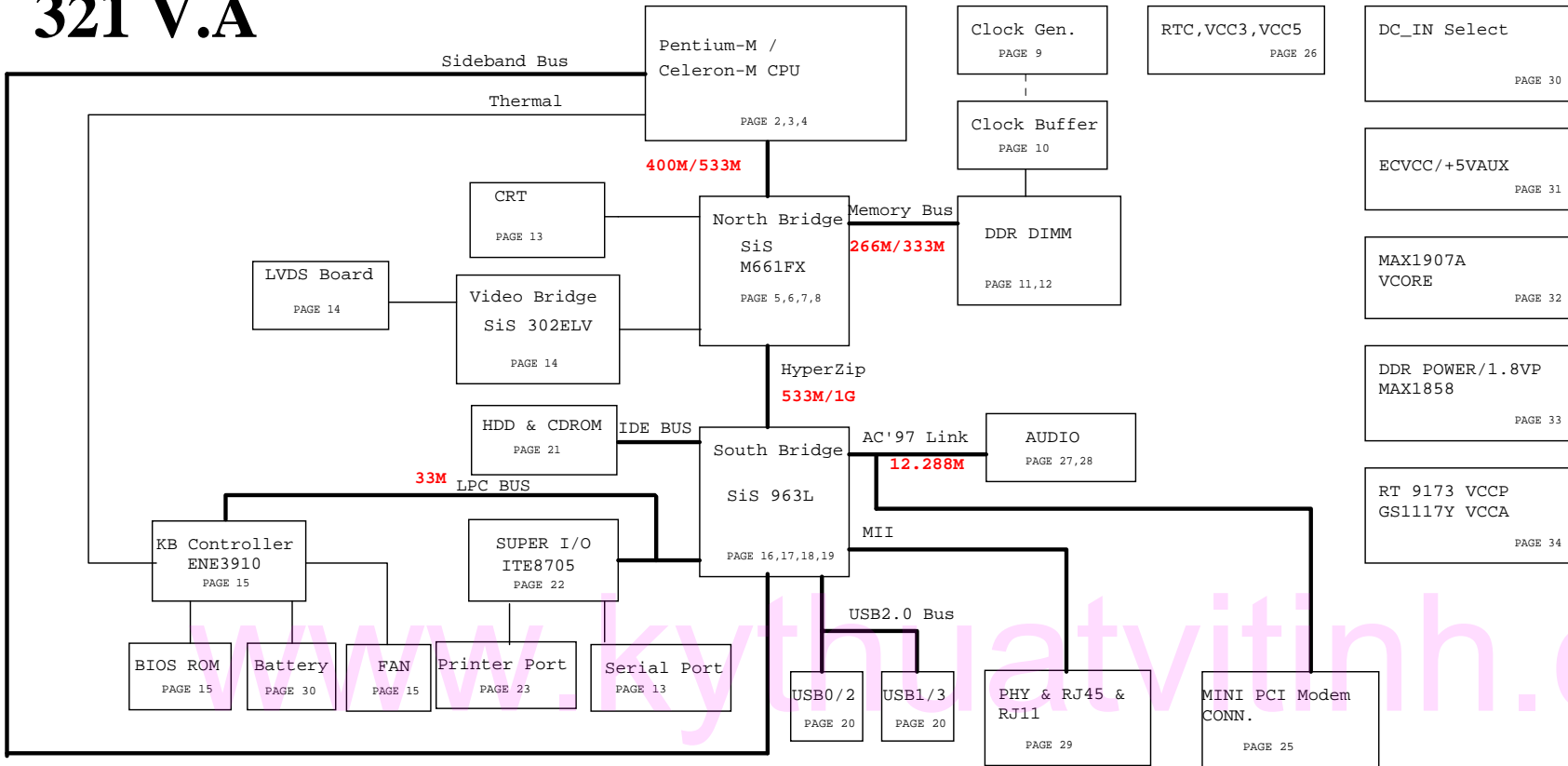


321 V.A

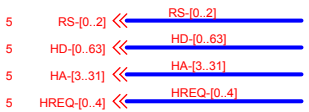
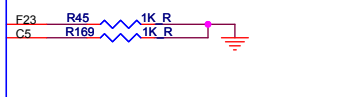
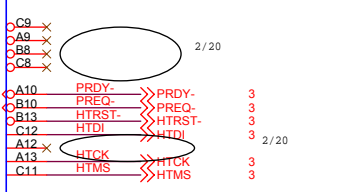
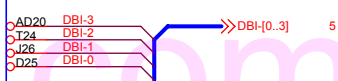
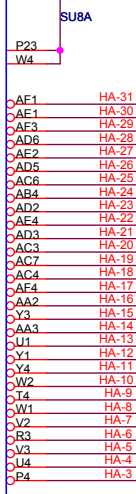


P/N :15-F61-010010
GERBER :

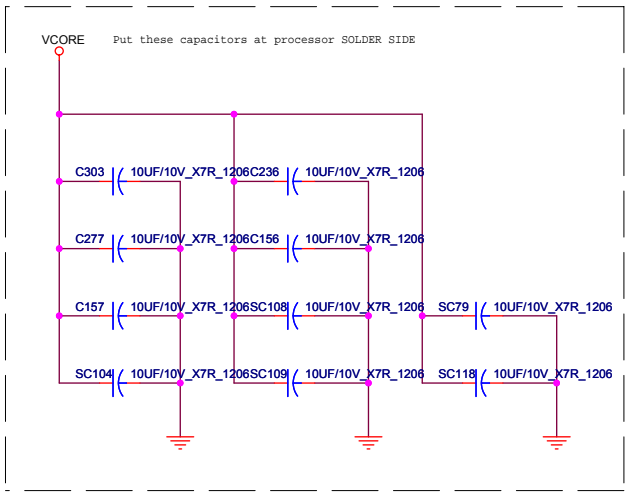
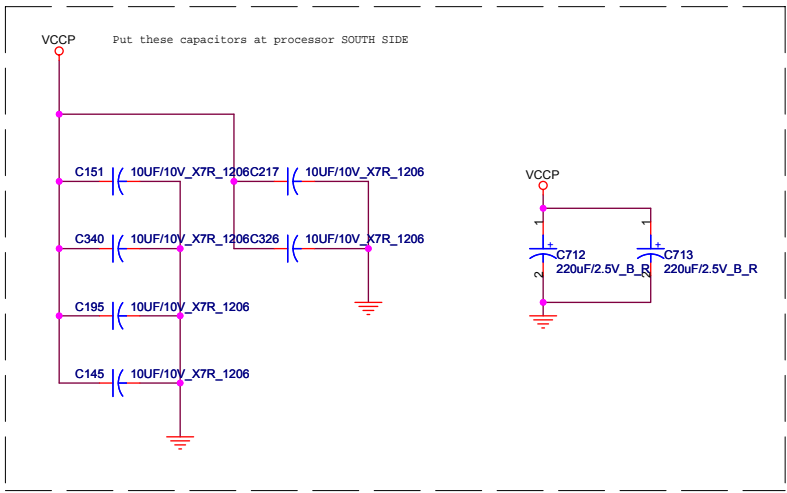
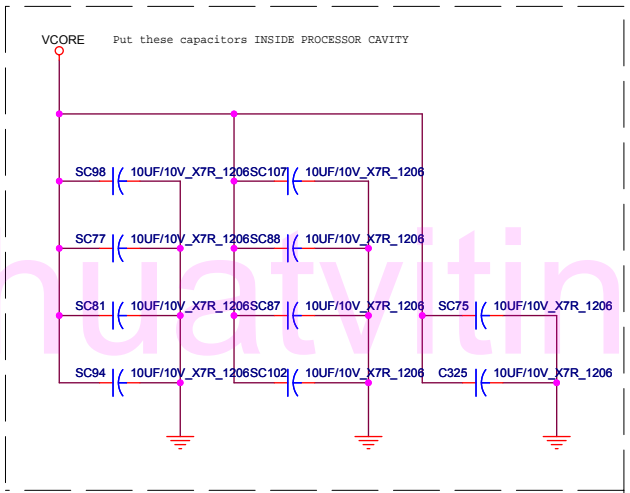
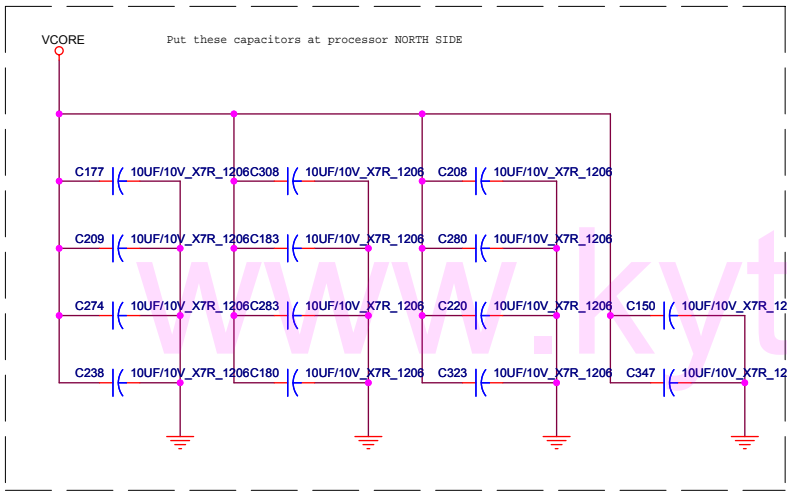
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REV	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0
DATE	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25

PAGE	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0
DATE	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25	2005/01/25

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Size B	Document Number 321-1-4-01	Rev A.0
Date:	Wednesday, February 02, 2005	Sheet 1 of 35



<i>Bus Signal</i>	<i>Data Bus Signals</i>	<i>Associated Strobe</i>
DINV[0]#	D[0..15]#	DSTBN[0]# DSTBP[0]#
DINV[1]#	D[16..31]#	DSTBN[1]# DSTBP[1]#
DINV[2]#	D[32..47]#	DSTBN[2]# DSTBP[2]#
DINV[3]#	D[48..63]#	DSTBN[3]# DSTBP[3]#



P.S. Choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.

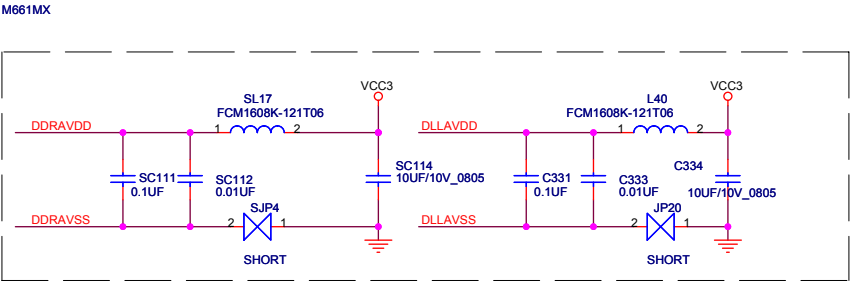
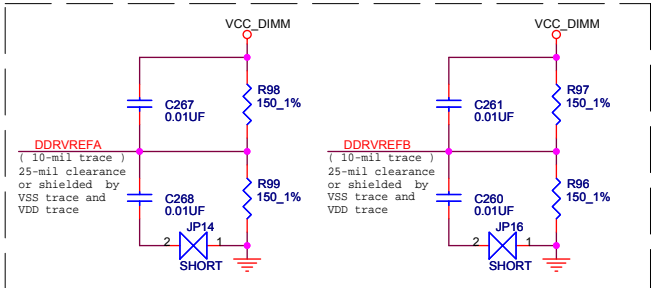
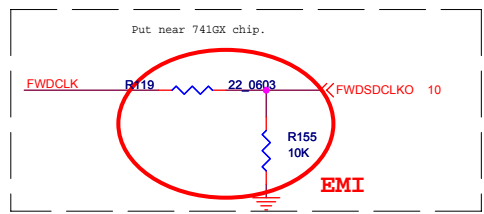
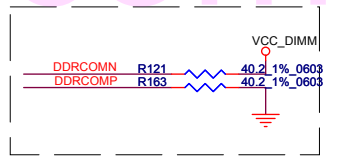
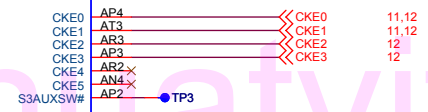
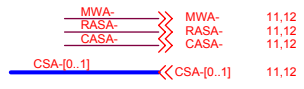
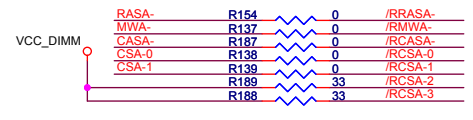
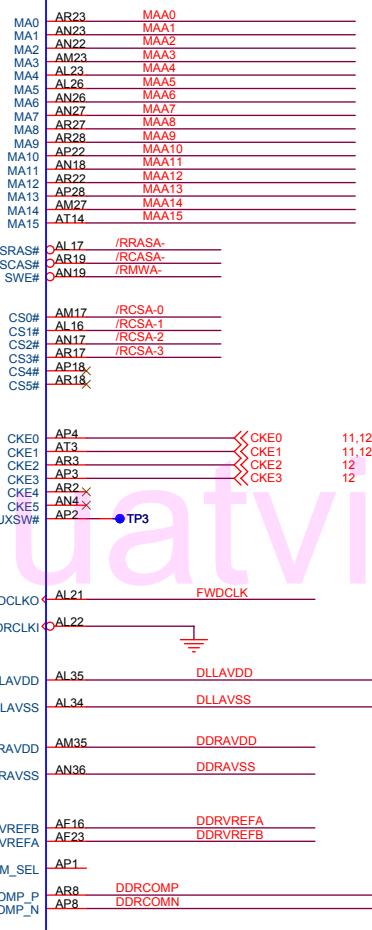
DQM[0..7] << DQM[0..7] 11,12
 DQS[0..7] << DQS[0..7] 11,12
 MD[0..63] << MD[0..63] 11,12

MAA[0..15] << MAA[0..15] 11,12

SU6B

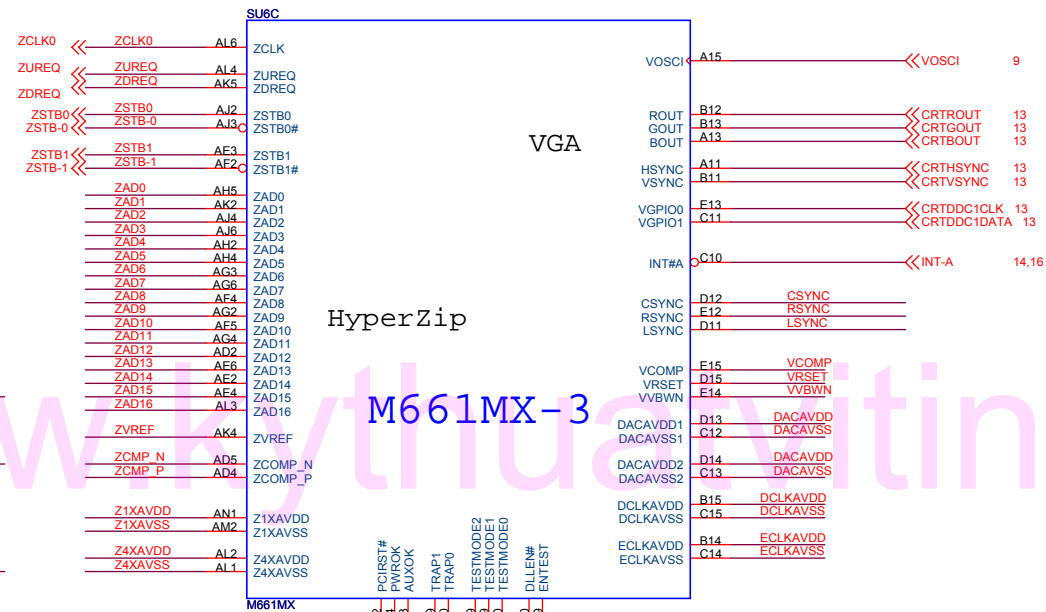
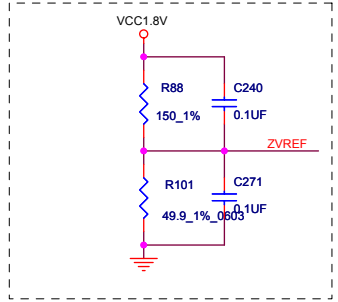
MD0 AN35 MD0
 MD1 AP36 MD1
 MD2 AK33 MD2
 MD3 AM33 MD3
 MD4 AN34 MD4
 MD5 AK32 MD5
 MD6 AR34 MD6
 MD7 AN33 MD7
 DQM0 AR35 DQM0
 DQS0 AP34 DQS0/CSB0#
 MD8 AM32 MD8
 MD9 AL31 MD9
 MD10 AR31 MD10
 MD11 AL30 MD11
 MD12 AN32 MD12
 MD13 AR33 MD13
 MD14 AN31 MD14
 MD15 AM31 MD15
 DQM1 AR32 DQM1
 DQS1 AP32 DQS1/CSB1#
 MD16 AP30 MD16
 MD17 AR30 MD17
 MD18 AM29 MD18
 MD19 AL27 MD19
 MD20 AN30 MD20
 MD21 AN29 MD21
 MD22 AL28 MD22
 MD23 AN28 MD23
 DQM2 AL29 DQM2
 DQS2 AR29 DQS2/CSB2#
 MD24 AP26 MD24
 MD25 AN25 MD25
 MD26 AR24 MD26
 MD27 AL24 MD27
 MD28 AL25 MD28
 MD29 AR26 MD29
 MD30 AM25 MD30
 MD31 AN24 MD31
 DQM3 AP24 DQM3
 DQS3 AR25 DQS3/CSB3#
 MD32 AN21 MD32
 MD33 AP20 MD33
 MD34 AN20 MD34
 MD35 AL18 MD35
 MD36 AP21 MD36
 MD37 AR21 MD37
 MD38 AL19 MD38
 MD39 AM19 MD39
 DQM4 AL20 DQM4
 DQS4 AR20 DQS4/CSB4#
 MD40 AL15 MD40
 MD41 AL14 MD41
 MD42 AN15 MD42
 MD43 AR15 MD43
 MD44 AN16 MD44
 MD45 AM15 MD45
 MD46 AN14 MD46
 MD47 AL13 MD47
 DQM5 AP16 DQM5
 DQS5 AR16 DQS5/CSB5#
 MD48 AM13 MD48
 MD49 AL12 MD49
 MD50 AL11 MD50
 MD51 AR12 MD51
 MD52 AP14 MD52
 MD53 AR14 MD53
 MD54 AN13 MD54
 MD55 AP12 MD55
 DQM6 AN12 DQM6
 DQS6 AR13 DQS6/CSB6#
 MD56 AL10 MD56
 MD57 AR11 MD57
 MD58 AM9 MD58
 MD59 AR9 MD59
 MD60 AM11 MD60
 MD61 AN11 MD61
 MD62 AP10 MD62
 MD63 AN8 MD63
 DQM7 AH0 DQM7
 DQS7 AR10 DQS7/CSB7#

M661MX-2

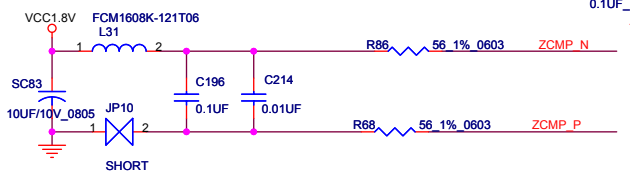
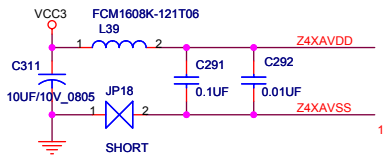
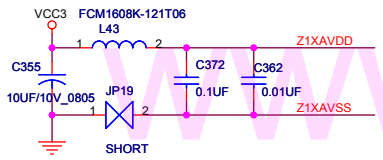
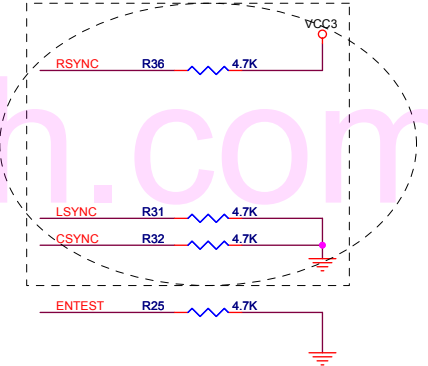


SW2 Pin	Description	ON/1	OFF/0	Default
S1	DILEN CPUCLK SDCLK PLL/DLL Circuit Enable	DISABLE	ENABLE	OFF
S2	TRAP0 Debug Mode Select	ENABLE	DISABLE	OFF
S3	TMODE1 MuTIOL (ASL) Initialize Series Mode	DISABLE	ENABLE	OFF
S4	TMODE2 NB ASL DBI REGISTER MODE	DISABLE	ENABLE	OFF
S5	TRAP1 MuTIOL Type (Version 1, 2)	Ver. 1	Ver. 2	OFF

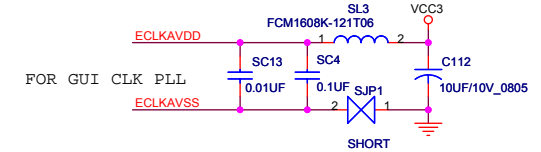
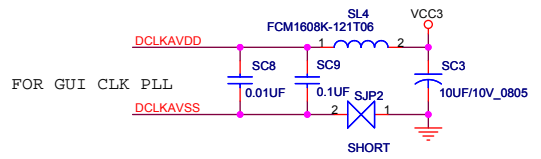
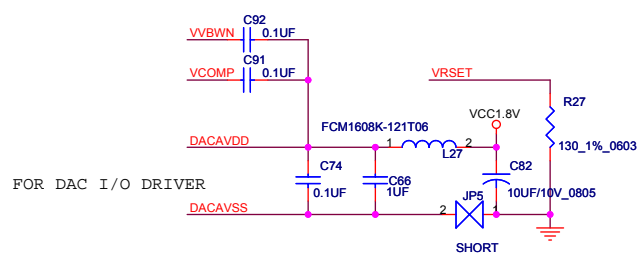
NB Hardware Trap internal pull-low



		Enable	Disable
RSYNC	VGA Interrupt	1	0
LSYNC	TBD	1	0
CSYNC	TBD	1	0

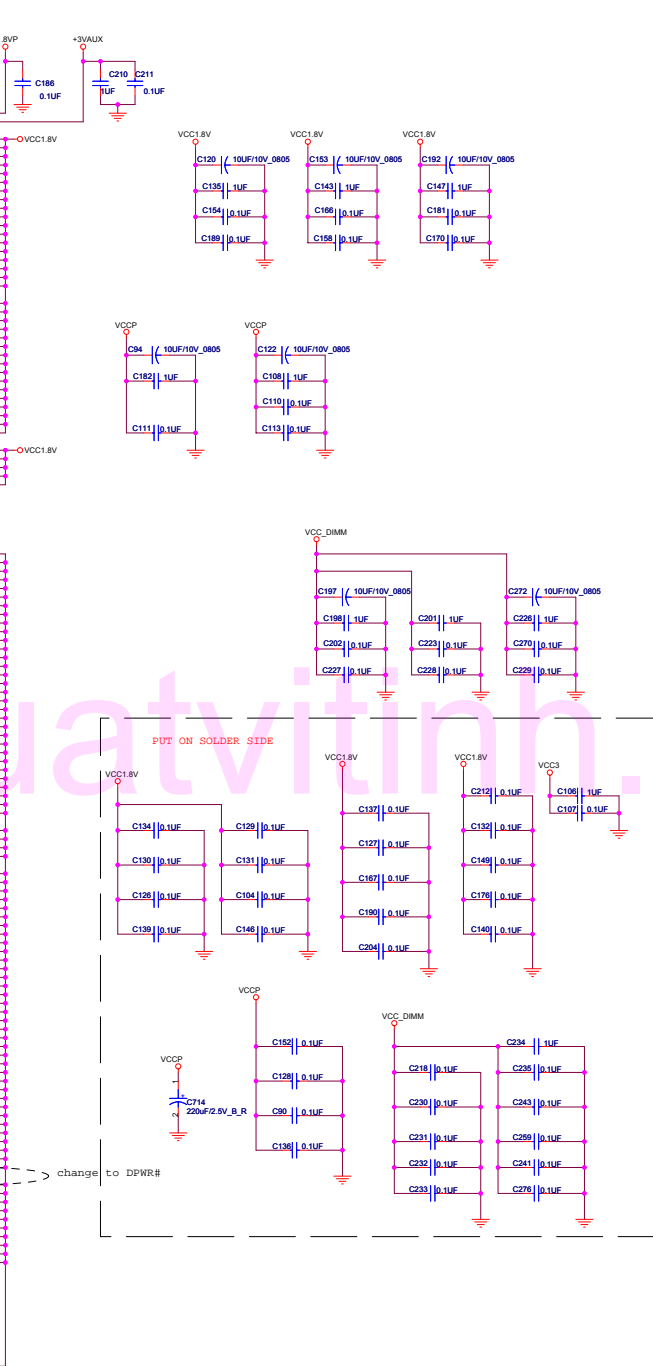


PCIRST-14,15,16,21,22,29
15,17,26,28,32
AUXOK

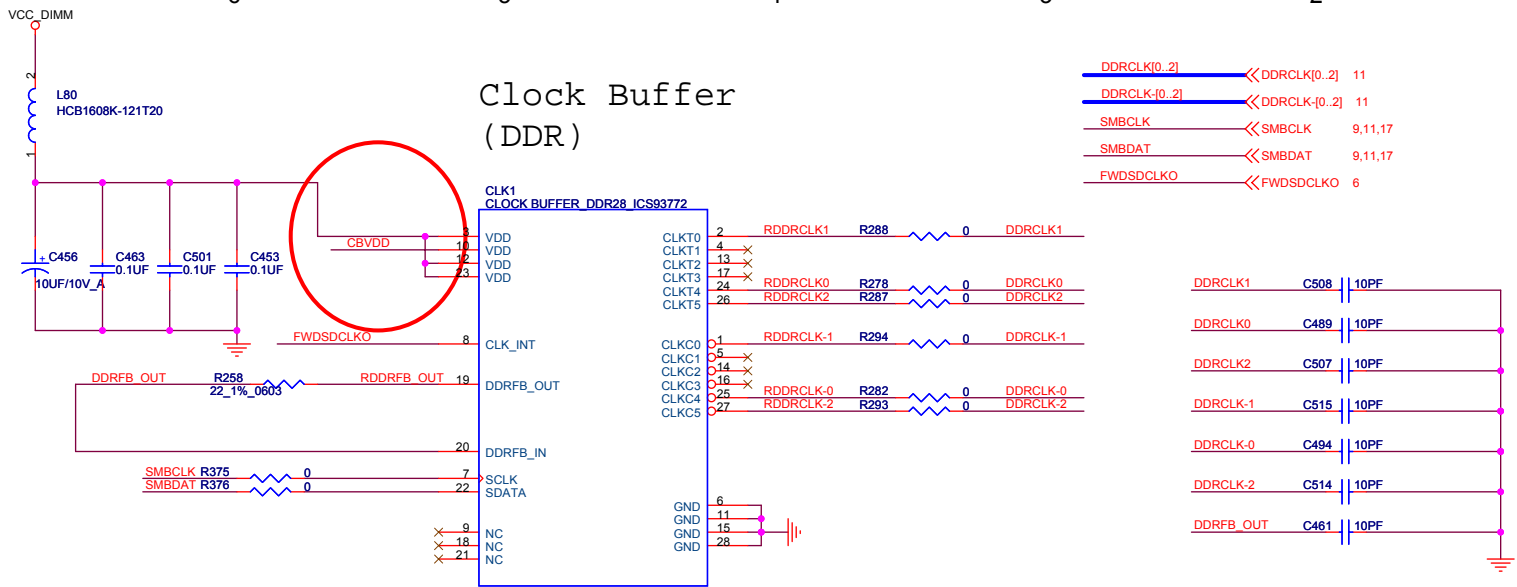


M661MX-4

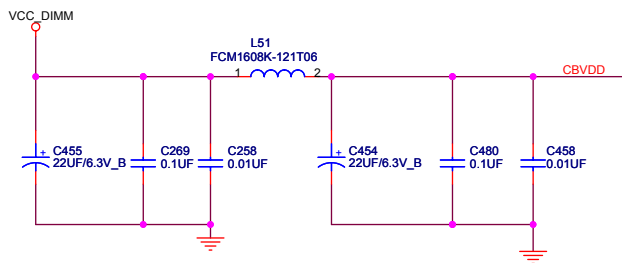
Power

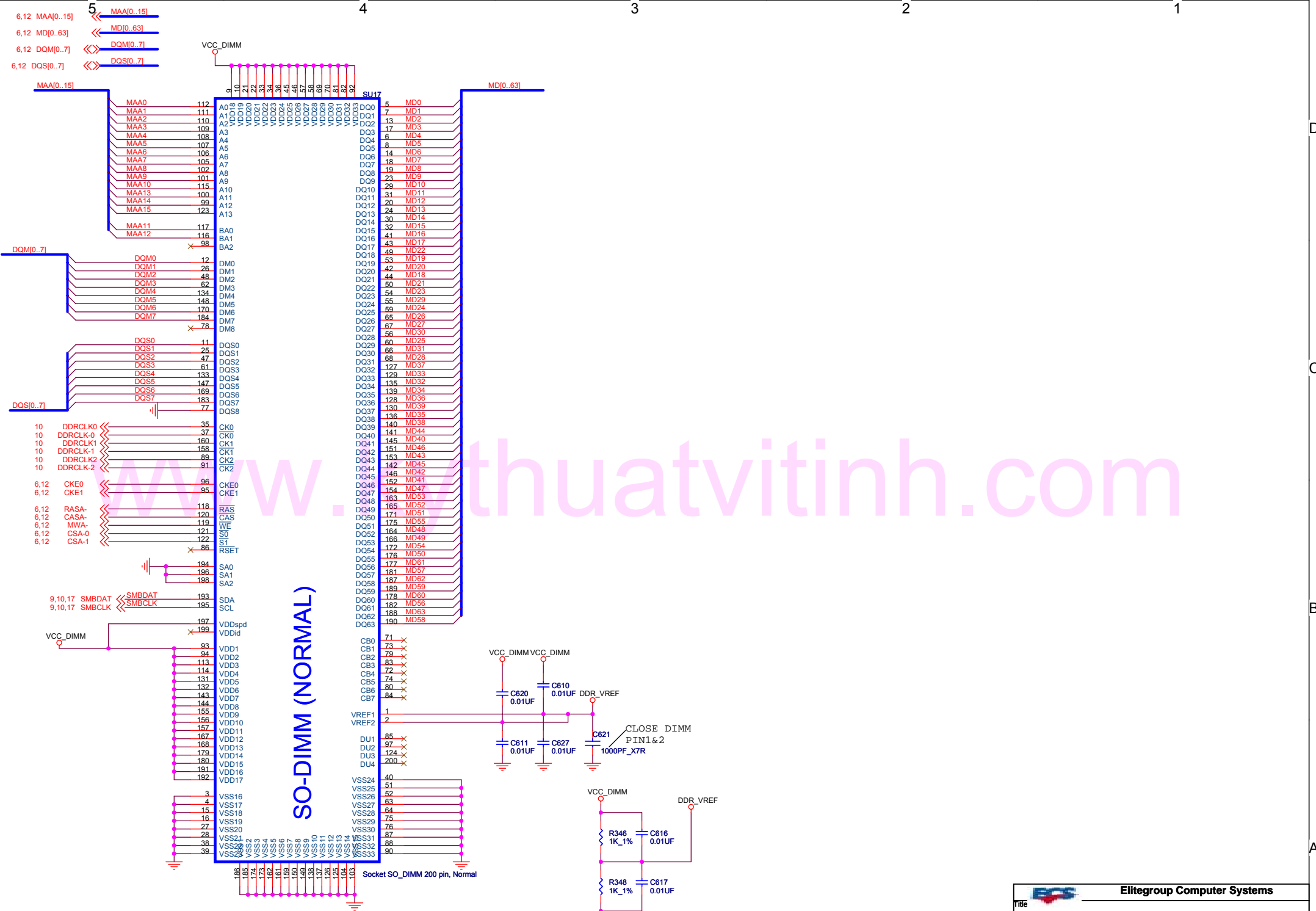


Clock Buffer (DDR)



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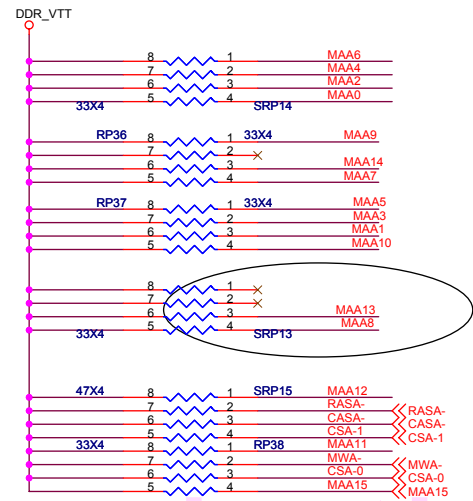
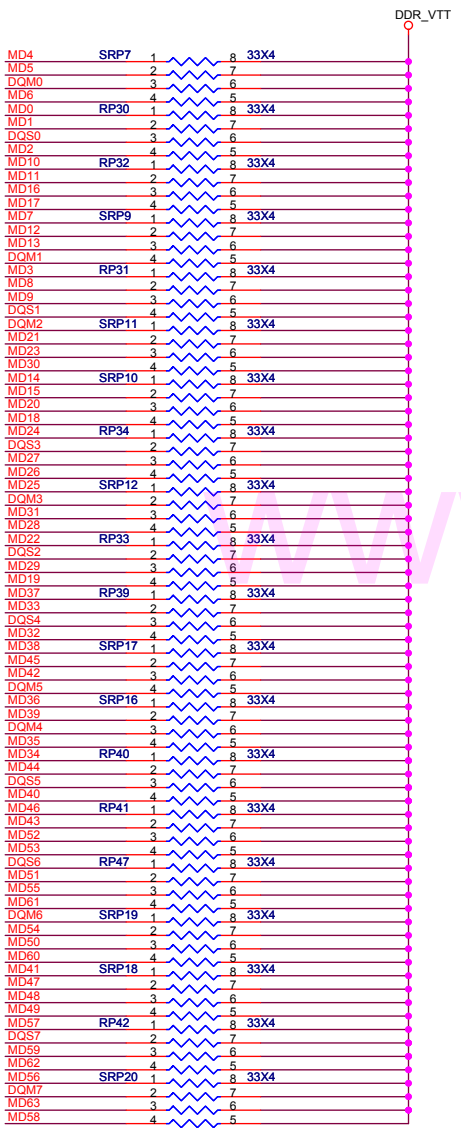
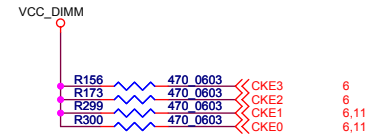
SO-DIMM no "WP" pin

- 6,11 MAA[15..0] << MAA[15..0]
- 6,11 MD[63..0] << MD[63..0]
- 6,11 DQM[7..0] << DQM[7..0]
- 6,11 DQS[7..0] << DQS[7..0]

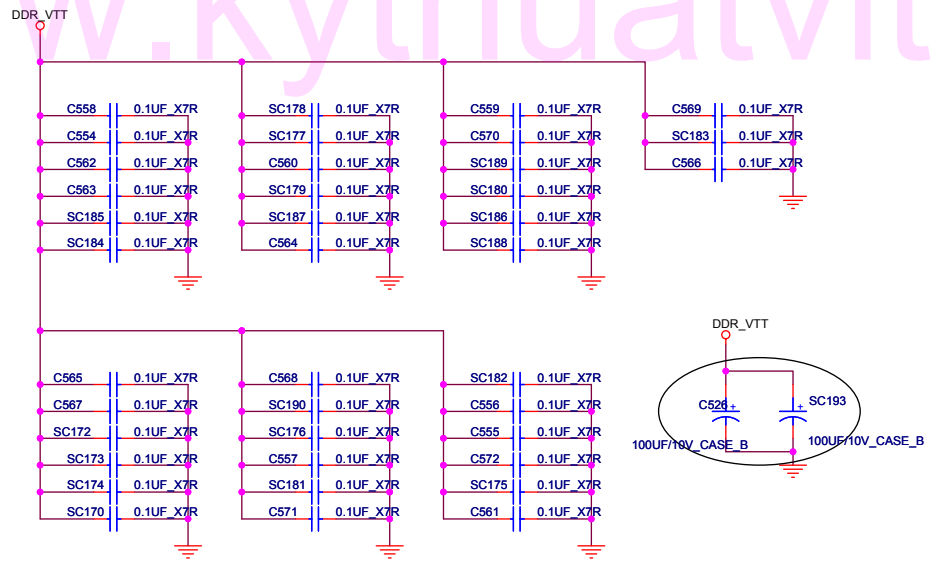
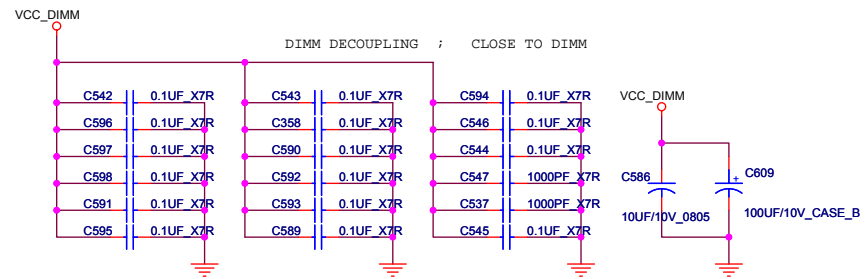
SSTL-2 Termination Resistors

	SDR	Pa	EDR	Pa	RLT
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	10	33
MA/Control	LV-CMOS	0	SSTL-2	0	33
CS	LV-CMOS	0	SSTL-2	0	47
CKE	DD 3.3V		DD 2.5V		

Control signals can NOT be placed within the same RPs as data , strobe , or command signals

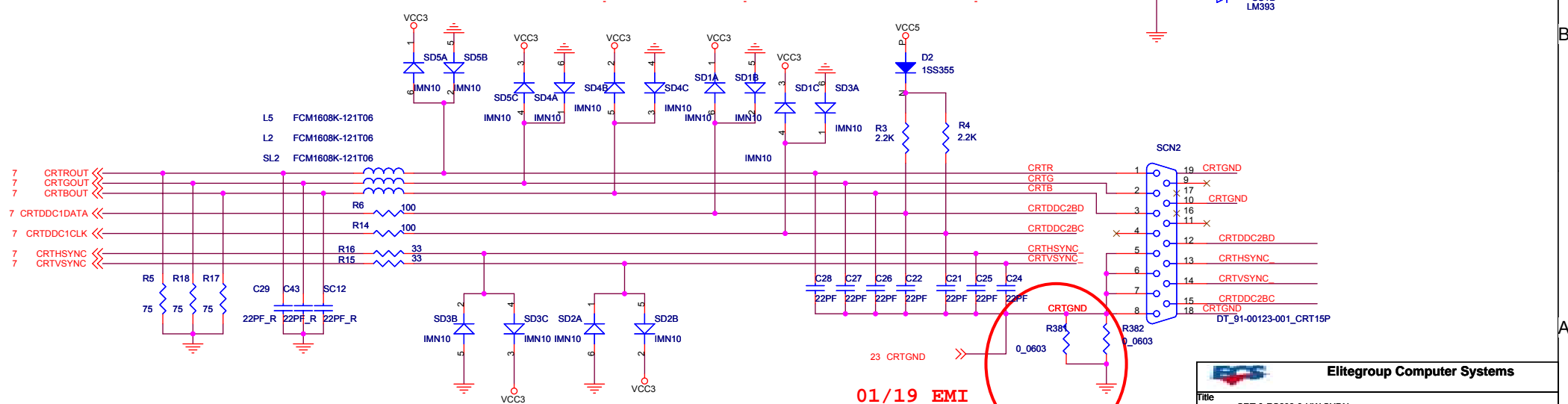
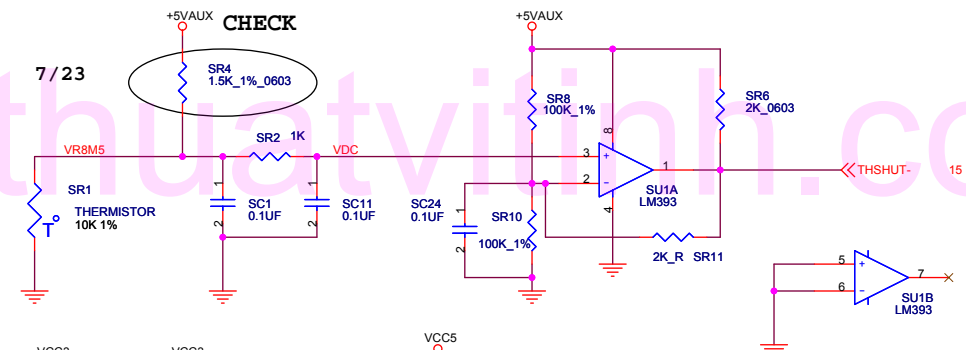
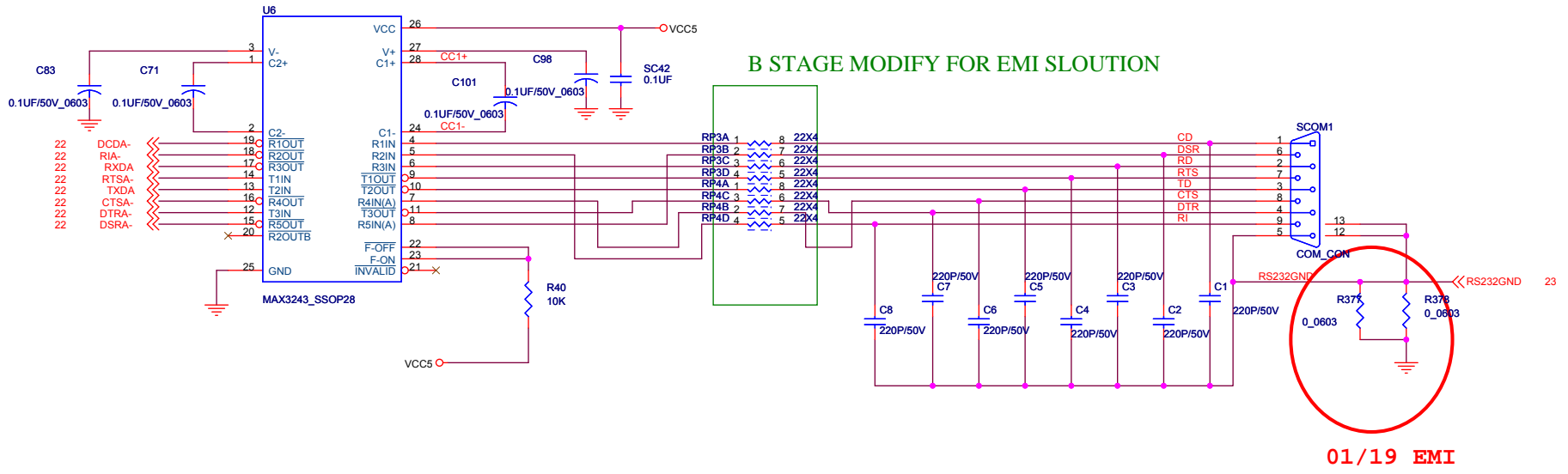


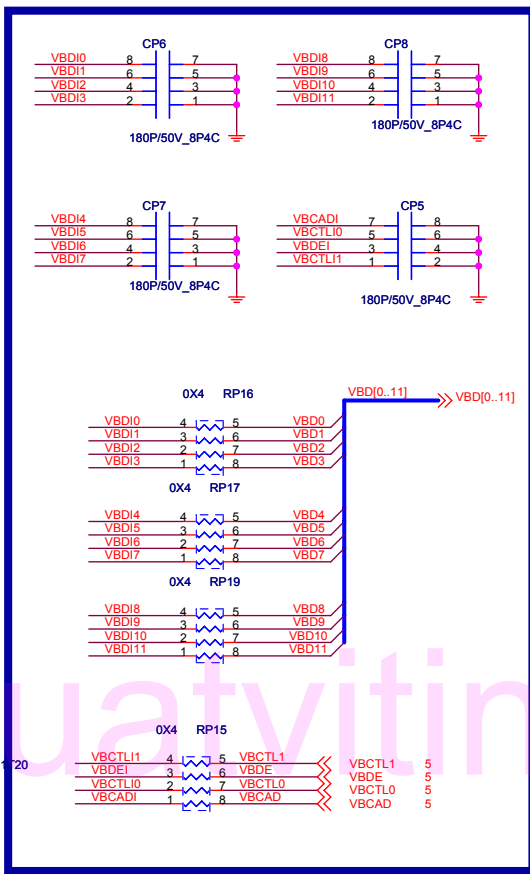
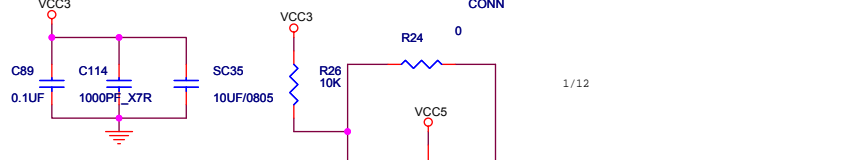
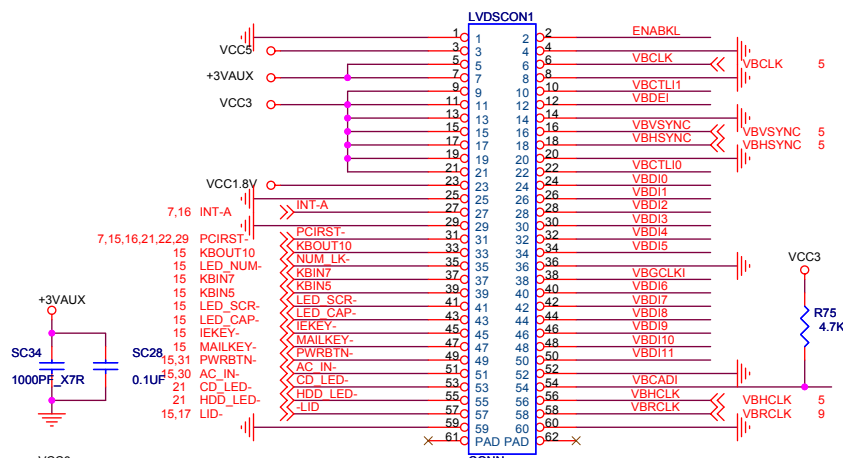
DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
402 Package placed within 300mils of VTT Termination R-packs



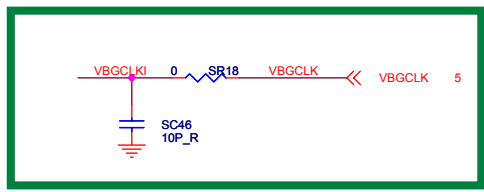
every 2 "RPs" put 3 CAPS

0.1UF X 39 pcs

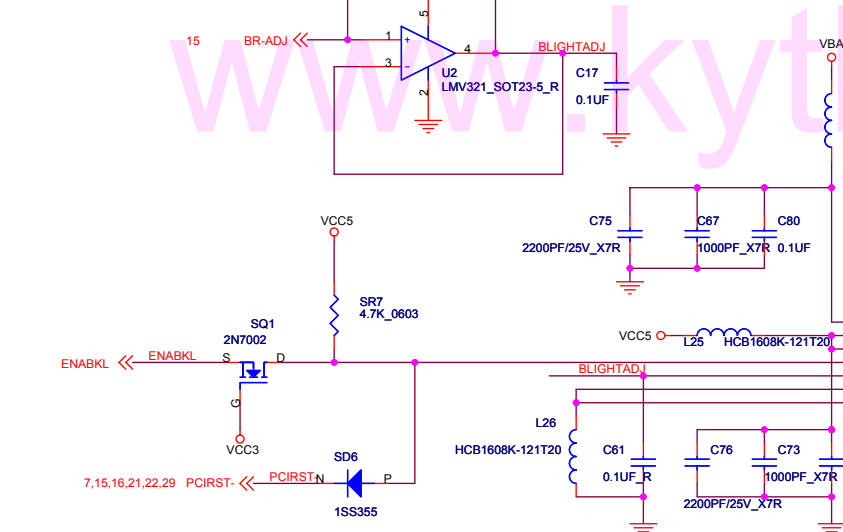




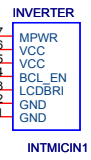
CLOSE BY SIS661FX

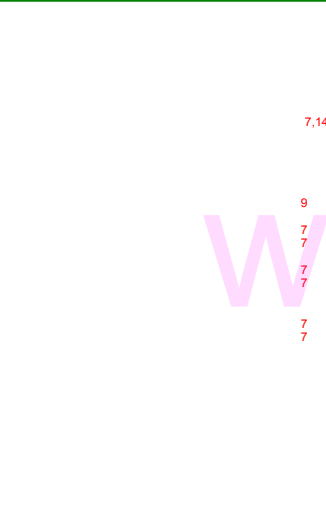
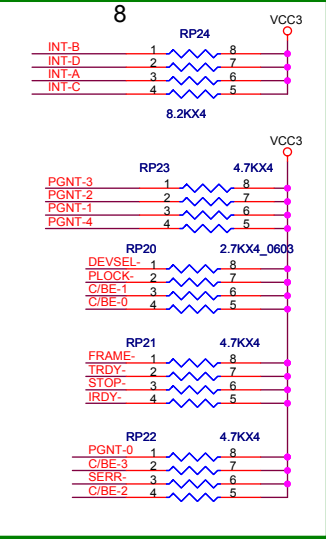


CLOSE BY SIS661FX



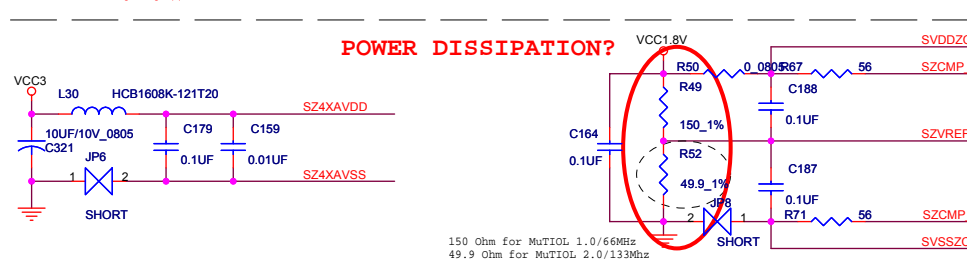
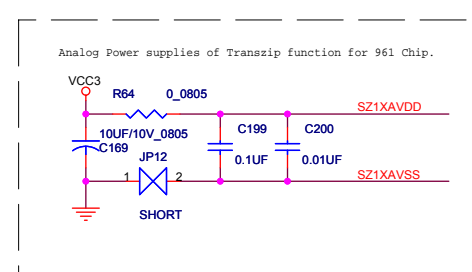
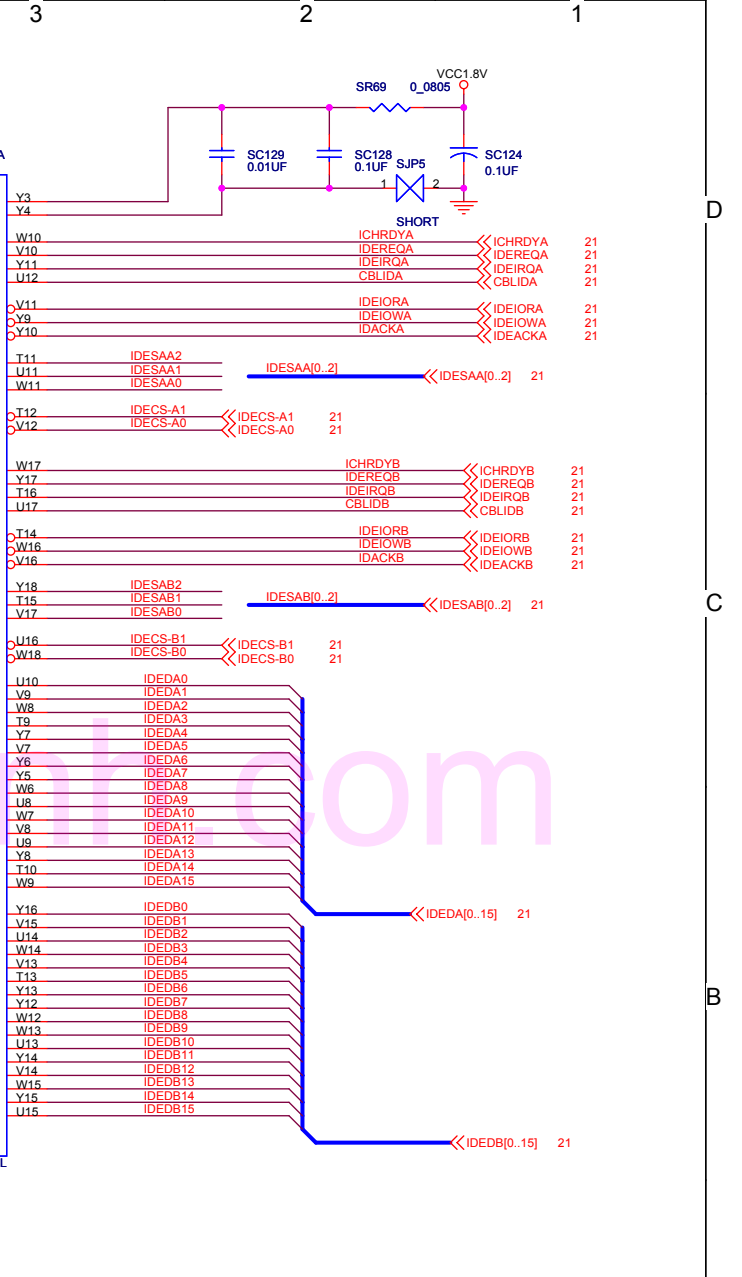
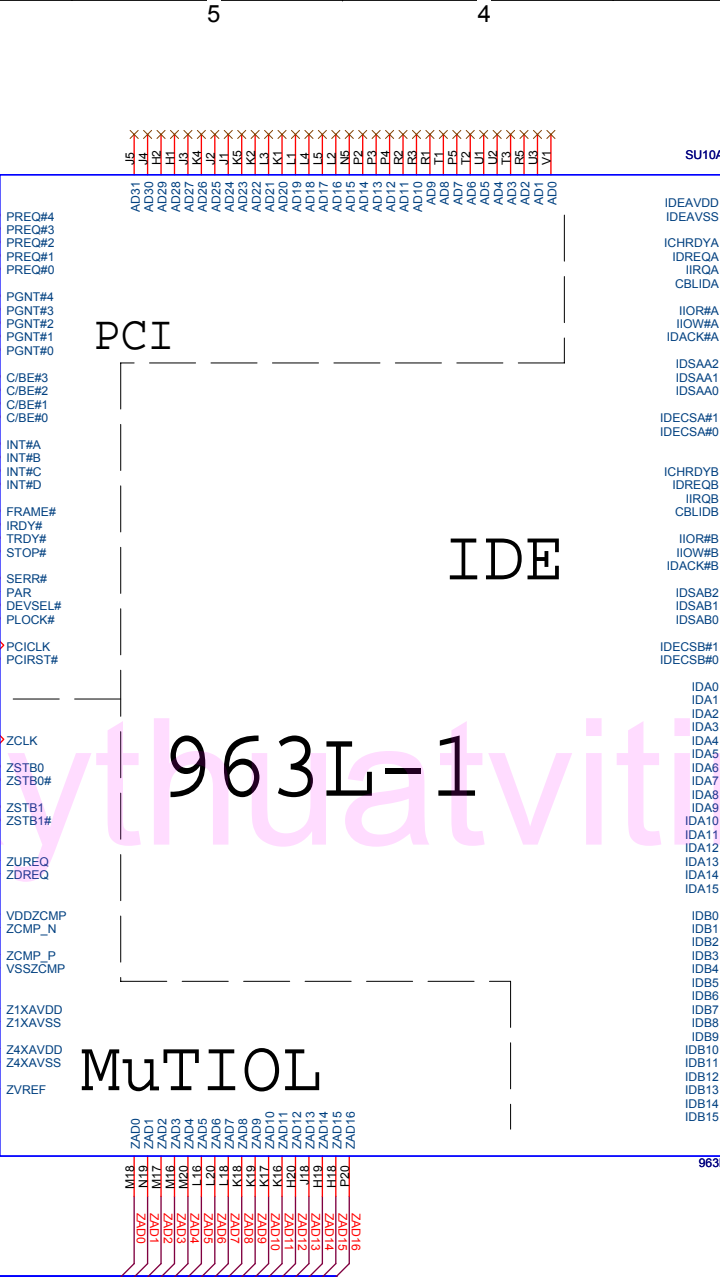
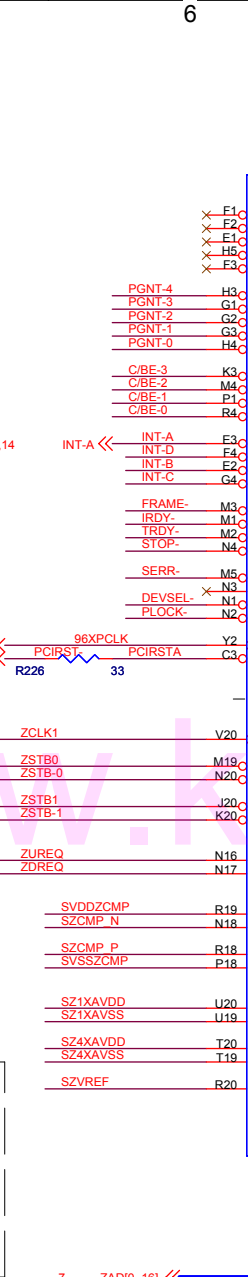
EMI

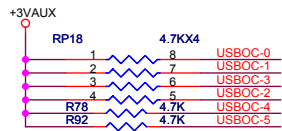




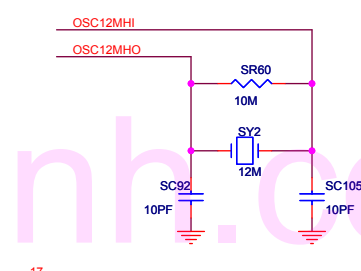
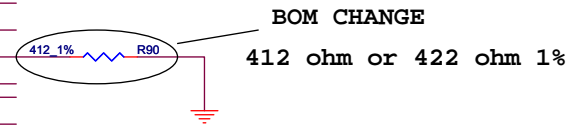
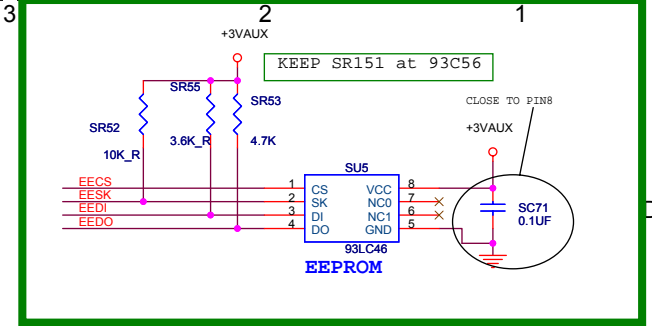
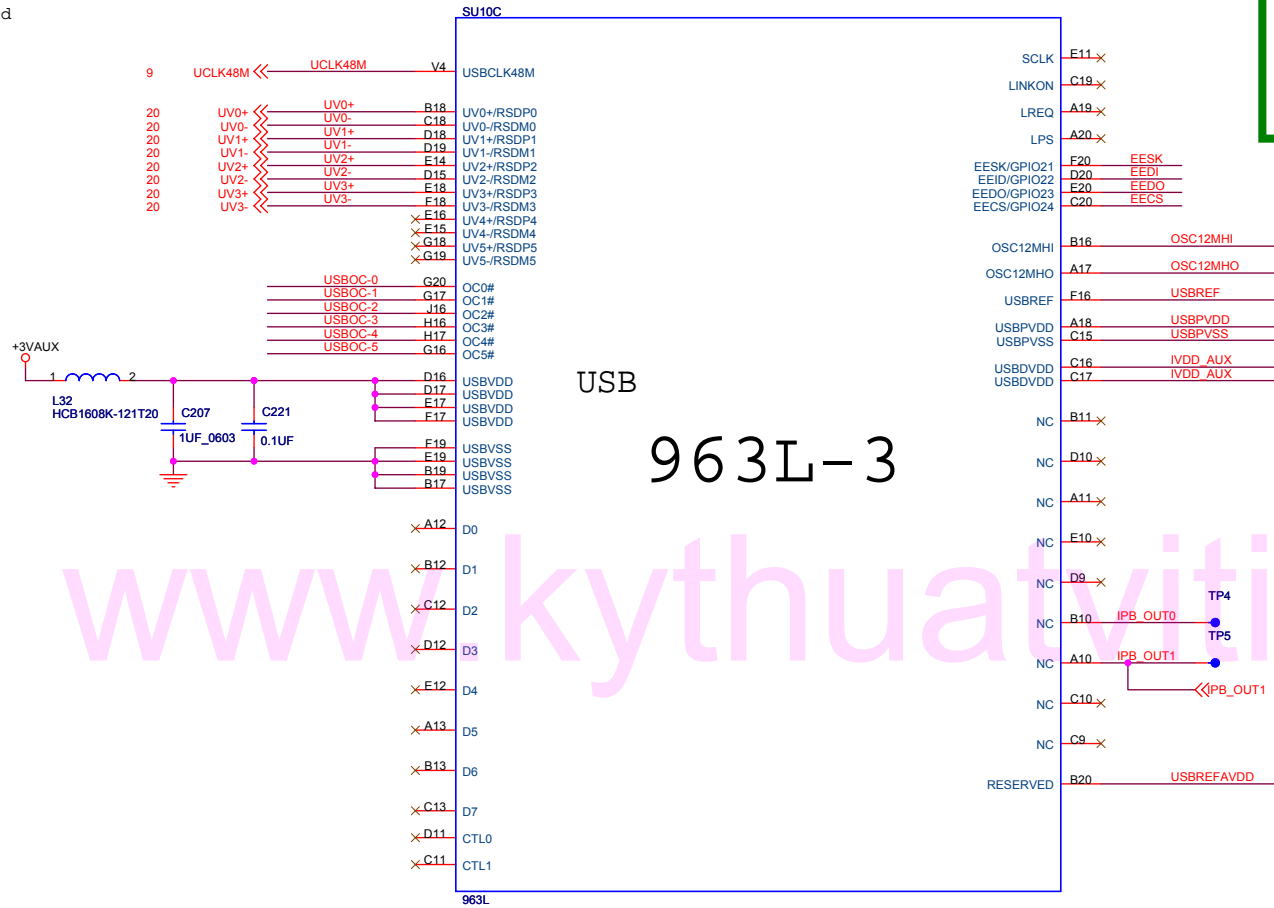
PCI Bus Configuration

Dev.	INT.	REQ.	GNT.	IDSEL.
MINIPCI	C	2	2	16
RTL8110S	B	0	0	18
M661MX	A			11, 12
SIS301LV	A			
963L				13, 14, 15



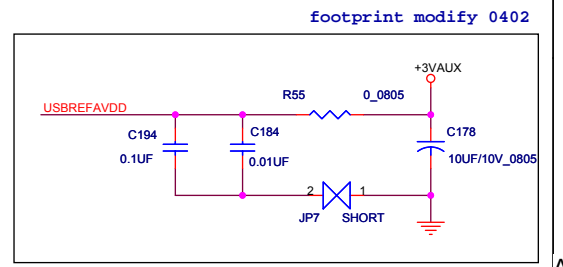
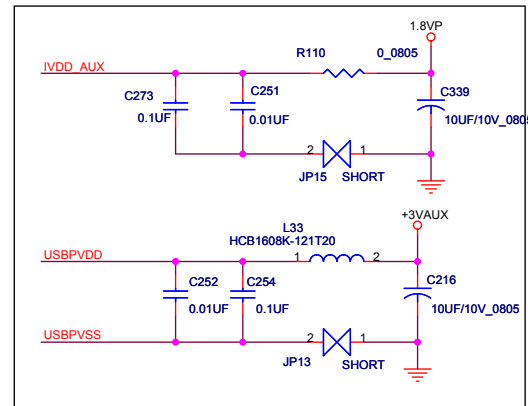


They don't need to be placed near the SiS963L



• Test Mode Funtion, Don't care.

SB Hardware Trap					
SW3 Pin		0	1	Default	Internal pull (30-50K Ohm)
S1	SPKR(LPC Addr Mapping)	Disable	Enable	OFF	Pull Low
S2	SDAIO(Trap Mode)	ROM	PCI AD	OFF	Pull Low
S3	SYNC(PCICLK PLL)	Enable	Disable	OFF	Pull Low
S4	OC4-(SB Debug Mode)	Enable	Disable	NONE	Pull High
S5	IPB_OUT0(MUTIOL Iq EN)	Enable	Disable	Enable	Pull Low
S6	IPB_OUT1(OP MODE SEL)	Partial	Full	Partial	Pull Low

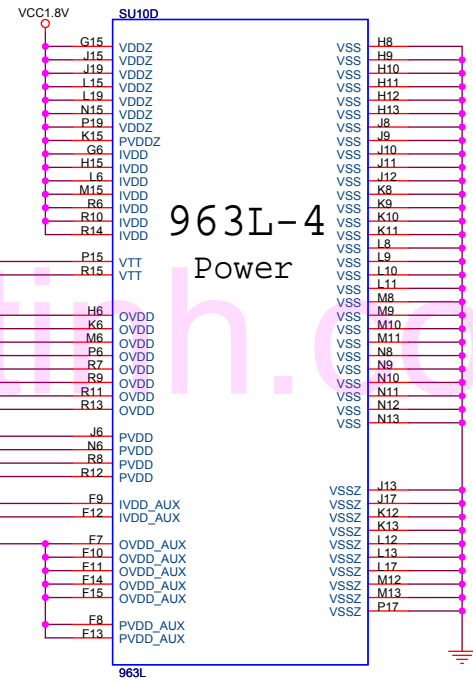
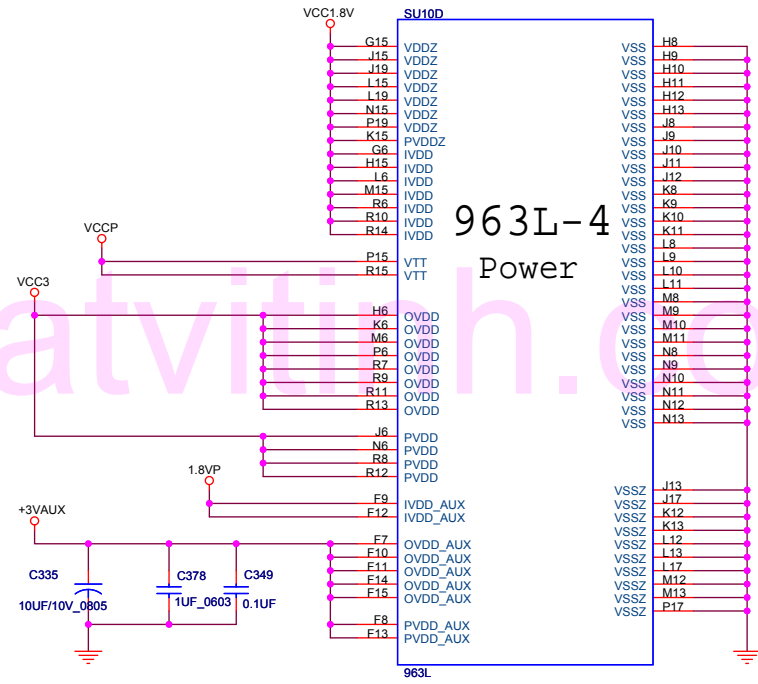
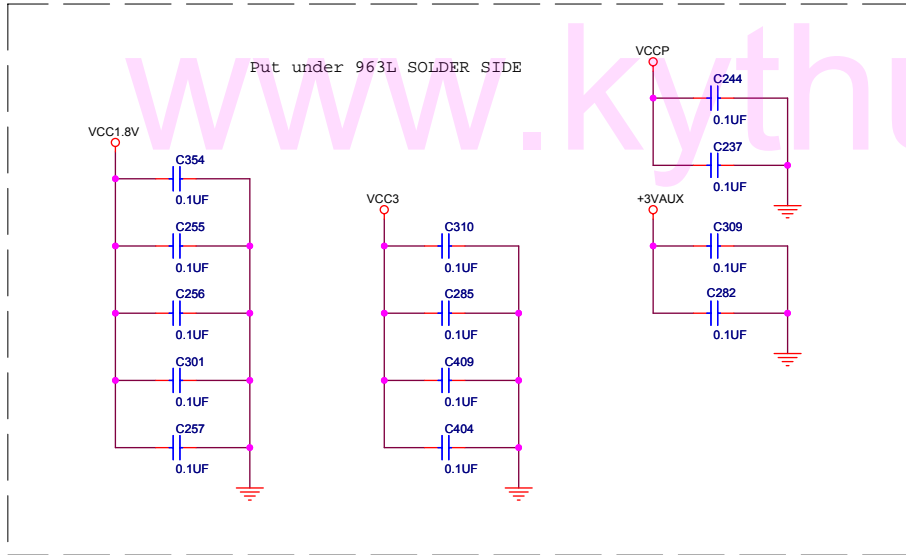
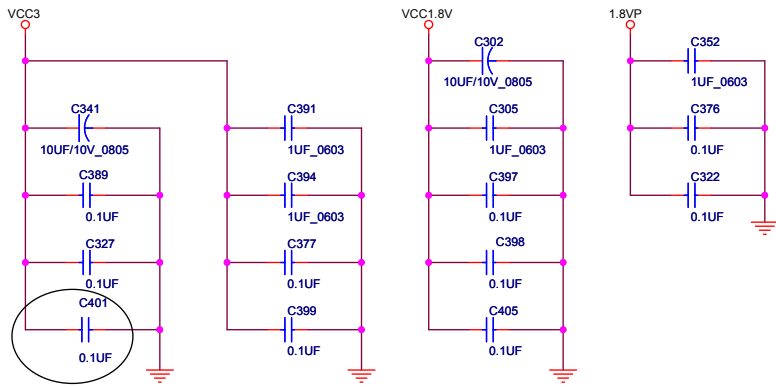


Elitegroup Computer Systems

Title: 963L-3(USB/OTHERS)

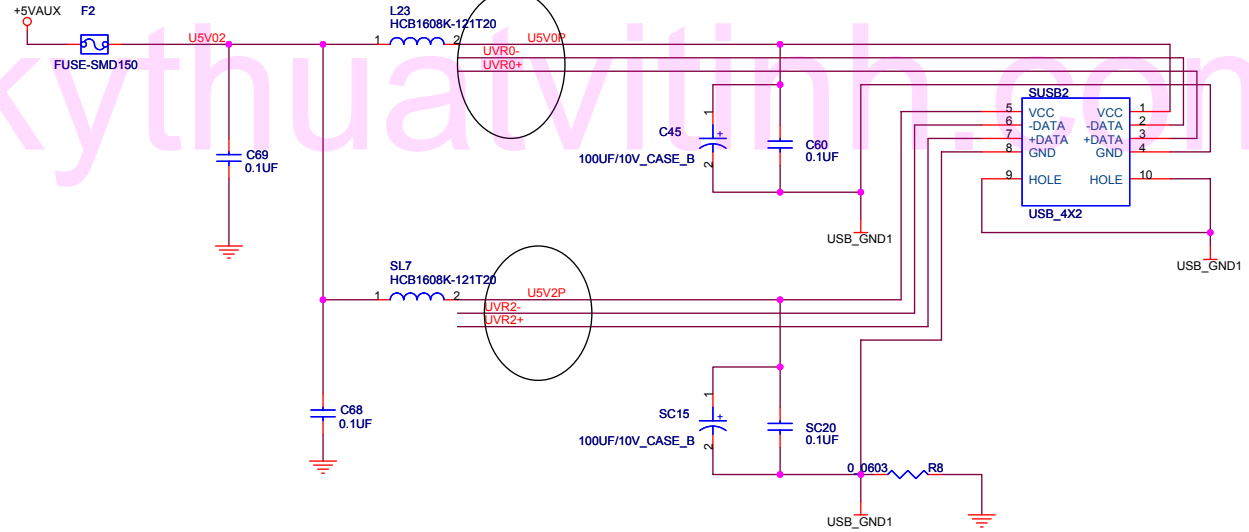
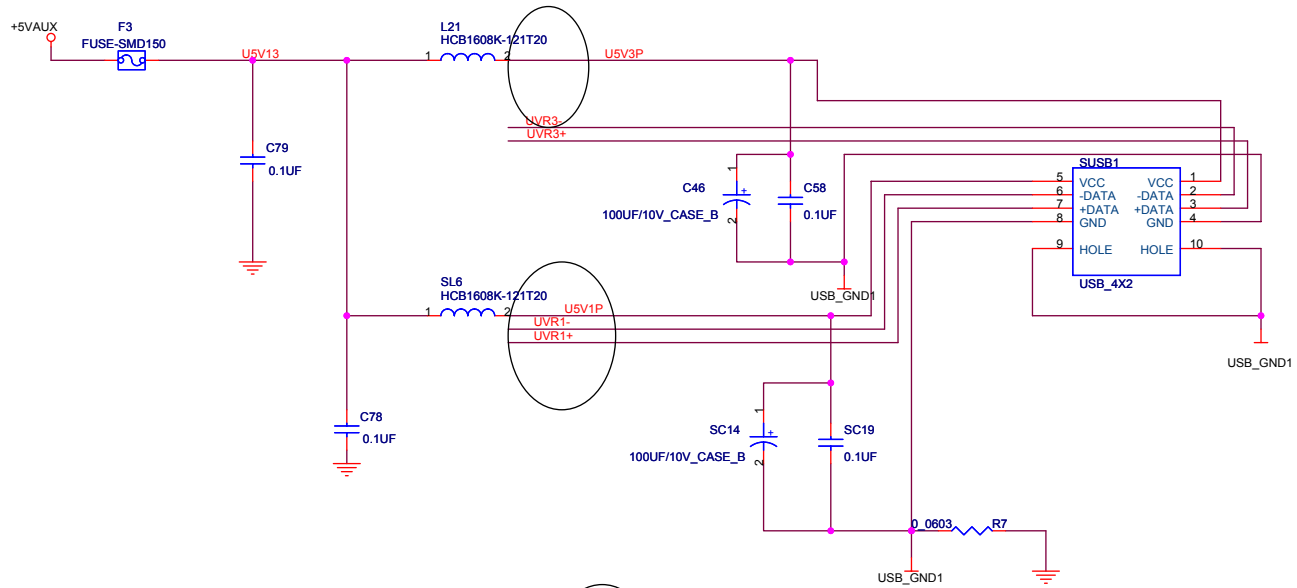
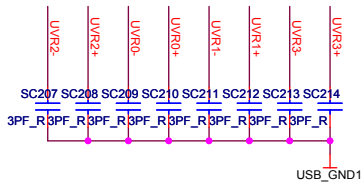
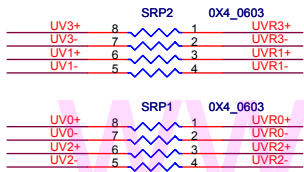
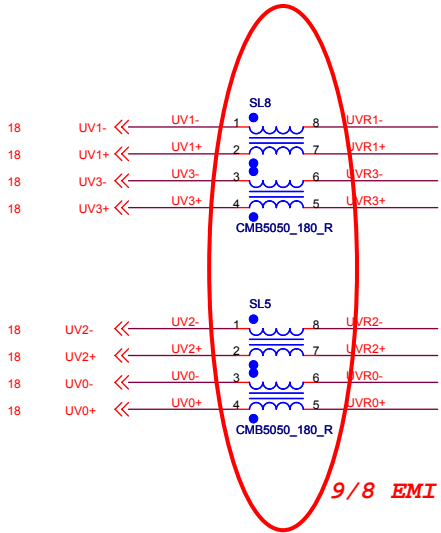
Size B Document Number 321-1-4-01 Rev A.0

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footprint modify 0402

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Title 963L-4 (Powers)		
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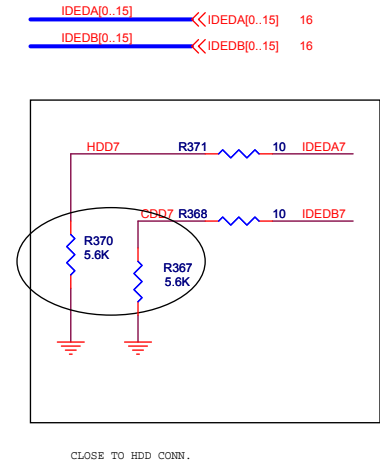
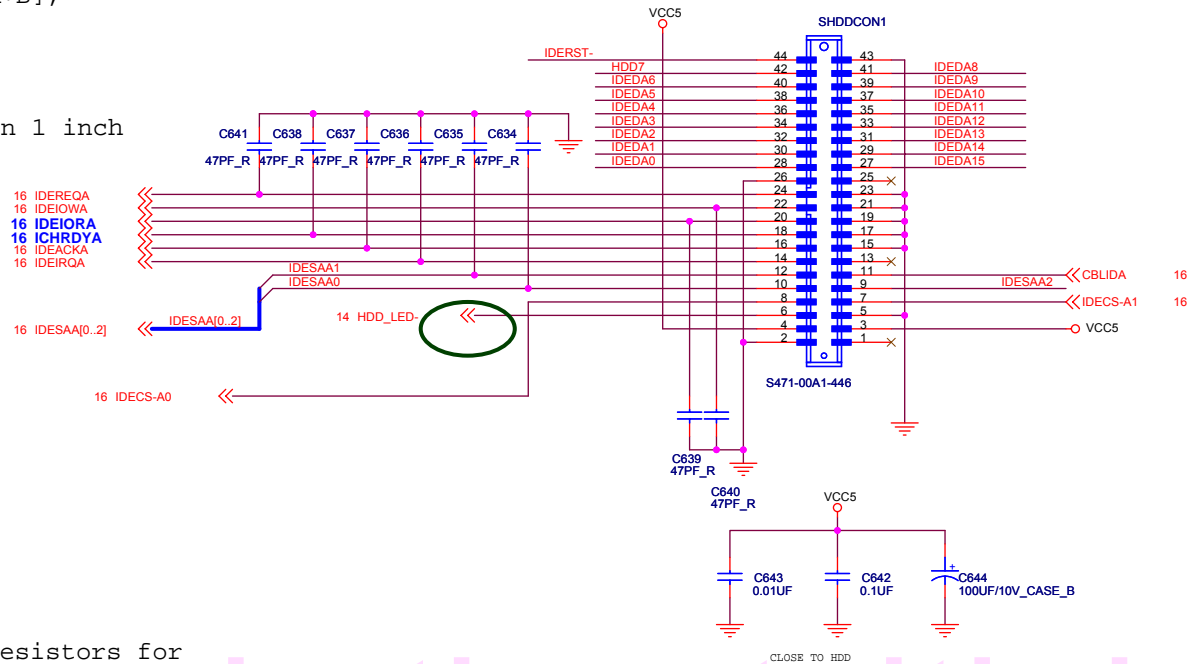


ALL THESE CLOSE TO CONNECTOR

footprint modify 0402

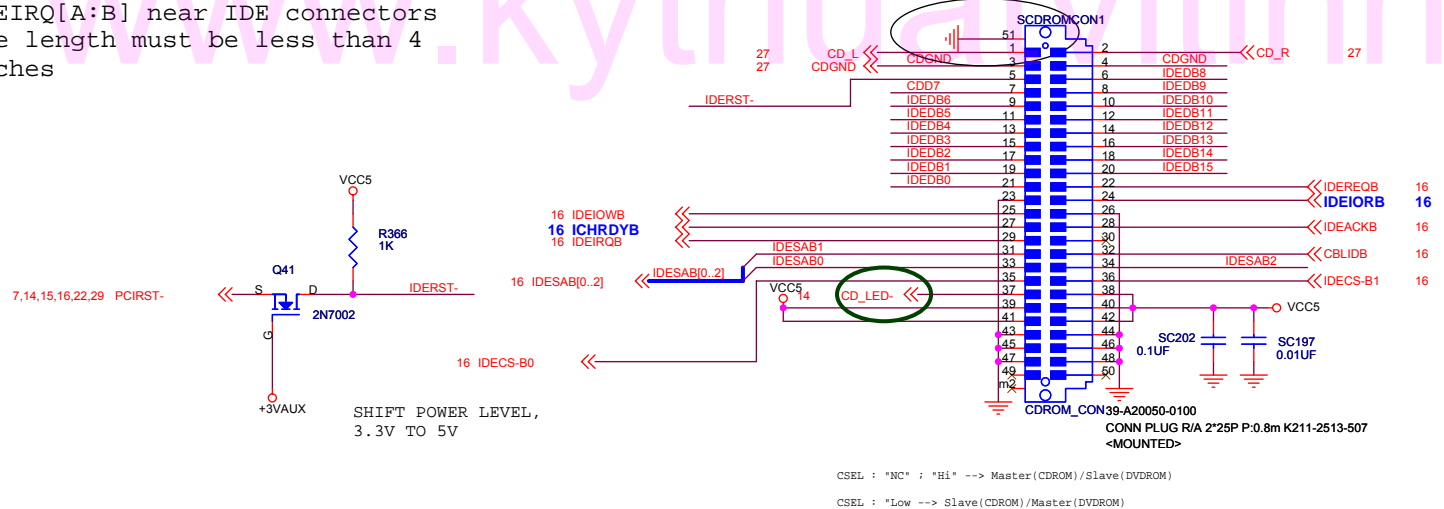
Elitegroup Computer Systems		
Title: USB PORT		
Size B	Document Number	Rev
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Date:	Wednesday, February 02, 2005	Sheet 20 of 35

Place the damping resistors for
 IDEA[2:0][A:B], IDECS[1:0][A:B],
 IDEIOR[A:B]#,
 IDEIOW[A:B]#, and
 IDACK[A:B]# near
 SiS962L
 The length must be less than 1 inch

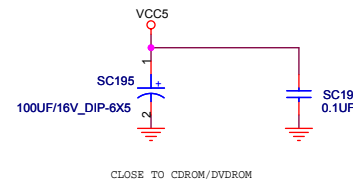


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Place the damping resistors for
 IDEDB[15:0][A:B], IDREQ[A:B],
 ICHRDY[A:B], and
 IDEIRQ[A:B] near IDE connectors
 The length must be less than 4
 inches

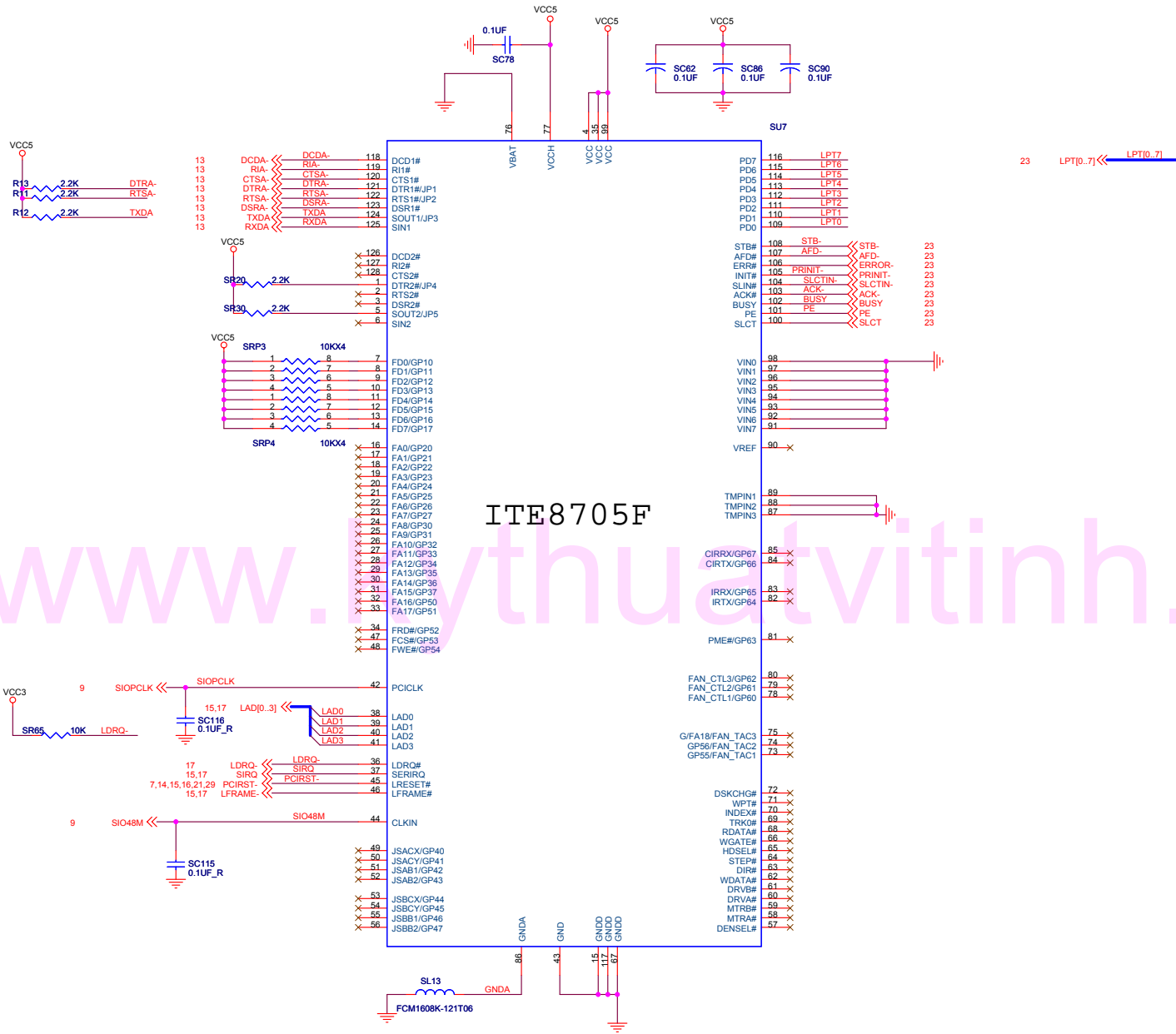


CSEL : "NC" ; "Hi" --> Master(CDRON)/Slave(DVDROM)
 CSEL : "Low" --> Slave(CDRON)/Master(DVDROM)

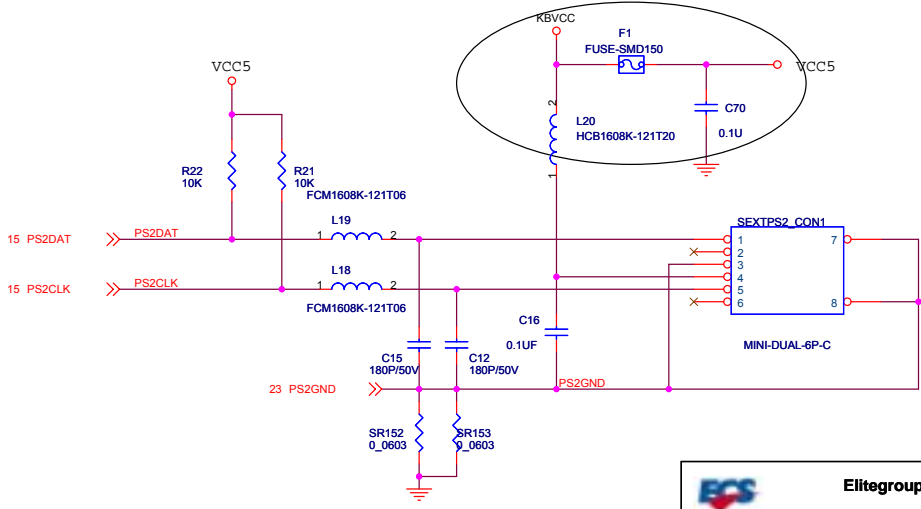
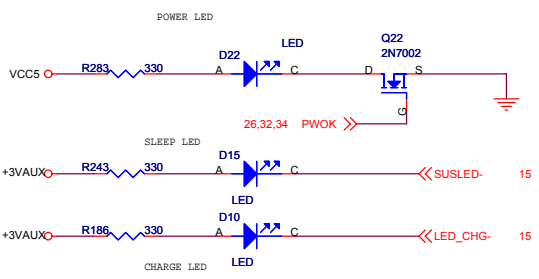
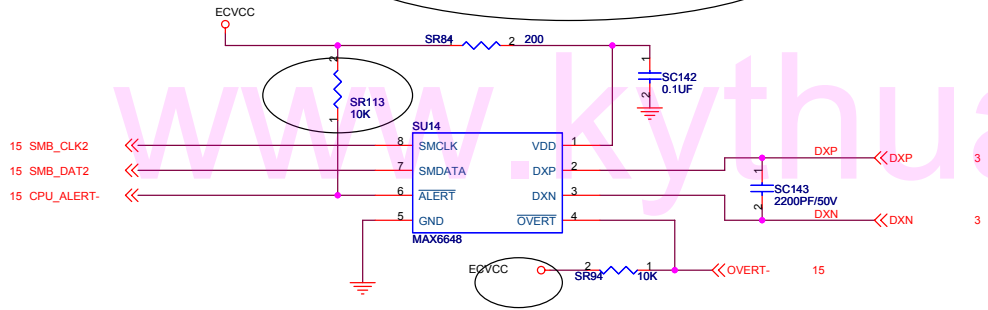


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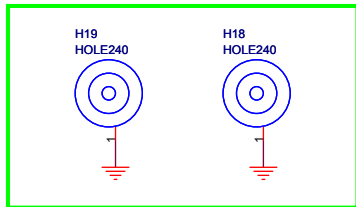
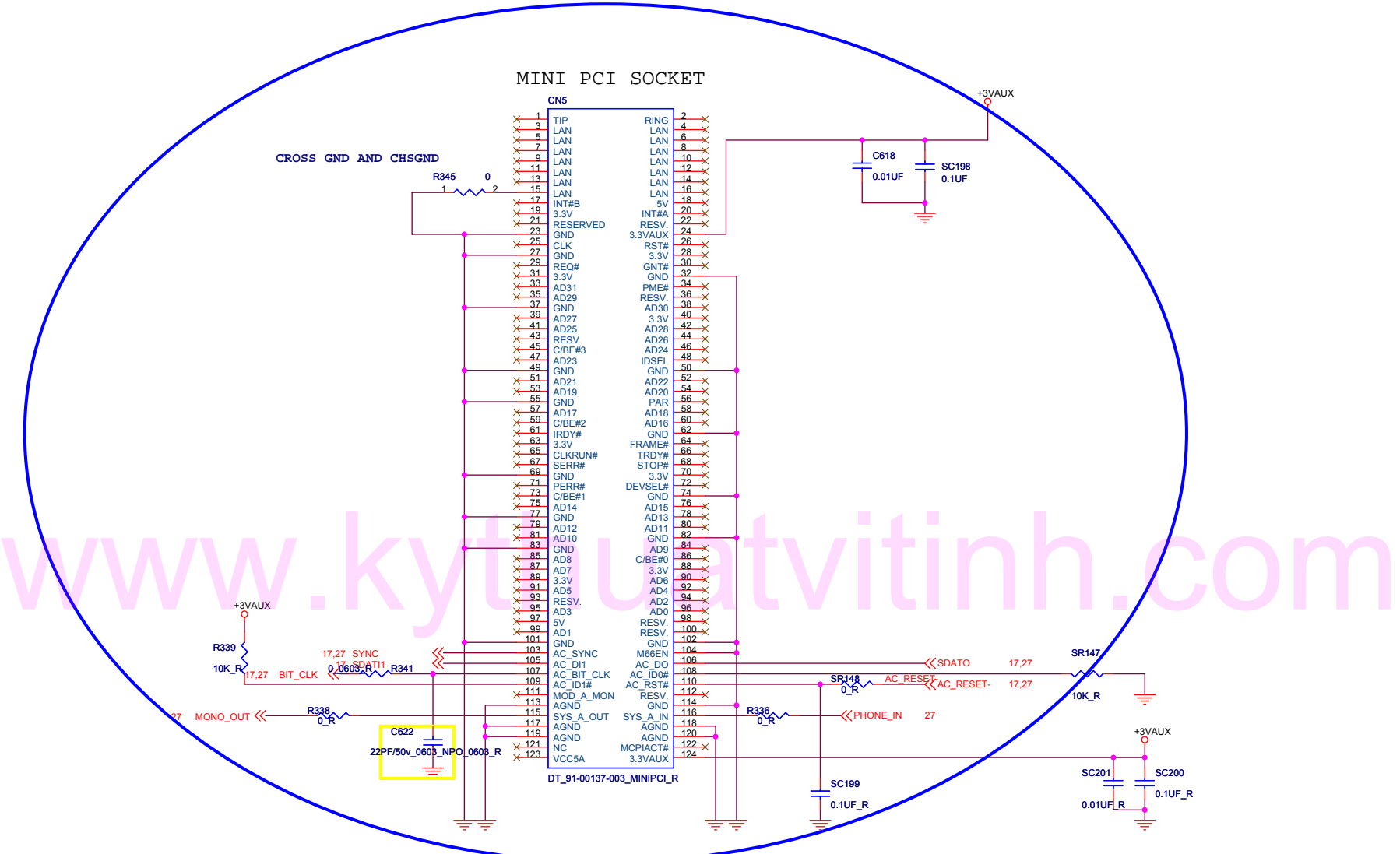
Elitegroup Computer Systems		
Title HDD & CDRON CONN.		
Size B	Document Number 321-1-4-01	Rev A.0
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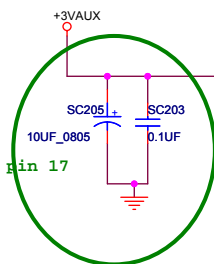
Slave Addresses=1001100



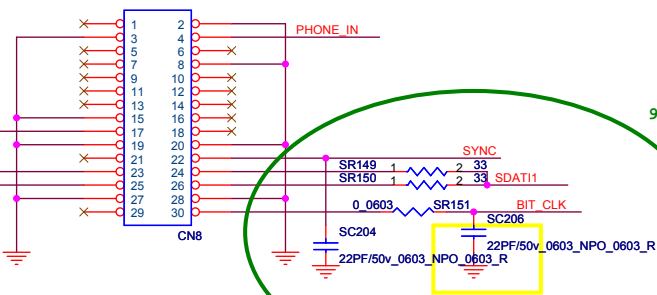
MINI PCI SOCKET



9/20 MODIFY close to MDC pin 17

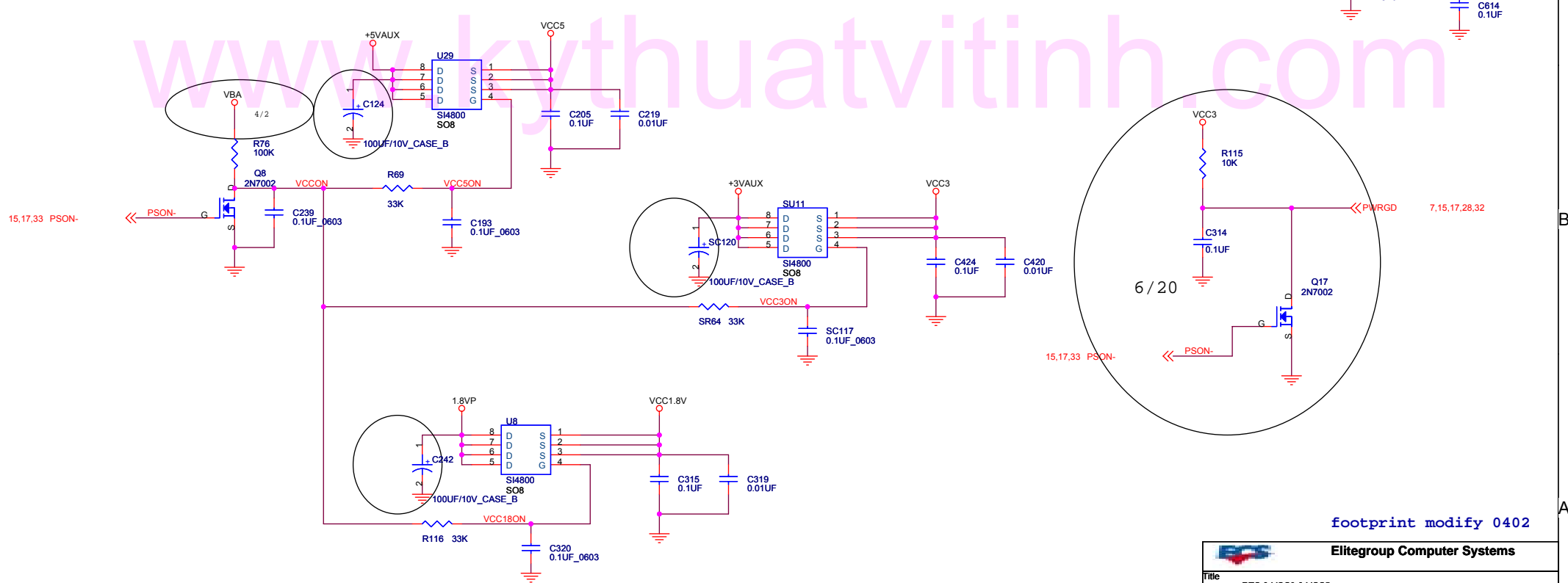
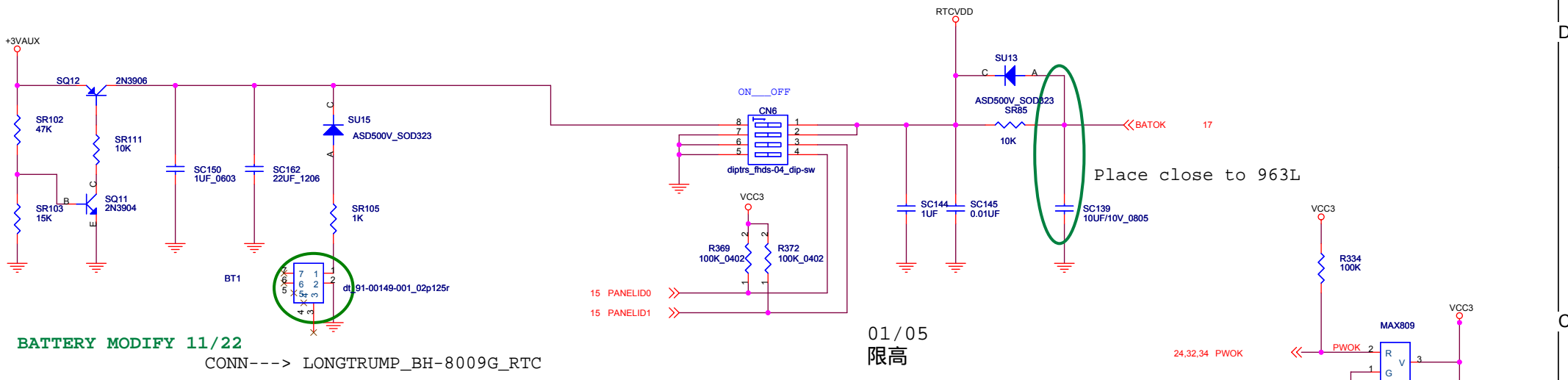


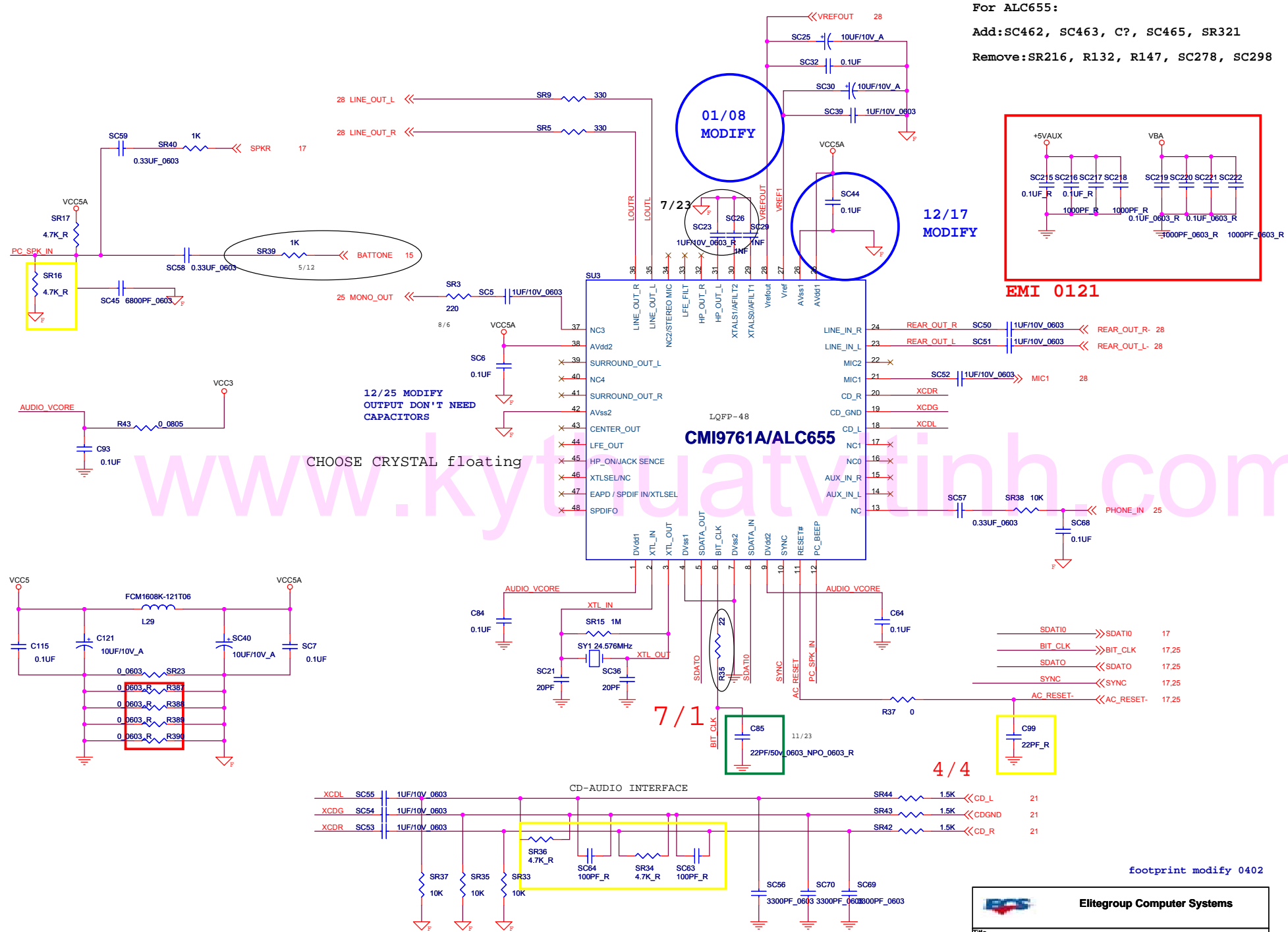
dt_91-00107-018_mdc-30p15h



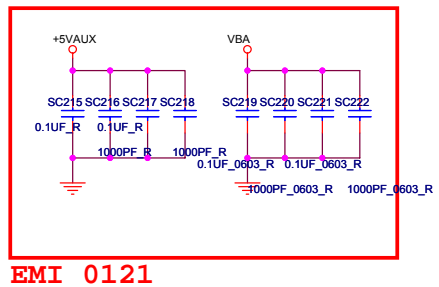
9/20 MODIFY

- RTC 8
- NOTE!
- 1.The RTCVDD is 3V
 - 2.Decoupling capacitor must be close to 963L RTCVDD pin.
 - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.





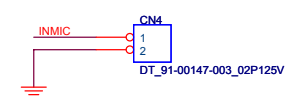
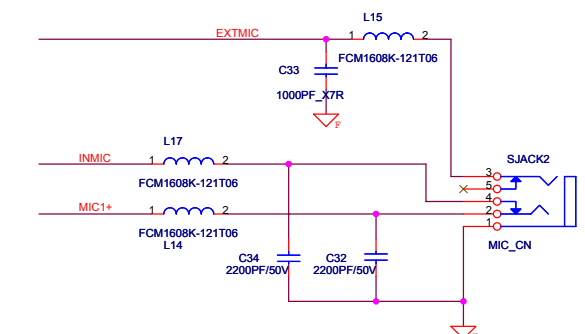
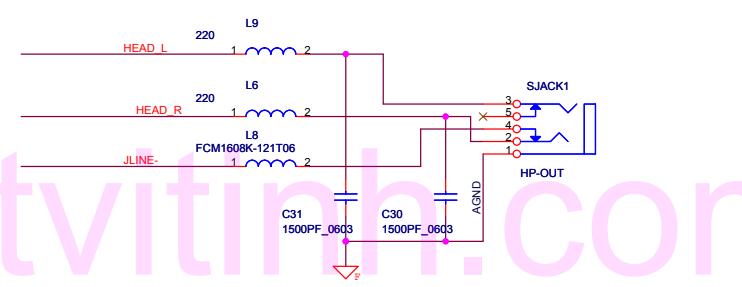
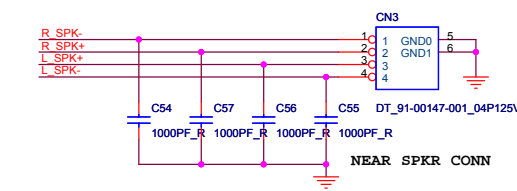
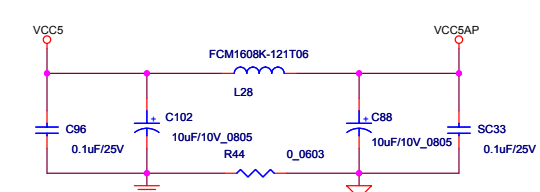
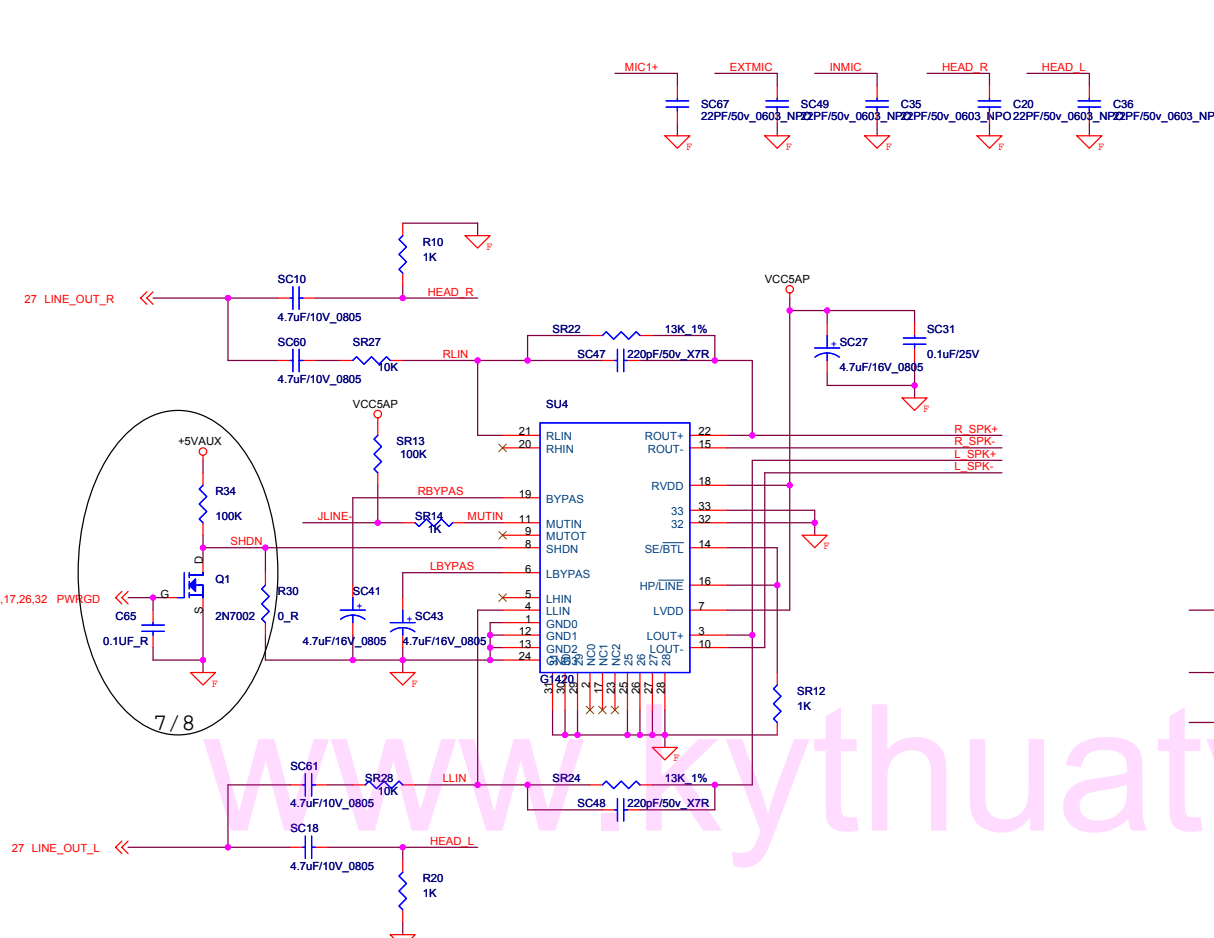
For ALC655:
 Add: SC462, SC463, C?, SC465, SR321
 Remove: SR216, R132, R147, SC278, SC298



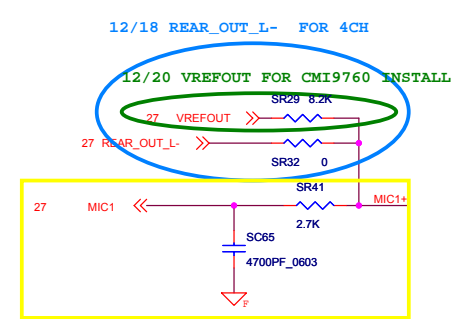
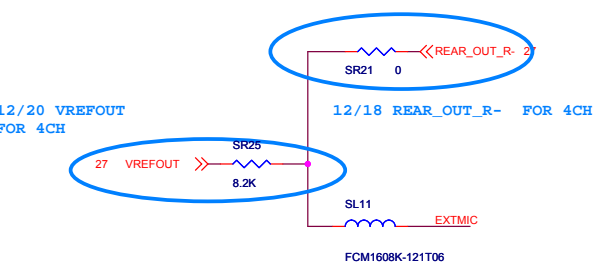
EMI 0121

Elitegroup Computer Systems		
Title AUDIO CODEC		
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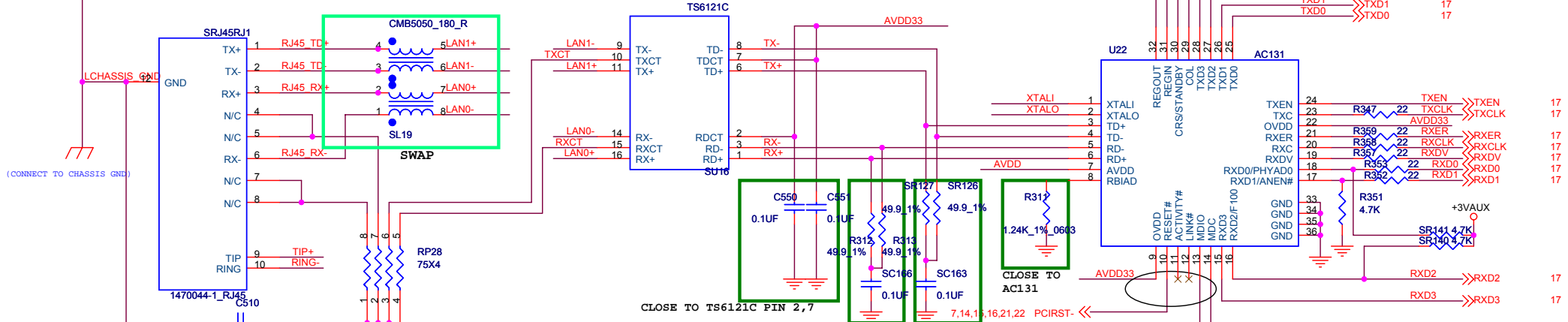
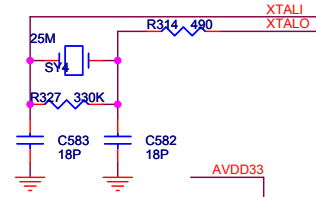
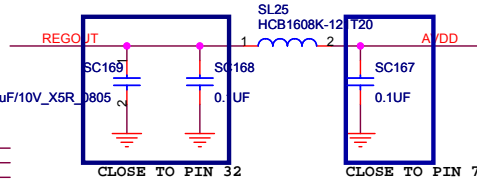
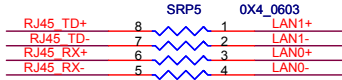
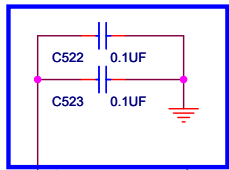


PC2001 SPEC. 12KHz--15KHz
 $F_c = 1 / [2 * 3.14 * R(2.7K) * C(4700PF)] = 12.548KHz$
 VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION



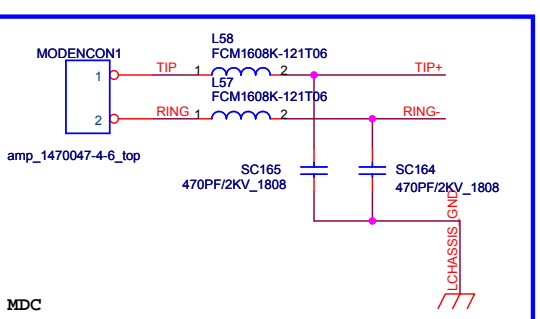
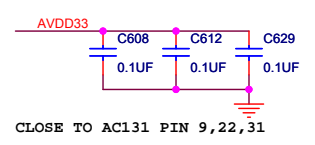
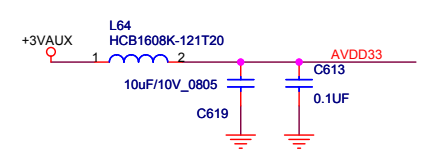
footprint modify 0402

Elitegroup Computer Systems		
Title OPA & AUDIO JACK		
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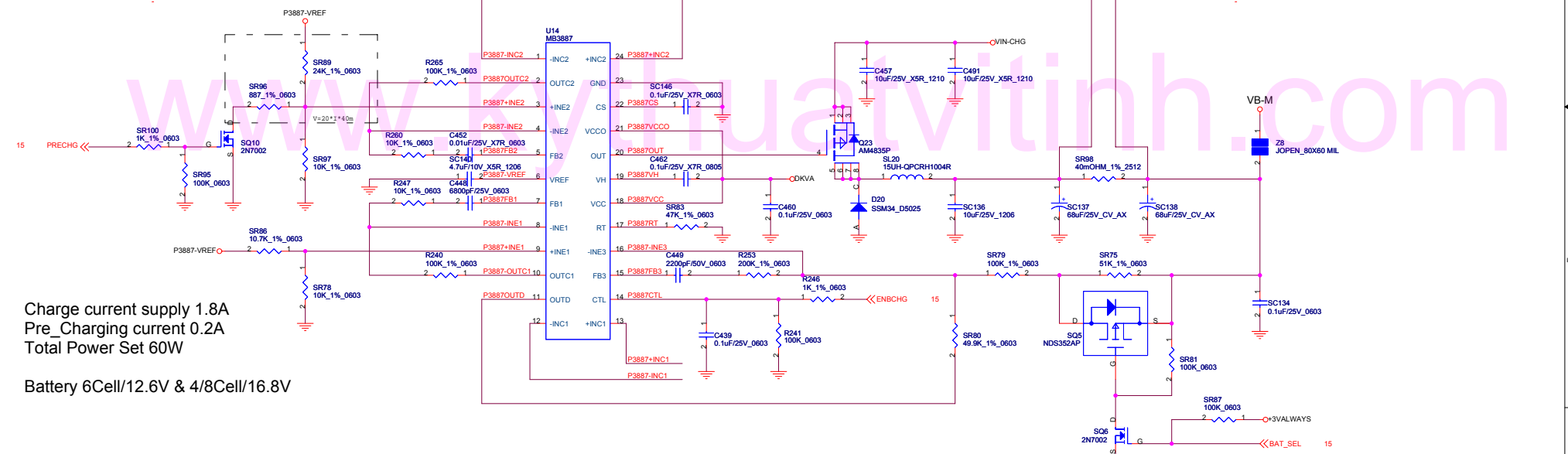
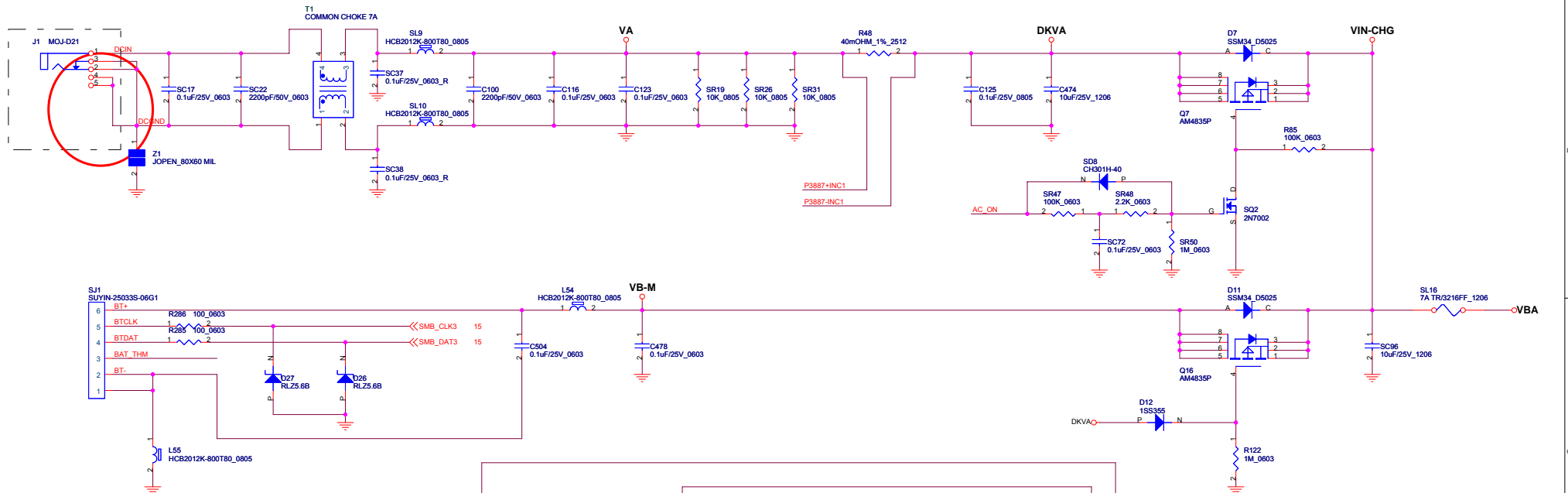


(CONNECT TO CHASSIS GND)

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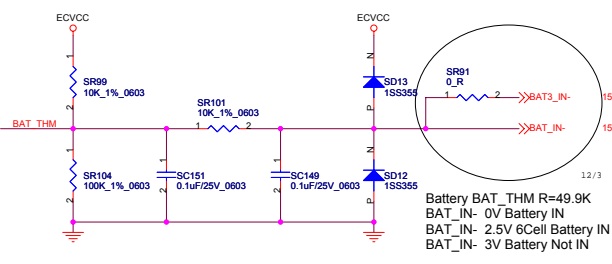
Title		
Broadcom PHY & RJ45		
Size	Document Number	Rev
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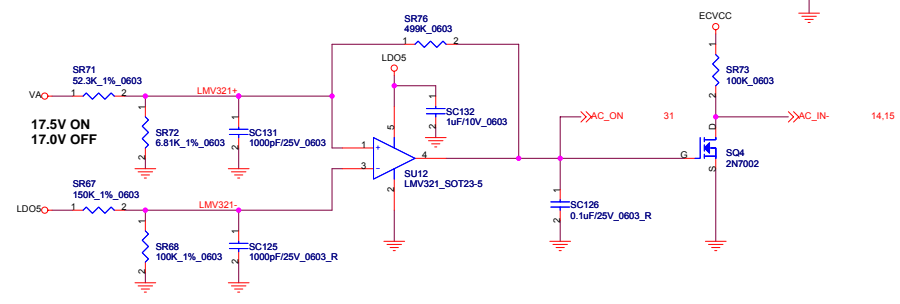
Charge current supply 1.8A
 Pre_Charging current 0.2A
 Total Power Set 60W

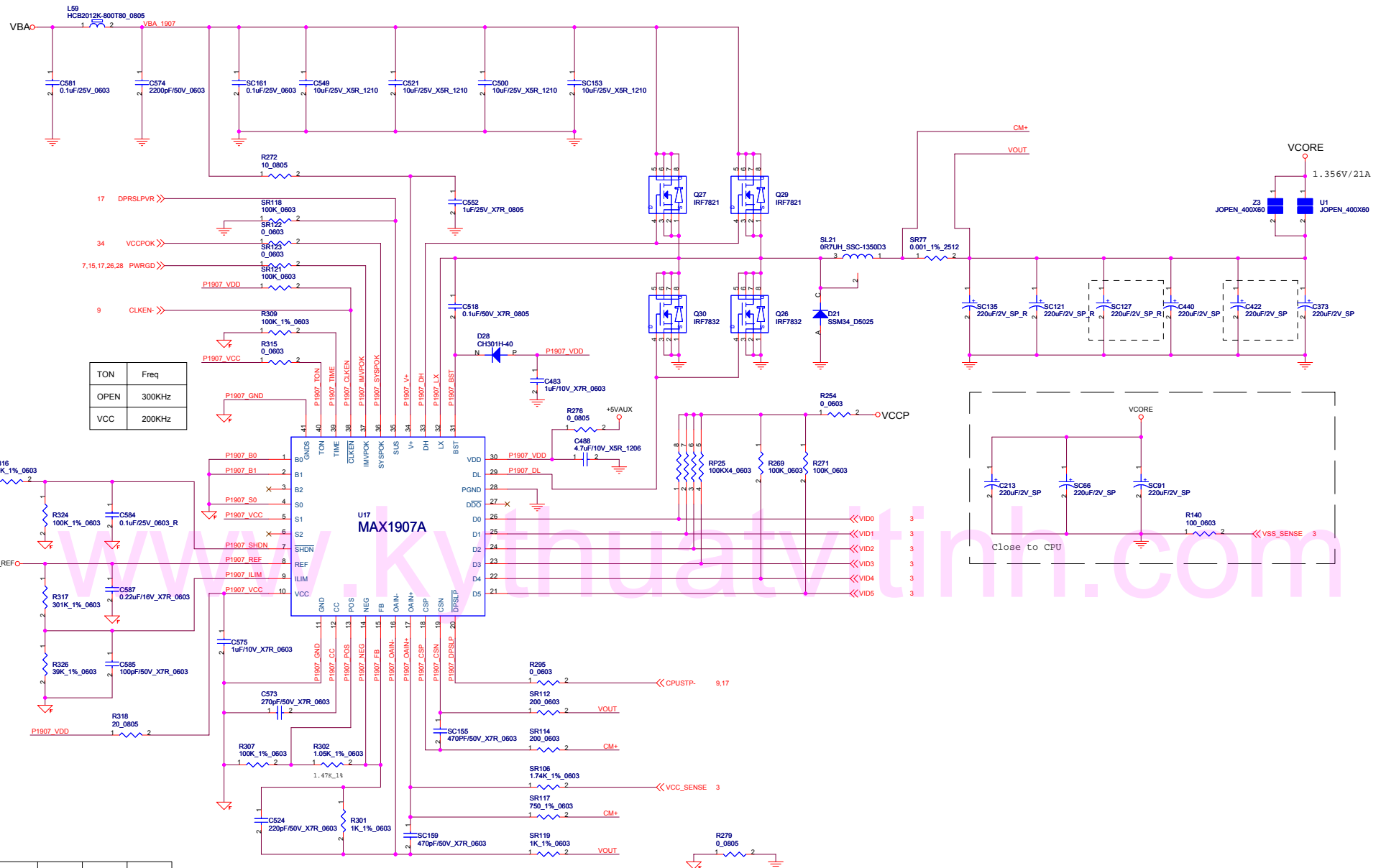
Battery 6Cell/12.6V & 4/8Cell/16.8V

BAT_SEL H->6Cell L->4Cell

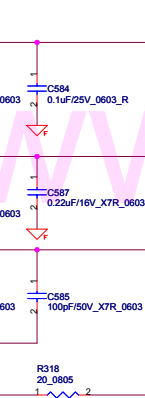


Battery BAT_THM R=49.9K
 BAT_IN- 0V Battery IN
 BAT_IN- 2.5V 6Cell Battery IN
 BAT_IN- 3V Battery Not IN

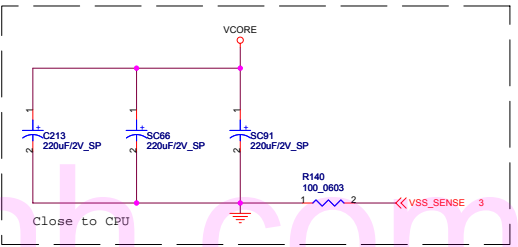




TON	Freq
OPEN	300KHz
VCC	200KHz

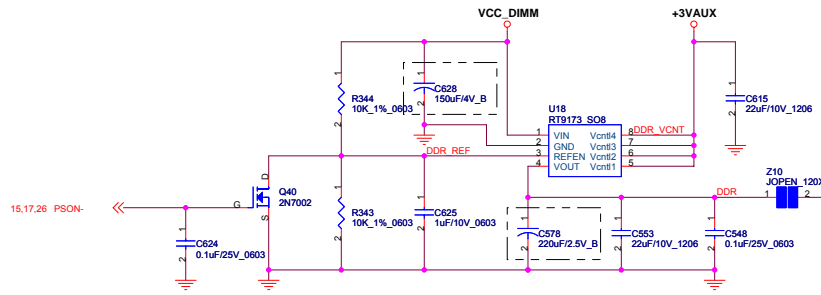
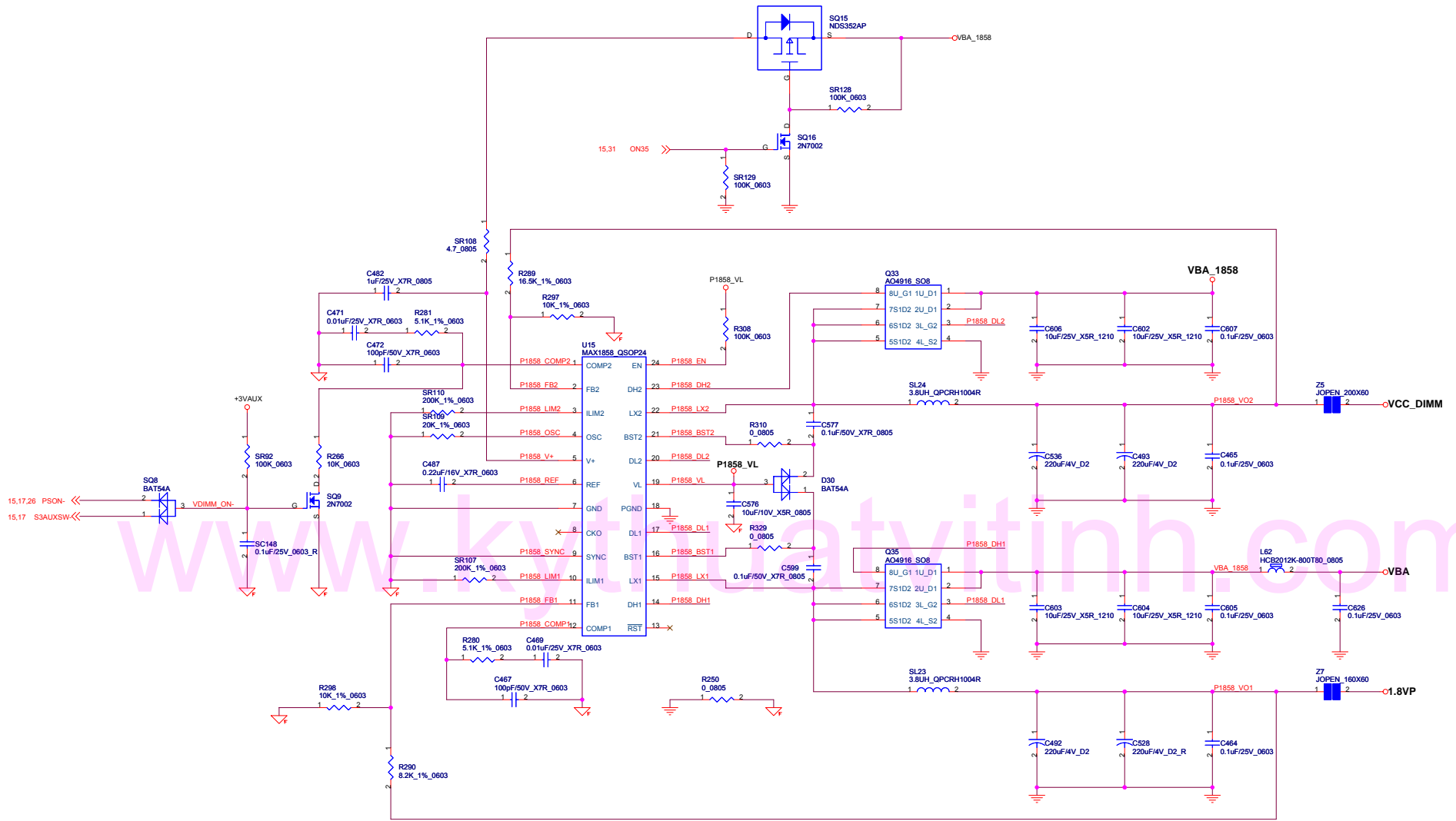


U17
MAX1907A



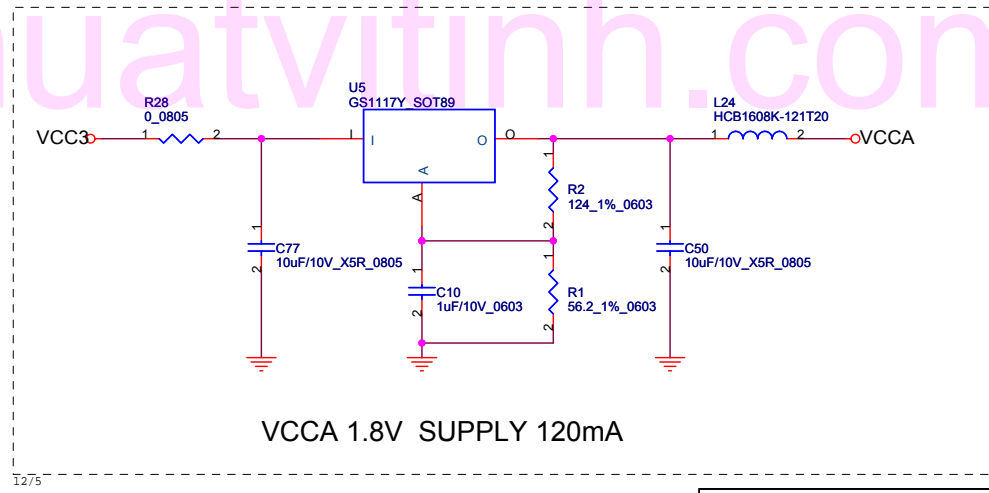
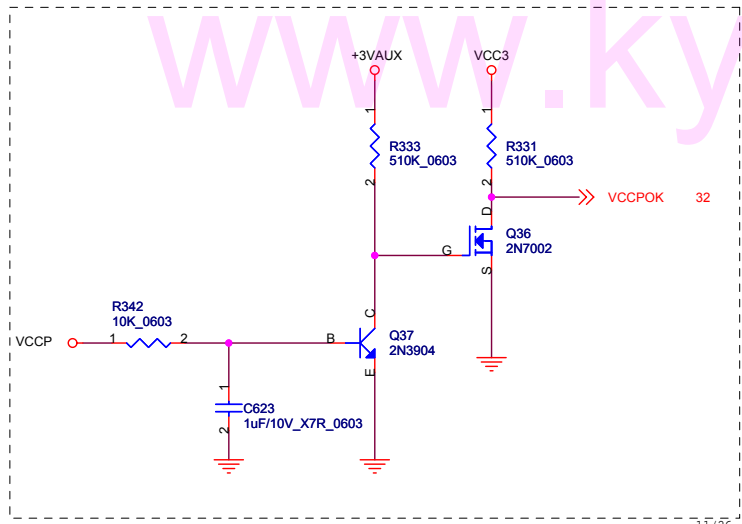
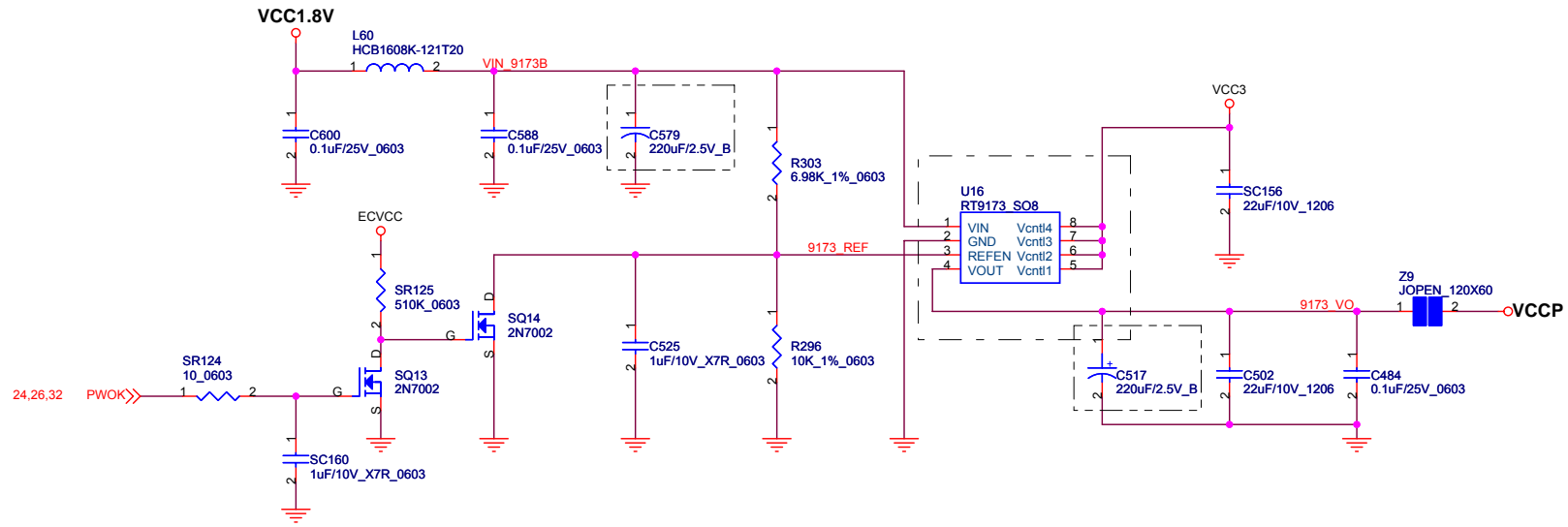
B2	B1	B0	Vout_B
REF	VCC	VCC	1.212
OPEN	GND	GND	1.196
OPEN	GND	REF	1.180

S2	S1	S0	Vout_S
OPEN	OPEN	VCC	0.764
OPEN	VCC	GND	0.748
OPEN	VCC	REF	0.732




SUPPLY DDR_VTT
1.25V/0.5A

ES ELITEGROUP		
Title SYSTEM MAX1858 1.8VP/ VCC_DIMM		
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ES ELITEGROUP		
Title		
VCCP / VCCPOK / VCCA		
Size	Document Number	Rev
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Date:	Wednesday, February 02, 2005	Sheet 34 of 35

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		Elitegroup Computer Systems	
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