

945G-M3

Rev: 1.0B Page Title of Schematic :

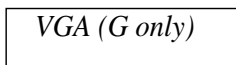
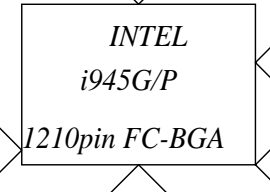
Schematics Version History Table :

Circuit Ver.	PCB Ver.	Total Page	Modified Page(s)	Date
A	A	36		02/24/ 05
1.0	1.0	36		04/01/ 05
1.0a	1.0a	36		05/10/ 05
1.0B	1.0B	36	24	06/14/ 05

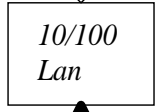
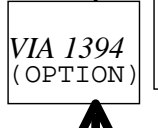
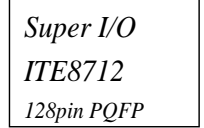
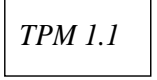
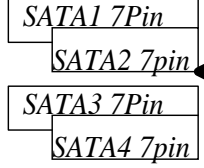
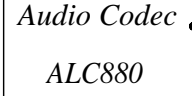
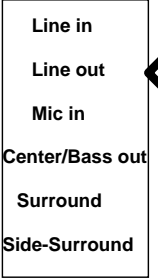
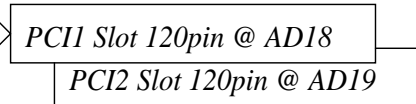
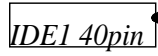
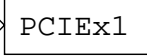
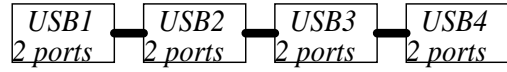
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LAN	28		
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PCI Slot 1&2	31		
PCIEX1	32		
Back I/O	33		
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DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	18	D/E/F/G	PREQ-1	PGNT-1
PCI2	19	E/F/G/H	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz
 BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz
 BW : 8.5GB/s @ FSB : 1066MHz & Freq : 266MHz



Analog Display
 RAMDAC: 400MHz
 Resolutions Up To 2048x1536@75Hz

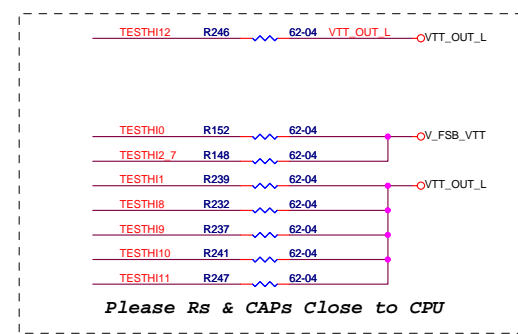
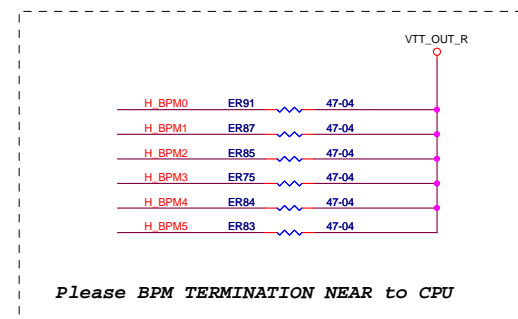
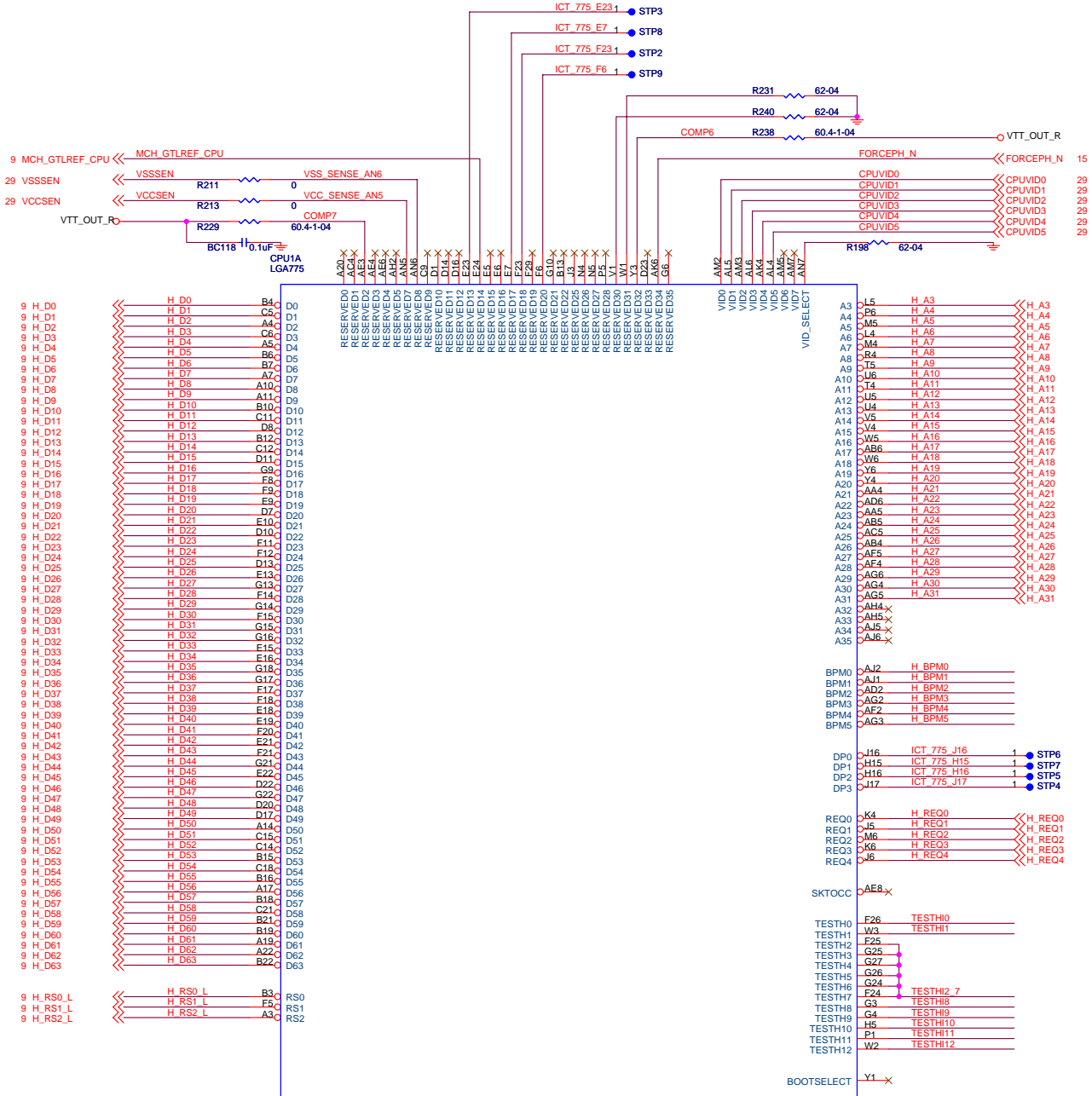


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Title: **System Block Diagram**

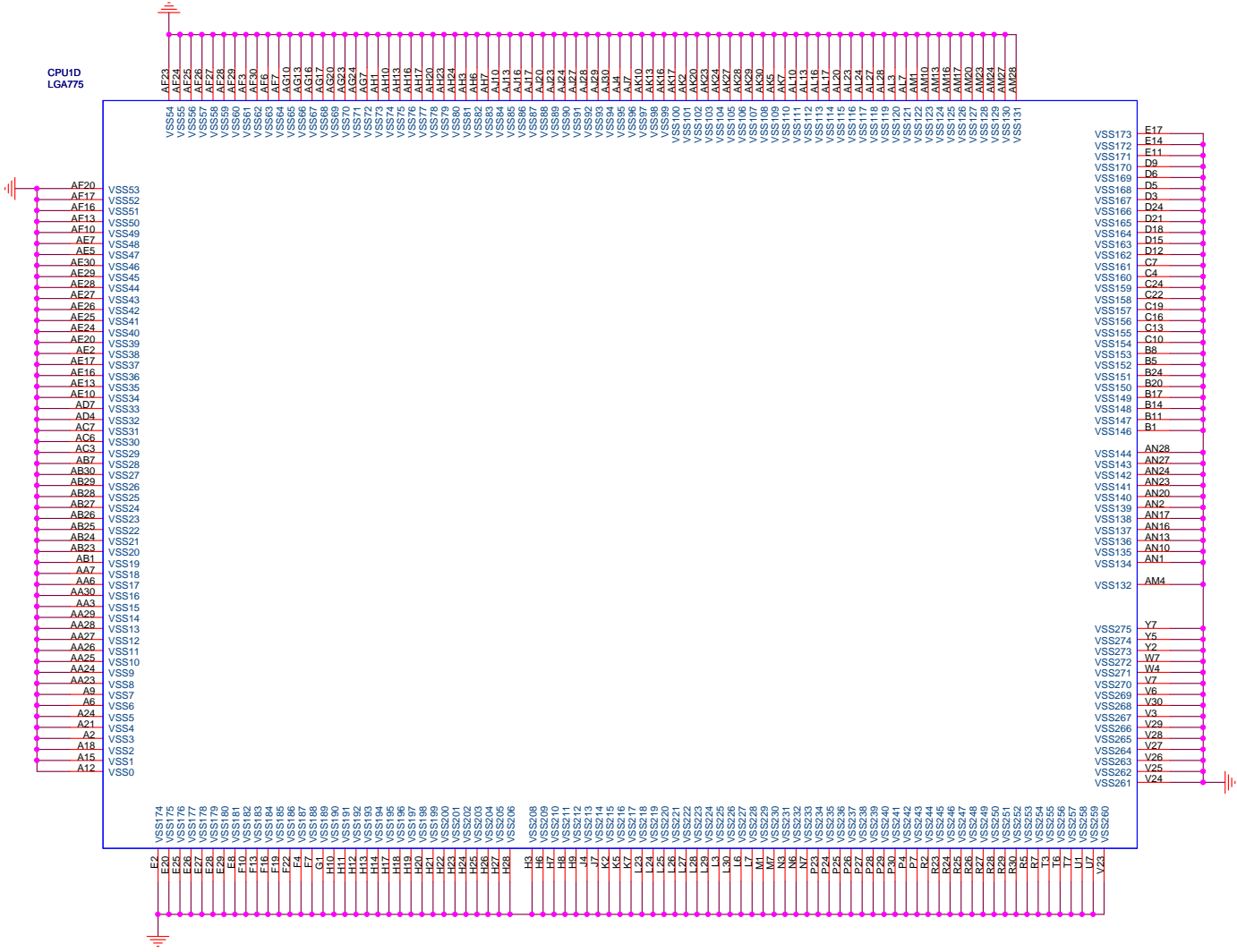
Size: Document Number **945G-M3** Rev **1.0B**

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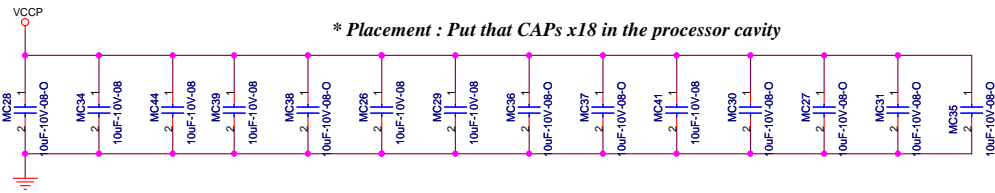
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 Title **P4 LGA775P Part A**
 Size Document Number **945G-M3** Rev **1.08**
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CPUID
LGA775



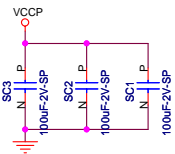
- VSS173 E17
- VSS172 E14
- VSS171 E11
- VSS170 D9
- VSS169 D6
- VSS168 D3
- VSS166 D24
- VSS165 D21
- VSS164 D18
- VSS163 D15
- VSS162 D12
- VSS161 C7
- VSS160 C4
- VSS159 C24
- VSS158 C22
- VSS157 C19
- VSS156 C16
- VSS155 C10
- VSS154 C13
- VSS153 B8
- VSS152 B5
- VSS151 B24
- VSS150 B20
- VSS149 B17
- VSS148 B14
- VSS147 B11
- VSS146 B1
- VSS144 AN28
- VSS143 AN27
- VSS142 AN24
- VSS141 AN23
- VSS140 AN20
- VSS139 AN2
- VSS138 AN17
- VSS137 AN16
- VSS136 AN13
- VSS135 AN10
- VSS134 AN1
- VSS132 AM4
- VSS275 Y7
- VSS274 Y5
- VSS273 Y2
- VSS272 W7
- VSS271 W4
- VSS270 W7
- VSS269 V6
- VSS268 V30
- VSS267 V3
- VSS266 V29
- VSS265 V28
- VSS264 V27
- VSS263 V26
- VSS262 V25
- VSS261 V24

P4 LGA775P Part D		
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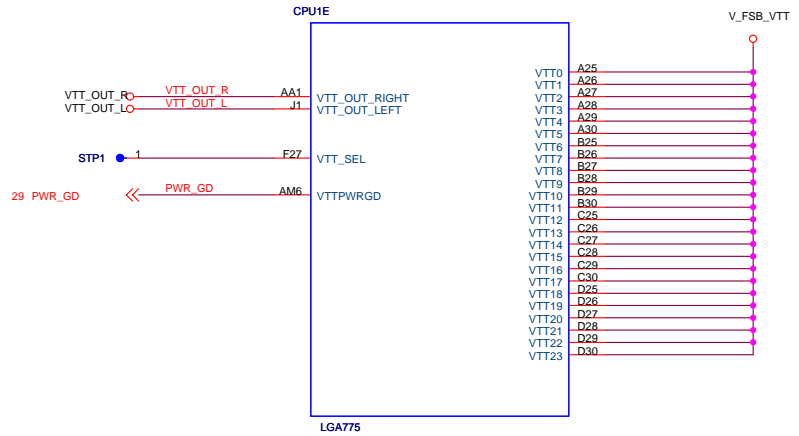


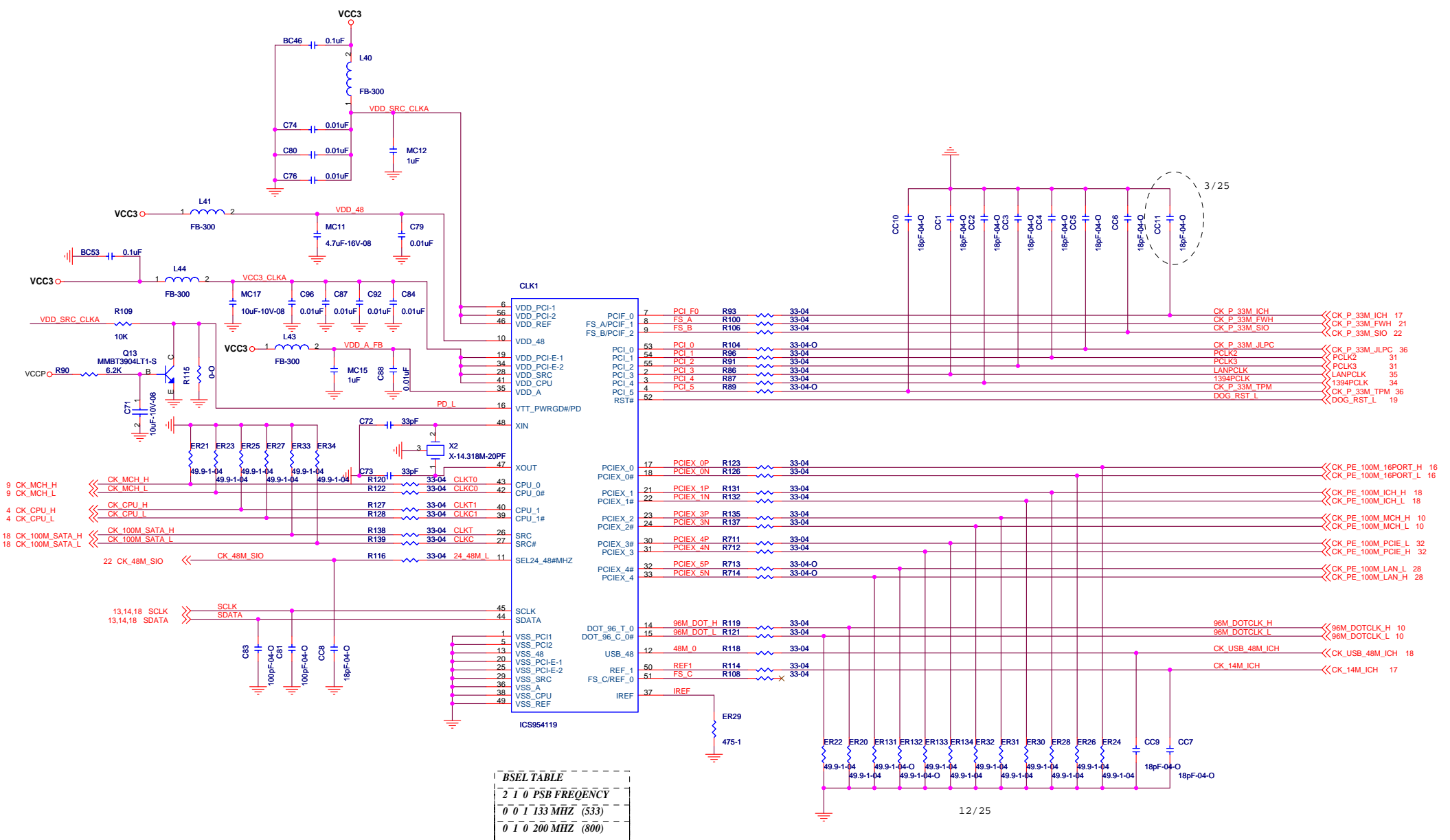
* Placement : Put that CAPs x18 in the processor cavity

* Placement : Put that CAPs x2 on solder side



VTT_SEL=0 for the Tejas processor





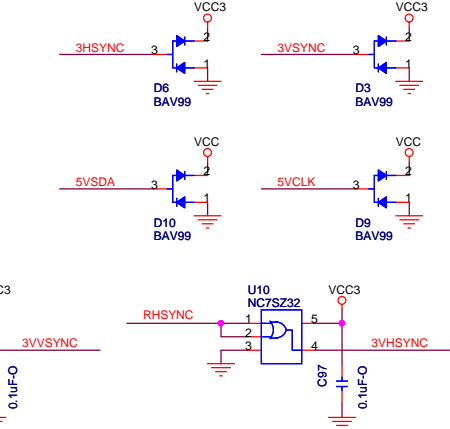
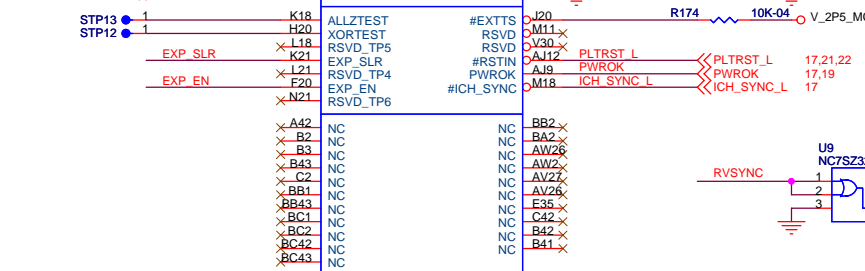
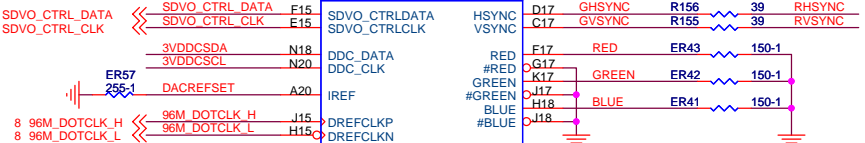
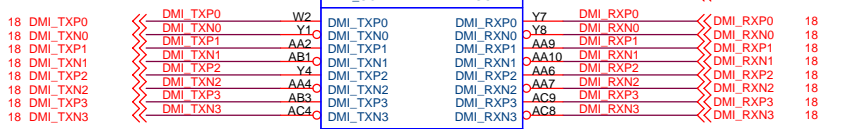
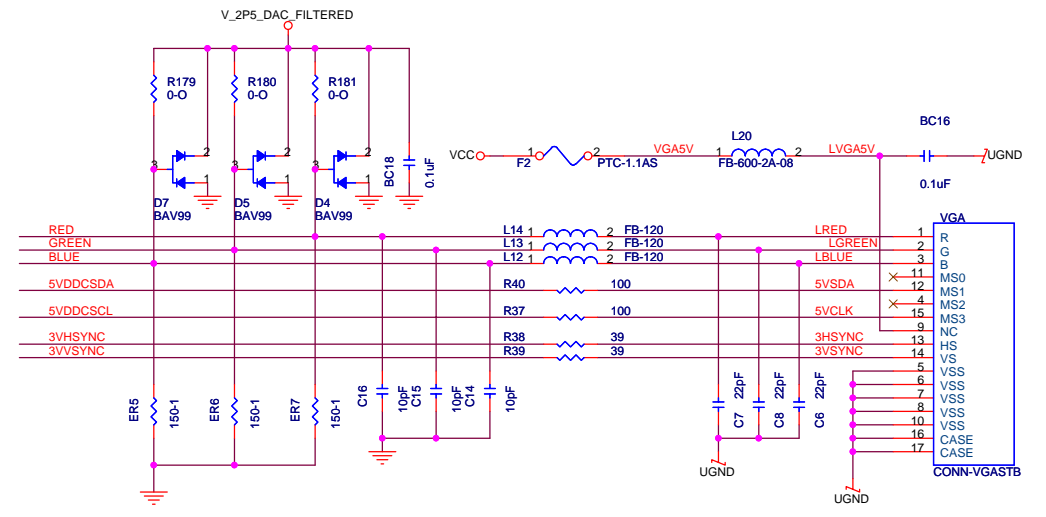
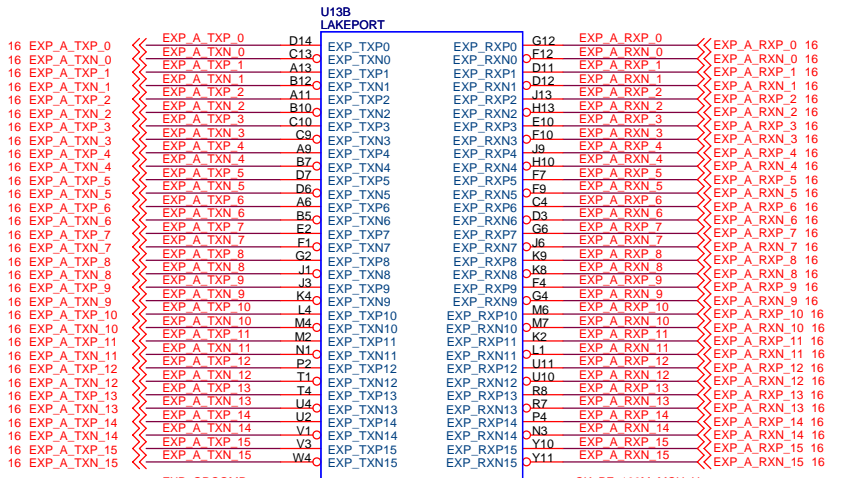
- FS_C R107 10K-04 H FSBSEL2 <<H_FSBSEL2 4.9
- FS_B R112 10K-04 H FSBSEL1 <<H_FSBSEL1 4.9
- FS_A R99 10K-04 H FSBSEL0 <<H_FSBSEL0 4.9

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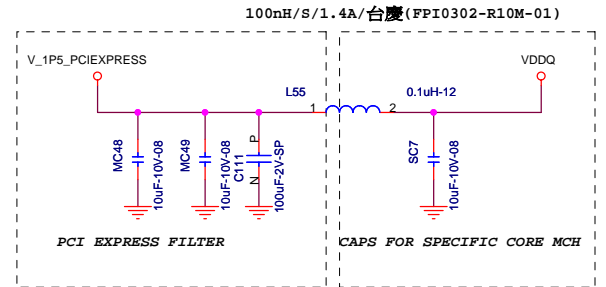
Title: **Clock Generator(CK410)**

Size: Custom Document Number **945G-M3** Rev **1.0B**

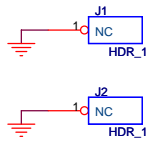
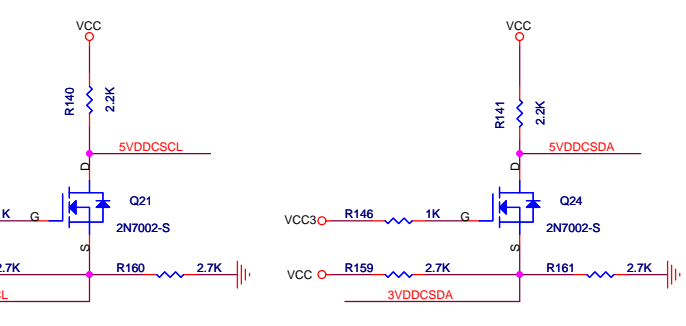
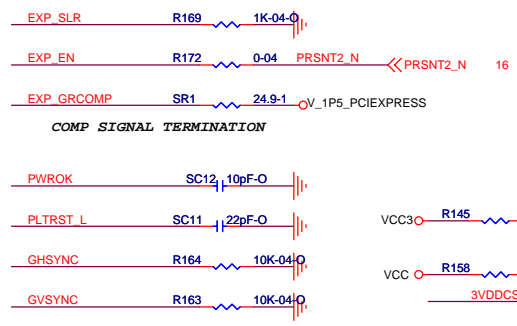
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Place close to GMCH 750mil.



The LC filter is required to source 1.4A of current with less than 30mV of drop across the filter.

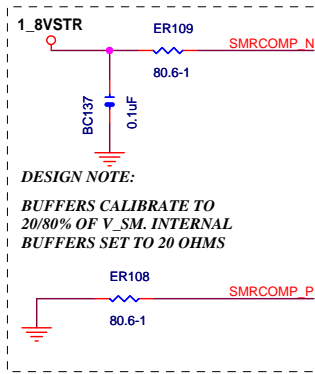
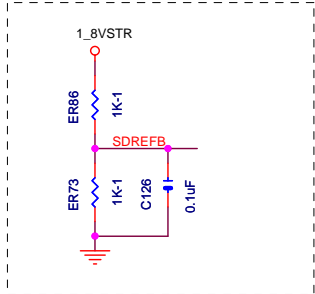
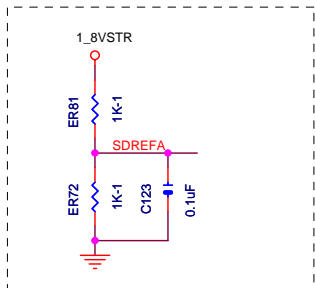


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Title: **I-LP(MCH)Part B**

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DESIGN NOTE:
BUFFERS CALIBRATE TO 20/80% OF V_{SM}. INTERNAL BUFFERS SET TO 20 OHMS

U13C LAKEPORT

DOS_H_A4	AU35	SDQS_A0	AU4	DOS_H_A0	SDQS_B4	AM8	DOS_H_B0
DOS_L_A4	AV35	#SDQS_A0	AR2	DOS_L_A0	#SDQS_B4	AM6	DOS_L_B0
MPD_A4	AT34	SDM_A4	AR3	MPD_A0	SDM_B4	AL11	MPD_B0
MD_A32	AP32	SDQ_A32	AP3	MD_A0	SDQ_B0	AL6	MD_B0
MD_A33	AV34	SDQ_A33	AP2	MD_A1	SDQ_B1	AL8	MD_B1
MD_A34	AV38	SDQ_A34	AU3	MD_A2	SDQ_B2	AP8	MD_B2
MD_A35	AU39	SDQ_A35	AV4	MD_A3	SDQ_B3	AP9	MD_B3
MD_A36	AV32	SDQ_A36	AN1	MD_A4	SDQ_B4	AL11	MD_B4
MD_A37	AT32	SDQ_A37	AP4	MD_A5	SDQ_B5	AL9	MD_B5
MD_A38	AR34	SDQ_A38	AU5	MD_A6	SDQ_B6	AM10	MD_B6
MD_A39	AU37	SDQ_A39	AU2	MD_A7	SDQ_B7	AP6	MD_B7
DOS_H_A5	AP42	SDQS_A5	BA3	DOS_H_A1	SDQS_B5	AV7	DOS_H_B1
DOS_L_A5	AP40	#SDQS_A5	BY2	DOS_L_A1	#SDQS_B5	AR9	DOS_L_B1
MPD_A5	AP39	SDM_A5	AB4	MPD_A1	SDM_B5	AW7	MPD_B1
MD_A40	AR41	SDQ_A40	AW3	MD_A8	SDQ_B40	AV7	MD_B8
MD_A41	AR42	SDQ_A41	A3	MD_A9	SDQ_B41	AU6	MD_B9
MD_A42	AN43	SDQ_A42	BA7	MD_A10	SDQ_B42	AV12	MD_B10
MD_A43	AM40	SDQ_A43	BB7	MD_A11	SDQ_B43	AM11	MD_B11
MD_A44	AU41	SDQ_A44	AV1	MD_A12	SDQ_B44	AR5	MD_B12
MD_A45	AU42	SDQ_A45	AW4	MD_A13	SDQ_B45	AR7	MD_B13
MD_A46	AP41	SDQ_A46	BC6	MD_A14	SDQ_B46	AR12	MD_B14
MD_A47	AN40	SDQ_A47	AY7	MD_A15	SDQ_B47	AR10	MD_B15
DOS_H_A6	AC42	SDQS_A6	AY11	DOS_H_A2	SDQS_B6	AV13	DOS_H_B2
DOS_L_A6	AG41	#SDQS_A6	BA10	DOS_L_A2	#SDQS_B6	AT13	DOS_L_B2
MPD_A6	AG40	SDM_A6	BB10	MPD_A2	SDM_B6	AP13	MPD_B2
MD_A48	AL41	SDQ_A48	AW12	MD_A16	SDQ_B48	AM15	MD_B16
MD_A49	AL42	SDQ_A49	AY10	MD_A17	SDQ_B49	AM13	MD_B17
MD_A50	AF39	SDQ_A50	BA12	MD_A18	SDQ_B50	AV15	MD_B18
MD_A51	AE40	SDQ_A51	BB12	MD_A19	SDQ_B51	AM17	MD_B19
MD_A52	AM41	SDQ_A52	BA9	MD_A20	SDQ_B52	AN12	MD_B20
MD_A53	AM42	SDQ_A53	BB9	MD_A21	SDQ_B53	AR13	MD_B21
MD_A54	AF41	SDQ_A54	BC11	MD_A22	SDQ_B54	AP15	MD_B22
MD_A55	AF42	SDQ_A55	AY12	MD_A23	SDQ_B55	AT15	MD_B23
DOS_H_A7	AC42	SDQS_A7	AU18	DOS_H_A3	SDQS_B7	AU23	DOS_H_B3
DOS_L_A7	AG41	#SDQS_A7	AB18	DOS_L_A3	#SDQS_B7	AP23	DOS_L_B3
MPD_A7	AC40	SDM_A7	AP18	MPD_A3	SDM_B7	AP23	MPD_B3
MD_A56	AD40	SDQ_A56	AM20	MD_A24	SDQ_B56	AM24	MD_B24
MD_A57	AD43	SDQ_A57	AM18	MD_A25	SDQ_B57	AM23	MD_B25
MD_A58	AA39	SDQ_A58	AV20	MD_A26	SDQ_B58	AV24	MD_B26
MD_A59	AA40	SDQ_A59	AM21	MD_A27	SDQ_B59	AM26	MD_B27
MD_A60	AE42	SDQ_A60	AP17	MD_A28	SDQ_B60	AP21	MD_B28
MD_A61	AE41	SDQ_A61	AR17	MD_A29	SDQ_B61	AR21	MD_B29
MD_A62	AB41	SDQ_A62	AP20	MD_A30	SDQ_B62	AP24	MD_B30
MD_A63	AB42	SDQ_A63	AT20	MD_A31	SDQ_B63	AT24	MD_B31
MAAA_0	BA32	SMA_A0	BB35	SWE_L_A	SMA_B0	BB23	SWE_L_B
MAAA_1	AW32	SMA_A1	BA37	SCAS_L_A	SMA_B1	AY24	SCAS_L_B
MAAA_2	BB30	SMA_A2	BA34	SRAS_L_A	SMA_B2	BA23	SRAS_L_B
MAAA_3	BA30	SMA_A3			SMA_B3		
MAAA_4	AY30	SMA_A4	BC33	SBSA_0	SMA_B4	AW23	SBSB_0
MAAA_5	BA27	SMA_A5	AY34	SBSA_1	SMA_B5	AY23	SBSB_1
MAAA_6	BC28	SMA_A6	BA26	SBSA_2	SMA_B6	AY17	SBSB_2
MAAA_7	AY27	SMA_A7			SMA_B7		
MAAA_8	AY28	SMA_A8	BB37	CSA_L_0	SMA_B8	BA40	CSB_L_0
MAAA_9	BB27	SMA_A9	BA39	CSA_L_1	SMA_B9	AW41	CSB_L_1
MAAA_10	AY33	SMA_A10	BA35		SMA_B10	BA41	
MAAA_11	AW27	SMA_A11	AY38		SMA_B11	AW40	
MAAA_12	BB26	SMA_A12			SMA_B12		
MAAA_13	BC38	SMA_A13	BB25	CKEA_0	SMA_B13	BA14	CKEB_0
			AY25	CKEA_1		AY16	CKEB_1
DCLKA_H0	BB32	SCLK_A0	BC24		SCLK_B0	BA13	
DCLKA_L0	AY32	#SCLK_A0	BA25		#SCLK_B0	BB13	
DCLKA_H1	AY5	SCLK_A1			SCLK_B1		
DCLKA_L1	BB5	#SCLK_A1	AW37	ODTA_0	#SCLK_B1	AY42	ODTB_0
DCLKA_H2	AK42	SCLK_A2	AY39	ODTA_1	SCLK_B2	AV40	ODTB_1
DCLKA_L2	AK41	#SCLK_A2	AL36		#SCLK_B2	AV43	
	BA31	SCLK_A3	BB40		SCLK_B3	AU40	
	BB31	#SCLK_A3			#SCLK_B3		
	AY6	SCLK_A4	BC16		SCLK_B4		
	BA5	#SCLK_A4	AY14		SCLK_B5		
	AH40	SCLK_A5	AW17		#SCLK_B5		
	AH43	#SCLK_A5	AW18				
STP22	1	AL17	AK40		RSVD_TP3	AL39	
STP21	1	AK17	AK23		RSVD_TP2	AM2	SDREFB
		SVREF0	AM4	SDREFA	SVREF1		

U13D LAKEPORT

DOS_H_B4	AT29	SDQS_B4	SDQS_B4	AM8	DOS_H_B0
DOS_L_B4	AV29	#SDQS_B4	#SDQS_B4	AM6	DOS_L_B0
MPD_B4	AR29	SDM_B4	SDM_B4	AL11	MPD_B0
MD_B32	AU27	SDQ_B32	SDQ_B0	AL6	MD_B0
MD_B33	AN29	SDQ_B33	SDQ_B1	AL8	MD_B1
MD_B34	AR31	SDQ_B34	SDQ_B2	AP8	MD_B2
MD_B35	AM31	SDQ_B35	SDQ_B3	AP9	MD_B3
MD_B36	AP27	SDQ_B36	SDQ_B4	AL11	MD_B4
MD_B37	AR27	SDQ_B37	SDQ_B5	AL9	MD_B5
MD_B38	AP31	SDQ_B38	SDQ_B6	AM10	MD_B6
MD_B39	AU31	SDQ_B39	SDQ_B7	AP6	MD_B7
DOS_H_B5	AP36	SDQS_B5	SDQS_B5	AV7	DOS_H_B1
DOS_L_B5	AM35	#SDQS_B5	#SDQS_B5	AR9	DOS_L_B1
MPD_B5	AR38	SDM_B5	SDM_B5	AW7	MPD_B1
MD_B40	AP35	SDQ_B40	SDQ_B8	AV7	MD_B8
MD_B41	AP37	SDQ_B41	SDQ_B9	AU6	MD_B9
MD_B42	AN32	SDQ_B42	SDQ_B10	AV12	MD_B10
MD_B43	AL35	SDQ_B43	SDQ_B11	AM11	MD_B11
MD_B44	AR35	SDQ_B44	SDQ_B12	AR5	MD_B12
MD_B45	AU38	SDQ_B45	SDQ_B13	AR7	MD_B13
MD_B46	AM38	SDQ_B46	SDQ_B14	AR12	MD_B14
MD_B47	AM34	SDQ_B47	SDQ_B15	AR10	MD_B15
DOS_H_B6	AG34	SDQS_B6	SDQS_B6	AV13	DOS_H_B2
DOS_L_B6	AG32	#SDQS_B6	#SDQS_B6	AT13	DOS_L_B2
MPD_B6	AJ39	SDM_B6	SDM_B6	AP13	MPD_B2
MD_B48	AL34	SDQ_B48	SDQ_B16	AM15	MD_B16
MD_B49	AJ34	SDQ_B49	SDQ_B17	AM13	MD_B17
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MD_B51	AF34	SDQ_B51	SDQ_B19	AM17	MD_B19
MD_B52	AL31	SDQ_B52	SDQ_B20	AN12	MD_B20
MD_B53	AJ32	SDQ_B53	SDQ_B21	AR13	MD_B21
MD_B54	AG35	SDQ_B54	SDQ_B22	AP15	MD_B22
MD_B55	AD32	SDQ_B55	SDQ_B23	AT15	MD_B23
DOS_H_B7	AD36	SDQS_B7	SDQS_B7	AU23	DOS_H_B3
DOS_L_B7	AD38	#SDQS_B7	#SDQS_B7	AP23	DOS_L_B3
MPD_B7	AD39	SDM_B7	SDM_B7	AP23	MPD_B3
MD_B56	AC32	SDQ_B56	SDQ_B24	AM24	MD_B24
MD_B57	AD34	SDQ_B57	SDQ_B25	AM23	MD_B25
MD_B58	Y32	SDQ_B58	SDQ_B26	AV24	MD_B26
MD_B59	AA32	SDQ_B59	SDQ_B27	AM26	MD_B27
MD_B60	AF35	SDQ_B60	SDQ_B28	AP21	MD_B28
MD_B61	AF37	SDQ_B61	SDQ_B29	AR21	MD_B29
MD_B62	AC33	SDQ_B62	SDQ_B30	AP24	MD_B30
MD_B63	AC35	SDQ_B63	SDQ_B31	AT24	MD_B31
MAAB_0	BB22	SMA_B0	SMA_B0	BB23	SWE_L_B
MAAB_1	BB21	SMA_B1	SMA_B1	AY24	SCAS_L_B
MAAB_2	BA21	SMA_B2	SMA_B2	BA23	SRAS_L_B
MAAB_3	AY21	SMA_B3	SMA_B3		
MAAB_4	RC20	SMA_B4	SMA_B4	AW23	SBSB_0
MAAB_5	AY19	SMA_B5	SMA_B5	AY23	SBSB_1
MAAB_6	AY20	SMA_B6	SMA_B6	AY17	SBSB_2
MAAB_7	BA18	SMA_B7	SMA_B7		
MAAB_8	BA19	SMA_B8	SMA_B8	BA40	CSB_L_0
MAAB_9	BB18	SMA_B9	SMA_B9	AW41	CSB_L_1
MAAB_10	BA22	SMA_B10	SMA_B10	BA41	
MAAB_11	BB17	SMA_B11	SMA_B11	AW40	
MAAB_12	BA17	SMA_B12	SMA_B12		
MAAB_13	AW42	SMA_B13	SMA_B13	BA14	CKEB_0
DCLKB_H0	AM29	SCLK_B0	SCLK_B0	AY16	CKEB_1
DCLKB_L0	AM27	#SCLK_B0	#SCLK_B0	BA13	
DCLKB_H1	AV9	SCLK_B1	SCLK_B1	BB13	
DCLKB_L1	AW9	#SCLK_B1	#SCLK_B1		
DCLKB_H2	AL38	SCLK_B2	SCLK_B2	AY42	ODTB_0
DCLKB_L2	AL36	#SCLK_B2	#SCLK_B2	AV40	ODTB_1
	AP26	SCLK_B3	SCLK_B3	AU40	
	AR26	#SCLK_B3	#SCLK_B3		
	AU10	SCLK_B4	SCLK_B4		
	AT10	#SCLK_B4	#SCLK_B4		
	AJ38	SCLK_B5	SCLK_B5		
	AJ36	#SCLK_B5	#SCLK_B5		
STP20	1	AK18	RSVD_TP3	AL39	
STP19	1	AK23	RSVD_TP2	AM2	SDREFB
		SVREF1	SVREF1		

13 MD_A[0..63]	←	MD_A[0..63]
13 DQS_L_A[0..7]	←	DQS_L_A[0..7]
13 DQS_H_A[0..7]	←	DQS_H_A[0..7]
13 MPD_A[0..7]	←	MPD_A[0..7]
13 MAAA_[0..13]	←	MAAA_[0..13]
13 CSA_L[0..1]	←	CSA_L[0..1]
13 CKEA_[0..1]	←	CKEA_[0..1]
13 DCLKA_L[0..2]	←	DCLKA_L[0..2]
13 DCLKA_H[0..2]	←	DCLKA_H[0..2]
13 ODTA_[0..1]	←	ODTA_[0..1]
13 SBSA_[0..2]	←	SBSA_[0..2]
13 SWE_L_A	←	SWE_L_A
13 SCAS_L_A	←	SCAS_L_A
13 SRAS_L_A	←	SRAS_L_A

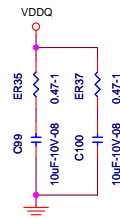
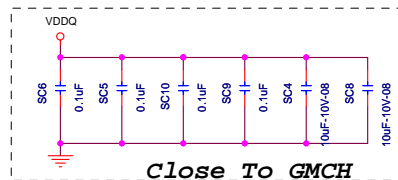
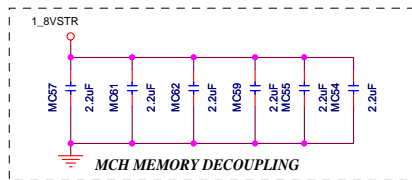
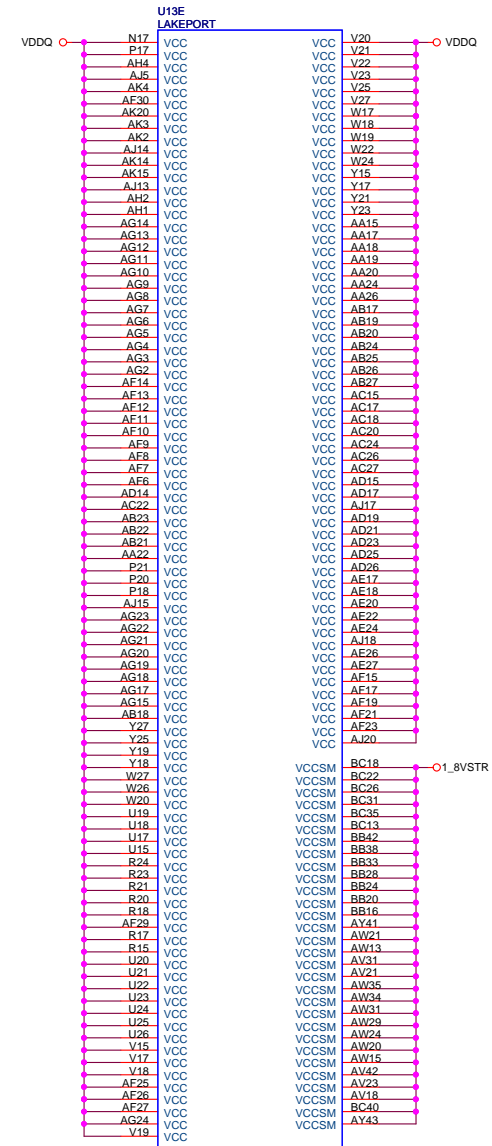
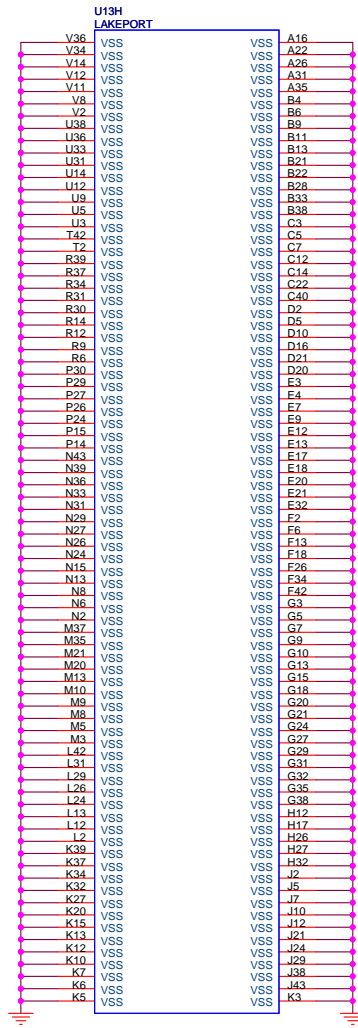
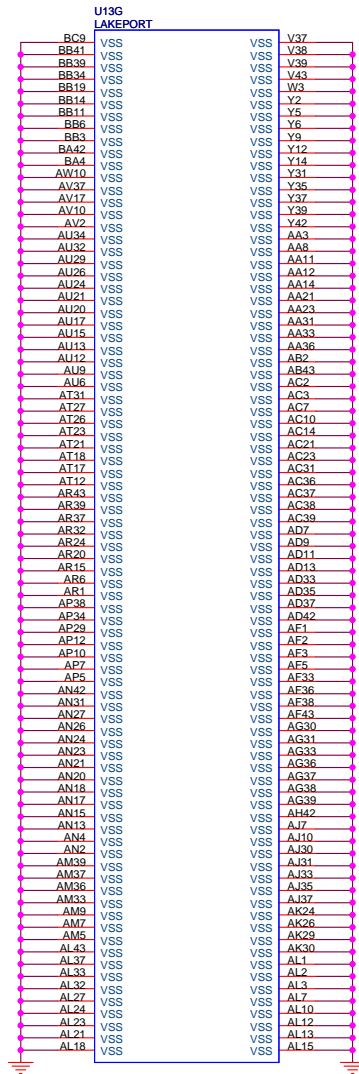
14 MD_B[0..63]	←	MD_B[0..63]
14 DQS_L_B[0..7]	←	DQS_L_B[0..7]
14 DQS_H_B[0..7]	←	DQS_H_B[0..7]
14 MPD_B[0..7]	←	MPD_B[0..7]
14 MAAB_[0..13]	←	MAAB_[0..13]
14 CSB_L[0..1]	←	CSB_L[0..1]
14 CKEB_[0..1]	←	CKEB_[0..1]
14 DCLKB_L[0..2]	←	DCLKB_L[0..2]
14 DCLKB_H[0..2]	←	DCLKB_H[0..2]
14 ODTB_[0..1]	←	ODTB_[0..1]
14 SBSB_[0..2]	←	SBSB_[0..2]
14 SWE_L_B	←	SWE_L_B
14 SCAS_L_B	←	SCAS_L_B
14 SRAS_L_B	←	SRAS_L_B

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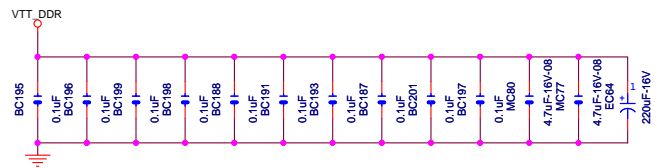
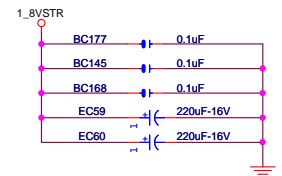
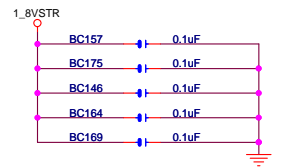
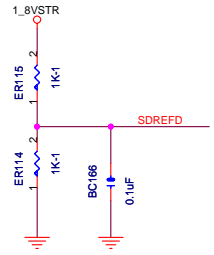
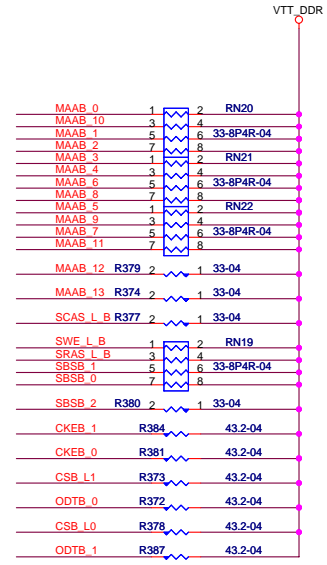
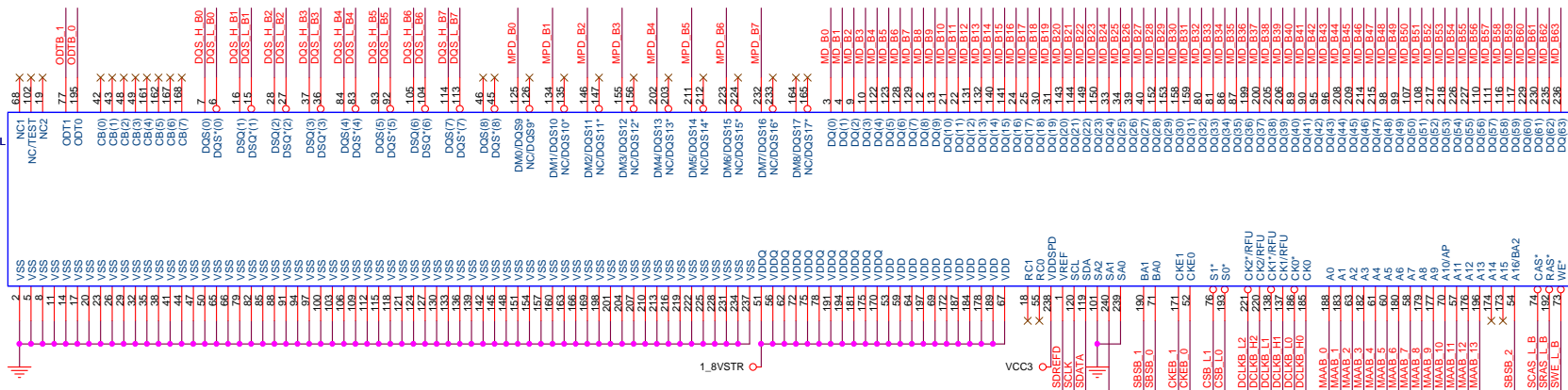
Title: **I-LP(MCH)Part C & D**

Size B Document Number: **945G-M3** Rev 1.0B

Date: Tuesday, June 14, 2005 Sheet 11 of 36



DIMM2
DDR2-BL



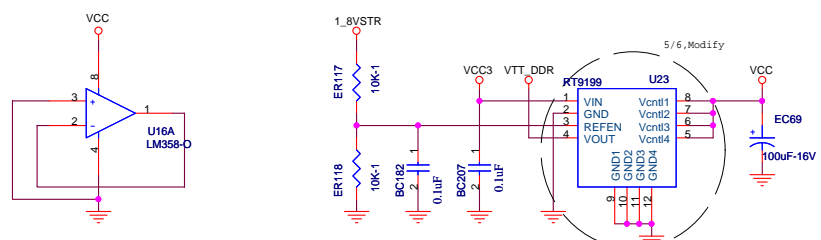
- 11 MD_B[0..63] <<< MD_B[0..63]
- 11 DQS_L_B[0..7] <<< DQS_L_B[0..7]
- 11 DQS_H_B[0..7] <<< DQS_H_B[0..7]
- 11 MPD_B[0..7] <<< MPD_B[0..7]
- 11 MAAB_[0..13] <<< MAAB_[0..13]
- 11 CSB_L_[0..1] <<< CSB_L_[0..1]
- 11 CKEB_[0..1] <<< CKEB_[0..1]
- 11 DCLKB_L_[0..2] <<< DCLKB_L_[0..2]
- 11 DCLKB_H_[0..2] <<< DCLKB_H_[0..2]
- 11 ODTB_[0..1] <<< ODTB_[0..1]
- 11 SBSB_[0..2] <<< SBSB_[0..2]
- 11 SWE_L_B <<< SWE_L_B
- 11 SCAS_L_B <<< SCAS_L_B
- 11 SRAS_L_B <<< SRAS_L_B
- 8.13.18 SDATA <<< SDATA
- 8.13.18 SCLK <<< SCLK

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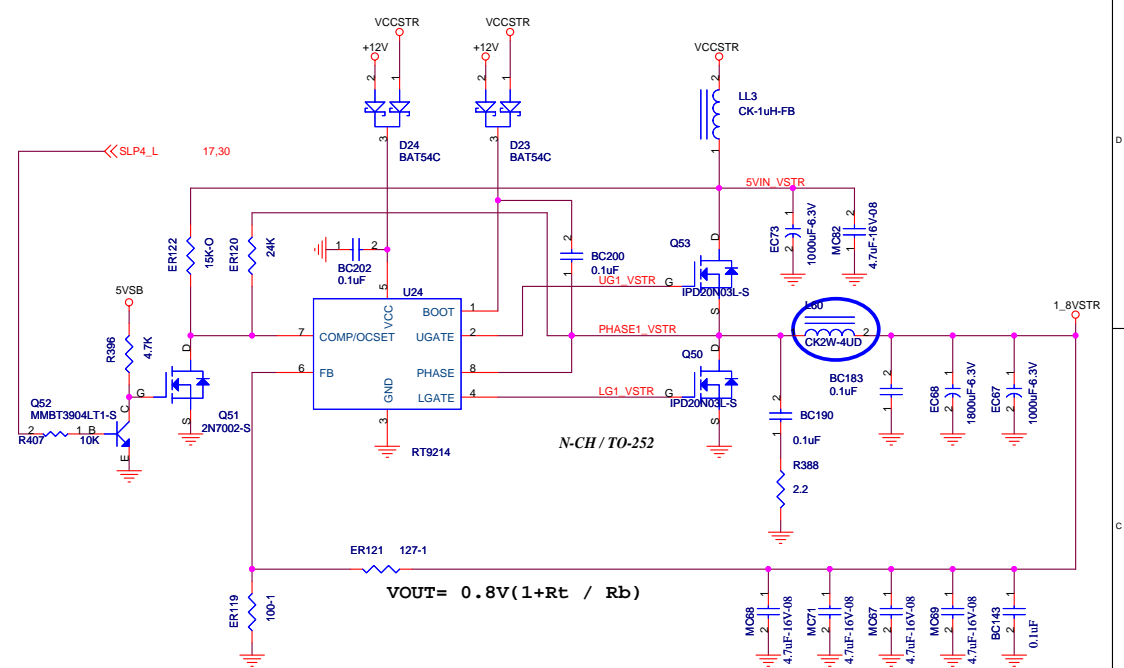
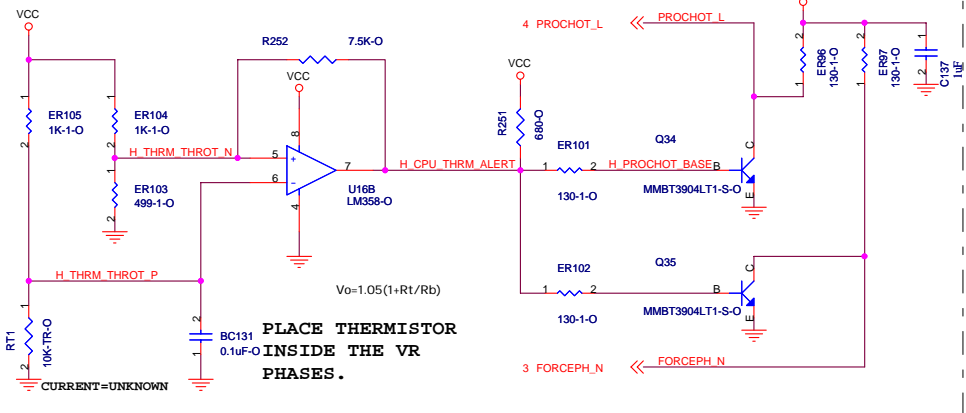
Title: **DIMM3&4 (DDR2 SDRAM)**

Size: Document Number **945G-M3** Rev **1.08**

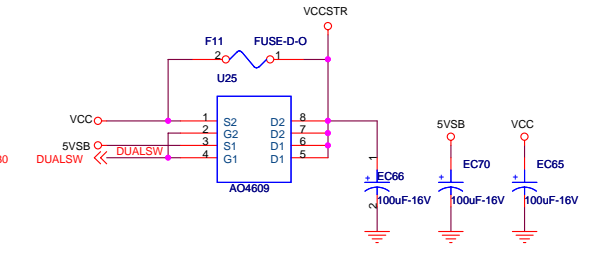
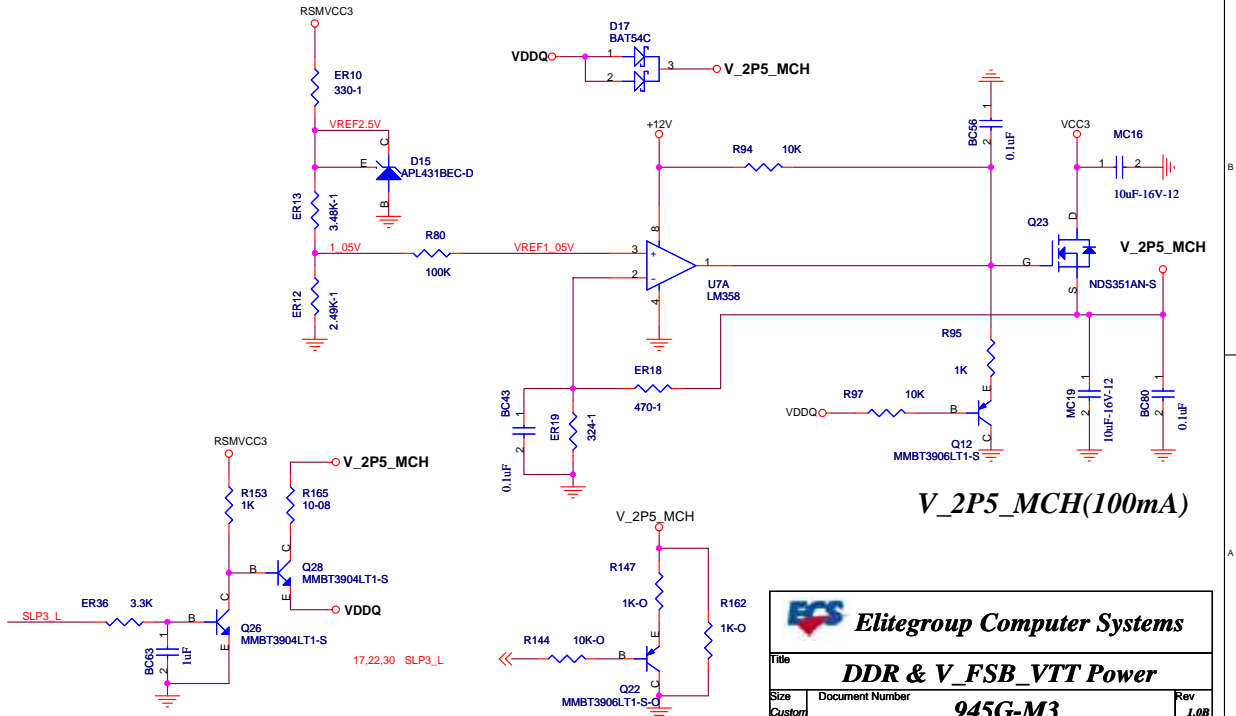
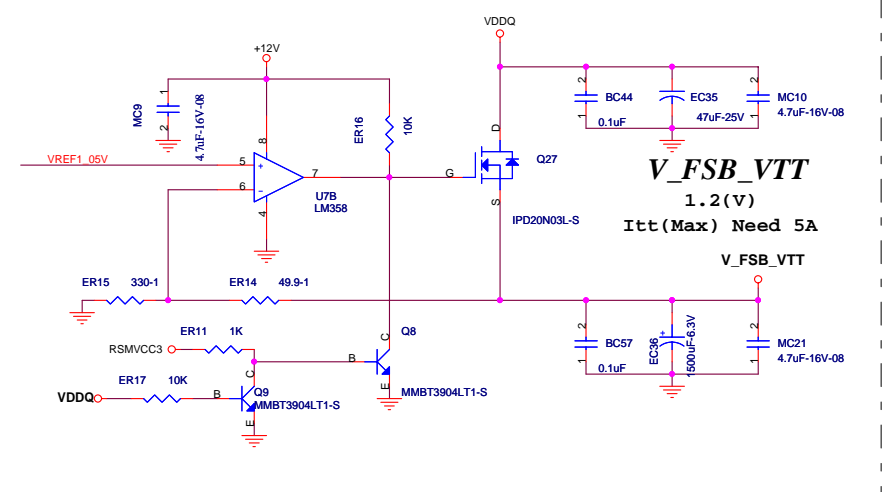
Date: Tuesday, June 14, 2005 Sheet 14 of 36

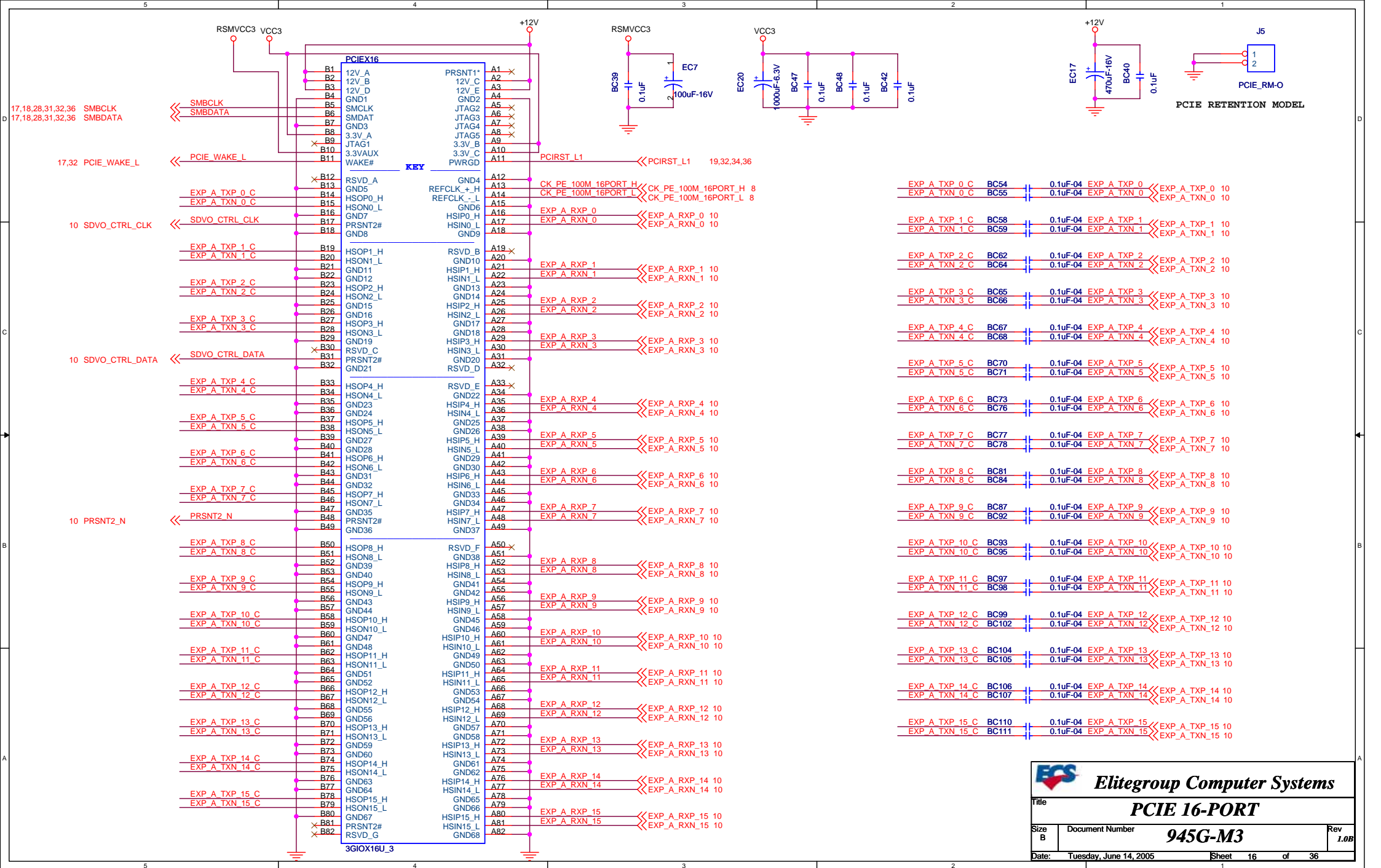


VR THERMAL THROTTLE CIRCUITRY



1.8VSTR should be able to support up to 14A





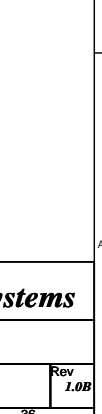
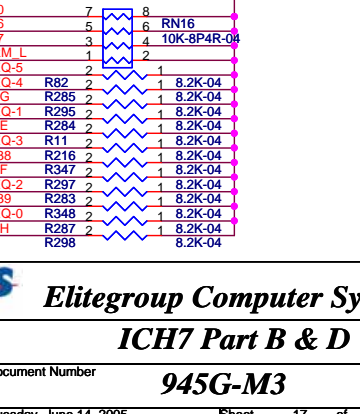
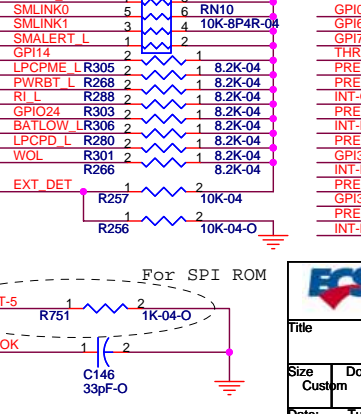
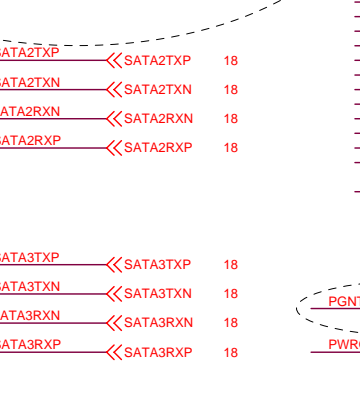
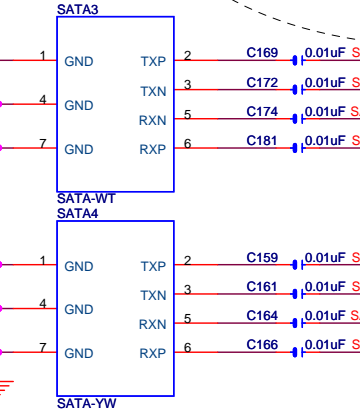
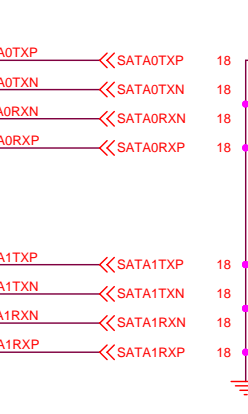
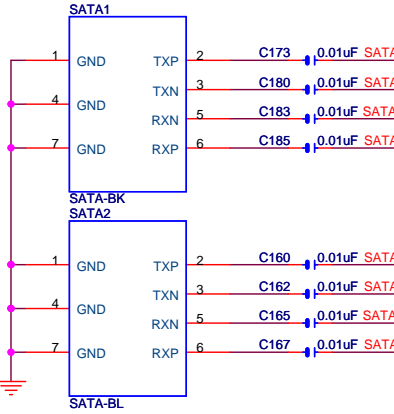
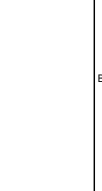
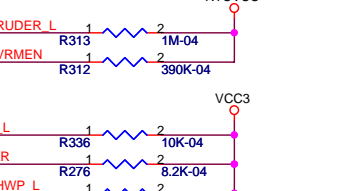
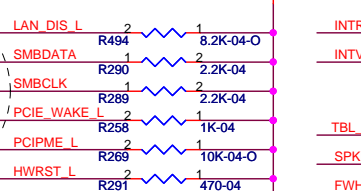
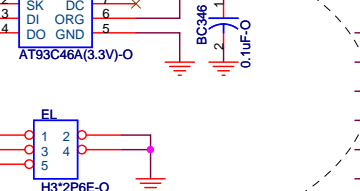
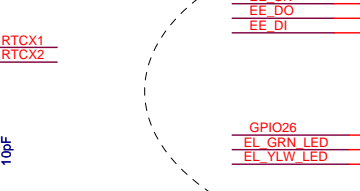
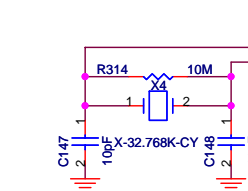
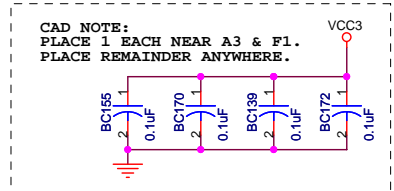
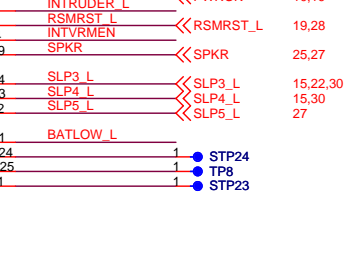
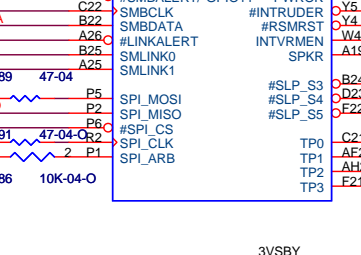
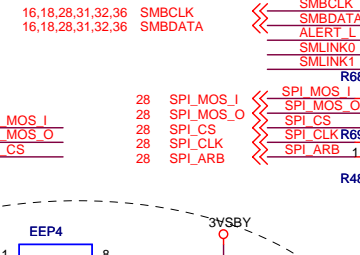
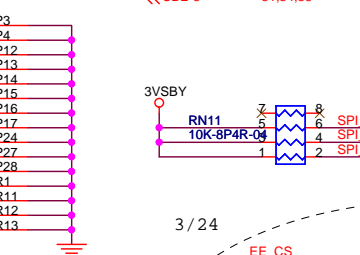
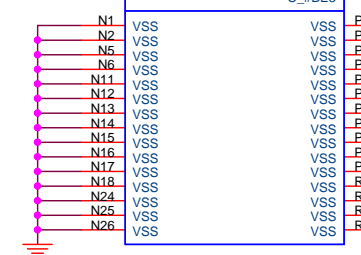
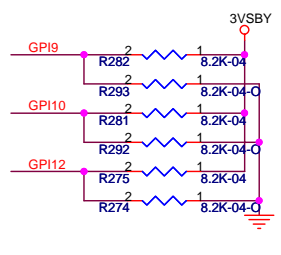
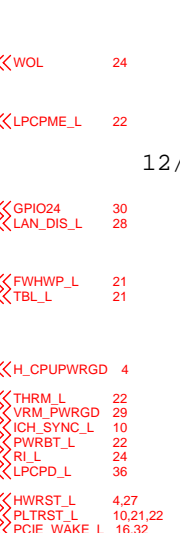
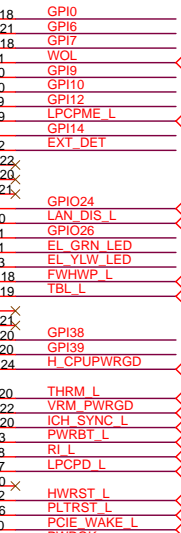
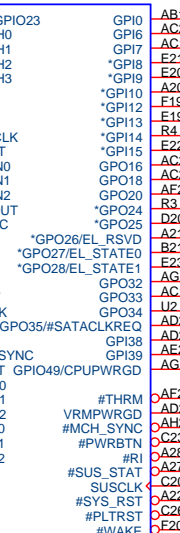
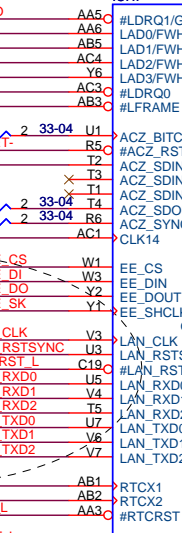
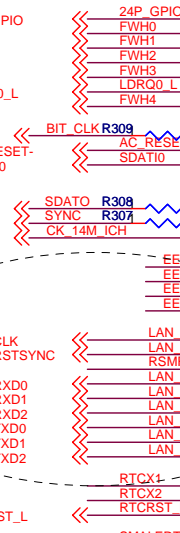
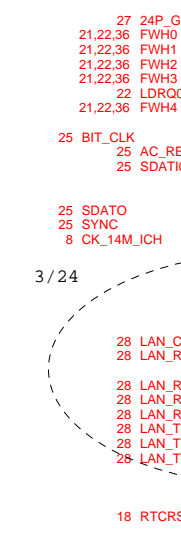
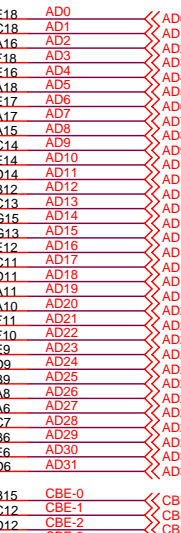
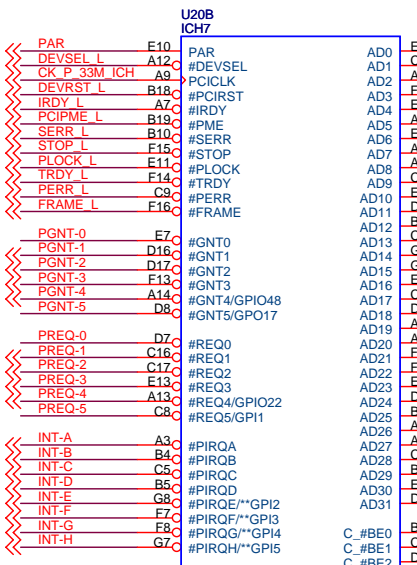
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Title: **PCIE 16-PORT**

Size B Document Number: **945G-M3** Rev 1.0B

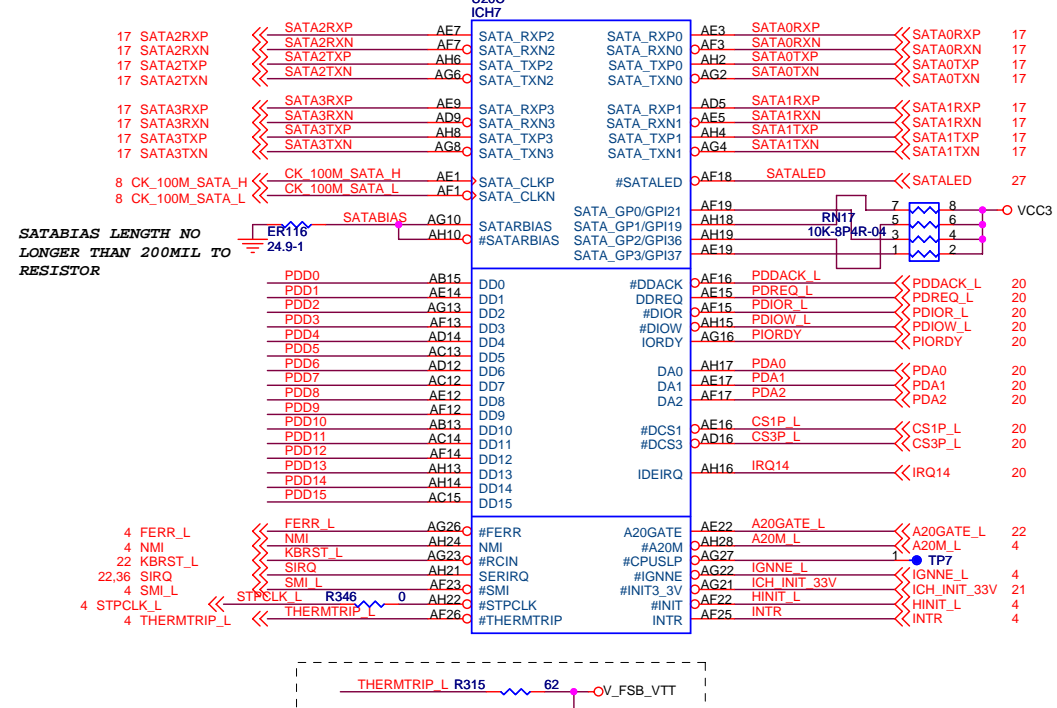
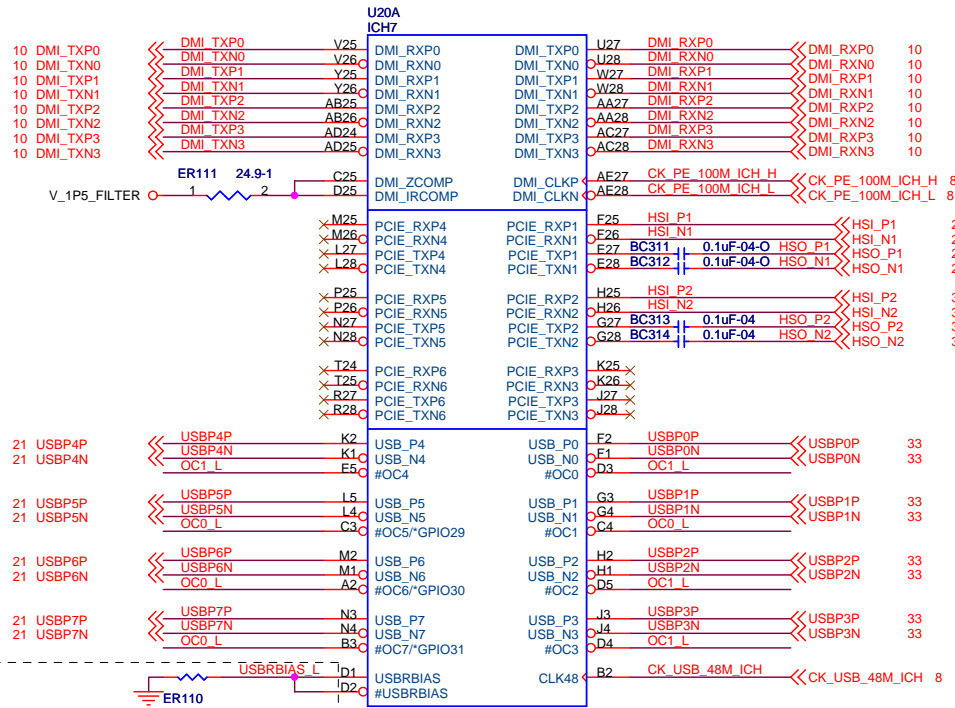
Date: Tuesday, June 14, 2005 Sheet 16 of 36

31,34,35 PAR
 31,34,35 DEVSEL_L
 8 CK_P_33M_ICH
 19 DEVRST_L
 31,34,35 IRDY_L
 31,34,35 PCIPME_L
 31,35 SERR_L
 31,34,35 STOP_L
 31,34,35 PLOCK_L
 31,34,35 TRDY_L
 31,34,35 PERR_L
 31,34,35 FRAME_L

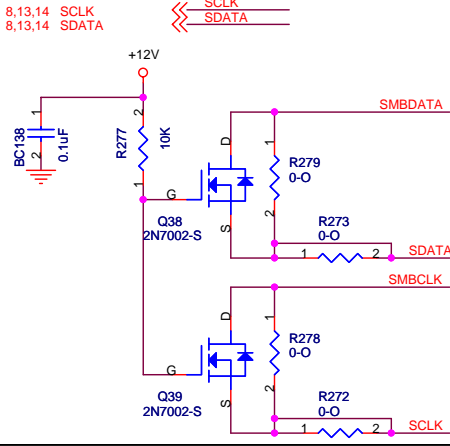
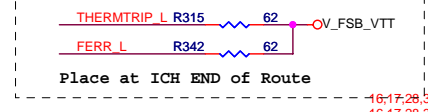
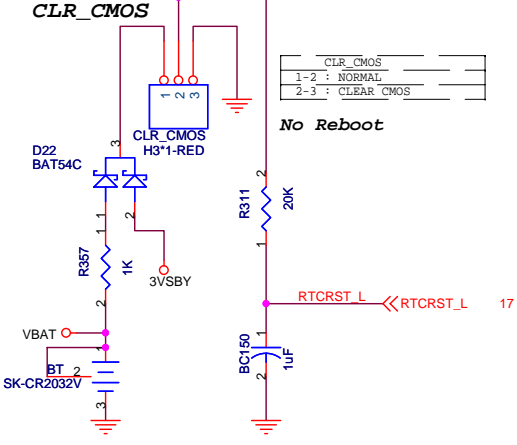
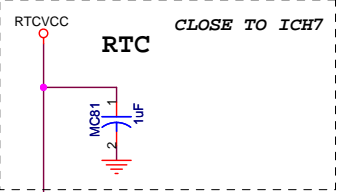
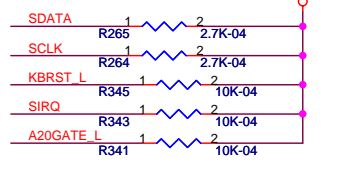
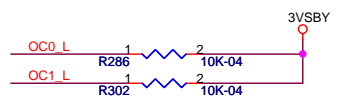
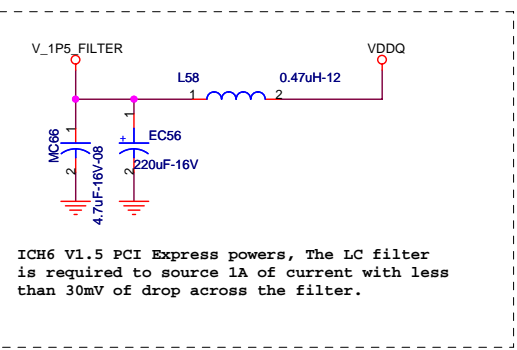


Elitegroup Computer Systems
ICH7 Part B & D

Title	Document Number	Rev
	945G-M3	1.0B
Size	Document Number	Rev
Custom		
Date:	Tuesday, June 14, 2005	Sheet 17 of 36



Must routing a trace to 22.6ohm pad, Don't direct connect with USBRBIAS_L.(two trace must < 500 mils)

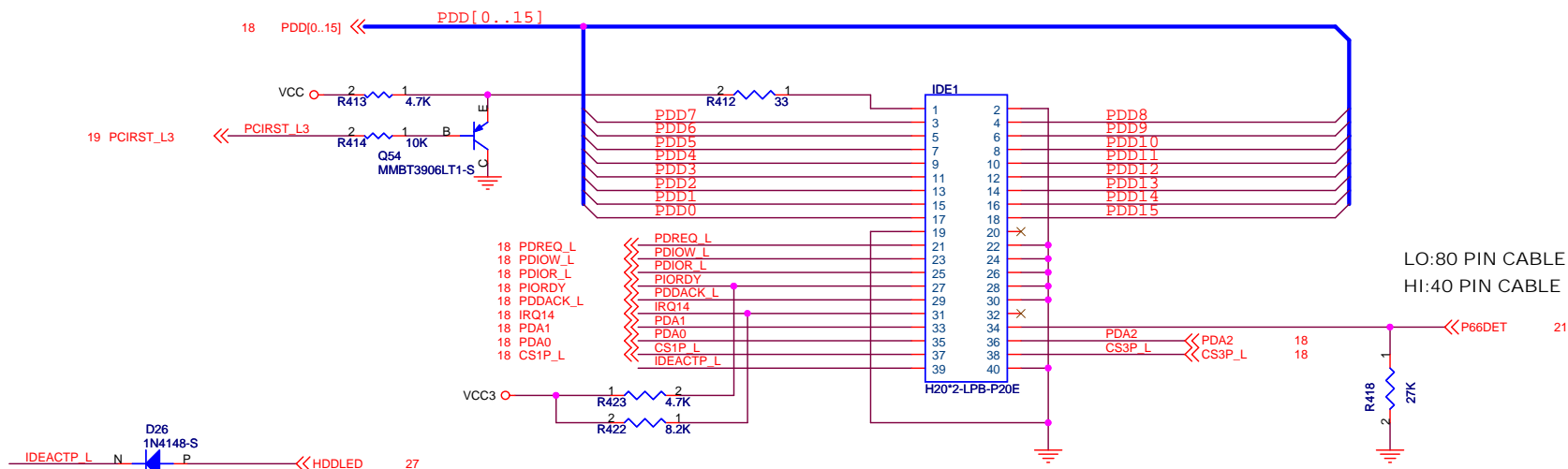


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Title: **ICH7 Part A & C**

Size: Custom Document Number: **945G-M3** Rev: **1.0B**

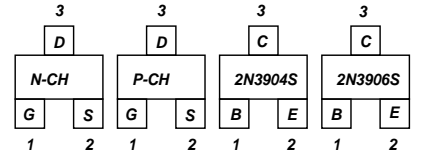
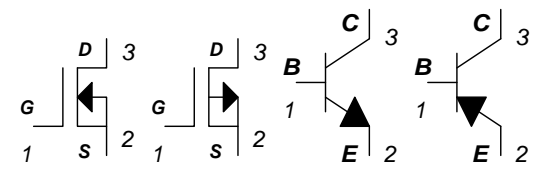
Date: Tuesday, June 14, 2005 Sheet 18 of 36



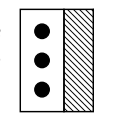
MAX TRACE LENGTH IS 8"

DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L, XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

Top View SOT-23

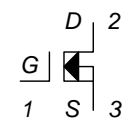


Fan Header

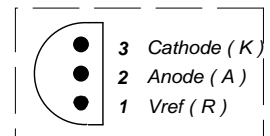


AMP640456-3

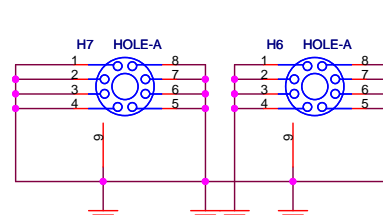
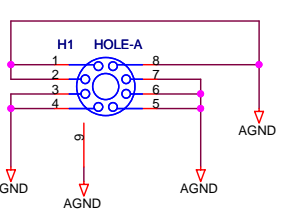
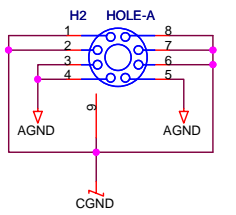
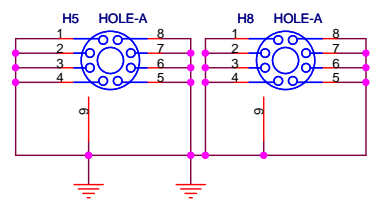
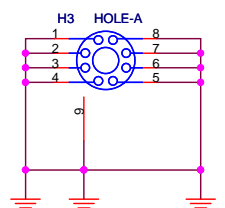
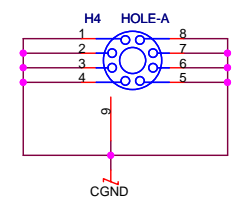
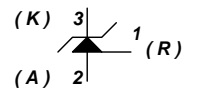
TO-263 / TO-252



Top View



TL431



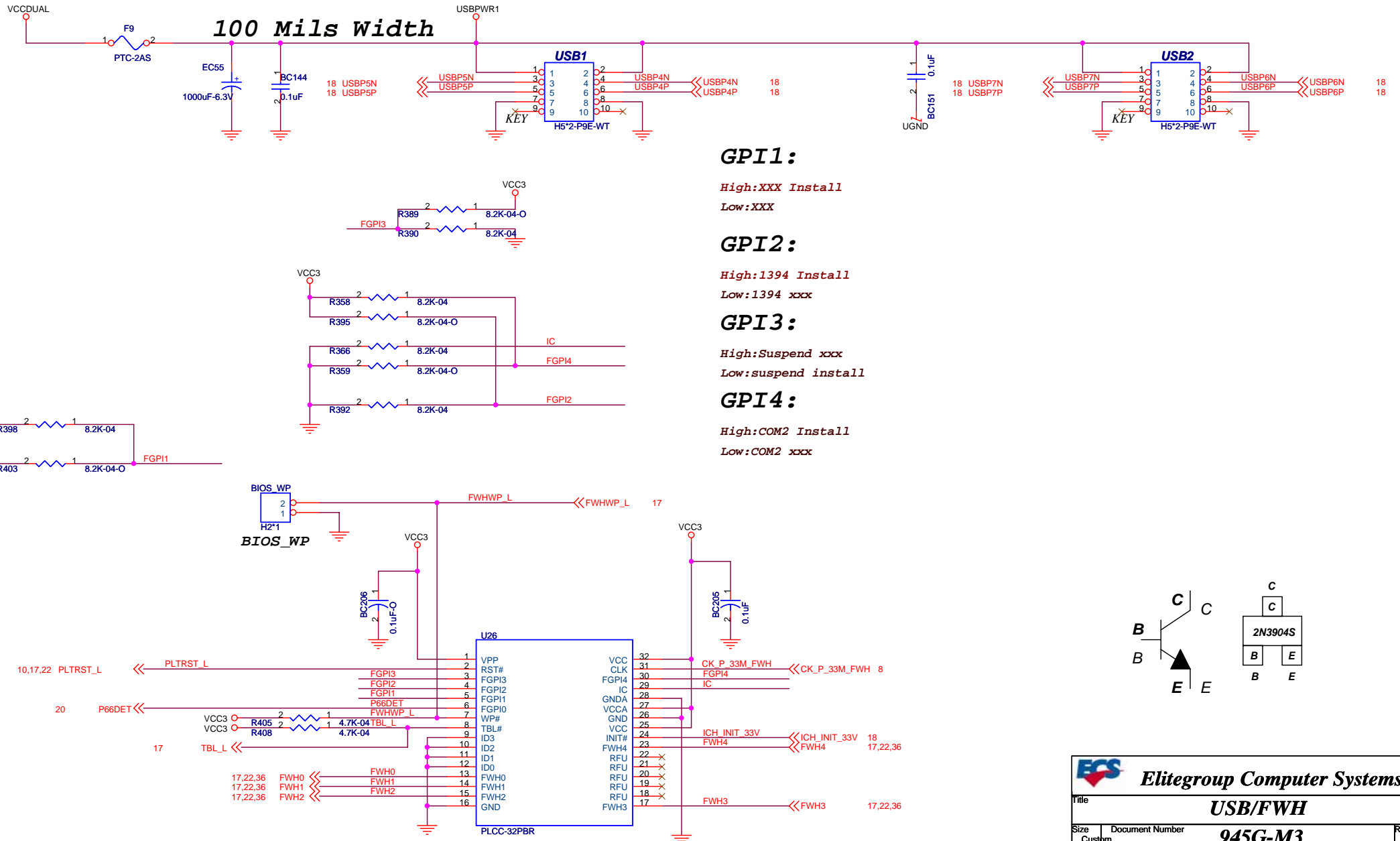
ECS Elitegroup Computer Systems

Title: **IDE Connector**

Size: Custom Document Number: **945G-M3** Rev: 1.0B

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USB PORT INTERFACE



GPI1:

High:XXX Install
Low:XXX

GPI2:

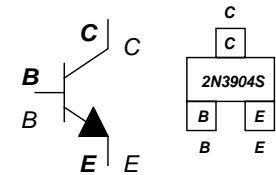
High:1394 Install
Low:1394 xxx

GPI3:

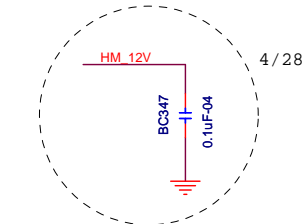
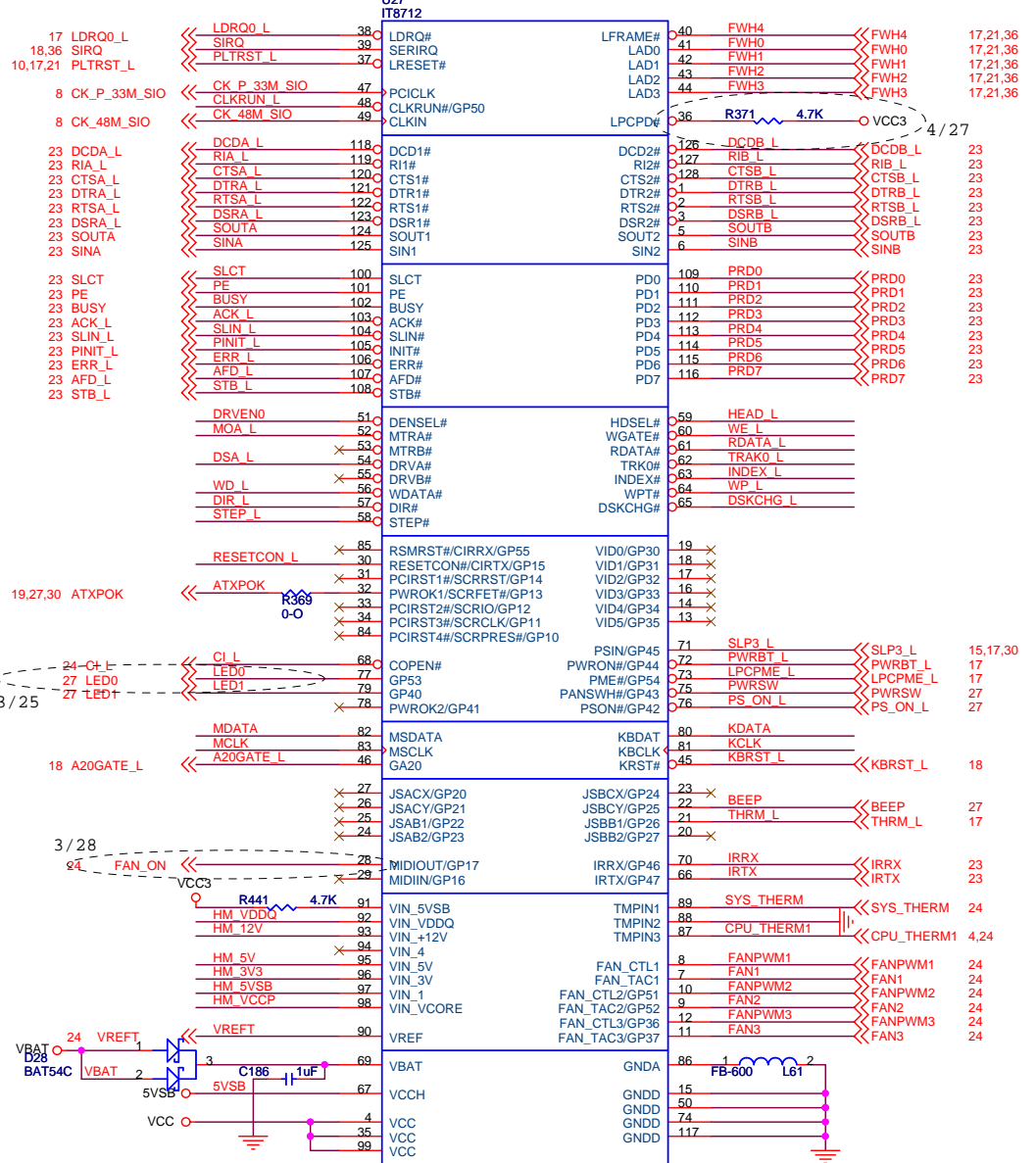
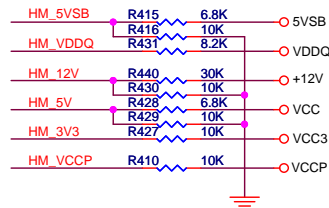
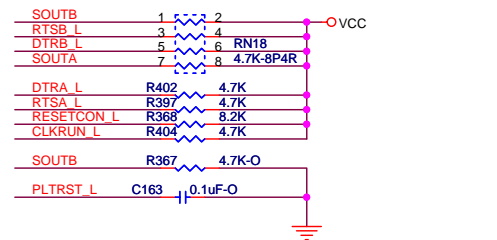
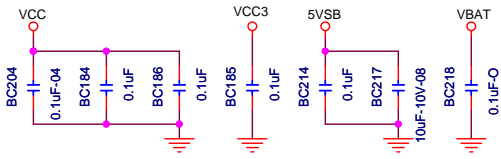
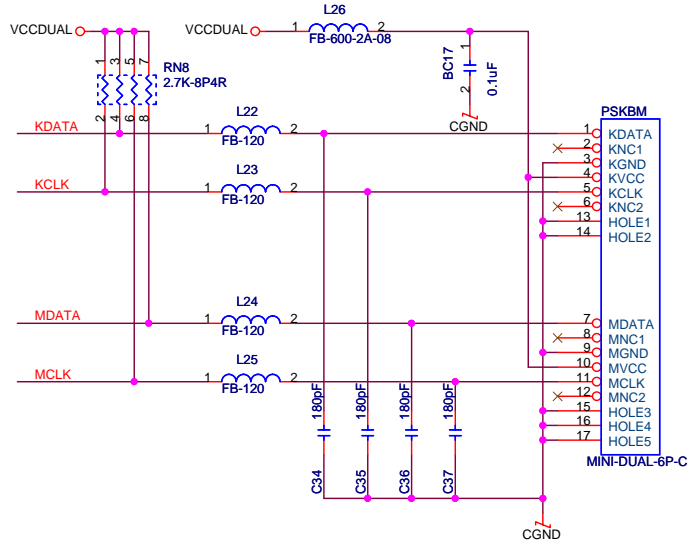
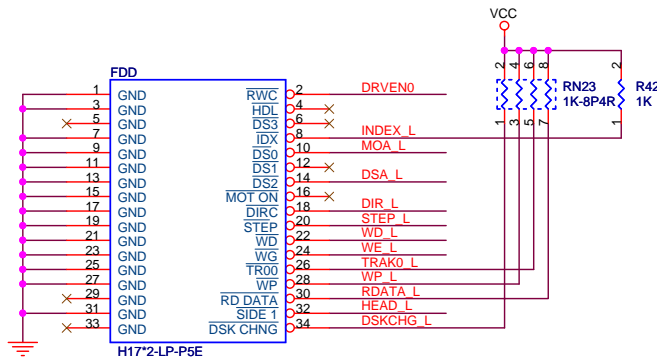
High:Suspend xxx
Low:suspend install

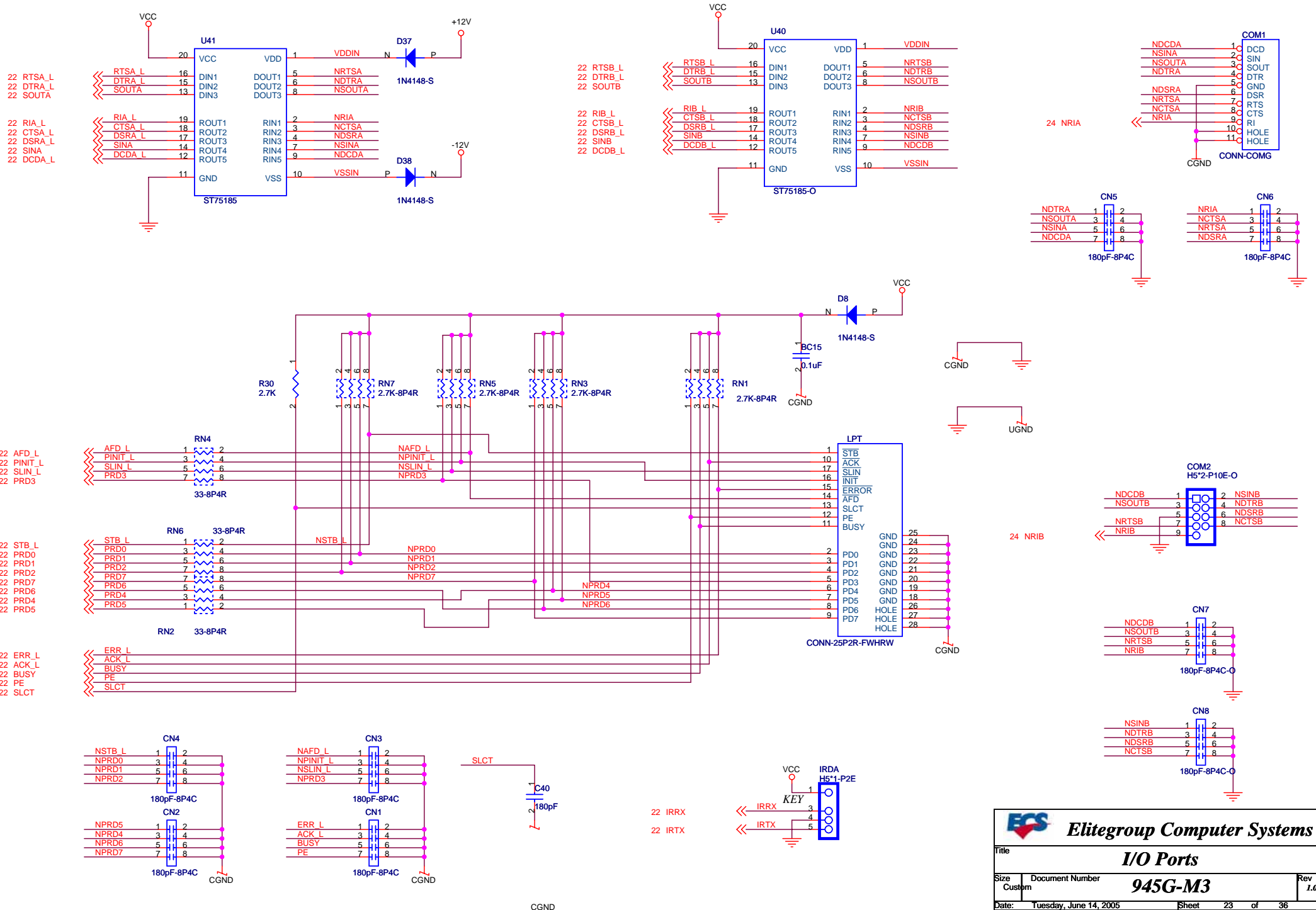
GPI4:

High:COM2 Install
Low:COM2 xxx



USB/FWH		
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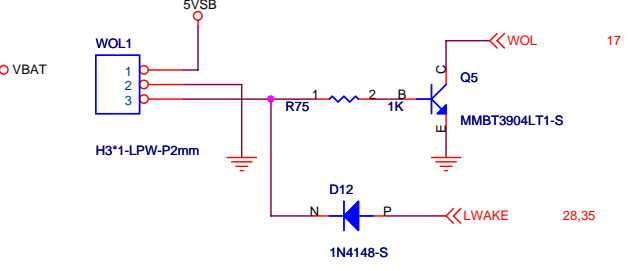
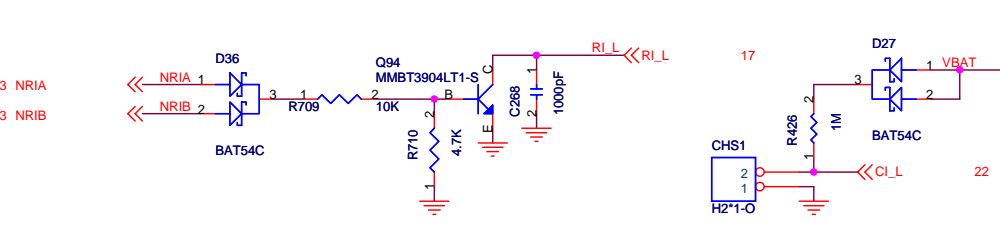
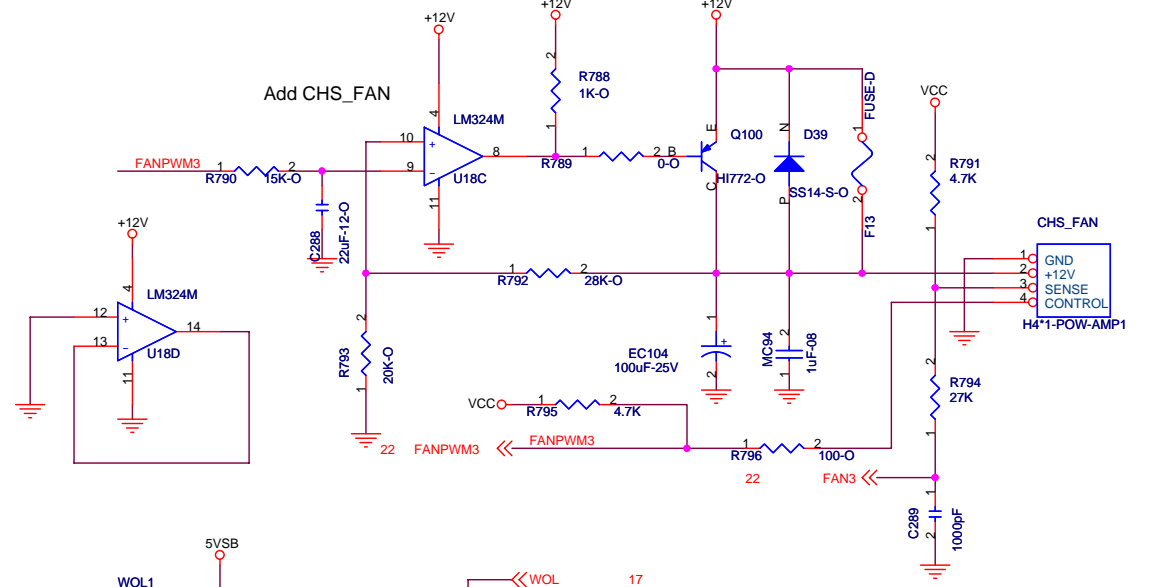
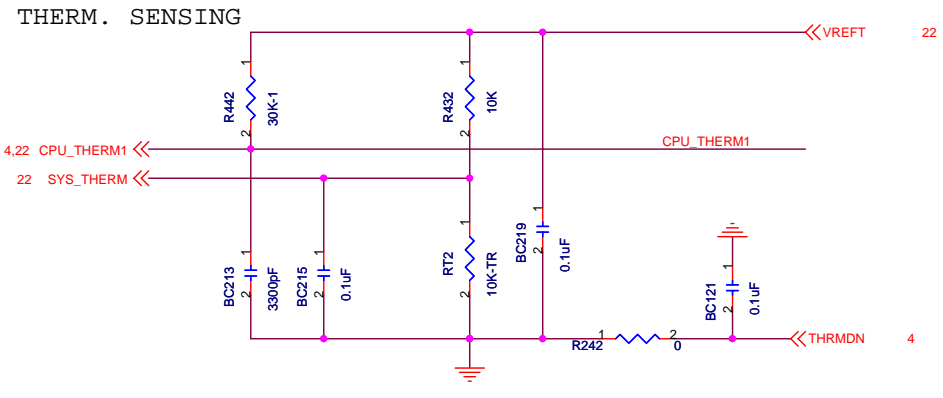
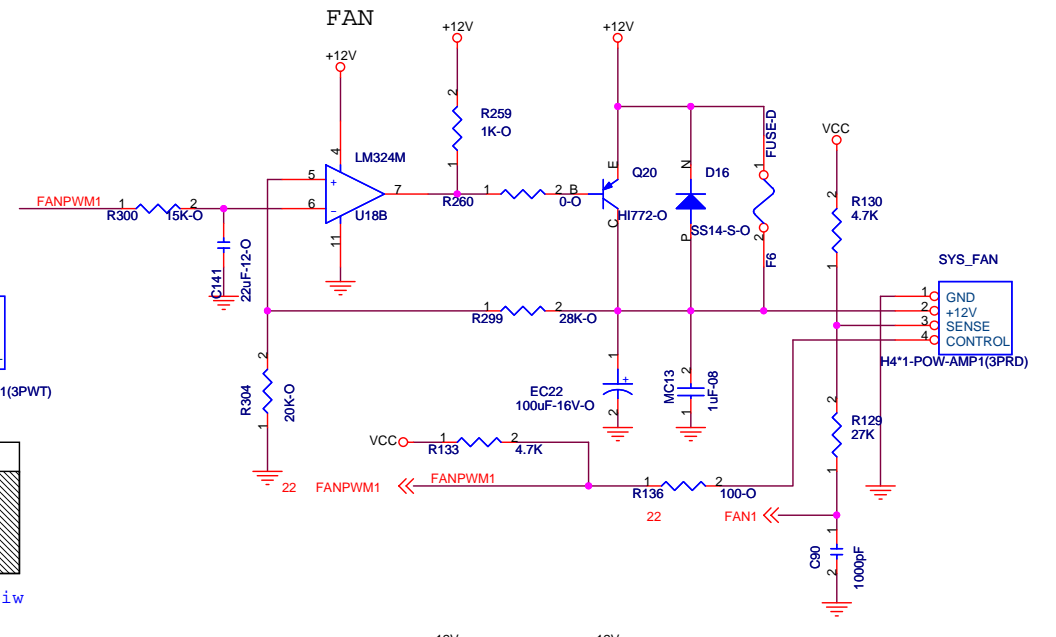
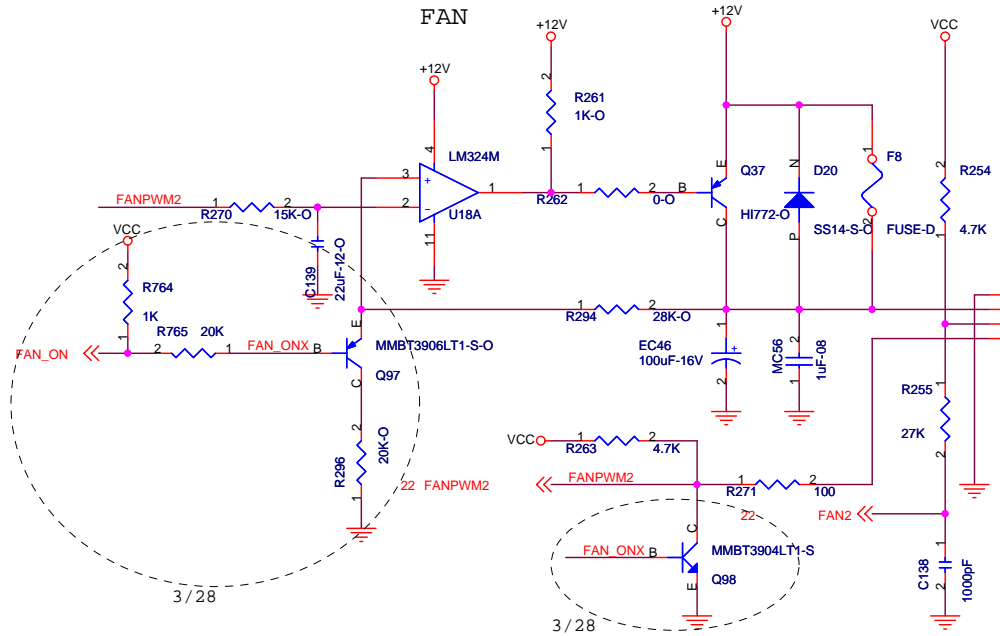




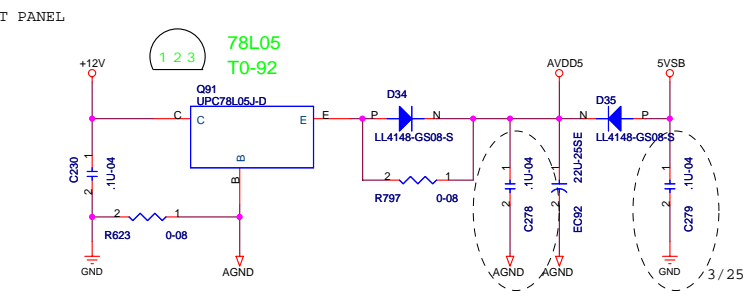
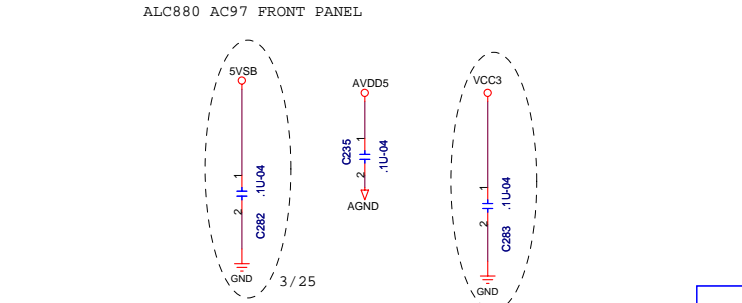
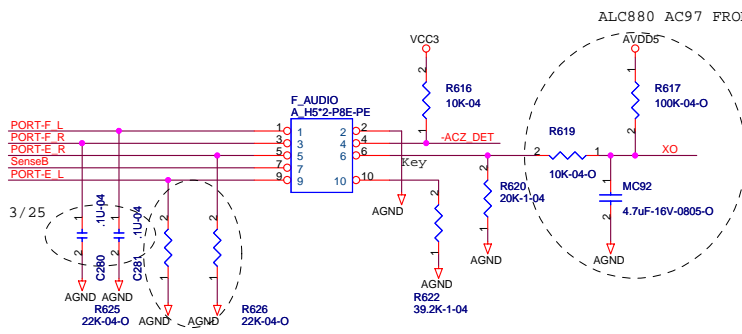
ECS *Elitegroup Computer Systems*

Title: **I/O Ports**

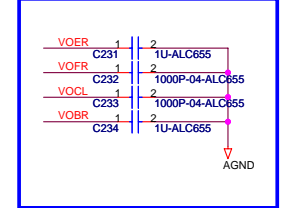
Size: Custom	Document Number: 945G-M3	Rev: 1.0B
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Elitegroup Computer Systems			
H/W Monitor			
Title		945G-M3	
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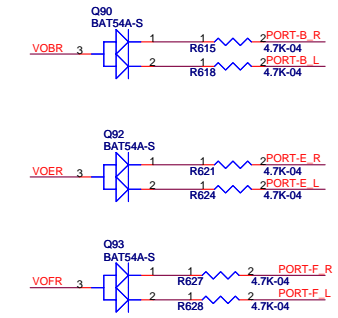


Place near CODEC each PIN

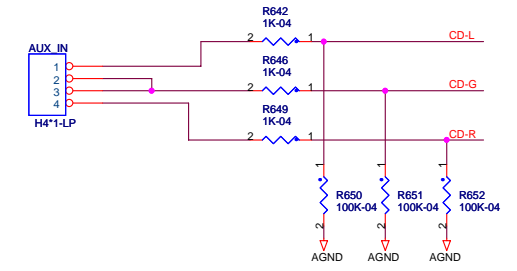
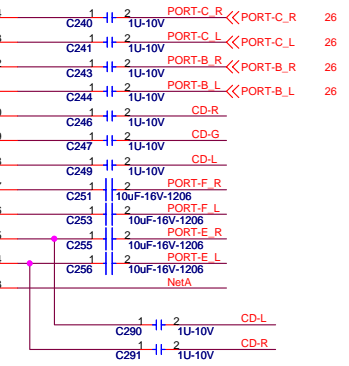
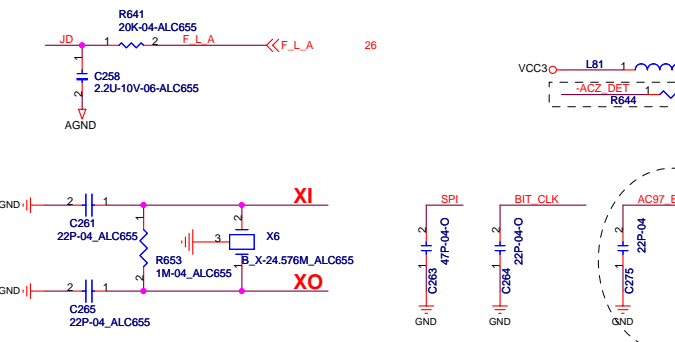
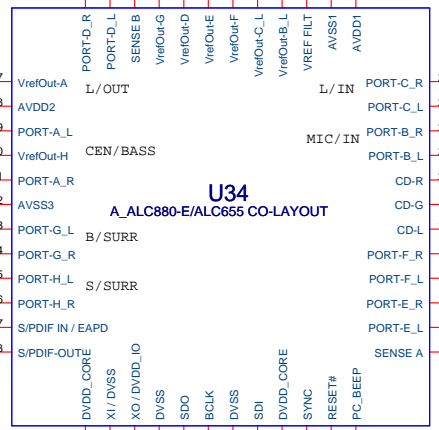
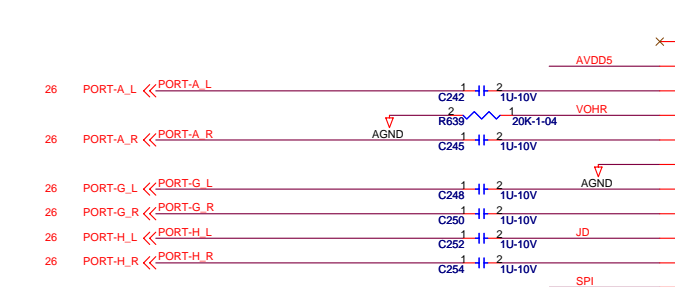
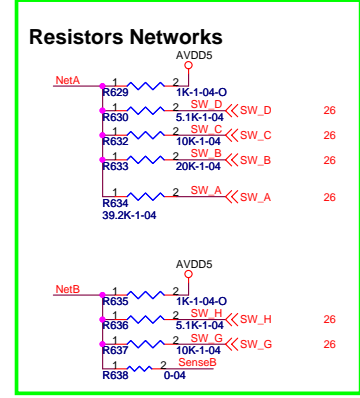


Verfout bias for stereo microphone.

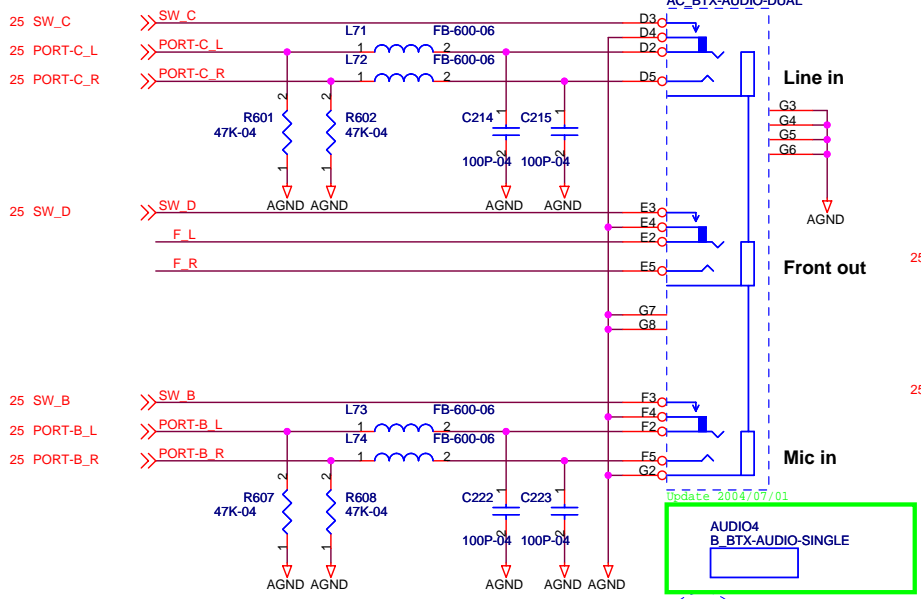
For CMI9880



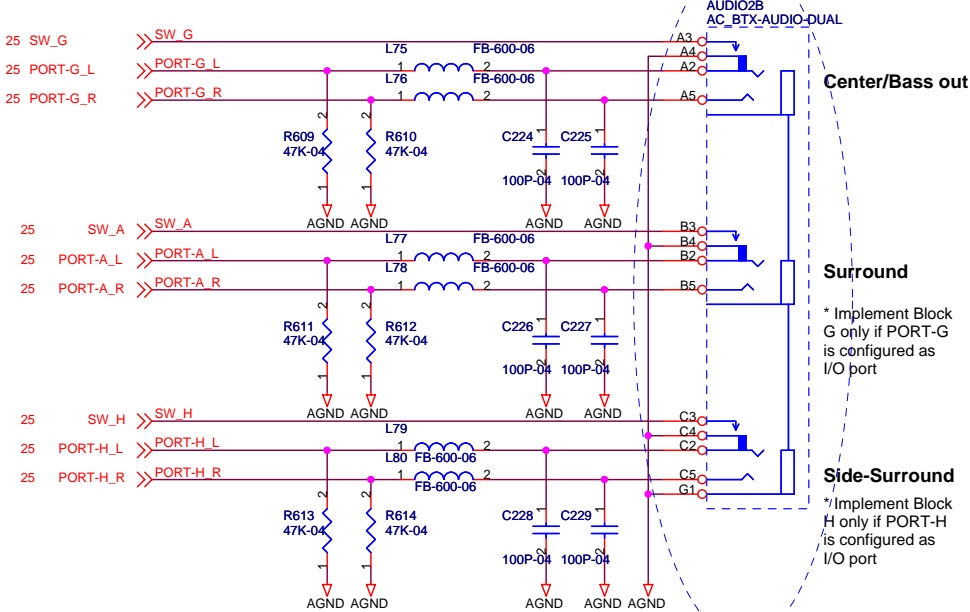
Place near Chip (U23)



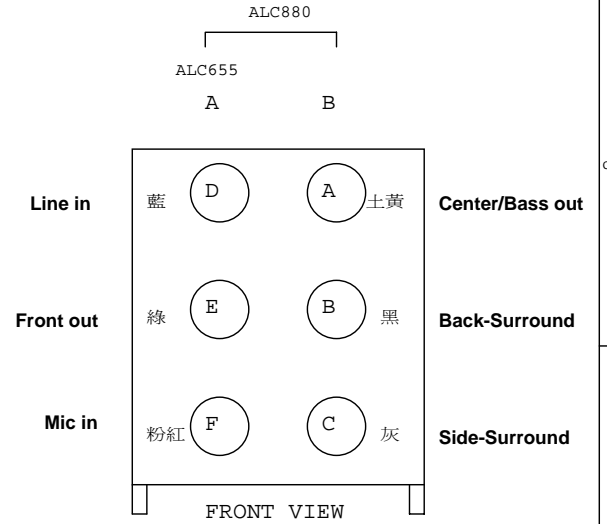
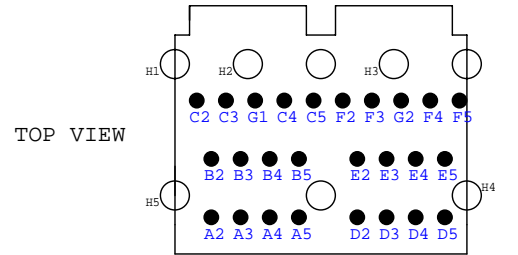
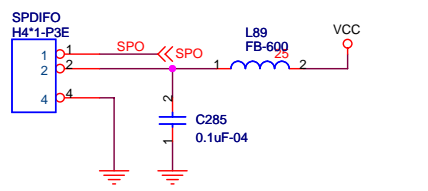
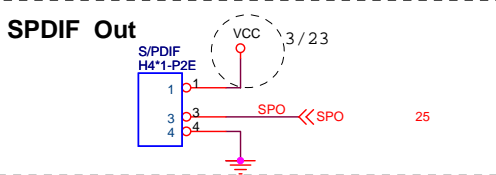
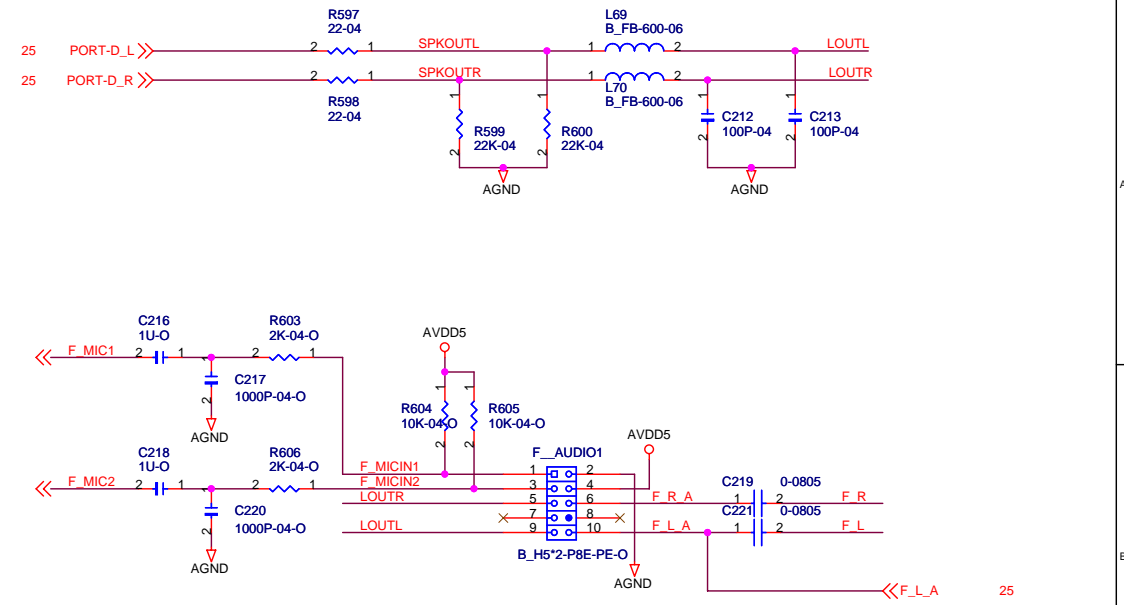
Rear Panel Onboard Analog I/O



Rear Panel (Optional Rear Audio Panel)



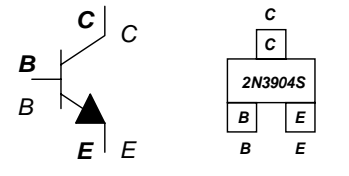
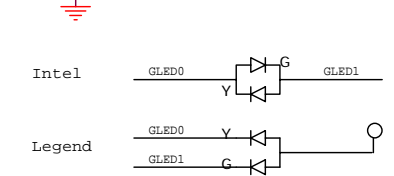
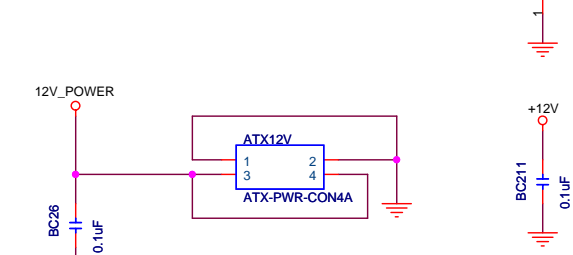
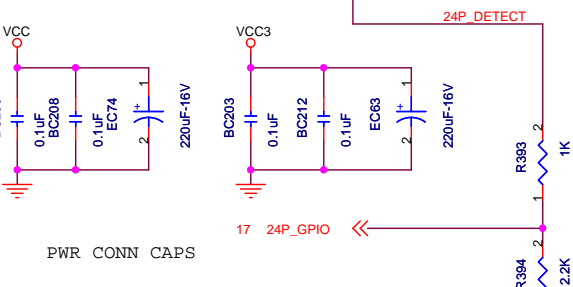
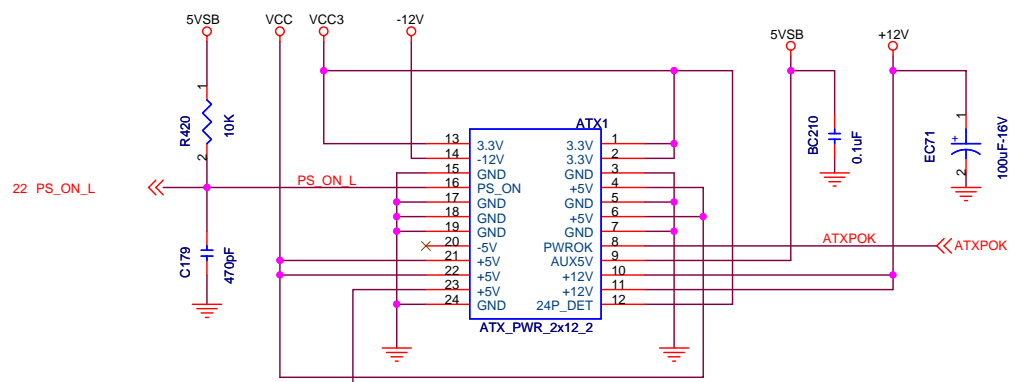
The schematic should consist with PINs define of I/O connector.



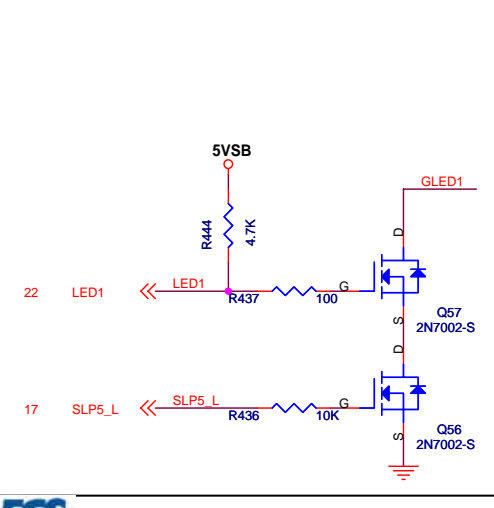
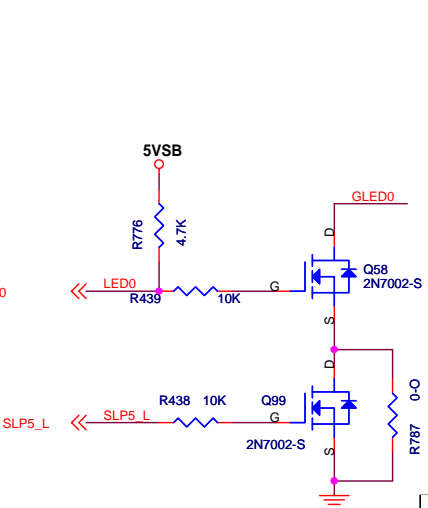
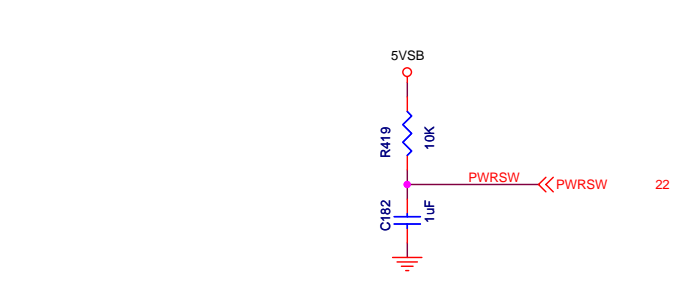
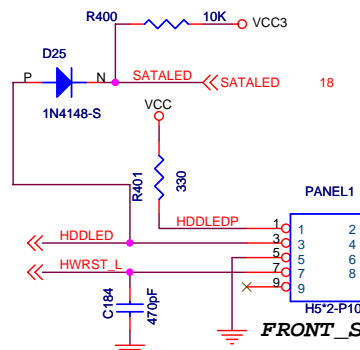
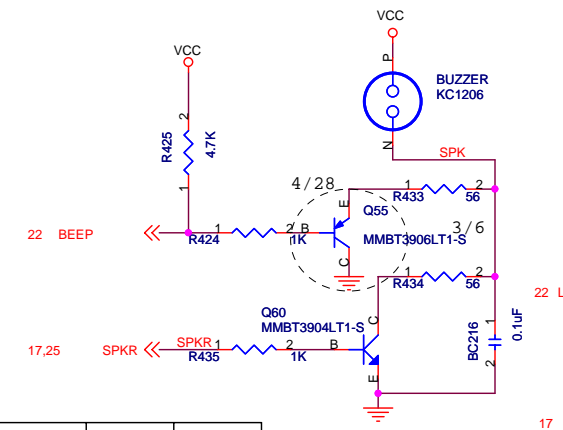
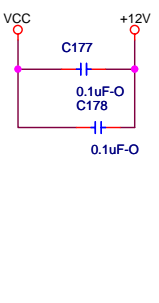
ECS Elitegroup Computer Systems

Title: **Audio Interface**

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	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking Yellow	Dark
LSJ1(1,2)	Dark	Dark	Light	Dark
SJ1(1,3)(2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH

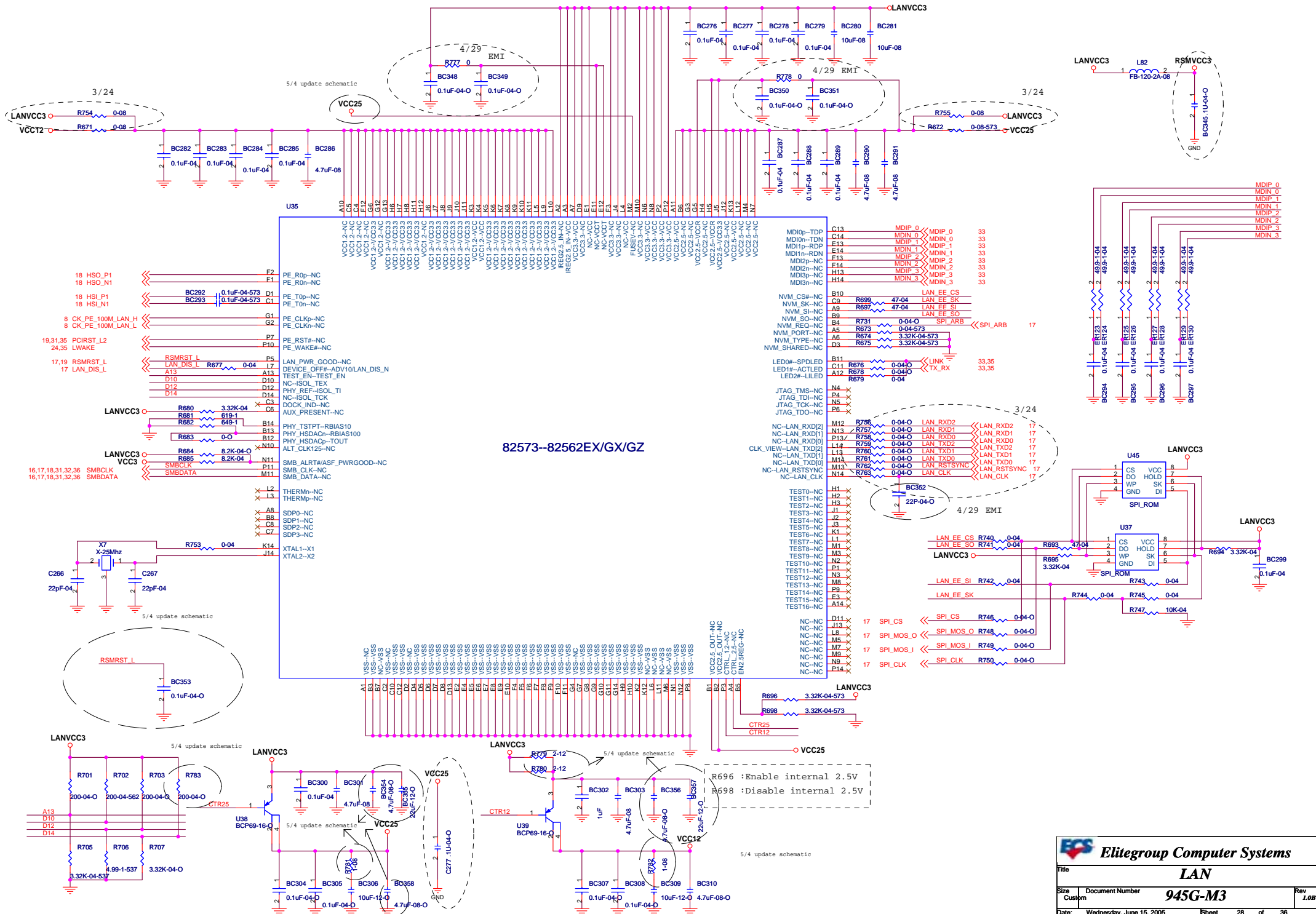


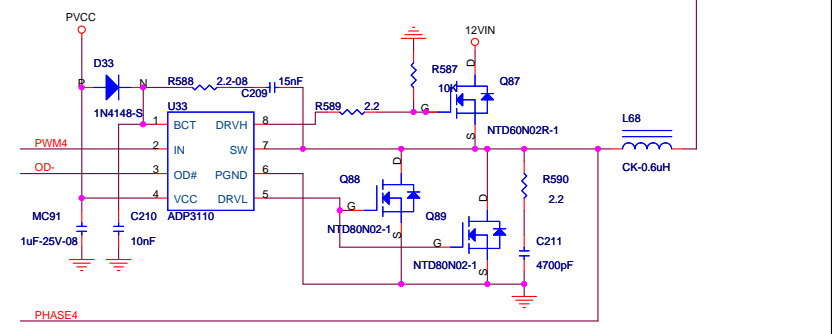
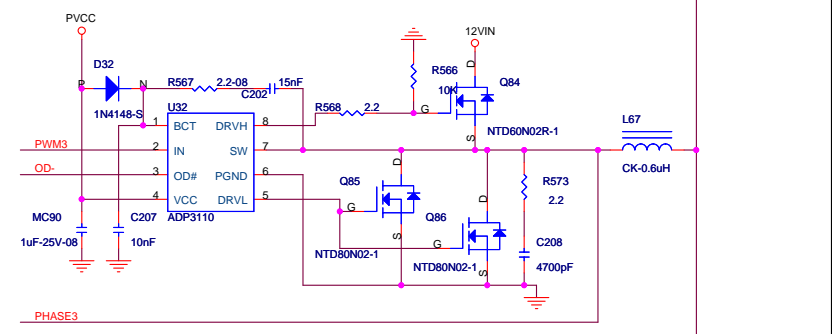
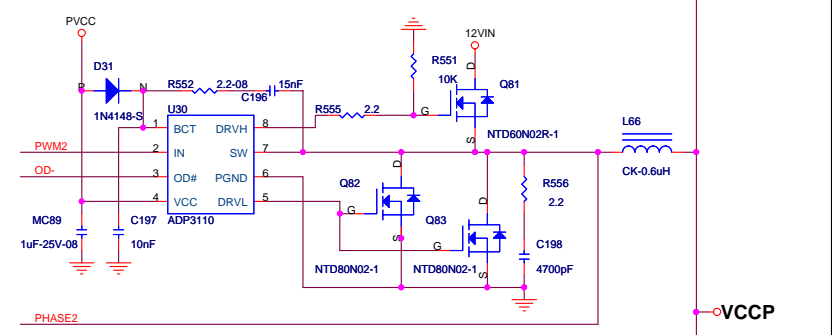
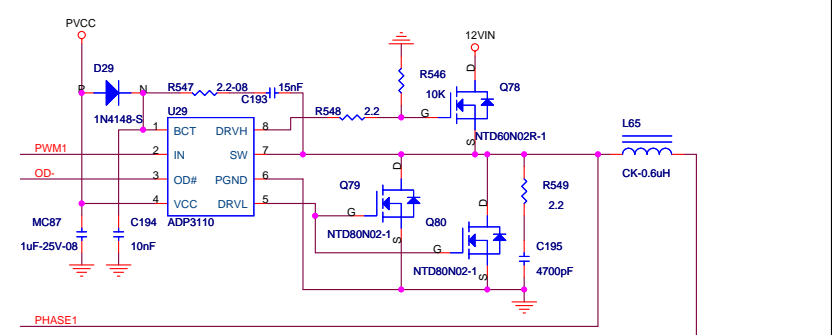
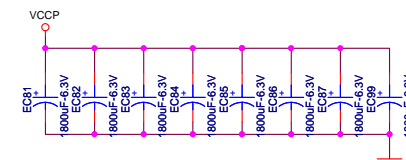
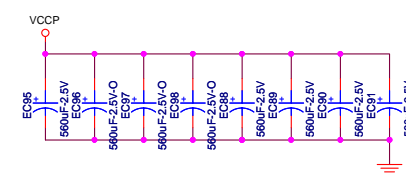
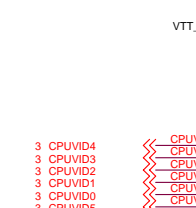
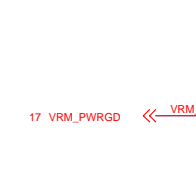
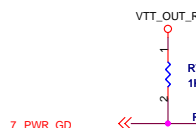
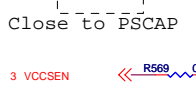
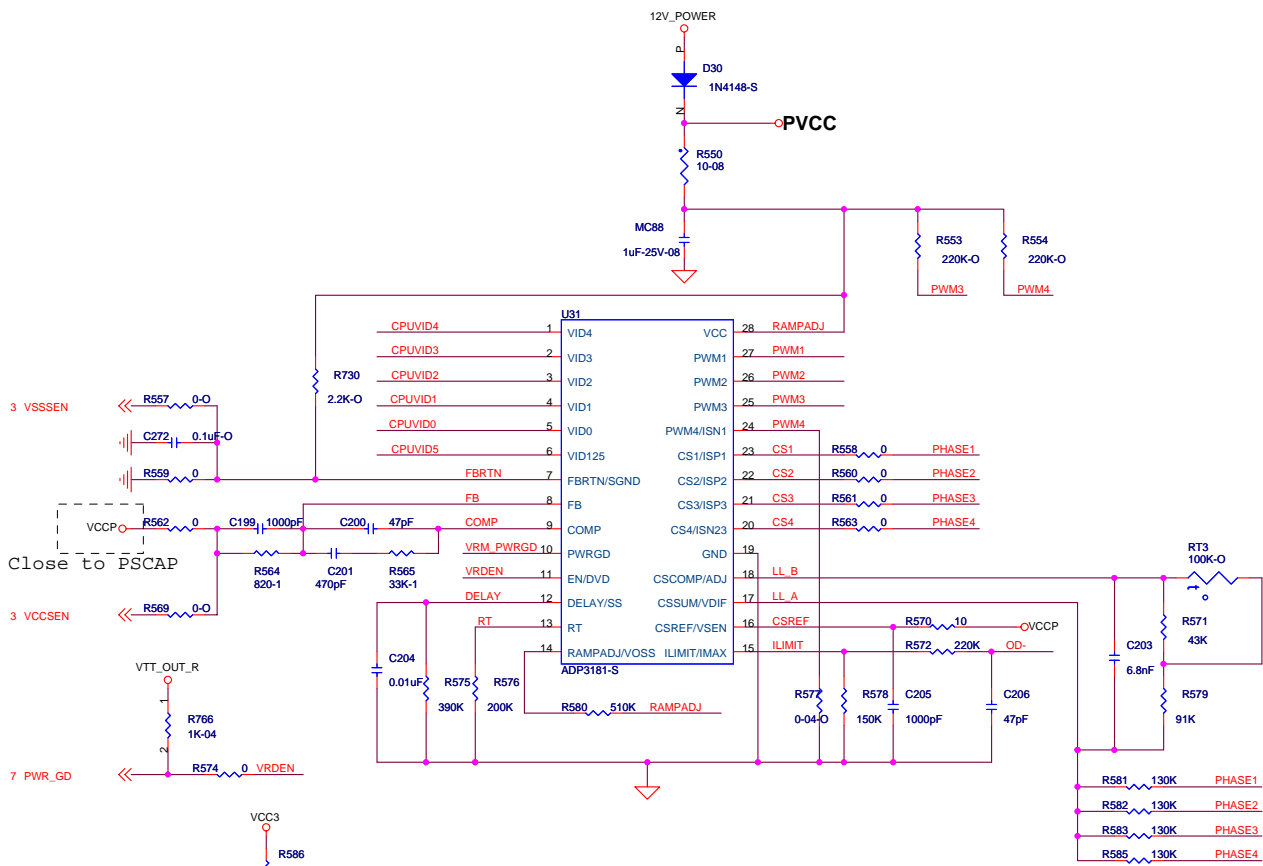
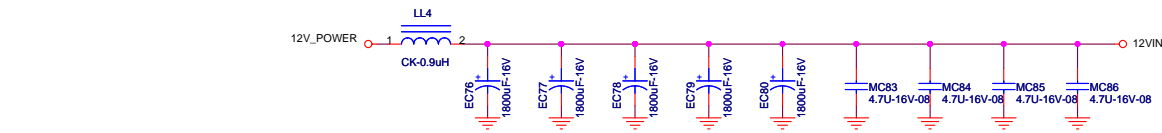
ECS Elitegroup Computer Systems

Title: **ATX Power & Front Panel**

Size B Document Number: **945G-M3** Rev **1.0B**

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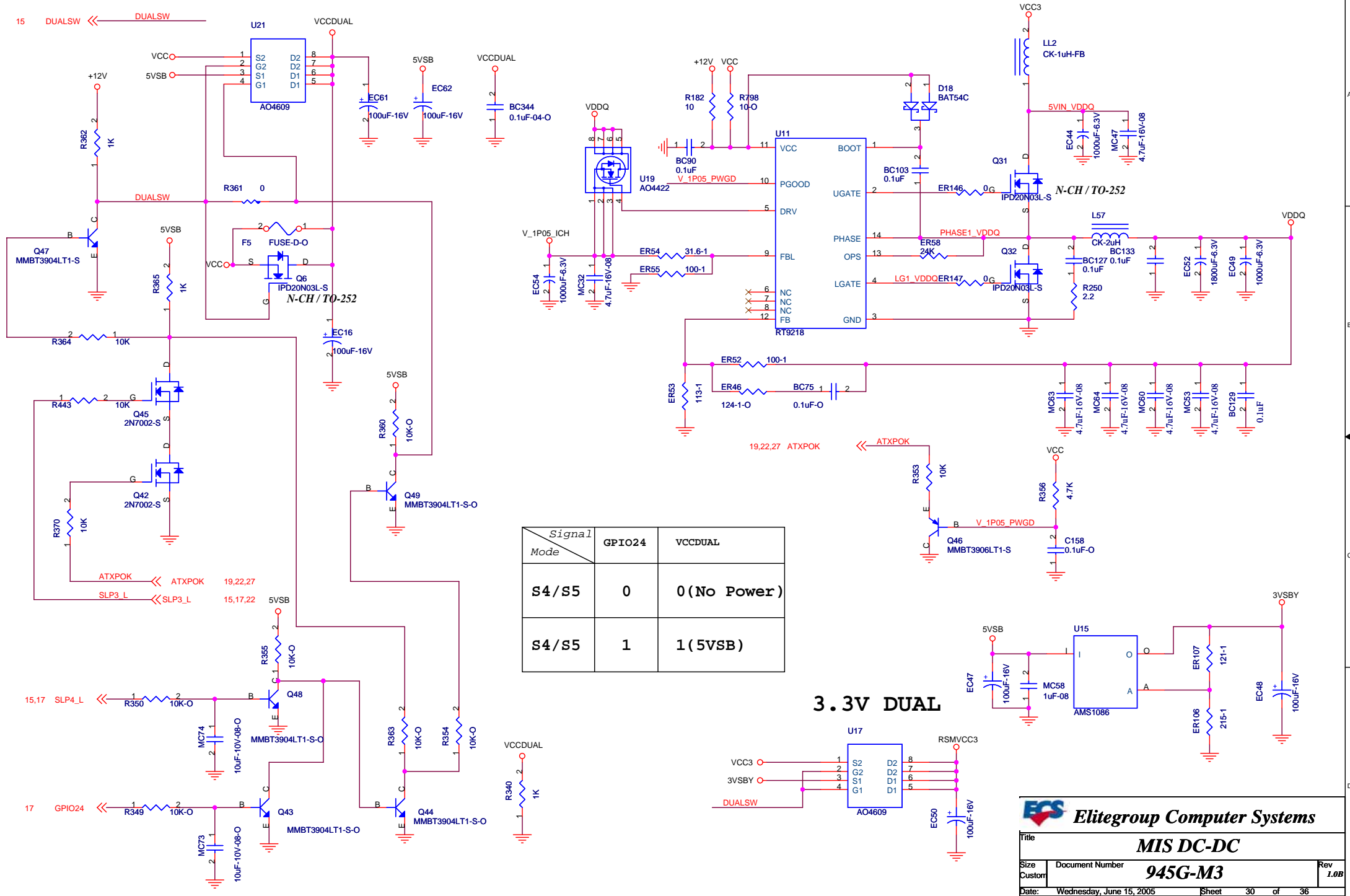




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Title: **VOCRE DC-DC**

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Signal Mode	GPIO24	VCCDUAL
S4/S5	0	0 (No Power)
S4/S5	1	1 (5VSB)

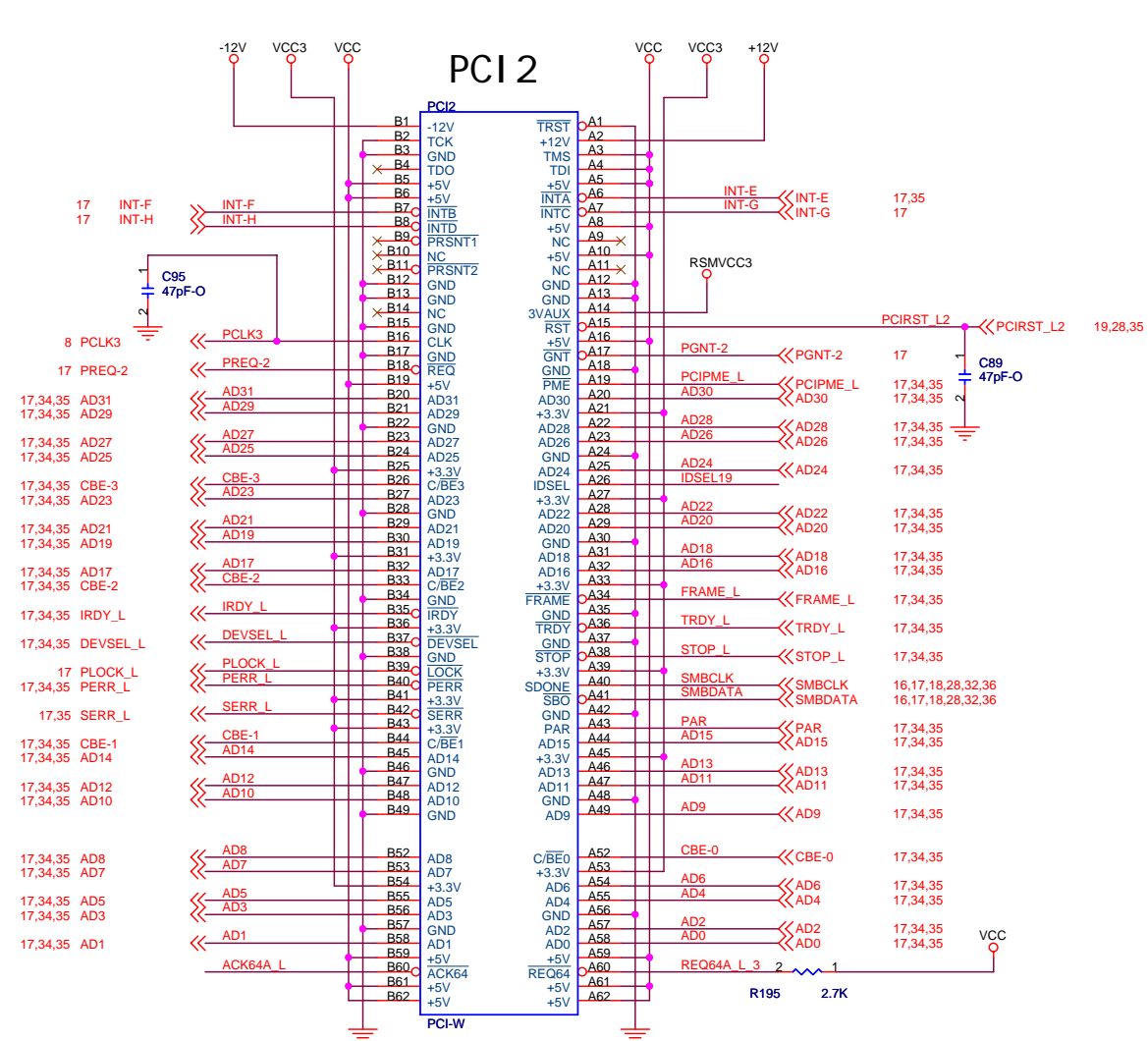
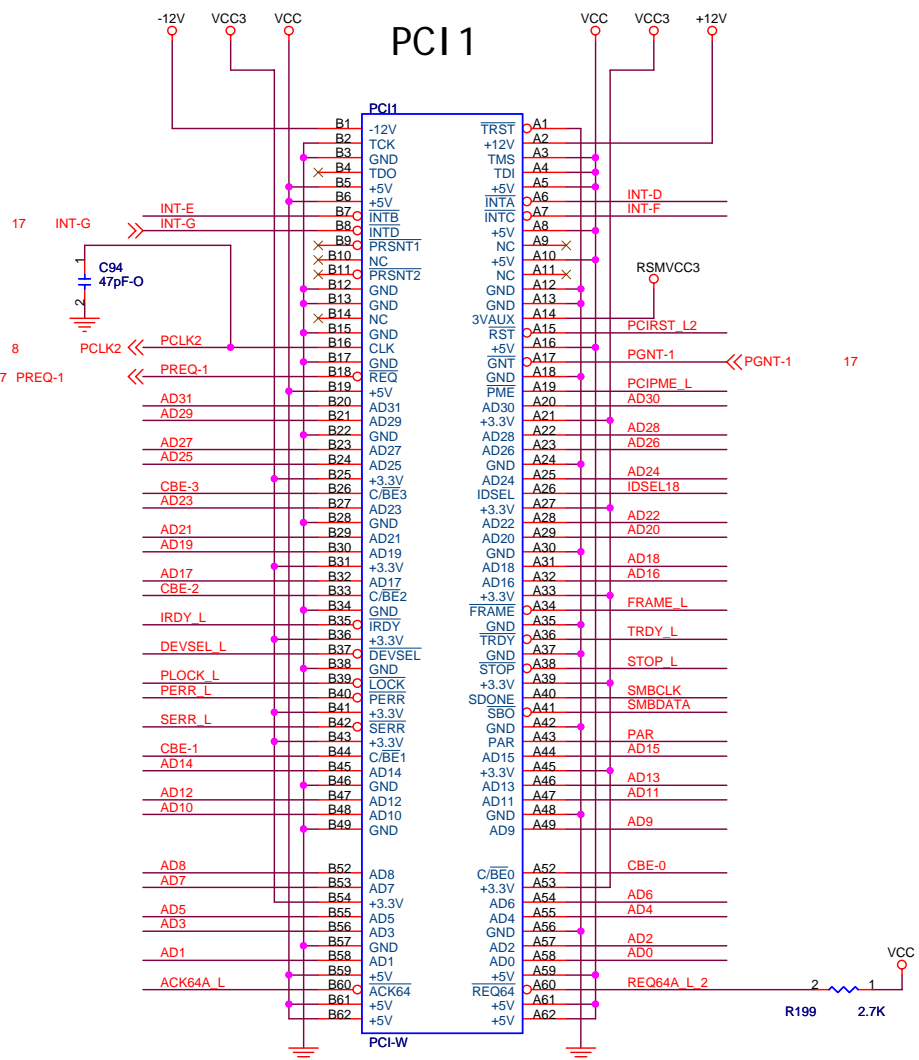
3.3V DUAL

ECS Elitegroup Computer Systems

Title: **MIS DC-DC**

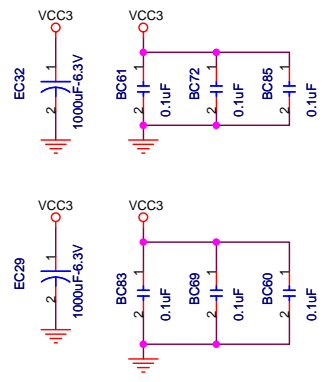
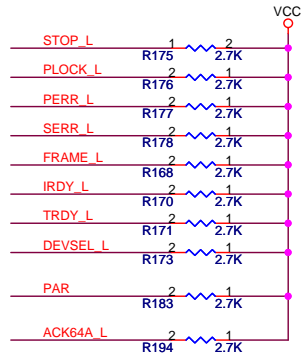
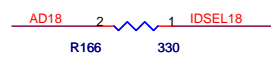
Size: Custom | Document Number: **945G-M3** | Rev: **1.0B**

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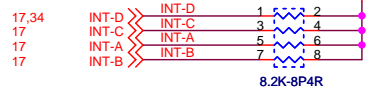
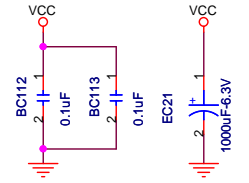
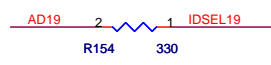
PCI2-INT :
 INTA: INTD
 INTB: INTE
 INTC: INTF
 INTD: INTG

IDSEL=AD18
 REQ=PREQ1#
 GNT=PGNT1#

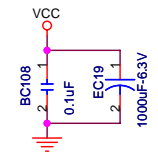
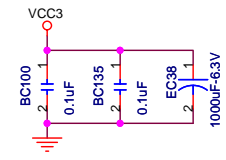
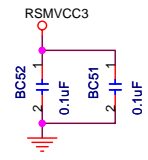
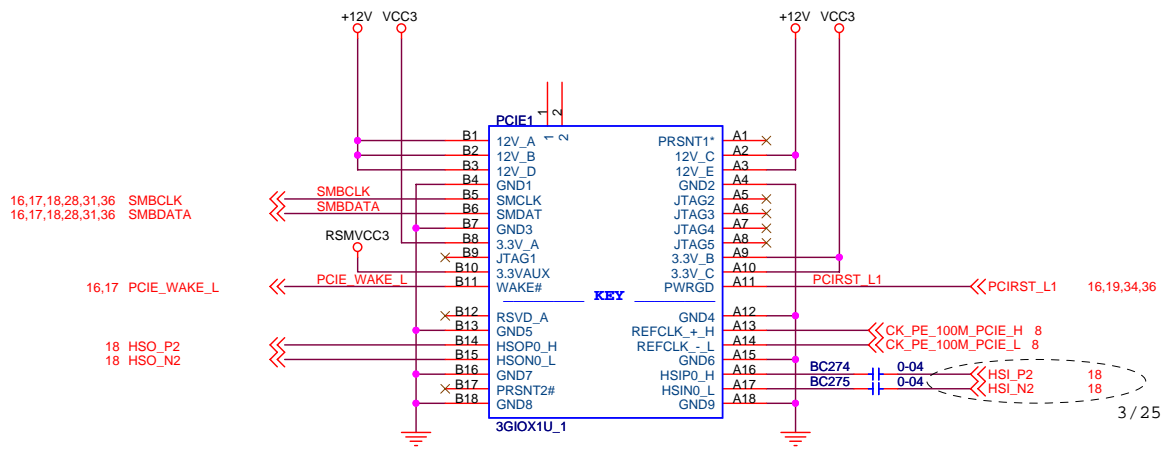


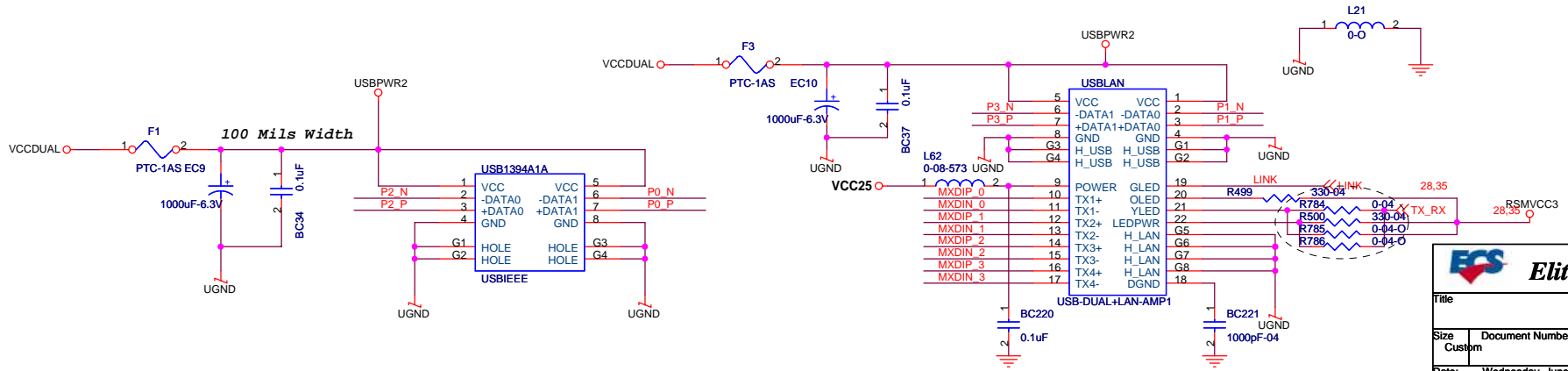
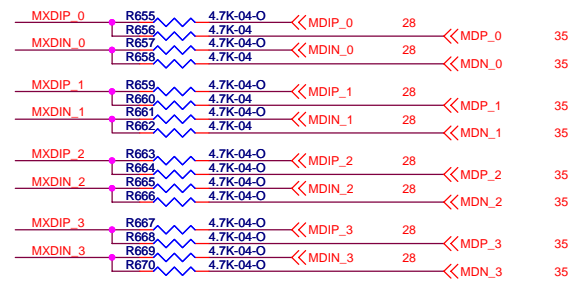
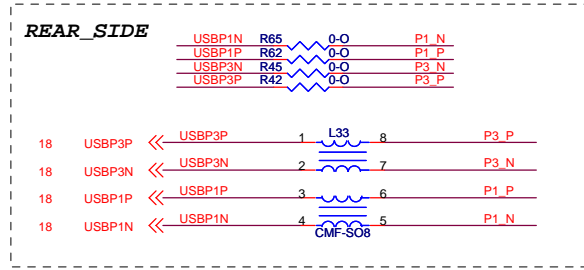
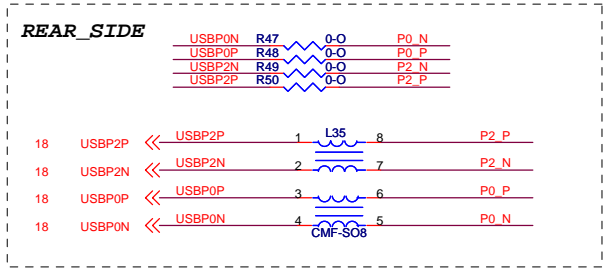
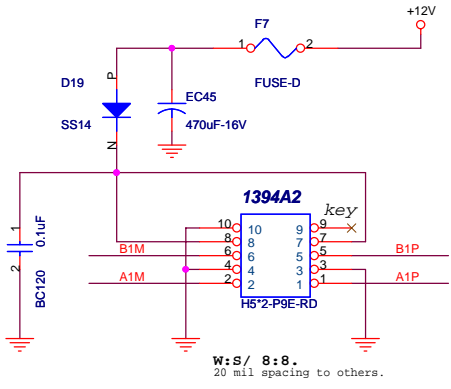
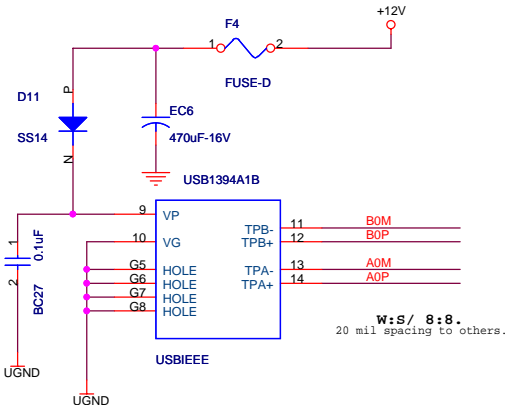
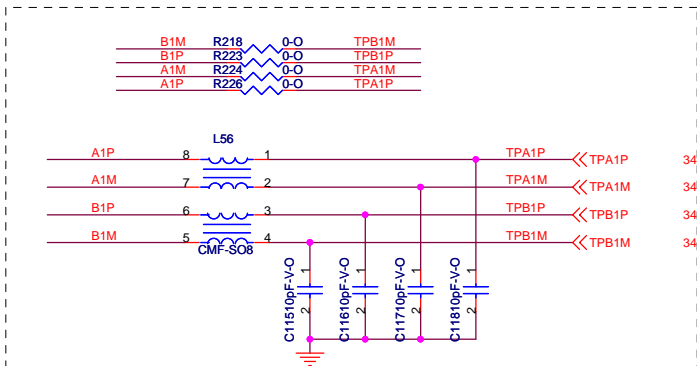
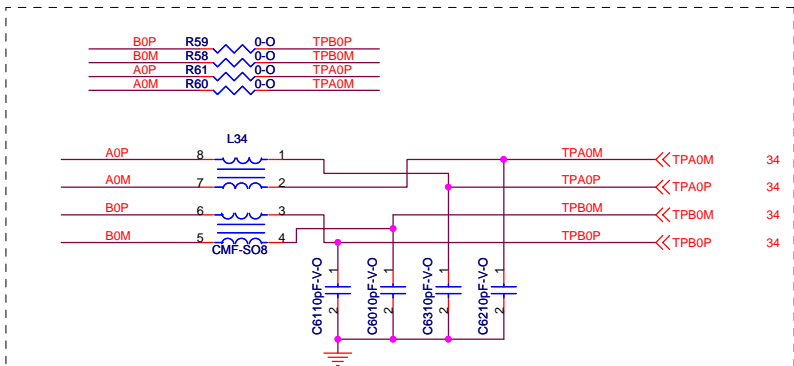
PCI3-INT :
 INTA: INTE
 INTB: INTF
 INTC: INTG
 INTD: INTH

IDSEL=AD19
 REQ=PREQ2#
 GNT=PGNT2#



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PCI Slot 1&2		
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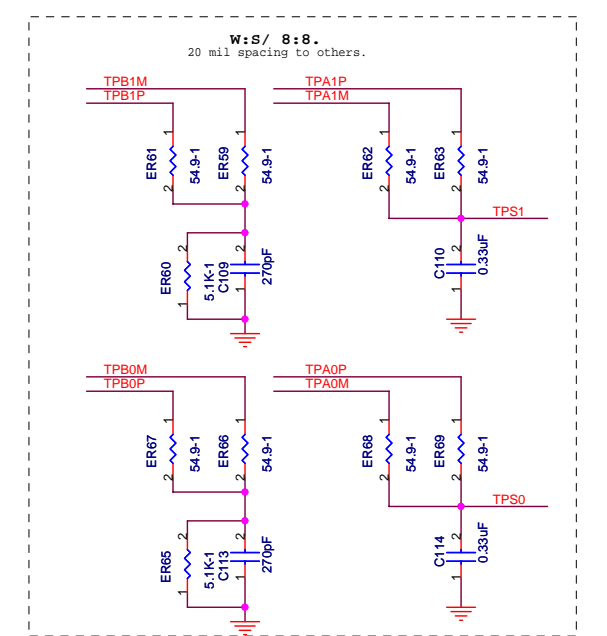
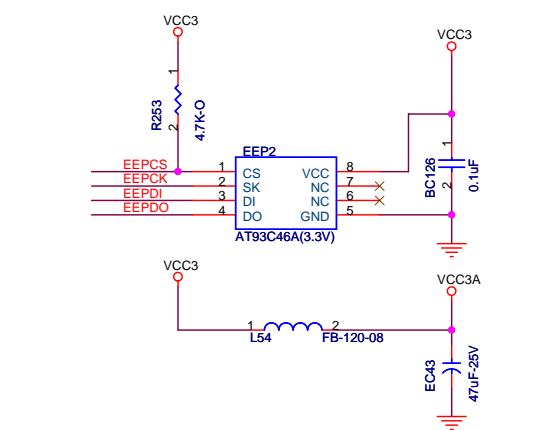
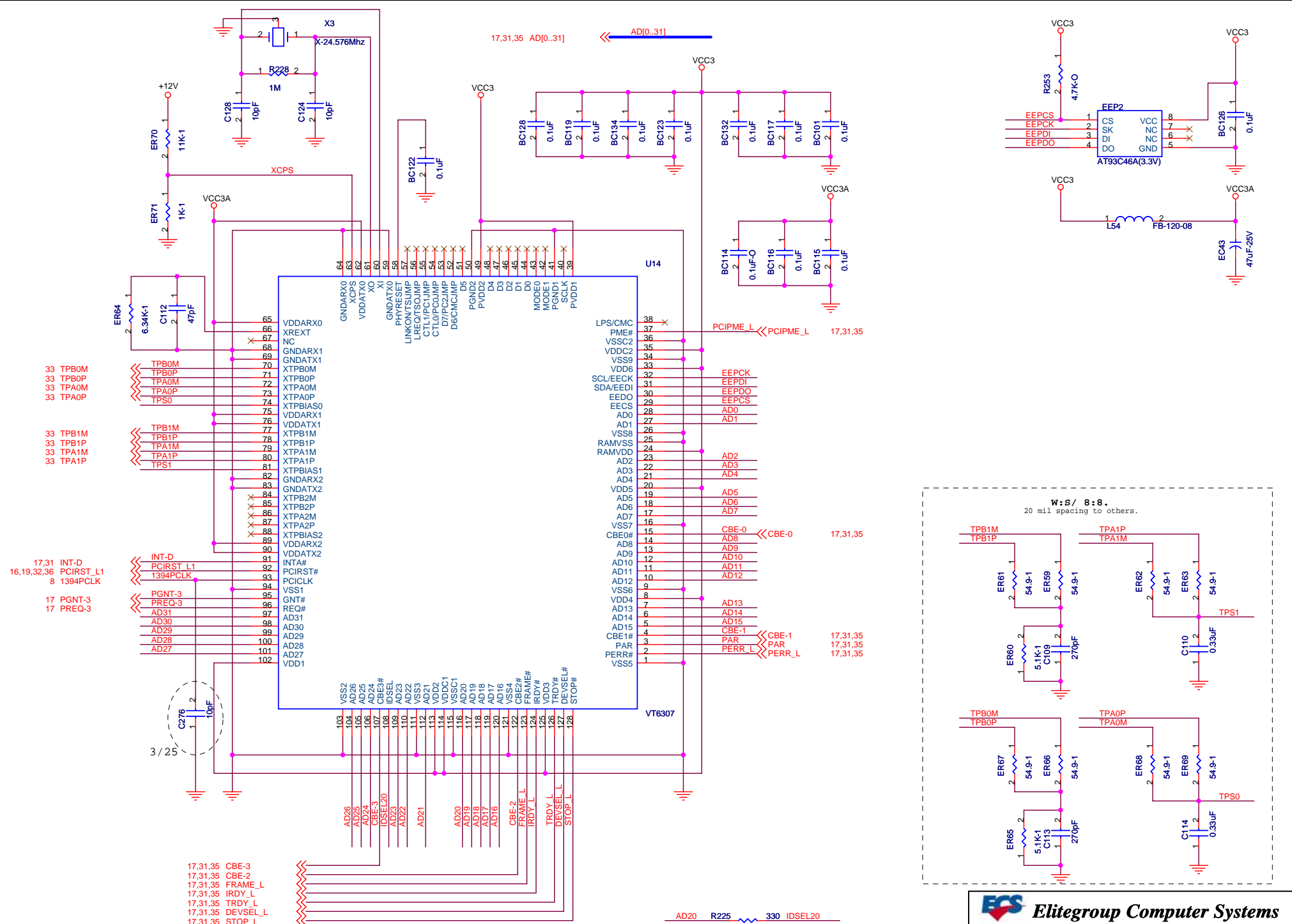


ECS Elitegroup Computer Systems

Title: **Back I/O**

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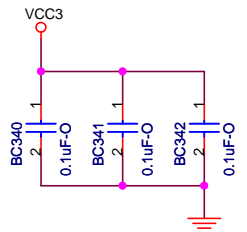
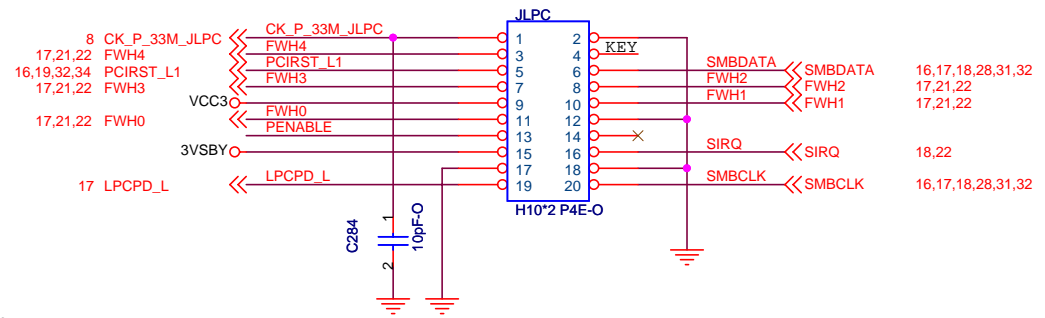
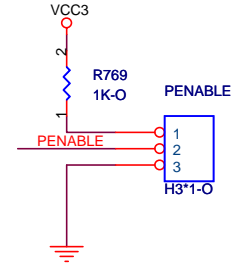
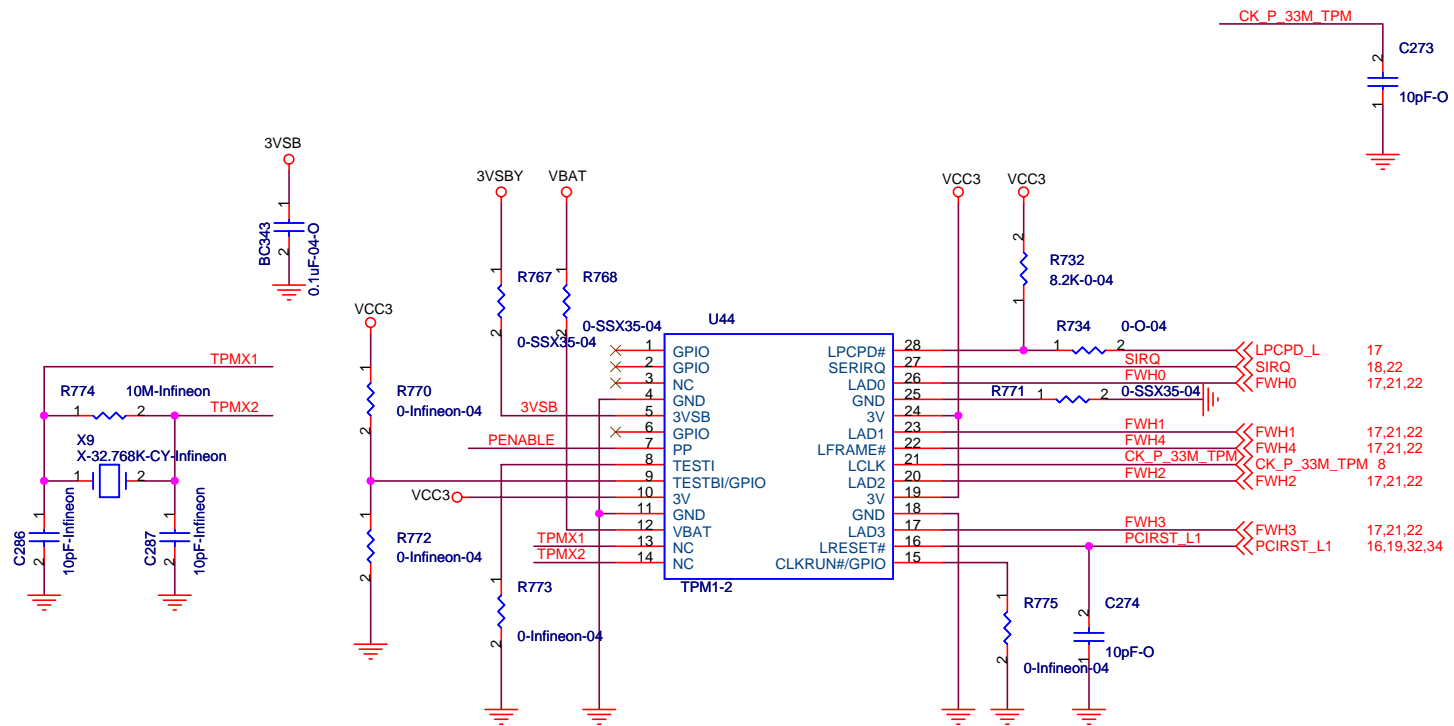
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