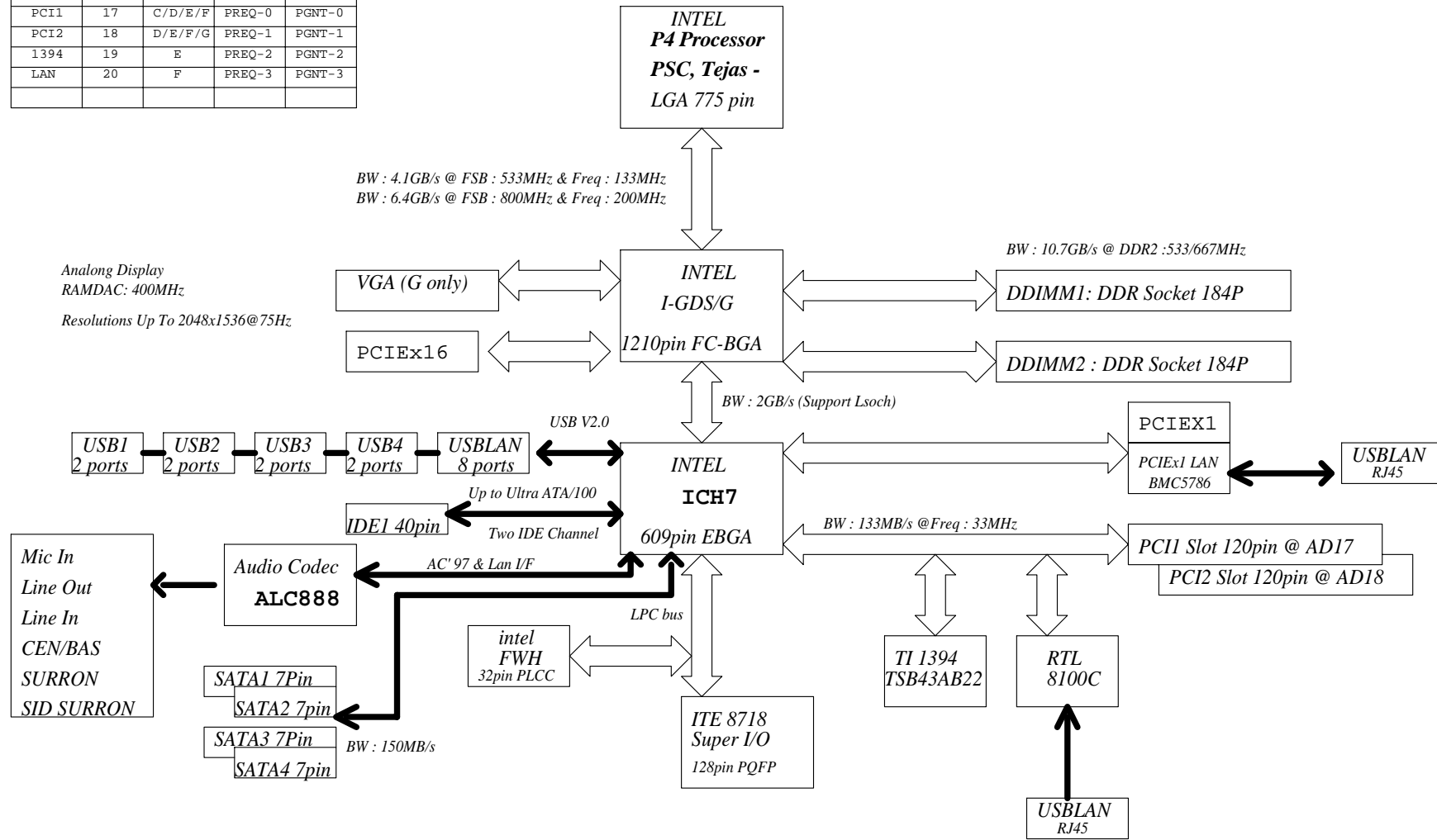
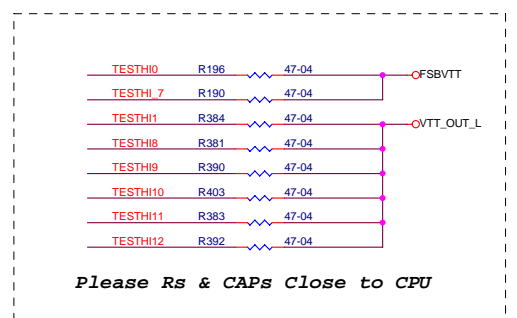
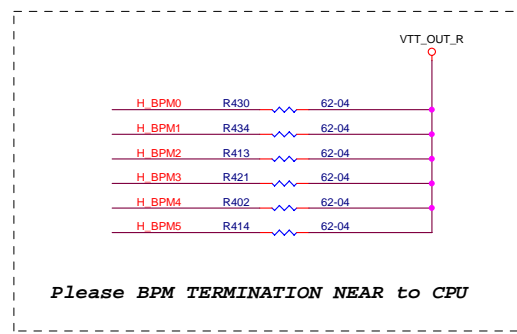
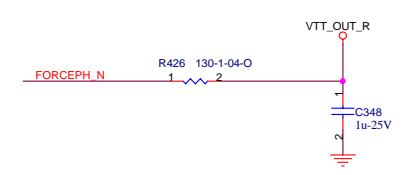
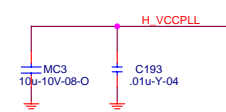
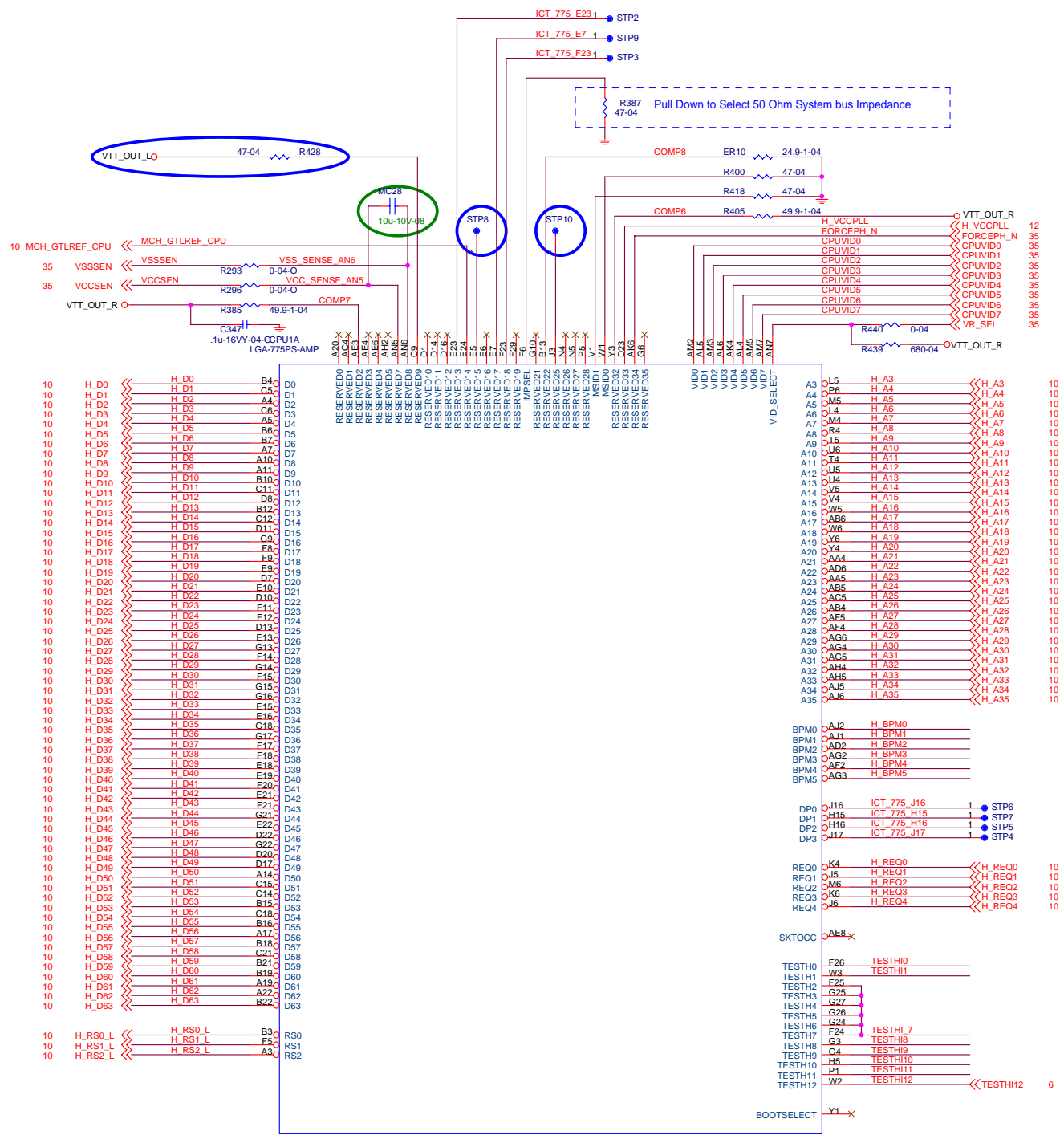


PCI LAN ICH7
 ALC888
 SIZE : Max 2GB (Four 512Mb X 8 Double-Sided DEVICES)

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
1394	19	E	PREQ-2	PGNT-2
LAN	20	F	PREQ-3	PGNT-3



PCB : 244 x 244 mm ; 4 layers



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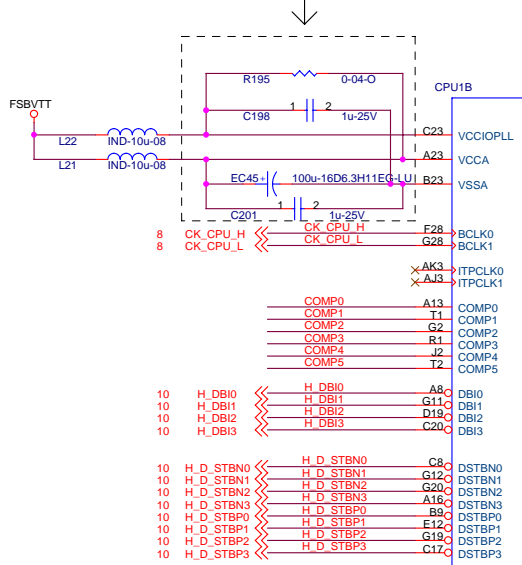
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Size: Document Number **946GZT-AM** Rev: A

Customer: **946GZT-AM**

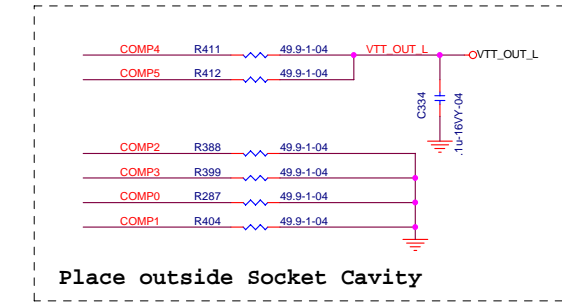
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Place components as close as possible to Processor socket trace width to cap must be no smaller than 12 Mills

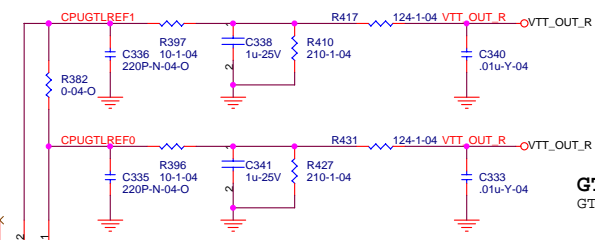


LL= LOAD LINE for load line select
STP14

LGA-775PS-AMP

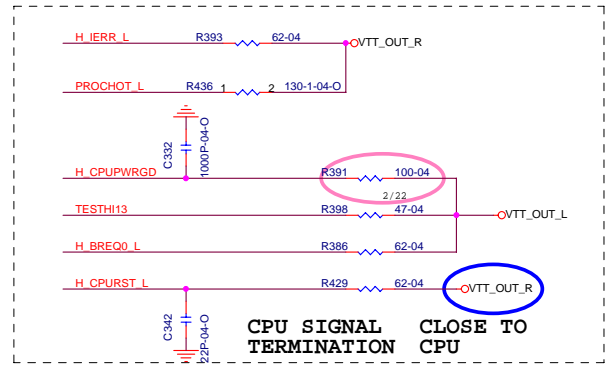


Place outside Socket Cavity

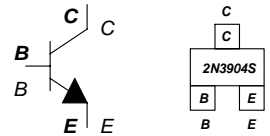
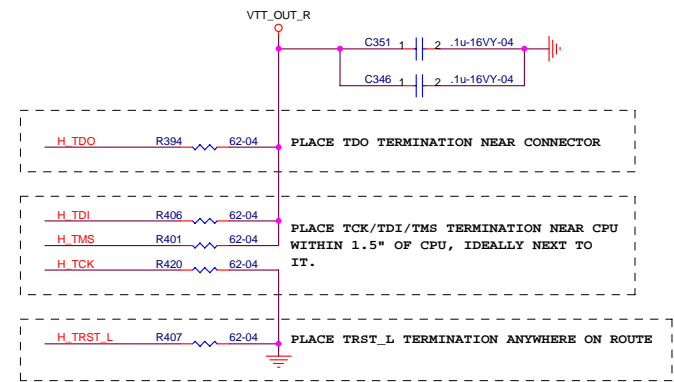
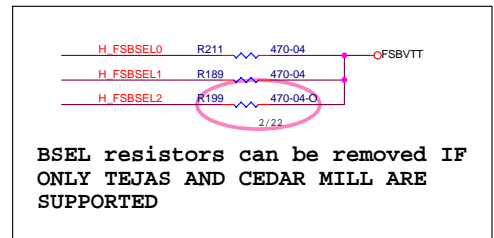


$GTLREF = 0.67 * VTT = 0.8V$
GTLREF GENERATION CIRCUITS

A20M	AD3	A20M_L	A20M_L	20
AD2	H ADS_L	H ADS_L	H ADS_L	10
ADSTB0	H A_STB0	H A_STB0	H A_STB0	10
ADSTB1	H A_STB1	H A_STB1	H A_STB1	10
AD33	X	X	X	10
BNR	H BNR_L	H BNR_L	H BNR_L	10
BPR1	H BPRI_L	H BPRI_L	H BPRI_L	10
BRO	H BREQ0_L	H BREQ0_L	H BREQ0_L	10
DBR	H DBSY_L	HWRST_L	HWRST_L	19,29
DBSY	H DBSY_L	H DBSY_L	H DBSY_L	10
DEFER	H DEFER_L	H DEFER_L	H DEFER_L	10
DRDY	H DRDY_L	H DRDY_L	H DRDY_L	10
EDRDY	FERR_L	STP13	STP13	20
FERR/PBE	H HIT_L	FERR_L	FERR_L	20
HIT	H HITM_L	H HITM_L	H HITM_L	10
HITM	H HITM_L	H HITM_L	H HITM_L	10
IERR	H IERR_L	H IERR_L	H IERR_L	10
IGNNE	IGNNE_L	IGNNE_L	IGNNE_L	20
INIT	HINIT_L	HINIT_L	HINIT_L	20
INIT	H LOCK_L	H LOCK_L	H LOCK_L	10
MCERR	X	X	X	10
PC_REQ	G6	PROCHOT_L	PECI	26
PROCHOT	N1	H CPUPWRGD	PROCHOT_L	35
PWRGOOD	G23	H CPURST_L	H CPURST_L	19
RESET	X	X	X	10
RSP	CH4	TESTHI13	TESTHI13	20
SPL	SMI_L	SMI_L	SMI_L	20
STPCLK	M3	STPCLK_L	STPCLK_L	20
TRDY	E3	H TRDY_L	H TRDY_L	20
TRST	AG1	H TRST_L	H TRST_L	10
THERMDA	AL1	CPU_THERM1	CPU_THERM1	25,26
THERMDC	AK1	THRMDN	THRMDN	25
THERMTRIP	CM2	THERMTRIP_L	THERMTRIP_L	20
BSEL0	G29	H_FSBSSEL0	H_FSBSSEL0	8,10
BSEL1	H30	H_FSBSSEL1	H_FSBSSEL1	8,10
BSEL2	G30	H_FSBSSEL2	H_FSBSSEL2	8,10
APO	U2	ICT_775_U2	STP16	1
API	U3	ICT_775_U3	STP11	1



CPU SIGNAL CLOSE TO TERMINATION CPU



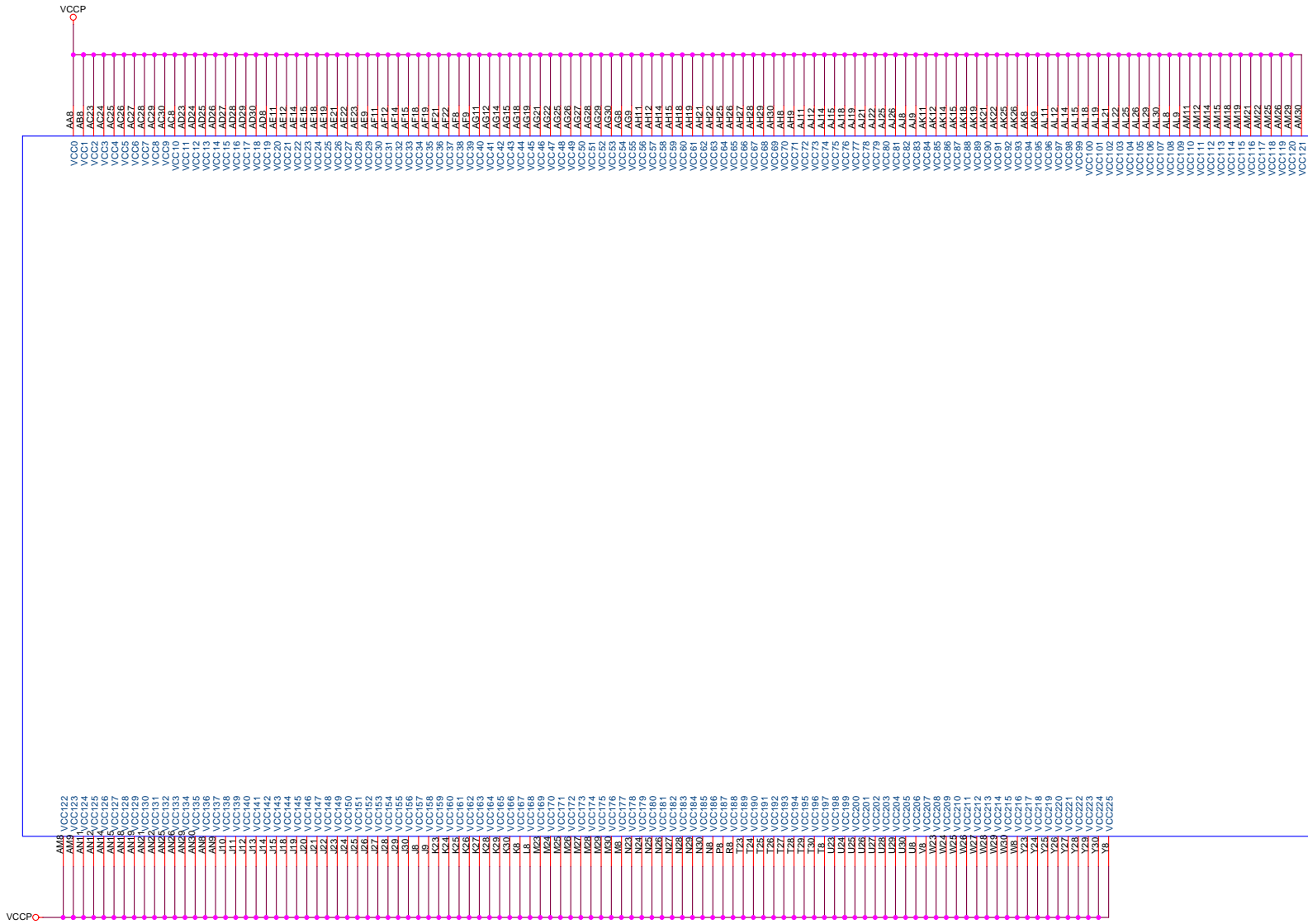
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Title: **LGA 775 Part B**


Size: Document Number: **946GZT-AM**

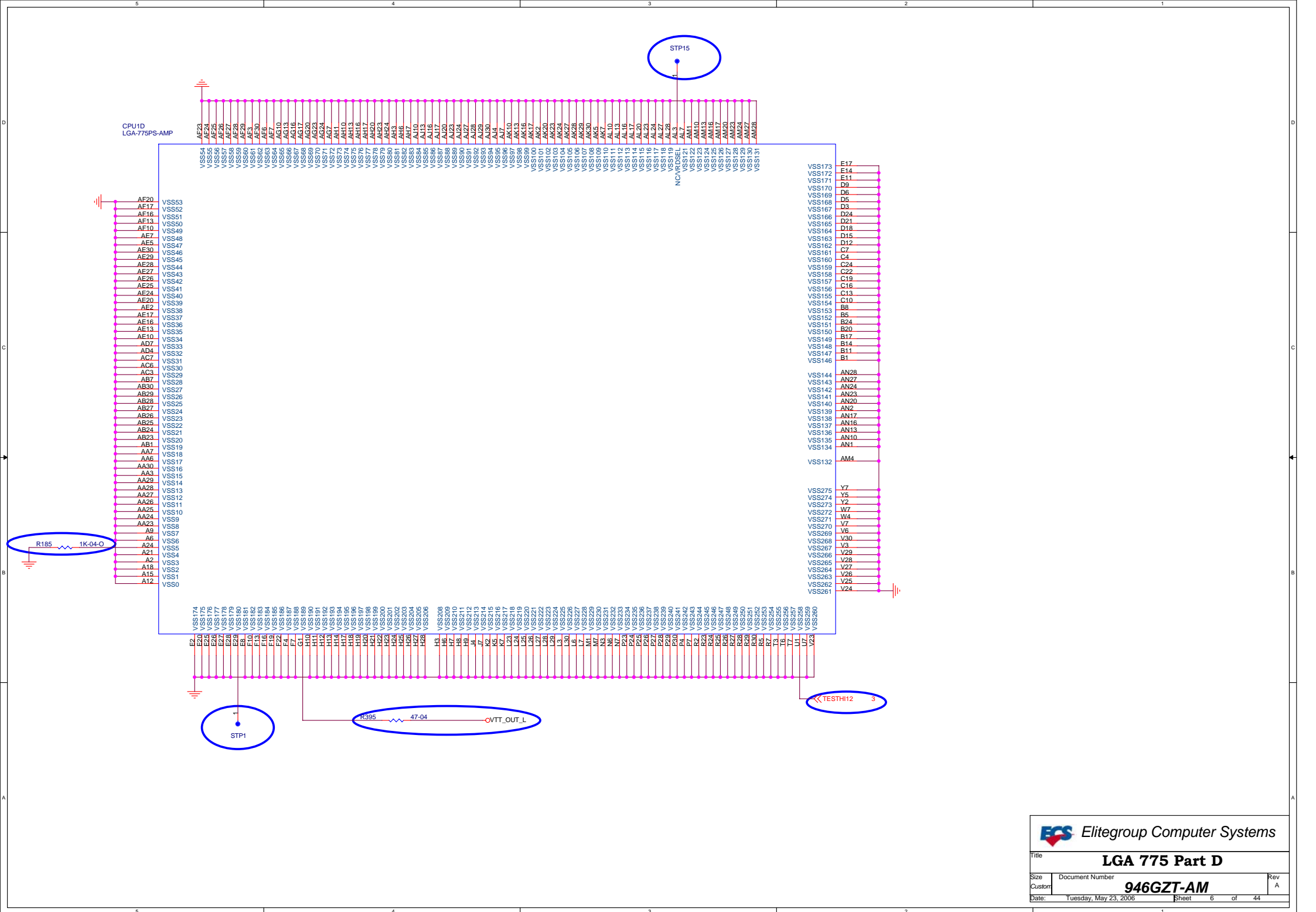
Customer: **946GZT-AM**

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CPU1C
LGA-775PS-AMP

 Elitegroup Computer Systems		
Title LGA 775 Part C		
Size Custom	Document Number 946GZT-AM	Rev A
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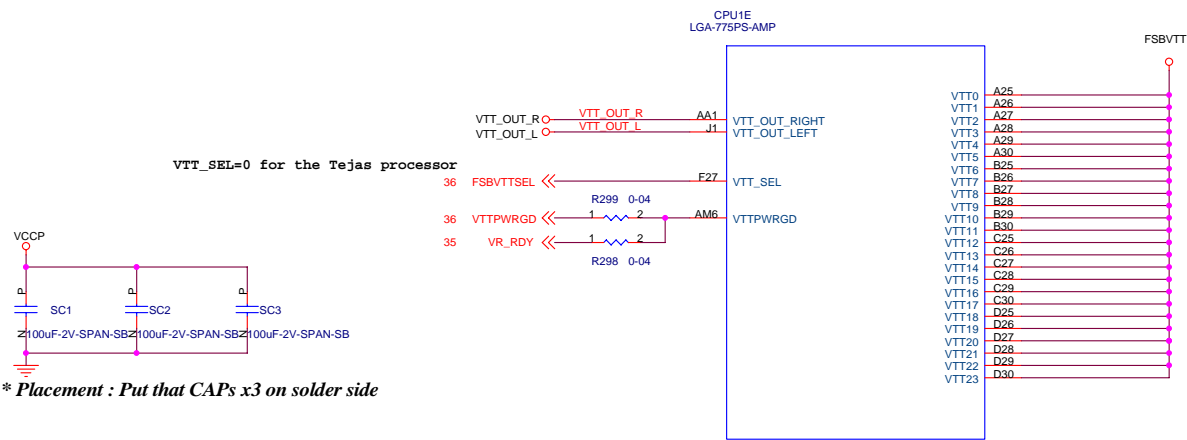
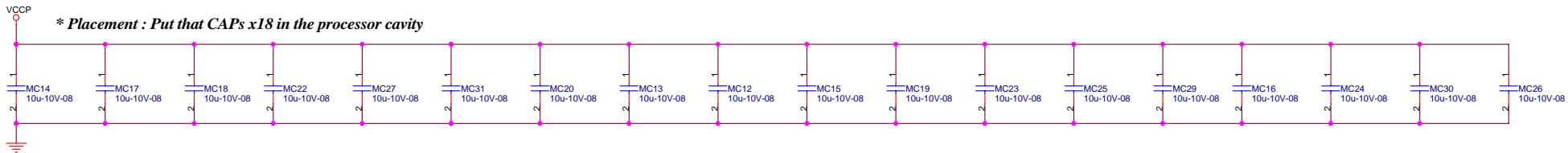


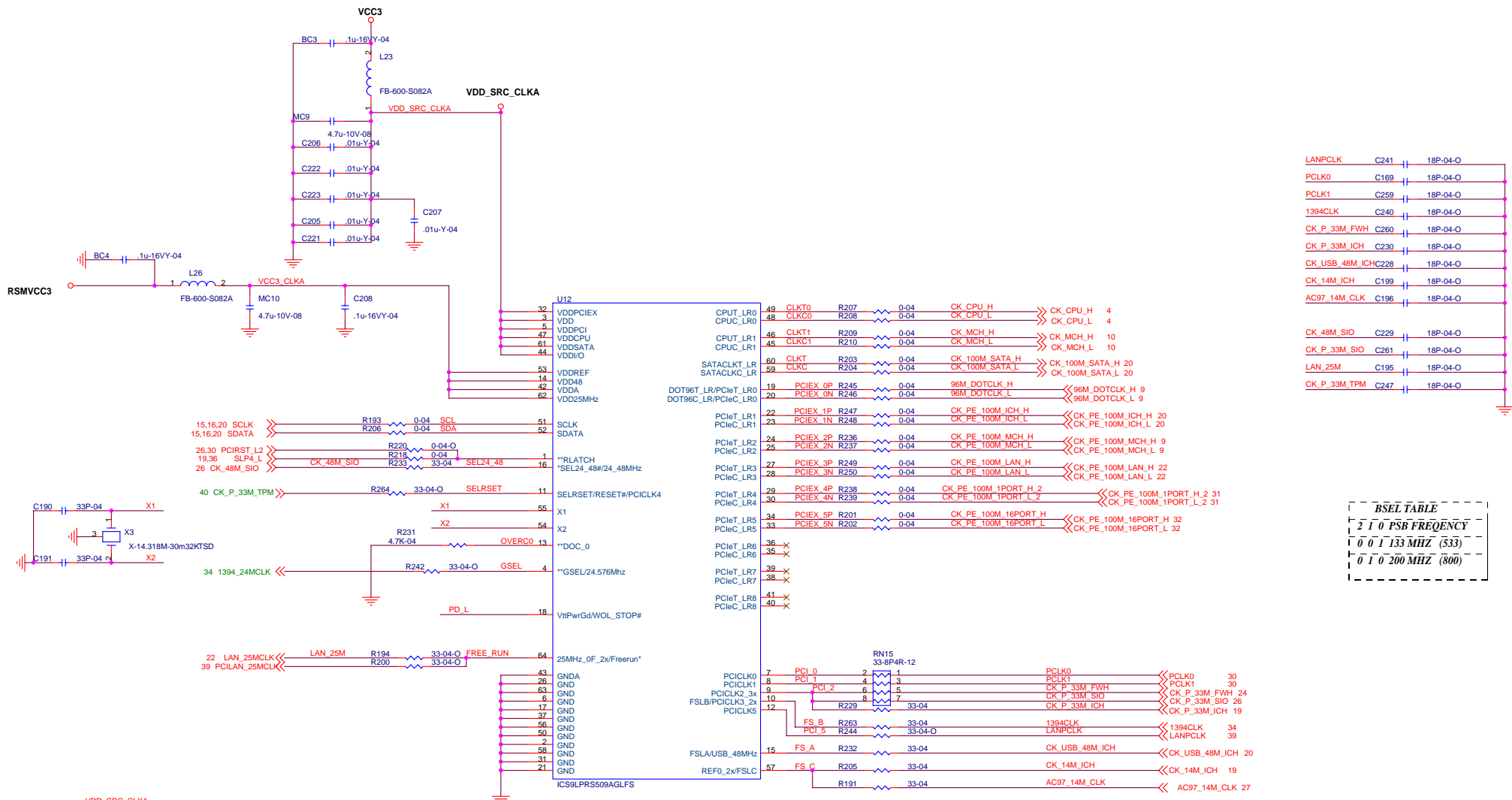
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Title: **LGA 775 Part D**

Size: Custom Document Number: **946GZT-AM** Rev: A

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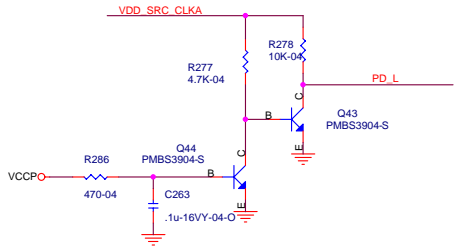




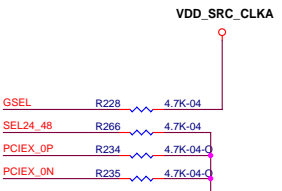
LANPCLK	C241	18P-04-O
PCLK0	C169	18P-04-O
PCLK1	C259	18P-04-O
1394CLK	C240	18P-04-O
CK_P_33M_FWH	C260	18P-04-O
CK_P_33M_ICH	C230	18P-04-O
CK_USB_48M_ICHC228		18P-04-O
CK_14M_ICH	C199	18P-04-O
AC97_14M_CLK	C196	18P-04-O
CK_48M_SIO	C229	18P-04-O
CK_P_33M_SIO	C261	18P-04-O
LAN_25M	C195	18P-04-O
CK_P_33M_TPM	C247	18P-04-O

2	1	0	FSB FREQUENCY
0	0	1	133 MHz (533)
0	1	0	200 MHz (800)

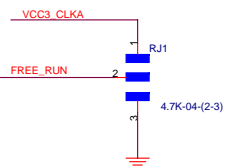
FS_C	R192	10K-04	18P-FSBSEL2	4,10
FS_B	R243	10K-04	18P-FSBSEL1	4,10
FS_A	R265	10K-04	18P-FSBSEL0	4,10



SELRSET = 0 selects PCICLK4



GSEL = 1, selects DOT 96Mhz
*SEL24_48# 0 =48Mhz

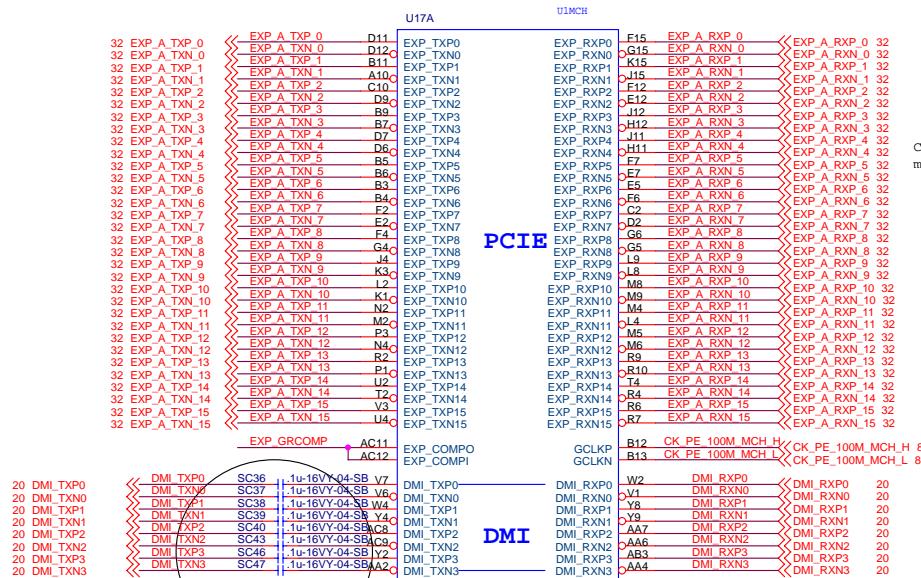


1=25Mhz Free Running
0=25Mhz Stopable

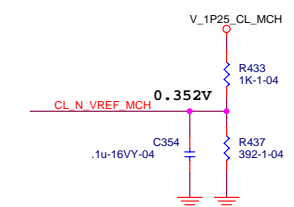
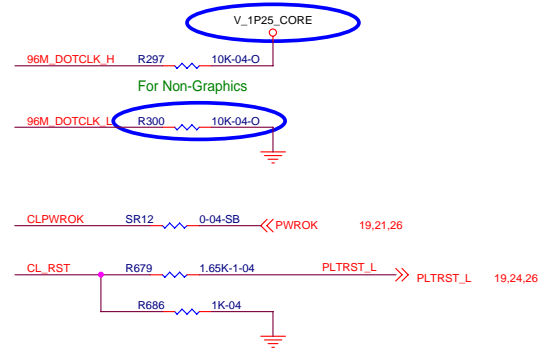
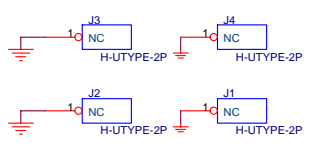
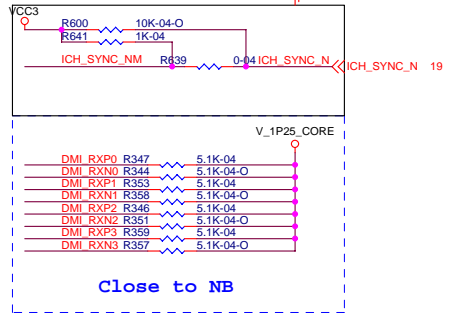
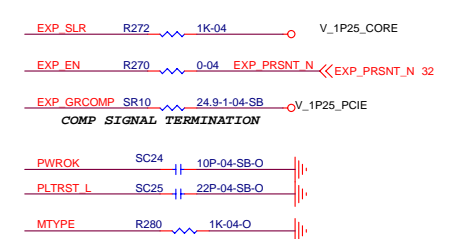
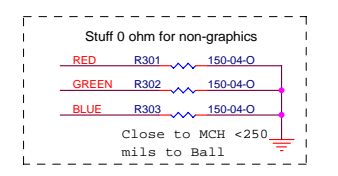
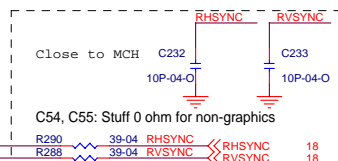
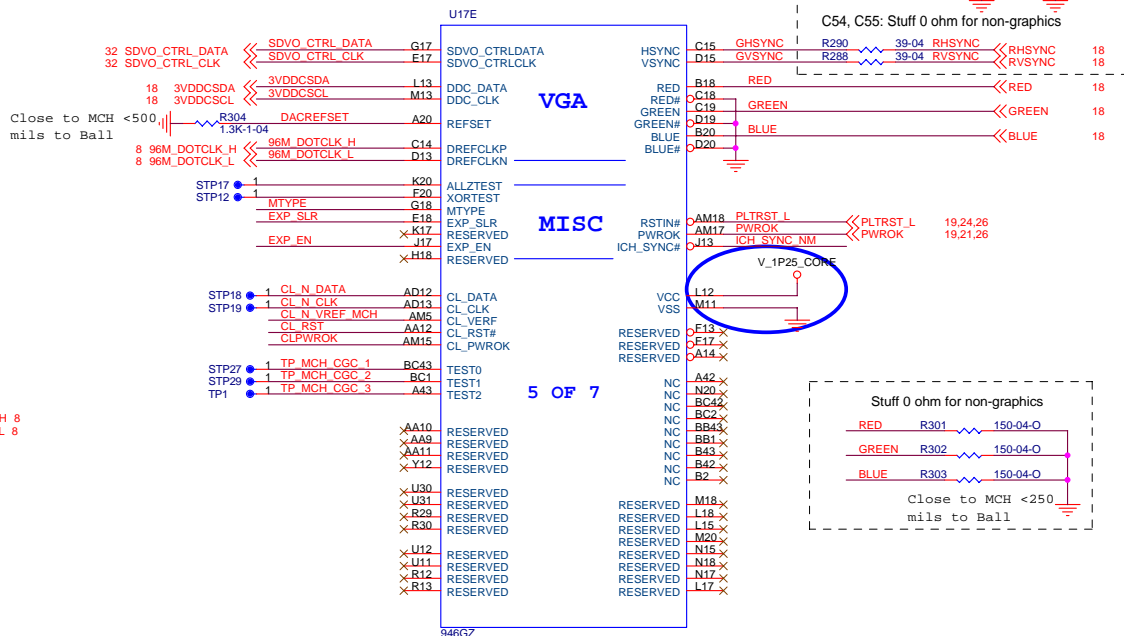
Elitegroup Computer Systems

Clock ICS LPR509

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- 20 DMI_TXP0
- 20 DMI_TXN0
- 20 DMI_TXP1
- 20 DMI_TXN1
- 20 DMI_TXP2
- 20 DMI_TXN2
- 20 DMI_TXP3
- 20 DMI_TXN3



ECS Elitegroup Computer Systems

Title: **BW(MCH) PartA&E**

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U17B U1MCH				
H D0	H D0	R40	HD0	HA#3
H D1	H D1	P41	HD1	HA#4
H D2	H D2	R41	HD2	HA#5
H D3	H D3	N40	HD3	HA#6
H D4	H D4	R42	HD4	HA#7
H D5	H D5	M33	HD5	HA#8
H D6	H D6	N41	HD6	HA#9
H D7	H D7	N42	HD7	HA#10
H D8	H D8	L41	HD8	HA#11
H D9	H D9	L42	HD9	HA#12
H D10	H D10	J41	HD10	HA#13
H D11	H D11	J41	HD11	HA#14
H D12	H D12	K41	HD12	HA#15
H D13	H D13	G40	HD13	HA#16
H D14	H D14	F42	HD14	HA#17
H D15	H D15	F43	HD15	HA#18
H D16	H D16	C42	HD16	HA#19
H D17	H D17	D41	HD17	HA#20
H D18	H D18	F38	HD18	HA#21
H D19	H D19	G37	HD19	HA#22
H D20	H D20	E42	HD20	HA#23
H D21	H D21	E38	HD21	HA#24
H D22	H D22	E37	HD22	HA#25
H D23	H D23	C38	HD23	HA#26
H D24	H D24	B38	HD24	HA#27
H D25	H D25	G33	HD25	HA#28
H D26	H D26	A37	HD26	HA#29
H D27	H D27	F38	HD27	HA#30
H D28	H D28	K32	HD28	HA#31
H D29	H D29	H32	HD29	HA#32
H D30	H D30	H32	HD30	HA#33
H D31	H D31	B34	HD31	HA#34
H D32	H D32	F32	HD32	HA#35
H D33	H D33	M31	HD33	
H D34	H D34	E31	HD34	
H D35	H D35	K31	HD35	
H D36	H D36	G31	HD36	
H D37	H D37	K29	HD37	
H D38	H D38	F31	HD38	
H D39	H D39	J29	HD39	
H D40	H D40	L27	HD40	
H D41	H D41	K27	HD41	
H D42	H D42	H28	HD42	
H D43	H D43	H28	HD43	
H D44	H D44	L28	HD44	
H D45	H D45	J28	HD45	
H D46	H D46	M26	HD46	
H D47	H D47	C33	HD47	
H D48	H D48	E41	HD48	
H D49	H D49	B41	HD49	
H D50	H D50	D40	HD50	
H D51	H D51	D38	HD51	
H D52	H D52	B40	HD52	
H D53	H D53	C38	HD53	
H D54	H D54	C38	HD54	
H D55	H D55	B40	HD55	
H D56	H D56	C38	HD56	
H D57	H D57	D37	HD57	
H D58	H D58	D33	HD58	
H D59	H D59	C34	HD59	
H D60	H D60	B36	HD60	
H D61	H D61	A32	HD61	
H D62	H D62	D32	HD62	
H D63	H D63	D32	HD63	

HREQ0#	F40	H REQ0	<< H REQ0	3
HREQ1#	L38	H REQ1	<< H REQ1	3
HREQ2#	G43	H REQ2	<< H REQ2	3
HREQ3#	J37	H REQ3	<< H REQ3	3
HREQ4#	J37	H REQ4	<< H REQ4	3

H A STB0	M34	H A STB0	<< H A STB0	4
H A STB1	U34	H A STB1	<< H A STB1	4

H D STBP0	L40	H D STBP0	<< H D STBP0	4
H D STBN0	M43	H D STBN0	<< H D STBN0	4
H D DBI0	M40	H D DBI0	<< H D DBI0	4
H D STBP1	G35	H D STBP1	<< H D STBP1	4
H D STBN1	H33	H D STBN1	<< H D STBN1	4
H D DBI1	J33	H D DBI1	<< H D DBI1	4
H D STBP2	G27	H D STBP2	<< H D STBP2	4
H D STBN2	H27	H D STBN2	<< H D STBN2	4
H D DBI2	G29	H D DBI2	<< H D DBI2	4
H D STBP3	B38	H D STBP3	<< H D STBP3	4
H D STBN3	D38	H D STBN3	<< H D STBN3	4
H D DBI3	E33	H D DBI3	<< H D DBI3	4

H ADS L	W40	H ADS L	<< H ADS L	4
H TRDY L	W40	H TRDY L	<< H TRDY L	4
H DRDY L	W41	H DRDY L	<< H DRDY L	4
H DEFER L	T43	H DEFER L	<< H DEFER L	4
H HITM L	Y43	H HITM L	<< H HITM L	4
H HIT L	U42	H HIT L	<< H HIT L	4
H LOCK L	V41	H LOCK L	<< H LOCK L	4
H BREQ0 L	AA42	H BREQ0 L	<< H BREQ0 L	4
H BNR L	W42	H BNR L	<< H BNR L	4
H BPRI L	G39	H BPRI L	<< H BPRI L	4
H DBSY L	U40	H DBSY L	<< H DBSY L	4
H RS0 L	U41	H RS0 L	<< H RS0 L	3
H RS1 L	AA41	H RS1 L	<< H RS1 L	3
H RS2 L	U39	H RS2 L	<< H RS2 L	3
H CPURST L	C31	H CPURST L	<< H CPURST L	4

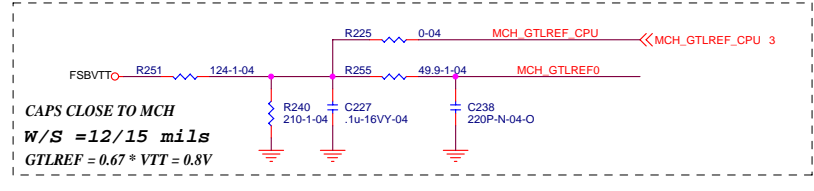
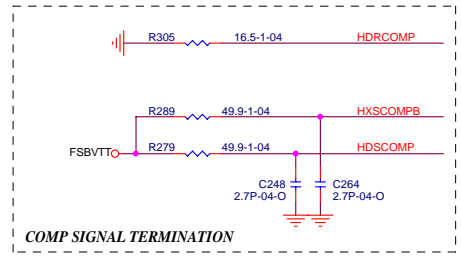
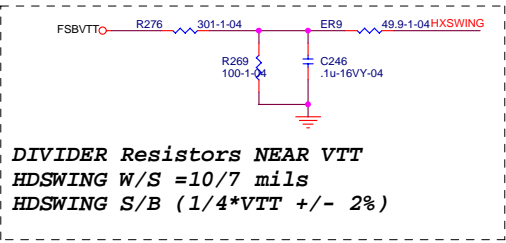
H SWING	B25	HSWING		
H DCOMP	C25	HSCOMP		
H RCOMP	D23	HRCOMP		

MCH_GTLREF0	D24	HDVREF		
	B24	HAVREF		

2 OF 7

BSEL0	G20	BSEL0	R282	10K-04	H_FSBSEL0	4,8
BSEL1	J20	BSEL1	R274	10K-04	H_FSBSEL1	4,8
BSEL2	J18	BSEL2	R273	10K-04	H_FSBSEL2	4,8

CK_MCH_H	CK_MCH_H	R32	HCLKP			
CK_MCH_L	CK_MCH_L	U32	HCLKN			



BSEL TABLE				
2	1	0	PSB	FREQUENCY
0	0	0	267	MHz (1067)
0	0	1	133	MHz (533)
0	1	0	200	MHz (800)

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Title: **BW(MCH) PartB**

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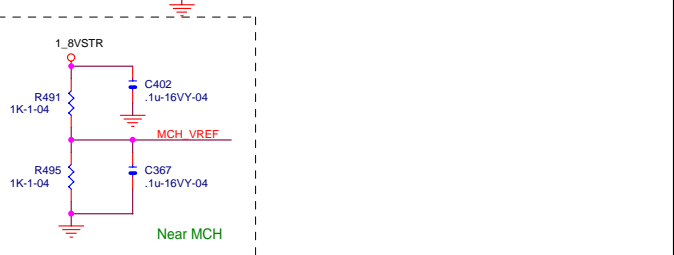
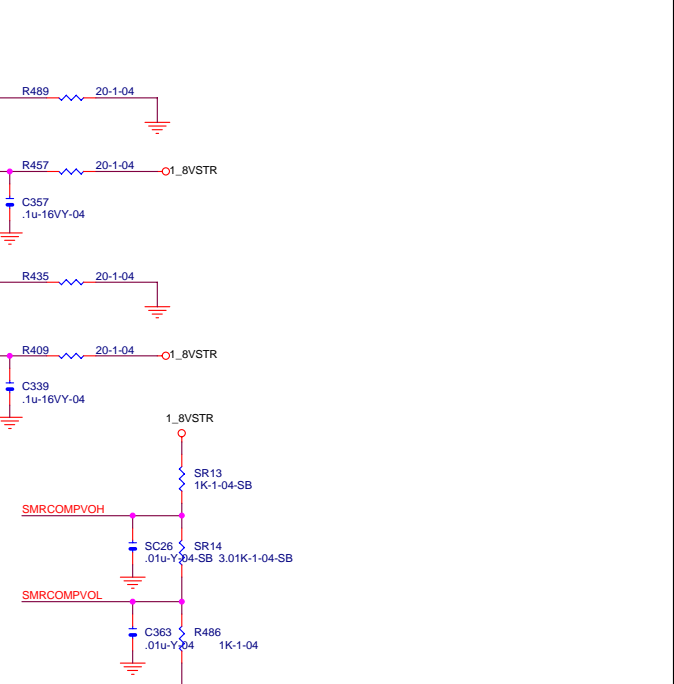
U17C		U1MCH	
DOS_H A4 AR41	SDQS_A4	SDQS_A0	AU4 DOS_H A0
DQS_L A4 AR40C	SDQS_A4#	SDQS_A0#	AR3 DOS_L A0
MPD A4 AU43	SDM_A4	SDM_A0	AR2 MPD A0
MD A32 AV42	SDQ_A32	SDQ_A0	AR5 MD A0
MD A33 AU40	SDQ_A33	SDQ_A1	AR4 MD A1
MD A34 AP42	SDQ_A34	SDQ_A2	AV3 MD A2
MD A35 AN39	SDQ_A35	SDQ_A3	AV2 MD A3
MD A36 AV40	SDQ_A36	SDQ_A4	AP2 MD A4
MD A37 AV41	SDQ_A37	SDQ_A5	AP2 MD A5
MD A38 AR42	SDQ_A38	SDQ_A6	AU1 MD A6
MD A39 AP41	SDQ_A39	SDQ_A7	AV4 MD A7
DQS_H A5 AL41	SDQS_A5	SDQS_A1	BB3 DOS_H A1
DQS_L A5 AL40C	SDQS_A5#	SDQS_A1#	BA4 DOS_L A1
MPD A5 AM43	SDM_A5	SDM_A1	BA2 MPD A1
MD A40 AN41	SDQ_A40	SDQ_A8	MD A8
MD A41 AM39	SDQ_A41	SDQ_A9	AY2 MD A8
MD A42 AK42	SDQ_A42	SDQ_A10	BB5 MD A10
MD A43 AK41	SDQ_A43	SDQ_A11	AV6 MD A11
MD A44 AN40	SDQ_A44	SDQ_A12	AW2 MD A12
MD A45 AN42	SDQ_A45	SDQ_A13	AW3 MD A13
MD A46 AL42	SDQ_A46	SDQ_A14	BA5 MD A14
MD A47 AL39	SDQ_A47	SDQ_A15	BB4 MD A15
DQS_H A6 AG42	SDQS_A6	SDQS_A2	BB9 DOS_H A2
DQS_L A6 AG41C	SDQS_A6#	SDQS_A2#	BA9 DOS_L A2
MPD A6 AG40	SDM_A6	SDM_A2	AY9 MPD A2
MD A48 AJ40	SDQ_A48	SDQ_A16	AY7 MD A16
MD A49 AH43	SDQ_A49	SDQ_A17	BC7 MD A17
MD A50 AF39	SDQ_A50	SDQ_A18	AW11 MD A18
MD A51 AE40	SDQ_A51	SDQ_A19	AY11 MD A19
MD A52 AJ42	SDQ_A52	SDQ_A20	BB6 MD A20
MD A53 AJ44	SDQ_A53	SDQ_A21	BA6 MD A21
MD A54 AF41	SDQ_A54	SDQ_A22	BA10 MD A22
MD A55 AE42	SDQ_A55	SDQ_A23	BB10 MD A23
DQS_H A7 AC42	SDQS_A7	SDQS_A3	AT20 DOS_H A3
DQS_L A7 AC41C	SDQS_A7#	SDQS_A3#	AU18 DOS_L A3
MPD A7 AC40	SDM_A7	SDM_A3	AN18 MPD A3
MD A56 AD40	SDQ_A56	SDQ_A24	AT18 MD A24
MD A57 AD43	SDQ_A57	SDQ_A25	AR18 MD A25
MD A58 AB41	SDQ_A58	SDQ_A26	AU21 MD A26
MD A59 AA40	SDQ_A59	SDQ_A27	AT21 MD A27
MD A60 AE42	SDQ_A60	SDQ_A28	AP17 MD A28
MD A61 AE41	SDQ_A61	SDQ_A29	AN17 MD A29
MD A62 AC39	SDQ_A62	SDQ_A30	AP20 MD A30
MD A63 AB42	SDQ_A63	SDQ_A31	AV20 MD A31
MAAA_0 BA31	SMA_A0	BB34 SWE_L A	
MAAA_1 BB25	SMA_A1	AY35 SCAS_L A	
MAAA_2 BA26	SMA_A2	BB33 SRAS_L A	
MAAA_3 BA25	SMA_A3		
MAAA_4 AY25	SMA_A4	BA33 SBSA_0	
MAAA_5 BA23	SMA_A5	AW32 SBSA_1	
MAAA_6 AY24	SMA_A6	BB21 SBSA_2	
MAAA_7 AY23	SMA_A7		
MAAA_8 BB23	SMA_A8	AW35 CSA_L0	
MAAA_9 BA22	SMA_A9	BA35 CSA_L1	
MAAA_10 AY33	SMA_A10	BA34 CSA_L2	
MAAA_11 BB22	SMA_A11	BB38 CSA_L3	
MAAA_12 AW21	SMA_A12		
MAAA_13 AY38	SMA_A13	BC20 CKEA_0	
MAAA_14 BA21	SMA_A14	AY20 CKEA_1	
		AY21 CKEA_2	
		BA19 CKEA_3	
		AY37 ODTA_0	
		BA38 ODTA_1	
		BB35 ODTA_2	
		BA39 ODTA_3	
		STP28 -1 AU29	
		STP33 -1 L AR29	
		STP30 -1 AV29	
		STP30 -1 AM27	
		STP20 -1 AN33	
		STP22 -1 AP32	
		BB2 RESERVED	
		AW42 RESERVED	
		AN32 RESERVED	
		AM31 RESERVED	
		AG32 RESERVED	
		AF32 RESERVED	
		BB19 RESERVED	

U17D		U1MCH	
DQS_H B4 AW39	SDQS_B4	SDQS_B0	AV6 DOS_H B0
DQS_L B4 AU39	SDQS_B4#	SDQS_B0#	AU5 DOS_L B0
MPD B4 AU37	SDM_B4	SDM_B0	AR7 MPD B0
MD B32 AW37	SDQ_B32	SDQ_B0	AN7 MD B0
MD B33 AV38	SDQ_B33	SDQ_B1	AN8 MD B1
MD B34 AN36	SDQ_B34	SDQ_B2	AW5 MD B2
MD B35 AN37	SDQ_B35	SDQ_B3	AW7 MD B3
MD B36 AU35	SDQ_B36	SDQ_B4	AN5 MD B4
MD B37 AR35	SDQ_B37	SDQ_B5	AN6 MD B5
MD B38 AN35	SDQ_B38	SDQ_B6	AN9 MD B6
MD B39 AR37	SDQ_B39	SDQ_B7	AU7 MD B7
DQS_H B5 AL35	SDQS_B5	SDQS_B1	AR12 DOS_H B1
DQS_L B5 AL34	SDQS_B5#	SDQS_B1#	AP12 DOS_L B1
MPD B5 AM37	SDM_B5	SDM_B1	AW9 MPD B1
MD B40 AM35	SDQ_B40	SDQ_B8	AT11 MD B8
MD B41 AM38	SDQ_B41	SDQ_B9	AU11 MD B9
MD B42 AJ34	SDQ_B42	SDQ_B10	AP13 MD B10
MD B43 AL38	SDQ_B43	SDQ_B11	AR13 MD B11
MD B44 AR39	SDQ_B44	SDQ_B12	AR11 MD B12
MD B45 AM34	SDQ_B45	SDQ_B13	AU9 MD B13
MD B46 AL37	SDQ_B46	SDQ_B14	AV12 MD B14
MD B47 AL32	SDQ_B47	SDQ_B15	AU12 MD B15
DQS_H B6 AG35	SDQS_B6	SDQS_B2	AP15 DOS_H B2
DQS_L B6 AG36	SDQS_B6#	SDQS_B2#	AR15 DOS_L B2
MPD B6 AG39	SDM_B6	SDM_B2	AW13 MPD B2
MD B48 AG38	SDQ_B48	SDQ_B16	AU15 MD B16
MD B49 AJ38	SDQ_B49	SDQ_B17	AV13 MD B17
MD B50 AF35	SDQ_B50	SDQ_B18	AU17 MD B18
MD B51 AF33	SDQ_B51	SDQ_B19	AT17 MD B19
MD B52 AJ37	SDQ_B52	SDQ_B20	AU13 MD B20
MD B53 AJ35	SDQ_B53	SDQ_B21	AM13 MD B21
MD B54 AG33	SDQ_B54	SDQ_B22	AV15 MD B22
MD B55 AF34	SDQ_B55	SDQ_B23	AU17 MD B23
DQS_H B7 AC36	SDQS_B7	SDQS_B3	AT24 DOS_H B3
DQS_L B7 AC37	SDQS_B7#	SDQS_B3#	AU26 DOS_L B3
MPD B7 AD38	SDM_B7	SDM_B3	AP23 MPD B3
MD B56 AD36	SDQ_B56	SDQ_B24	AV24 MD B24
MD B57 AC33	SDQ_B57	SDQ_B25	AT23 MD B25
MD B58 AA34	SDQ_B58	SDQ_B26	AT26 MD B26
MD B59 AA36	SDQ_B59	SDQ_B27	AP26 MD B27
MD B60 AD34	SDQ_B60	SDQ_B28	AU23 MD B28
MD B61 AF38	SDQ_B61	SDQ_B29	AW23 MD B29
MD B62 AC34	SDQ_B62	SDQ_B30	AR24 MD B30
MD B63 AA33	SDQ_B63	SDQ_B31	AN26 MD B31
MAAB_0 BB17	SMA_B0	CBA27 SWE_L B	
MAAB_1 AY17	SMA_B1	CAW26 SCAS_L B	
MAAB_2 BA17	SMA_B2	CAW26 SRAS_L B	
MAAB_3 BC16	SMA_B3		
MAAB_4 AW15	SMA_B4		
MAAB_5 BA15	SMA_B5	AY19 SBSB_0	
MAAB_6 BA15	SMA_B6	BA18 SBSB_1	
MAAB_7 BA14	SMA_B7	BC12 SBSB_2	
MAAB_8 AY15	SMA_B8		
MAAB_9 BB14	SMA_B9	CB27 CSB_L0	
MAAB_10 AW18	SMA_B10	CB30 CSB_L1	
MAAB_11 BB13	SMA_B11	CA27 CSB_L2	
MAAB_12 BA13	SMA_B12	AY31 CSB_L3	
MAAB_13 AY29	SMA_B13		
MAAB_14 AY13	SMA_B14		
DCLKB_H0 AV31	SCKL_B0	AY12 CKEB_0	
DCLKB_L0 AW31	SCKL_B0#	AW12 CKEB_1	
DCLKB_H1 AU27	SCKL_B1	BB11 CKEB_2	
DCLKB_L1 AT27	SCKL_B1#	BA11 CKEB_3	
DCLKB_H2 AV32	SCKL_B2		
DCLKB_L2 AT32	SCKL_B2#		
	SCKL_B3		
	SCKL_B3#		
	SCKL_B4		
	SCKL_B4#		
	SCKL_B5		
	SCKL_B5#		
	SRCOMP0	AN2 SRCOMP0	
	SRCOMP1	AN3 SRCOMP1	
	SRCOMP2	BB40 SRCOMP2	
	SRCOMP3	BA40 SRCOMP3	
	SMRCOMPVOL	AM8 SMRCOMPVOL	
	SMRCOMPVOH	AM10 SMRCOMPVOH	
	RESERVED	AM2X	
	SVREF	AM6 MCH_VREF	
	RESERVED	AP21X	
	RESERVED	AA33X	

DDR_0		3 OF 7	
DCLKA_H0 AU31	SCKL_A0		
DCLKA_L0 AR31	SCKL_A0#		
DCLKA_H1 AP27	SCKL_A1		
DCLKA_L1 AN27	SCKL_A1#		
DCLKA_H2 AV33	SCKL_A2		
DCLKA_L2 AW33	SCKL_A2#		
STP25 -1 AP29	SCKL_A3		
STP31 -1 AP31	SCKL_A3#		
STP21 -1 AM26	SCKL_A4		
STP23 -1 AM27	SCKL_A4#		
STP26 -1 AT33	SCKL_A5		
STP24 -1 AU33	SCKL_A5#		
	RESERVED		

DDR_1		4 OF 7	
DCLKB_H0 AV31	SCKL_B0		
DCLKB_L0 AW31	SCKL_B0#		
DCLKB_H1 AU27	SCKL_B1		
DCLKB_L1 AT27	SCKL_B1#		
DCLKB_H2 AV32	SCKL_B2		
DCLKB_L2 AT32	SCKL_B2#		
	SCKL_B3		
	SCKL_B3#		
	SCKL_B4		
	SCKL_B4#		
	SCKL_B5		
	SCKL_B5#		
	SRCOMP0		
	SRCOMP1		
	SRCOMP2		
	SRCOMP3		
	SMRCOMPVOL		
	SMRCOMPVOH		
	RESERVED		
	SVREF		
	RESERVED		
	RESERVED		
	RESERVED		
	RESERVED		

AV6 DOS_H B0	MD A10_63]	MD A10_63]
AU5 DOS_L B0	DQS_L A10_7]	DQS_L B10_7]
AR7 MPD B0	DOS_H A10_7]	DOS_H B10_7]
AN7 MD B0	MPD A10_7]	MPD B10_7]
AN8 MD B1	MAAA_0_14]	MAAA_0_14]
AW5 MD B2	CSA_L10_3]	CSA_L_10_3]
AW7 MD B3	CKEA_0_3]	CKEA_0_3]
AN5 MD B4		
AN6 MD B5		
AN9 MD B6		
AU7 MD B7		
AR12 DOS_H B1	ODTB_0_3]	ODTB_0_3]
AP12 DOS_L B1	SBSA_0_2]	SBSA_0_2]
AW9 MPD B1	SWE_L B	SWE_L B
AT11 MD B8	SCAS_L B	SCAS_L B
AU11 MD B9	SRAS_L B	SRAS_L B
AP13 MD B10		
AR13 MD B11		
AR11 MD B12		
AU9 MD B13		
AV12 MD B14		
AU12 MD B15		
AP15 DOS_H B2		
AR15 DOS_L B2		
AW13 MPD B2		
AU15 MD B16		
AV13 MD B17		
AU17 MD B18		
AT17 MD B19		
AU13 MD B20		
AM13 MD B21		
AV15 MD B22		
AU17 MD B23		
AT24 DOS_H B3		
AU26 DOS_L B3		
AP23 MPD B3		
AV24 MD B24		
AT23 MD B25		
AT26 MD B26		
AP26 MD B27		
AU23 MD B28		
AW23 MD B29		
AR24 MD B30		
AN26 MD B31		
CBA27 SWE_L B		
CAW26 SCAS_L B		
CAW26 SRAS_L B		
AY19 SBSB_0		
BA18 SBSB_1		
BC12 SBSB_2		
CB27 CSB_L0		
CB30 CSB_L1		
CA27 CSB_L2		
AY31 CSB_L3		
AY12 CKEB_0		
AW12 CKEB_1		
BB11 CKEB_2		
BA11 CKEB_3		
BA23 ODTB_0		
BA20 ODTB_1		
BB29 ODTB_2		
BB31 ODTB_3		
AN2 SRCOMP0		
AN3 SRCOMP1		
BB40 SRCOMP2		
BA40 SRCOMP3		
AM8 SMRCOMPVOL		
AM10 SMRCOMPVOH		
AM2X		
AM6 MCH_VREF		
AP21X		
AA33X		
DCLKB_L10_2]	DCLKB_L10_2]	DCLKB_L10_2]
DCLKB_H10_2]	DCLKB_H10_2]	DCLKB_H10_2]
DCLKA_L10_2]	DCLKA_L10_2]	DCLKA_L10_2]
DCLKA_H10_2]	DCLKA_H10_2]	DCLKA_H10_2]
MD B10_63]	MD B10_63]	MD B10_63]
DQS_L B10_7]	DQS_L B10_7]	DQS_L B10_7]
DOS_H B10_7]	DOS_H B10_7]	DOS_H B10_7]
MPD B10_7]	MPD B10_7]	MPD B10_7]
MAAB_0_14]	MAAB_0_14]	MAAB_0_14]
CSB_L10_3]	CSB_L10_3]	CSB_L10_3]
CKEB_0_3]	CKEB_0_3]	CKEB_0_3]
ODTB_0_3]	ODTB_0_3]	ODTB_0_3]
SBSB_0_2]	SBSB_0_2]	SBSB_0_2]
SWE_L B	SWE_L B	SWE_L B
SCAS_L B	SCAS_L B	SCAS_L B
SRAS_L B	SRAS_L B	SRAS_L B



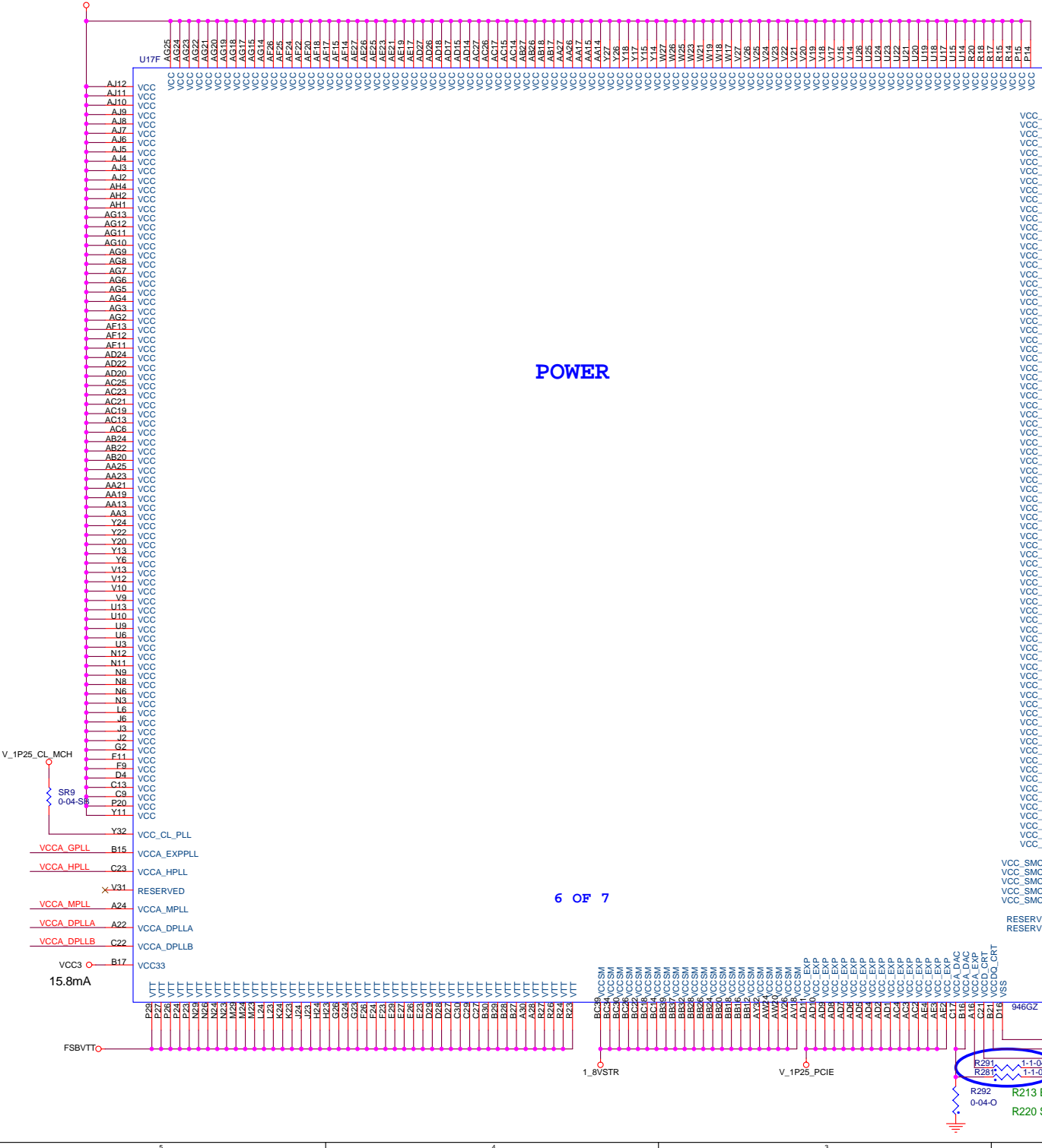
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File: **BW(MCH) PartC&D**

Size: Document Number **946GZT-AM** Rev: A

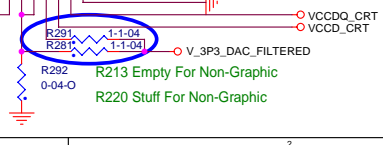
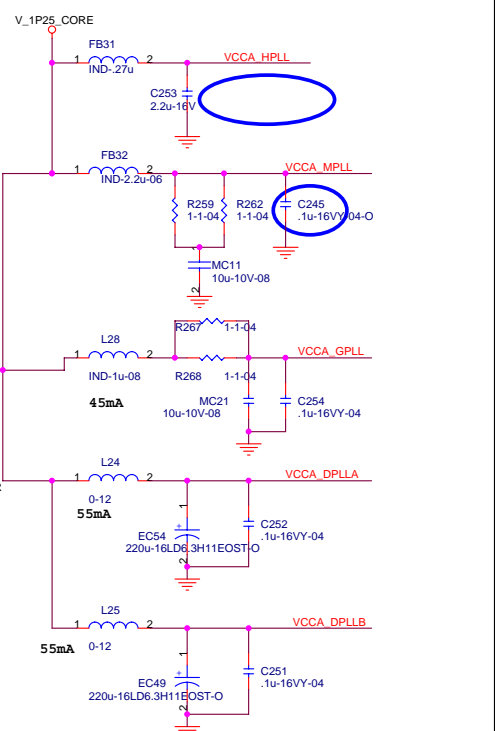
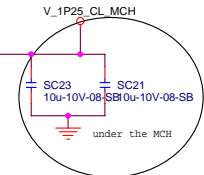
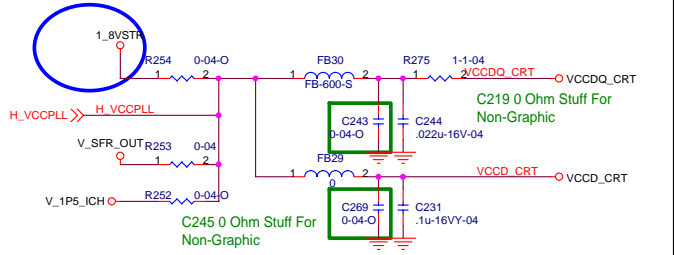
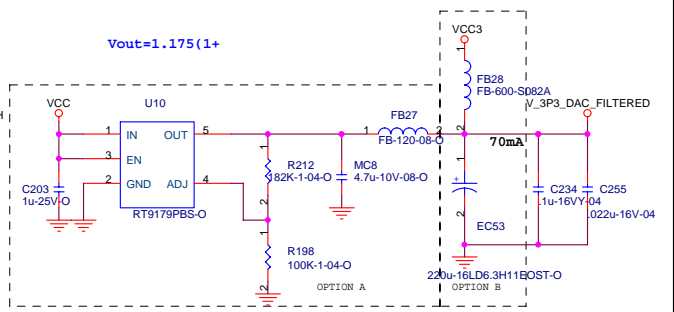
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POWER

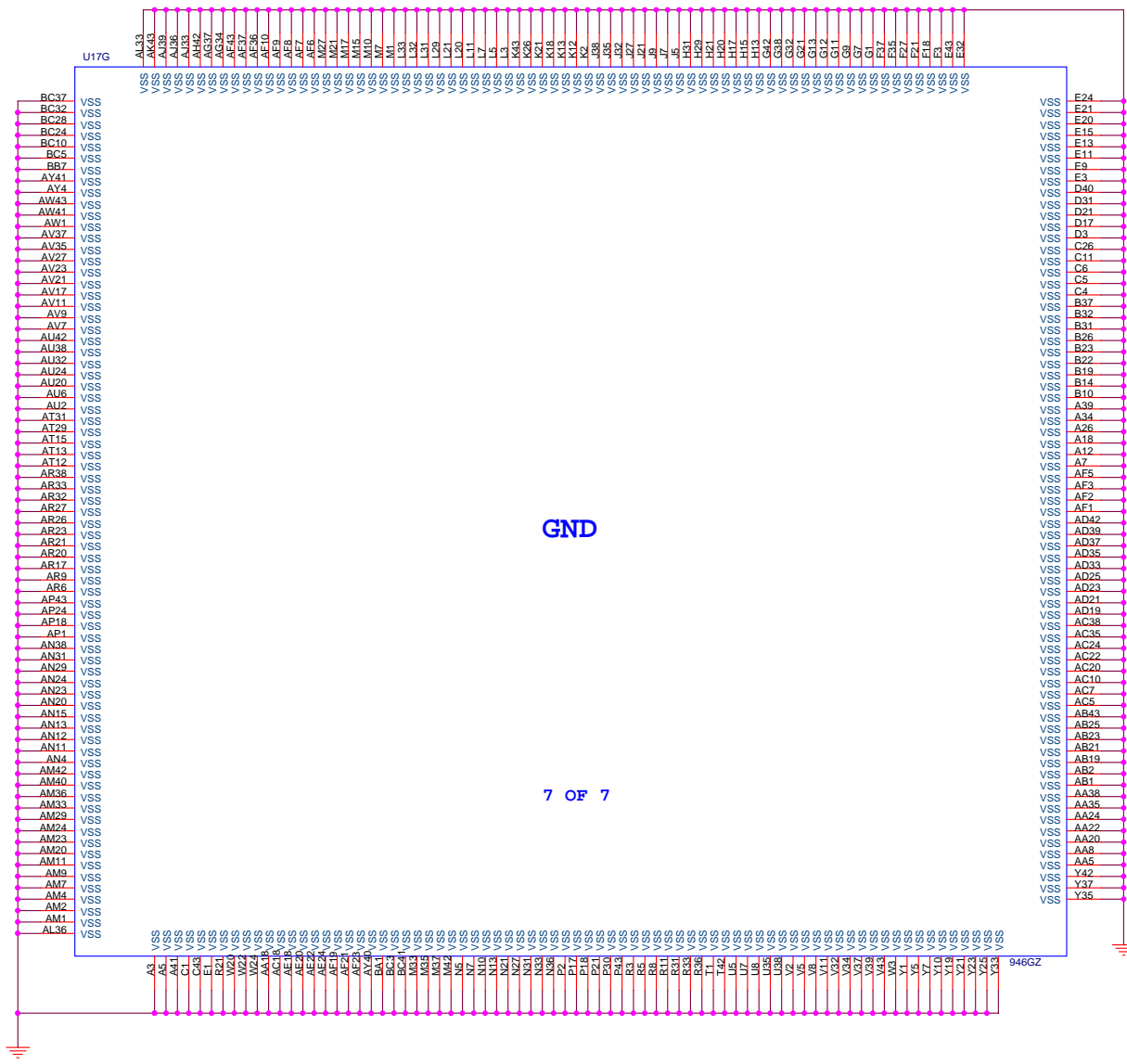
6 OF 7

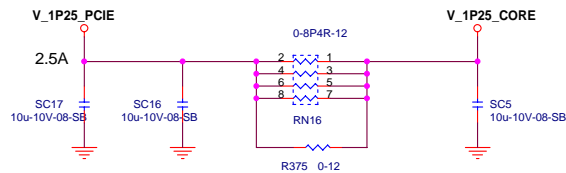
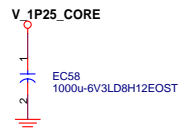
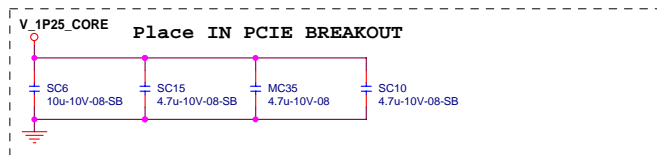
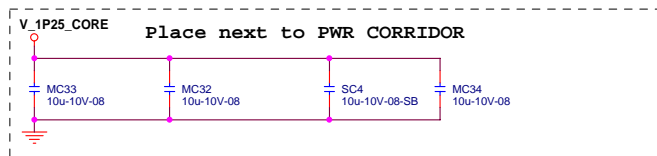
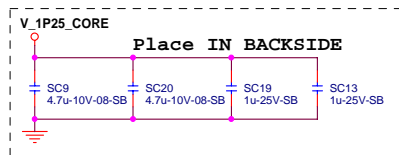
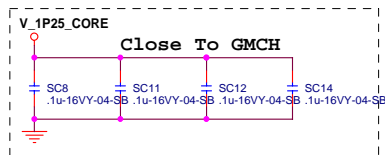
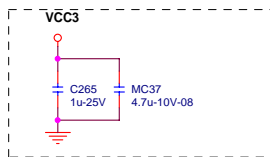
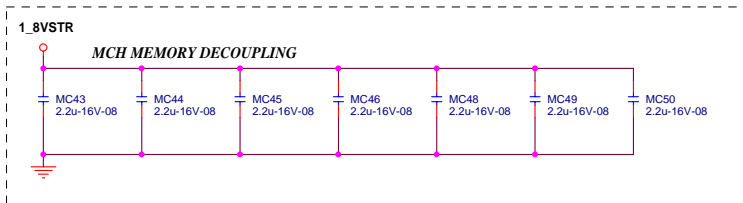
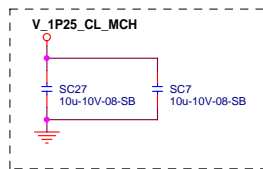
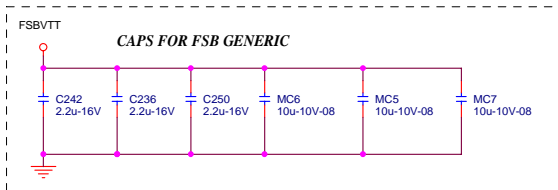


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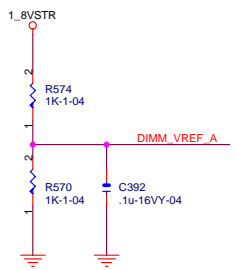
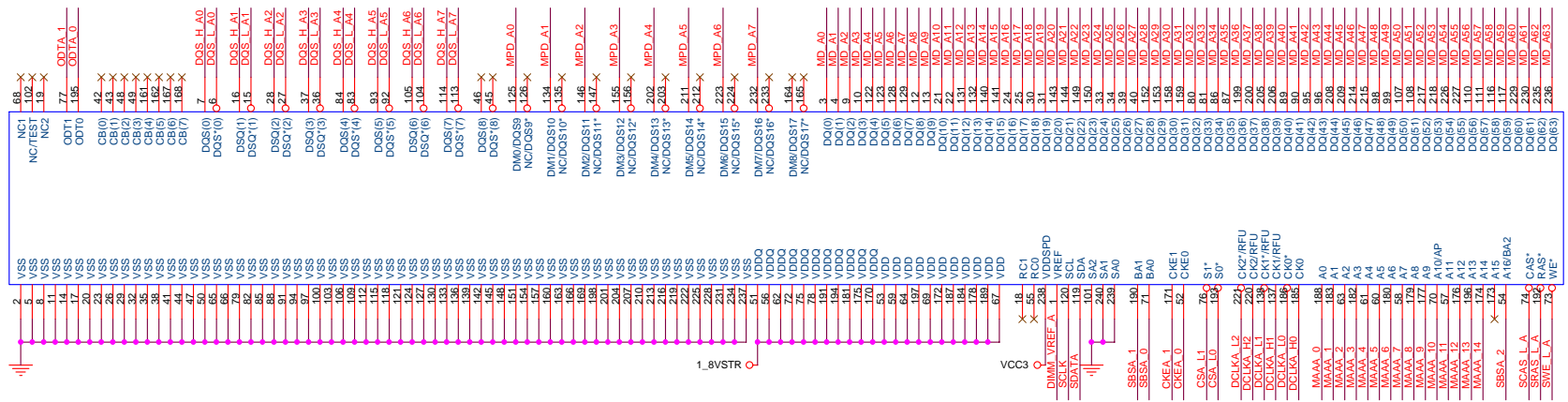
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 Custor: **946GZT-AM**
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DIMM1
DDR2-8L-0RA



- 11 MD_A[0..63] << MD A[0..63]
- 11 DQS_L_A[0..7] << DQS L A[0..7]
- 11 DQS_H_A[0..7] << DQS H A[0..7]
- 11 MPD_A[0..7] << MPD A[0..7]
- 11 MAAA_0[0..14] << MAAA_0[0..14]
- 11 CSA_L[0..3] << CSA L[0..3]
- 11 CKEA_0[0..3] << CKEA_0[0..3]
- 11 DCLKA_L[0..2] << DCLKA L[0..2]
- 11 DCLKA_H[0..2] << DCLKA H[0..2]
- 11 ODTA_0[0..3] << ODTA_0[0..3]
- 11 SBASA_0[0..2] << SBASA_0[0..2]
- 11 SWE_L_A << SWE_L_A
- 11 SCAS_L_A << SCAS_L_A
- 11 SRAS_L_A << SRAS_L_A

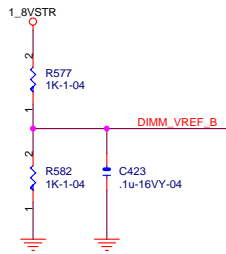
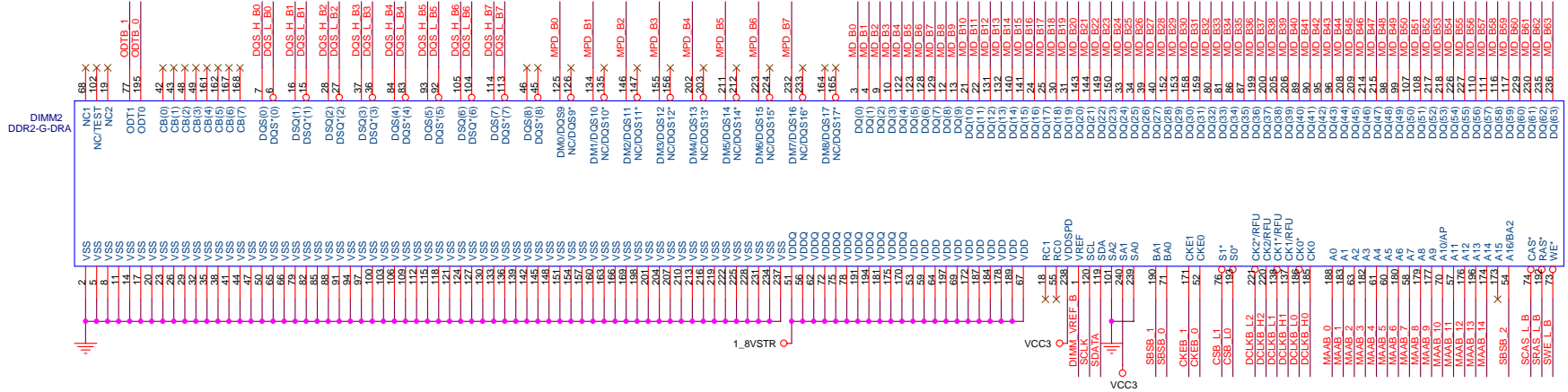
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- MAAA 7 R546 33-04
- MAAA 11 R544 33-04
- MAAA 12 R543 33-04
- MAAA 10 R557 33-04
- MAAA 0 R555 33-04
- MAAA 1 R552 33-04
- MAAA 2 R553 33-04
- MAAA 4 R550 33-04
- MAAA 6 R549 33-04
- MAAA 8 R547 33-04
- MAAA 5 R548 33-04
- MAAA 13 R564 33-04
- MAAA 3 R551 33-04
- MAAA 14 R541 33-04
- SCAS_L_A R562 33-04
- SWE_L_A R561 33-04
- SRAS_L_A R559 33-04

VTT_DDR

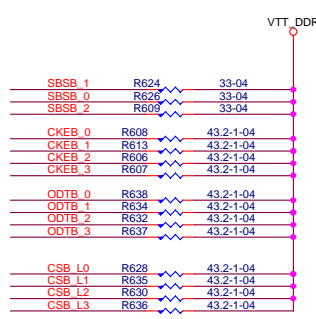
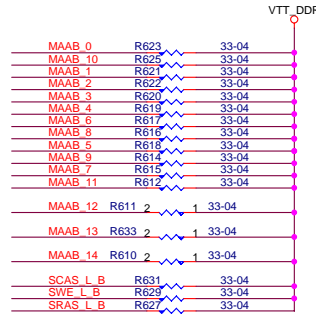
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- SBASA 1 R556 33-04
- SBASA 2 R542 33-04
- CKEA 0 R539 43.2-1-04
- CKEA 1 R538 43.2-1-04
- CKEA 2 R540 43.2-1-04
- CKEA 3 R537 43.2-1-04
- CSA L0 R561 43.2-1-04
- CSA L1 R568 43.2-1-04
- CSA L2 R560 43.2-1-04
- CSA L3 R565 43.2-1-04
- ODTA 0 R578 43.2-1-04
- ODTA 1 R566 43.2-1-04
- ODTA 2 R563 43.2-1-04
- ODTA 3 R567 43.2-1-04



Title		
DIMM1(DDR2SDRAM)		
Size	Document Number	Rev
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- 11 MD_B[0..63] << MD_B[0..63]
- 11 DQS_L_B[0..7] << DQS_L_B[0..7]
- 11 DQS_H_B[0..7] << DQS_H_B[0..7]
- 11 MPD_B[0..7] << MPD_B[0..7]
- 11 MAAB_[0..14] << MAAB_[0..14]
- 11 CSB_L[0..3] << CSB_L[0..3]
- 11 CKEB_[0..3] << CKEB_[0..3]
- 11 DCLKB_L[0..2] << DCLKB_L[0..2]
- 11 DCLKB_H[0..2] << DCLKB_H[0..2]
- 11 ODTB_[0..3] << ODTB_[0..3]
- 11 SBSB_[0..2] << SBSB_[0..2]
- 11 SWE_L_B << SWE_L_B
- 11 SCAS_L_B << SCAS_L_B
- 11 SRAS_L_B << SRAS_L_B
- 8,15,20 SDATA << SDATA
- 8,15,20 SCLK << SCLK

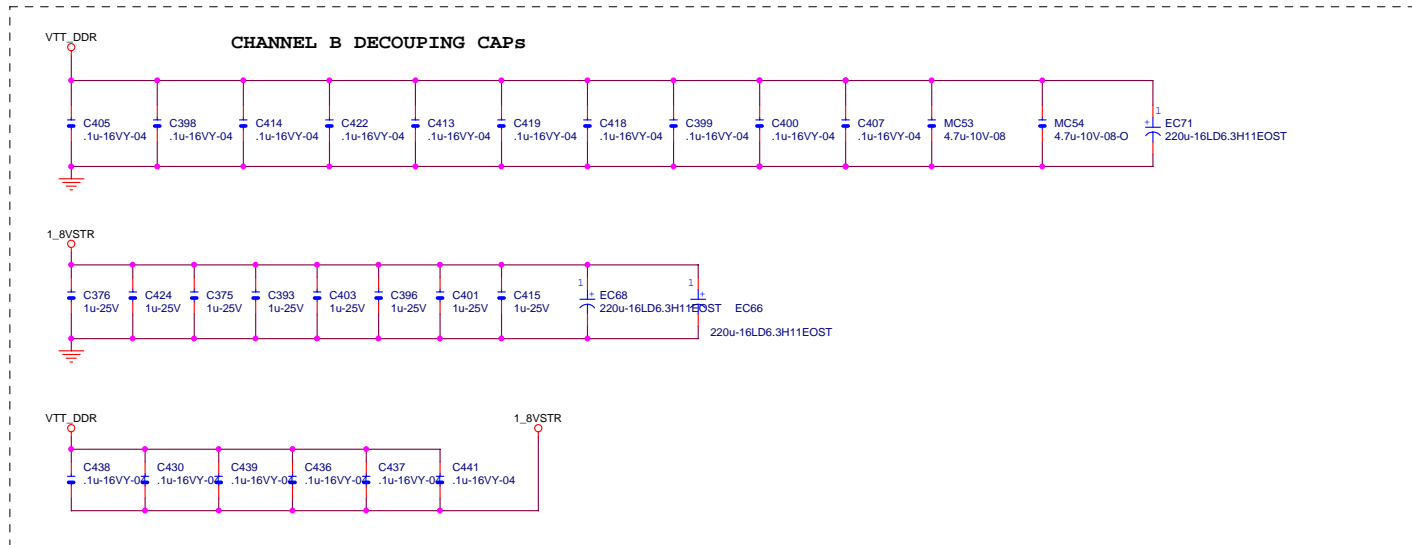
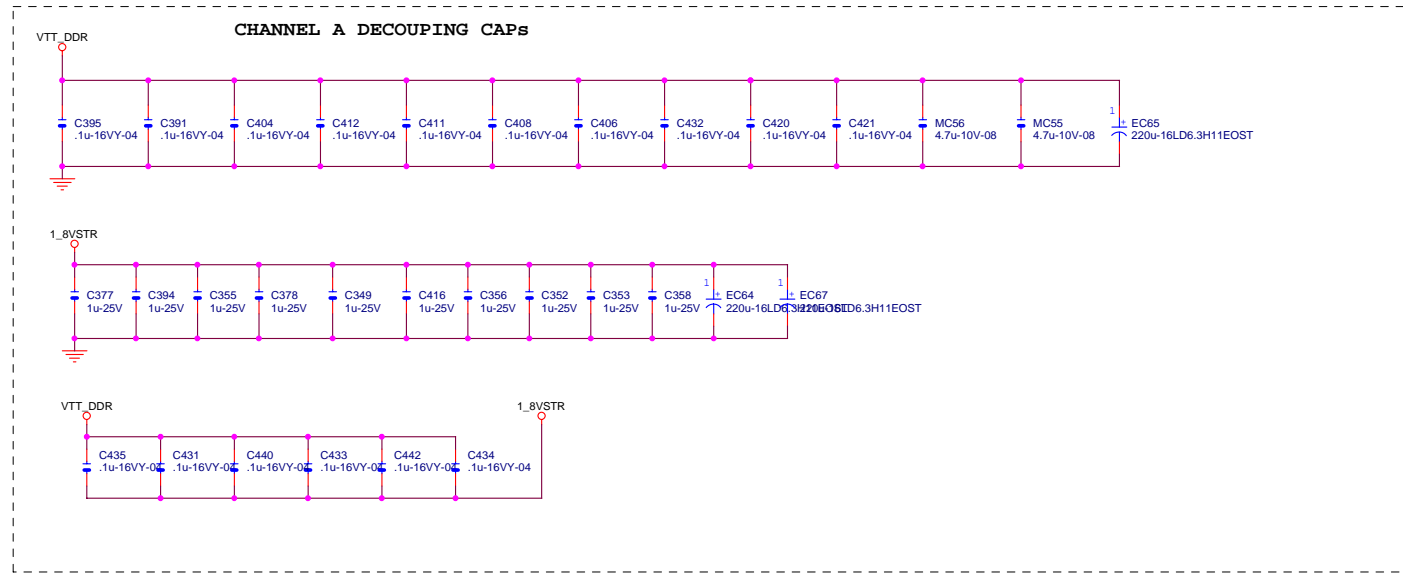


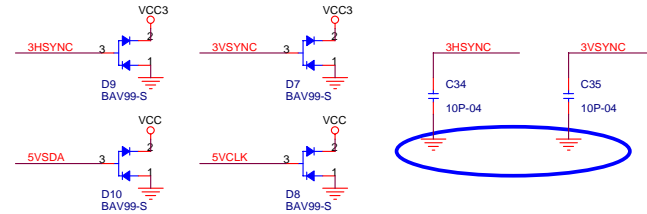
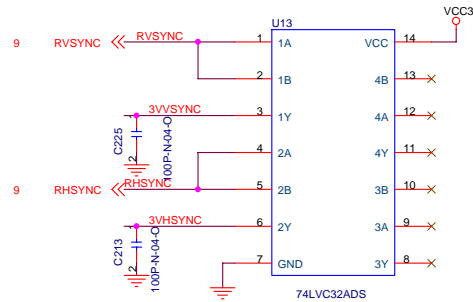
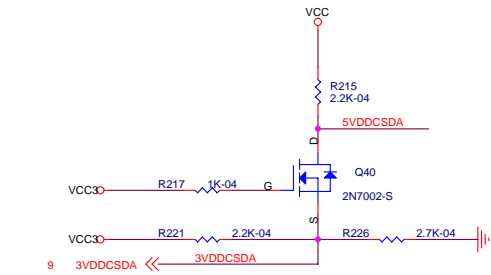
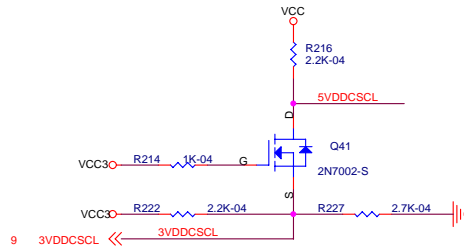
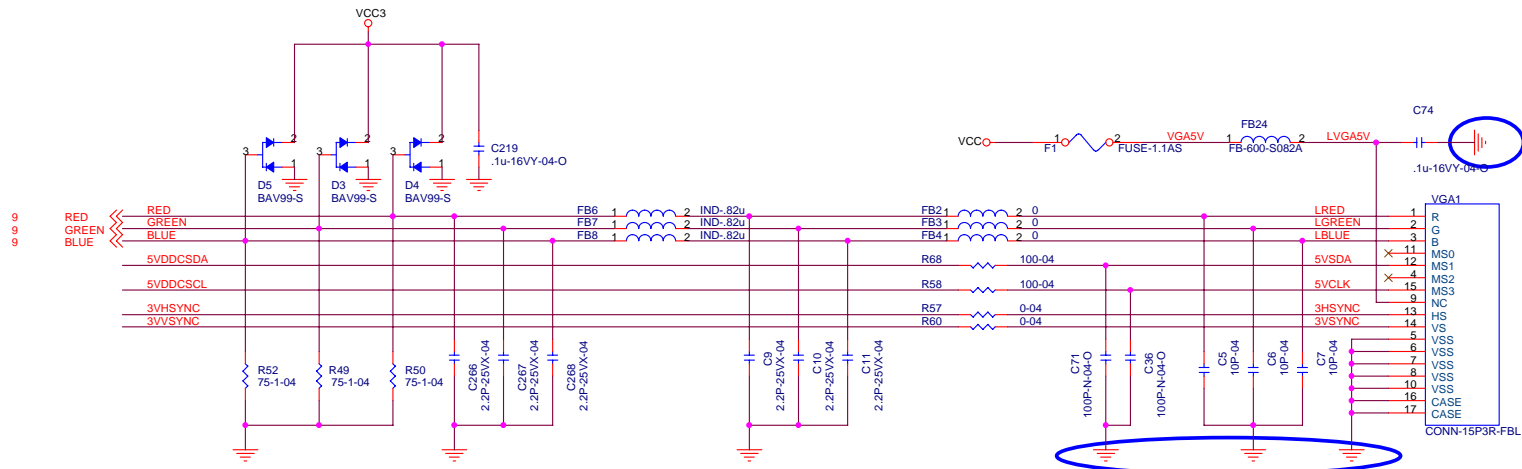
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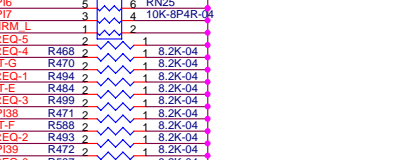
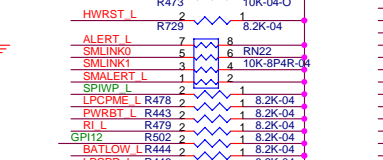
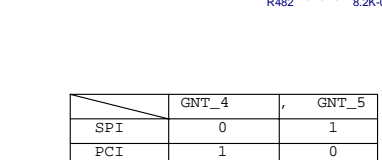
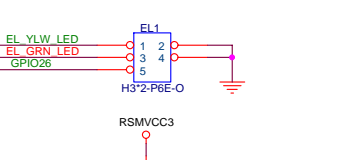
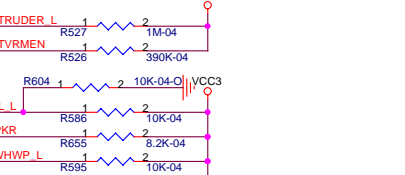
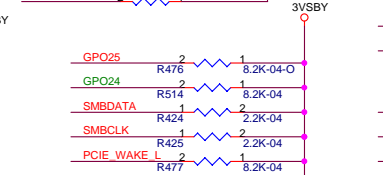
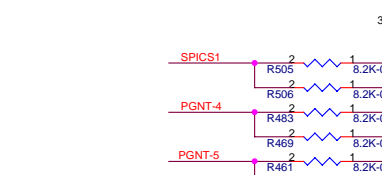
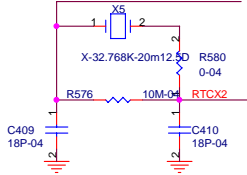
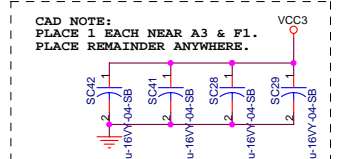
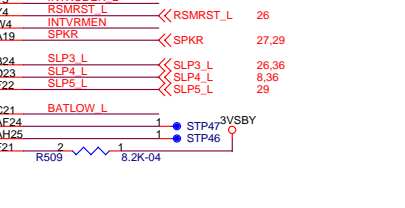
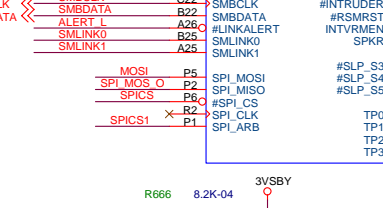
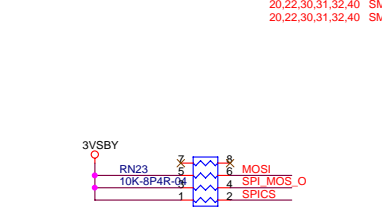
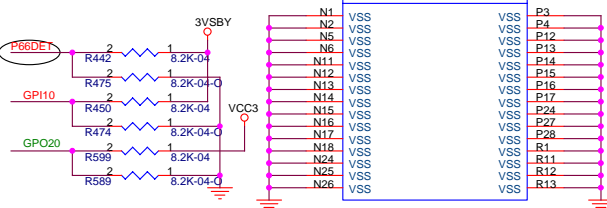
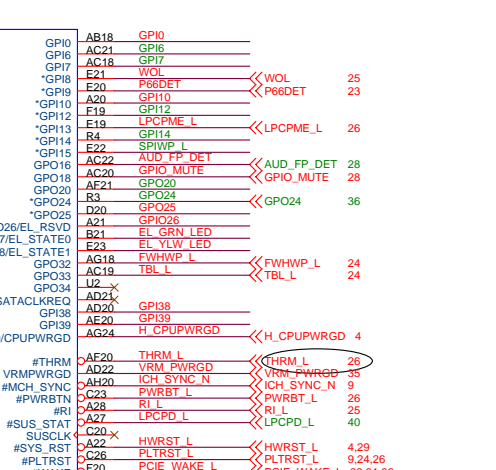
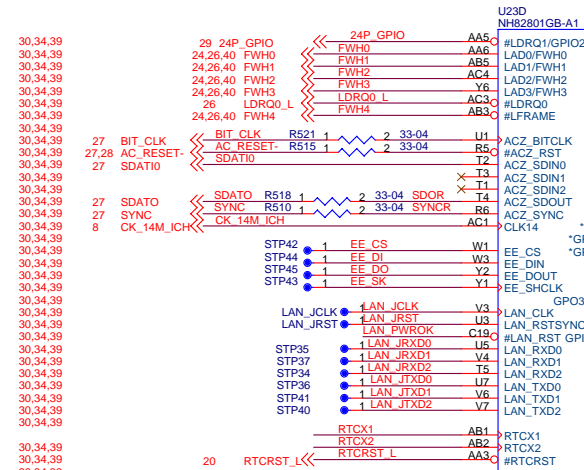
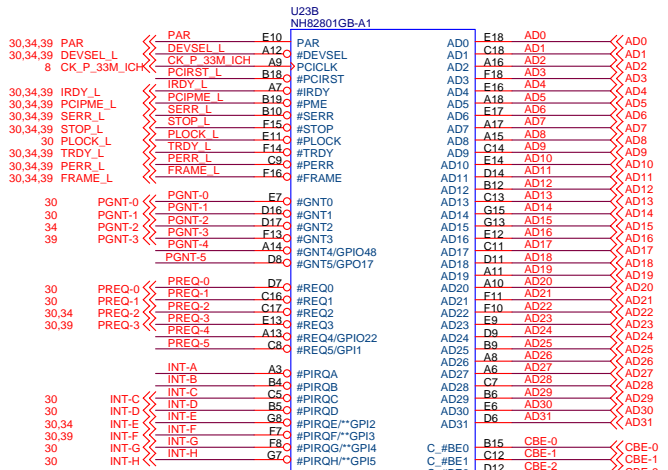
Title: **DIMM2(DDR2SDRAM)**

Size: Document Number **946GZT-AM** Rev: A

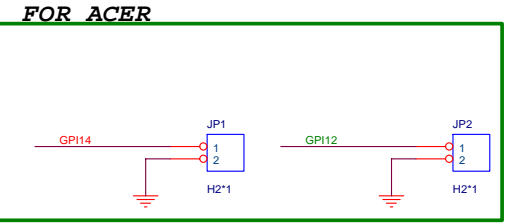
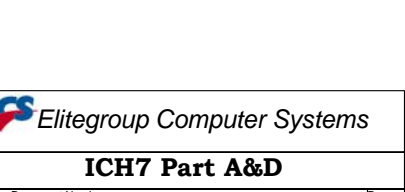
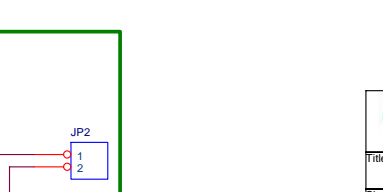
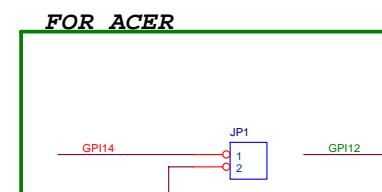
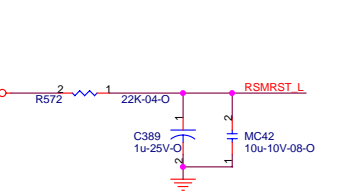
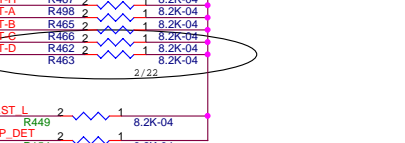
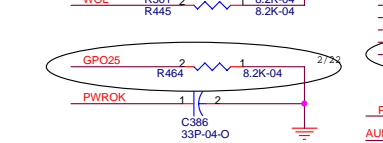
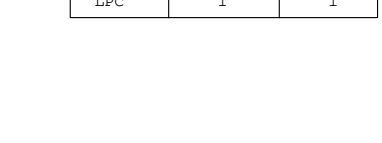
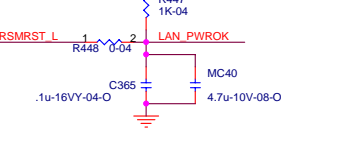
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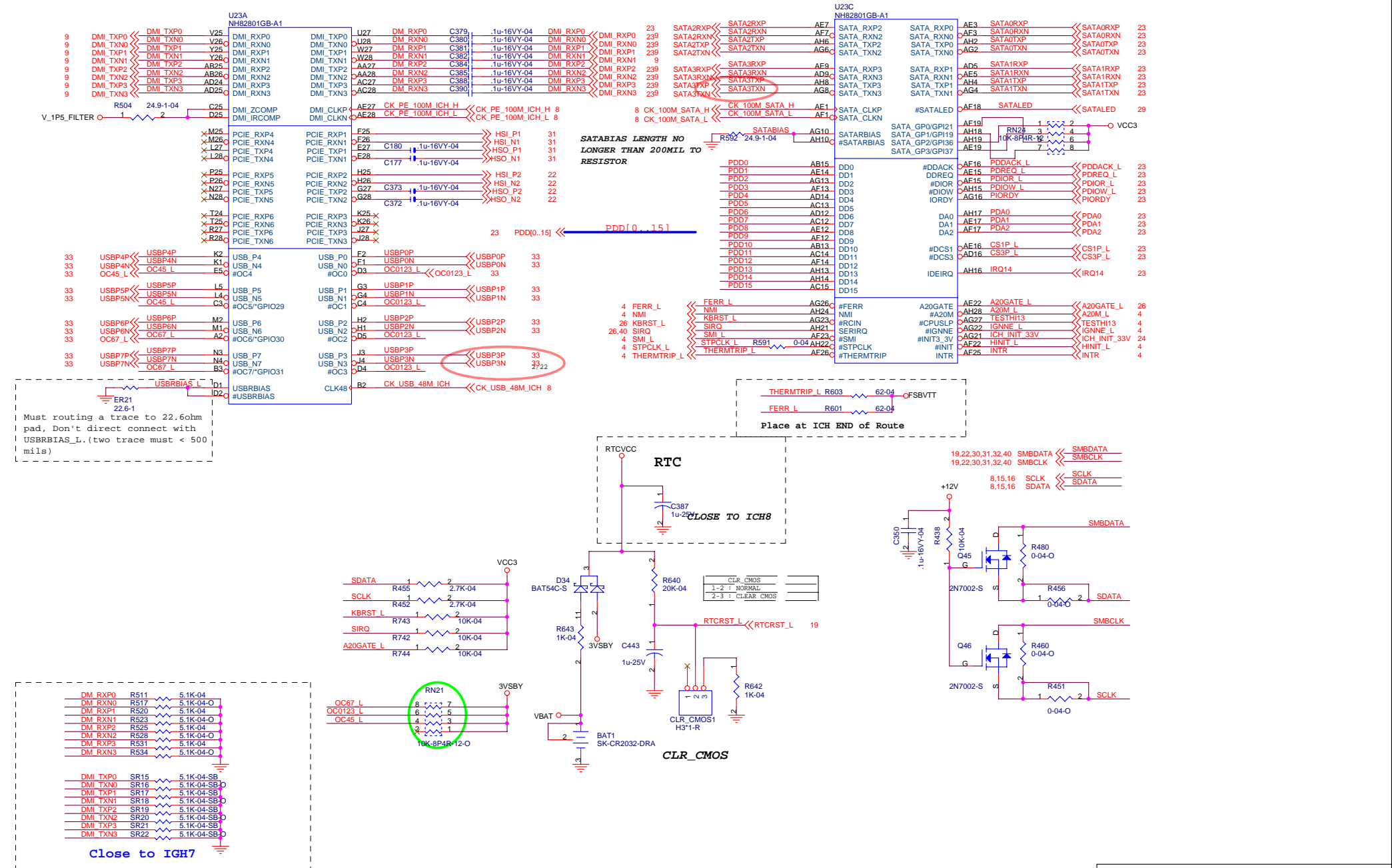
	GNT_4	GNT_5
SPI	0	1
PCI	1	0
LPC	1	1



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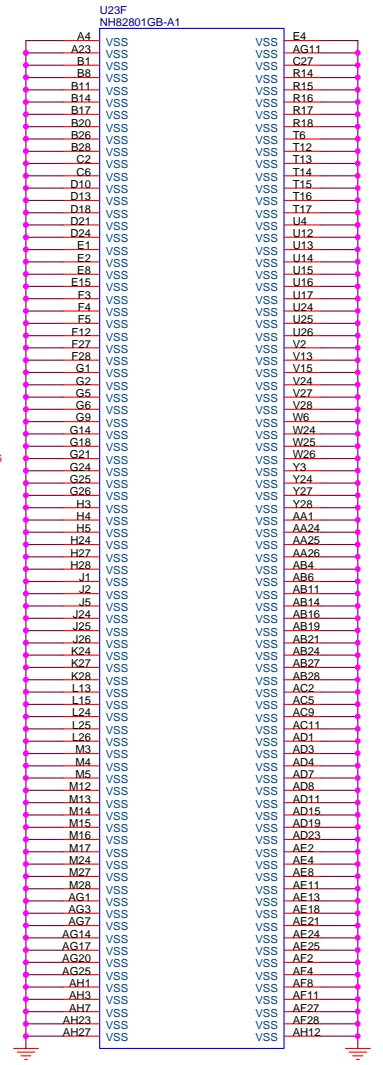
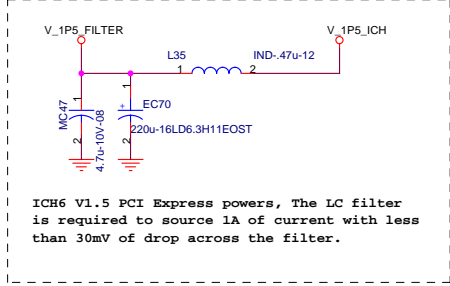
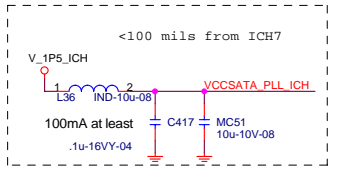
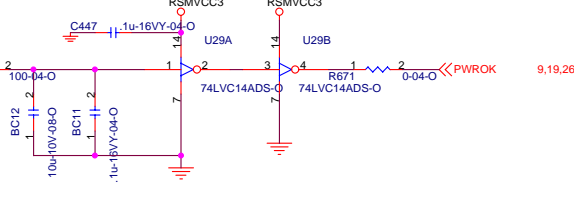
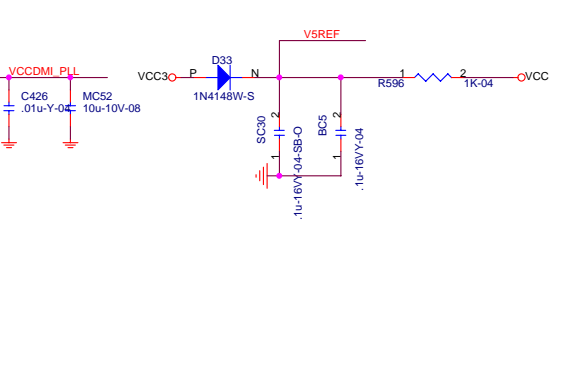
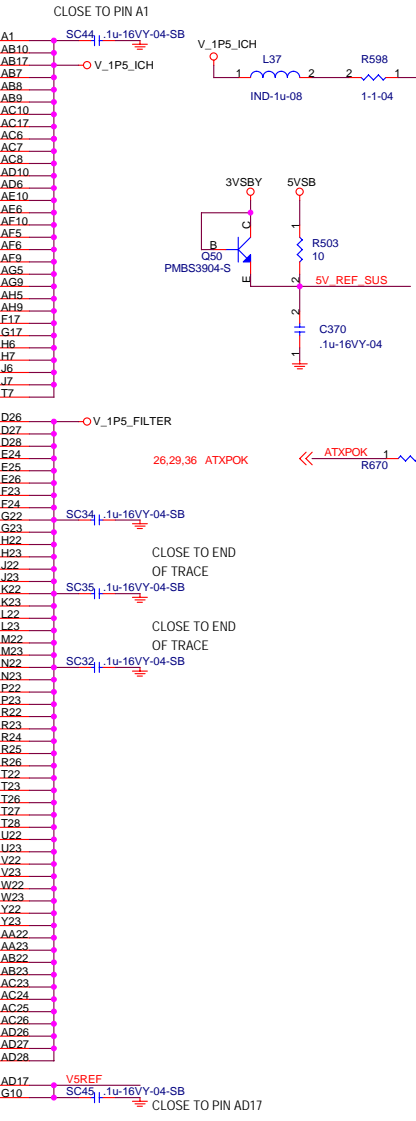
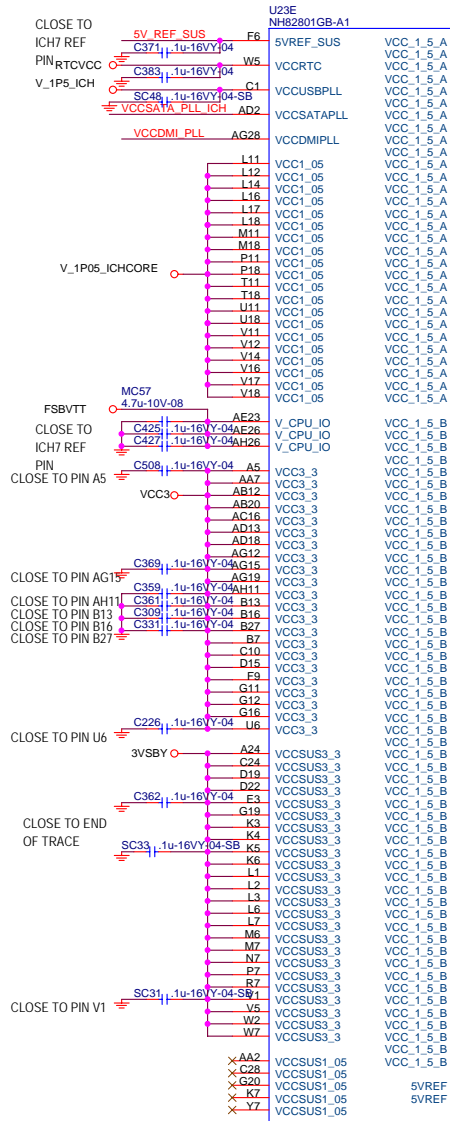
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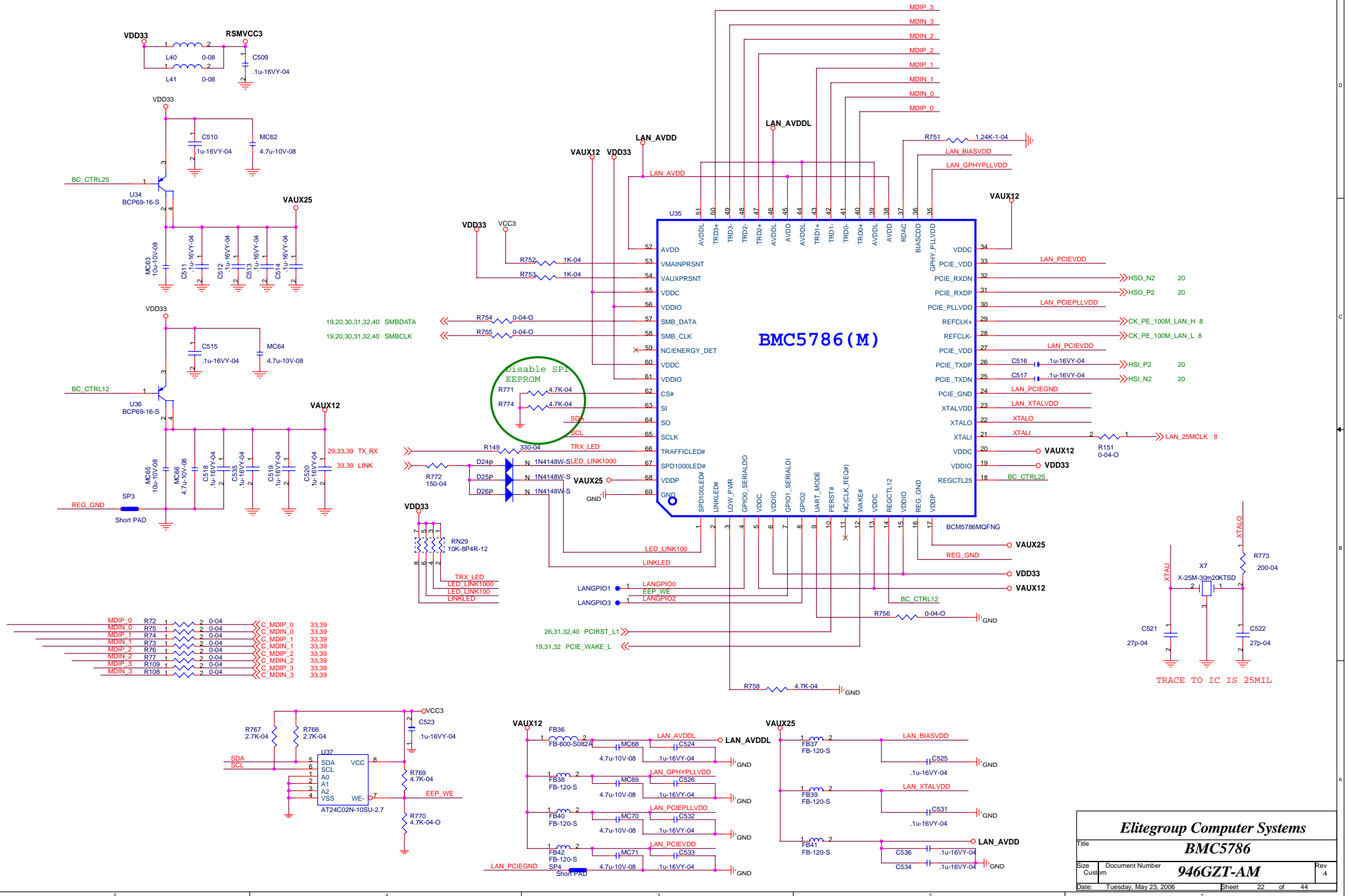
Size: Document Number
 Custom: **946GZT-AM**
 Date: Tuesday, May 23, 2006 Sheet 19 of 44



Must routing a trace to 22.6ohm pad, Don't direct connect with USBRBIAS_L (two trace must < 500 mils)

Place at ICH END of Route



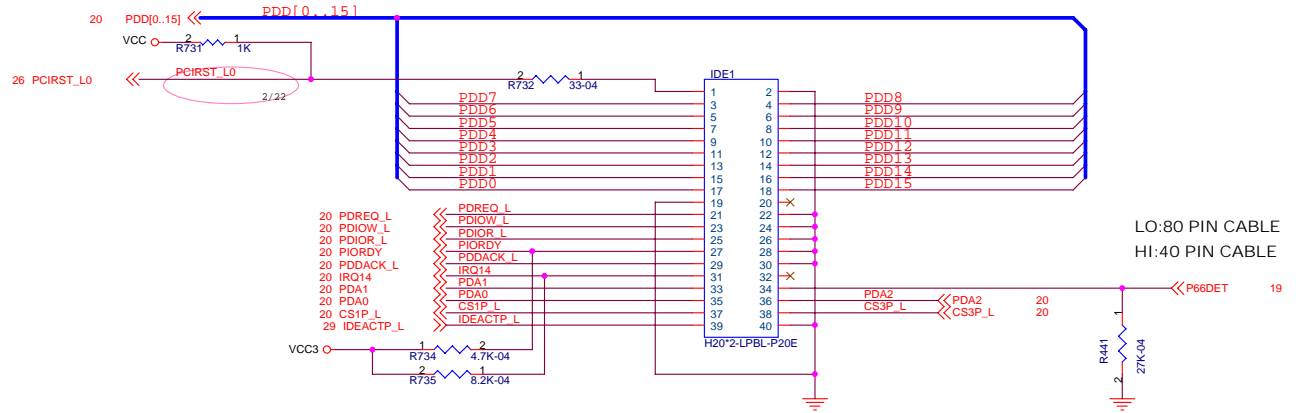
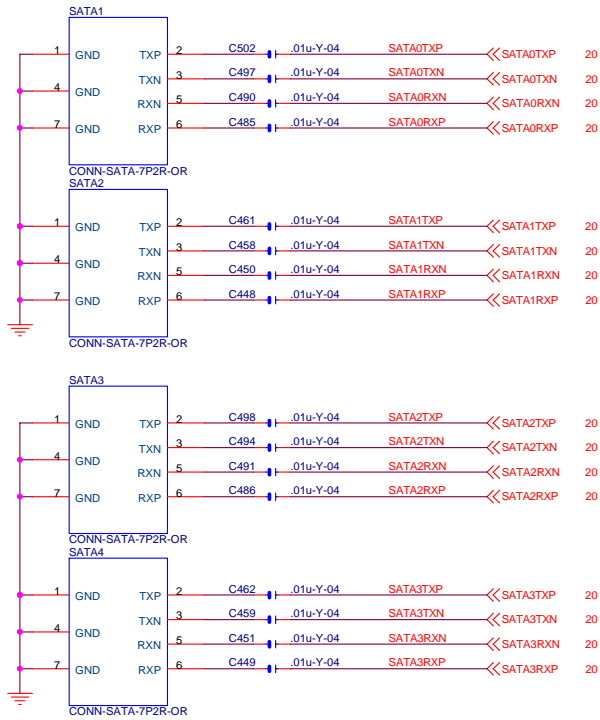


BMC5786 (M)

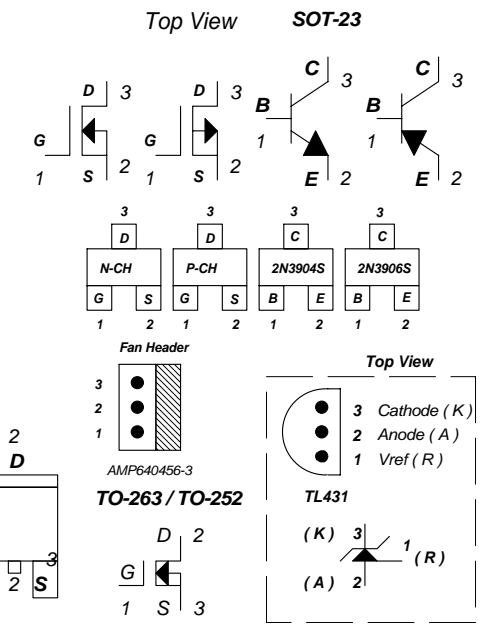
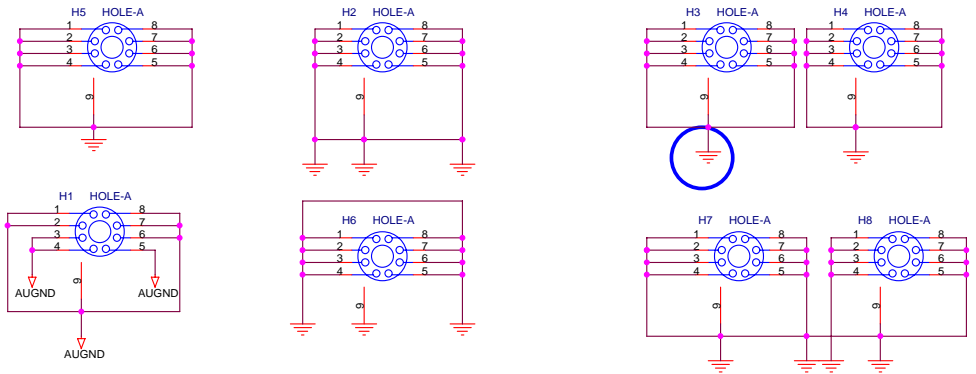
Disable SPI EEPROM

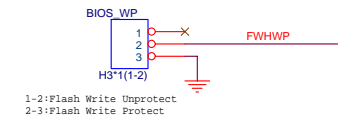
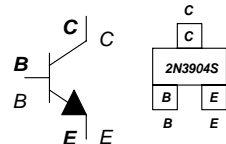
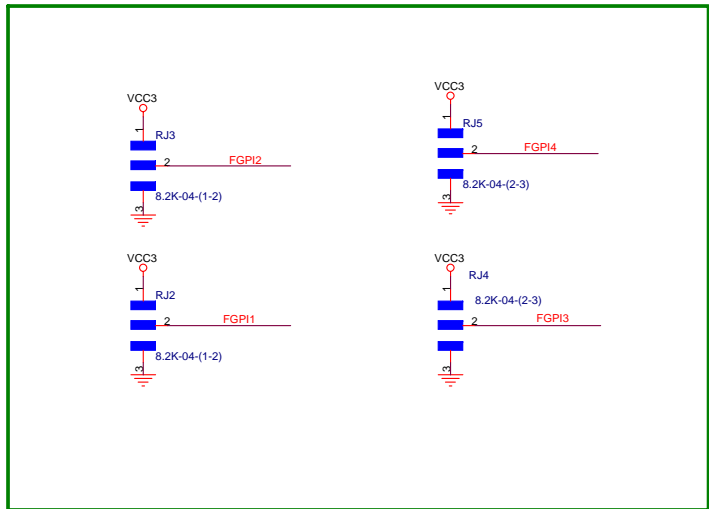
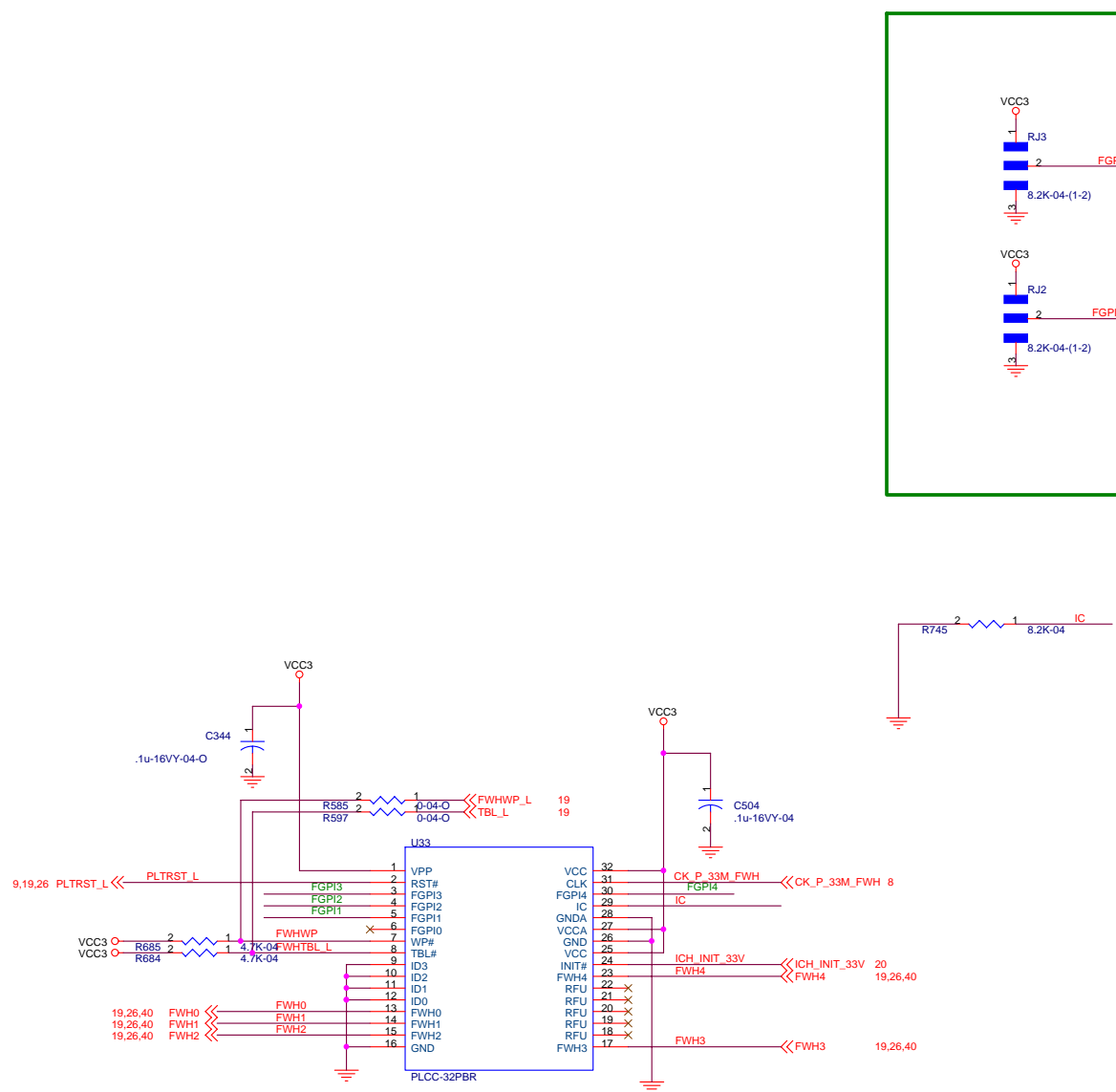
TRACE TO IC IS 25MIL

Elitegroup Computer Systems			
BMC5786			
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LO:80 PIN CABLE
HI:40 PIN CABLE





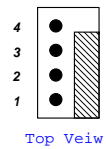
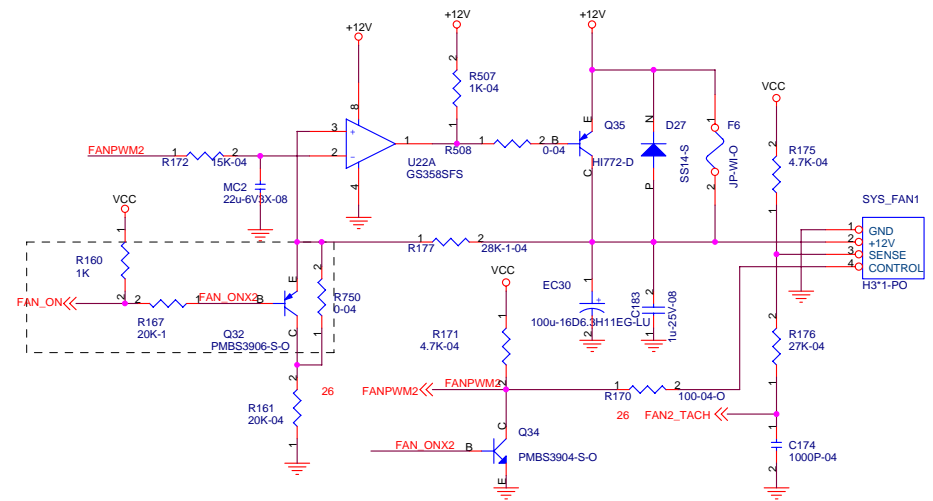
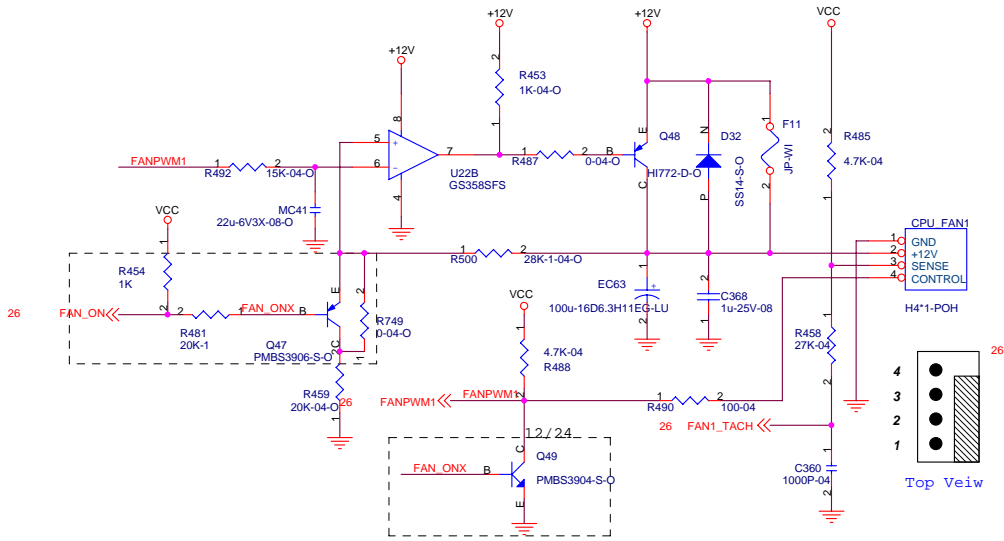
1-2:Flash Write Unprotect
2-3:Flash Write Protect

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Title: **FWH & SPI**

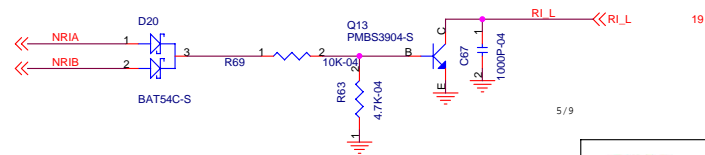
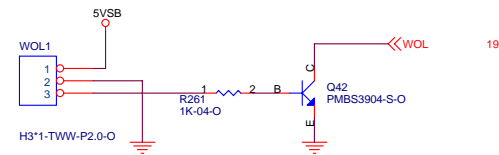
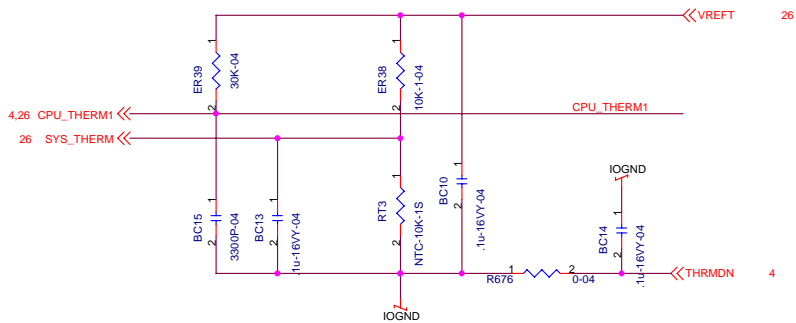
Size: Custom Document Number: **946GZT-AM** Rev: A

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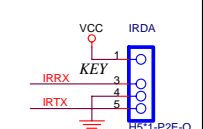
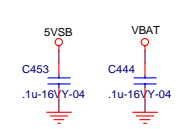
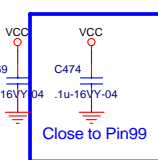
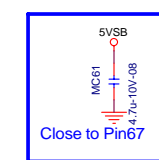
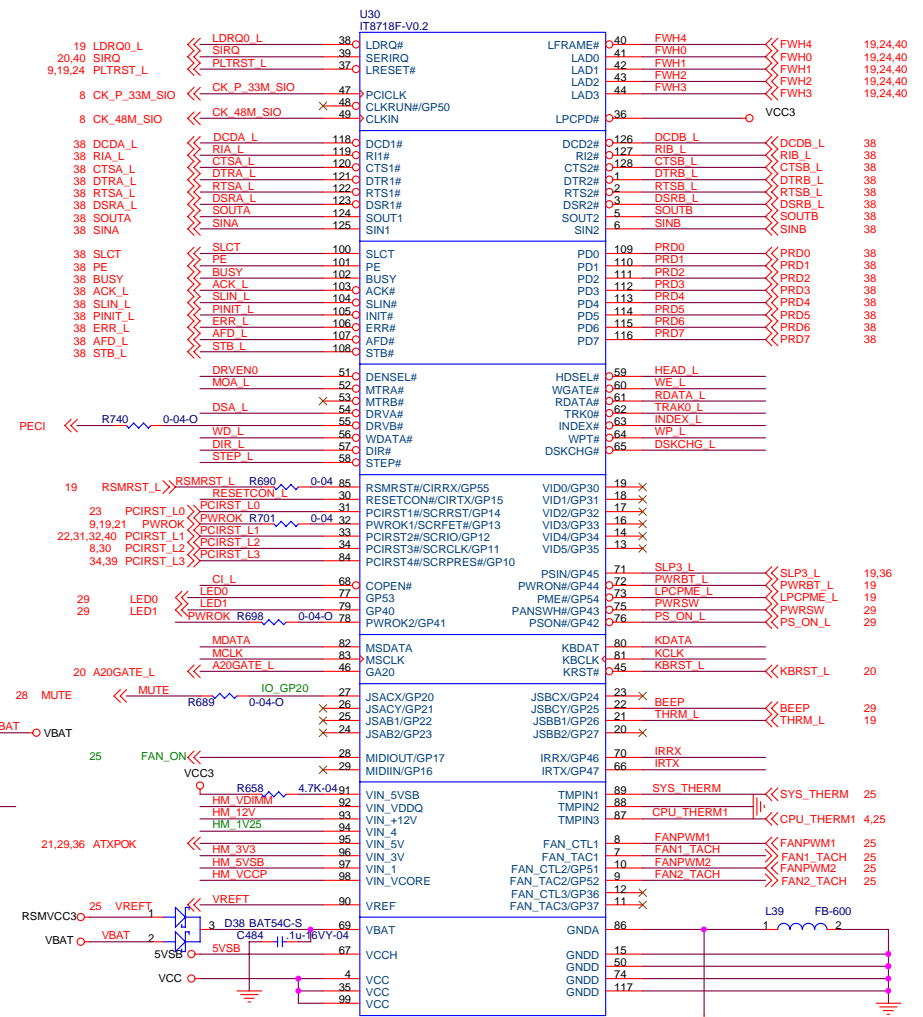
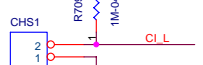
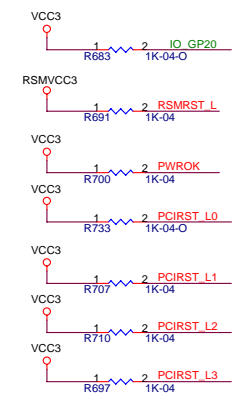
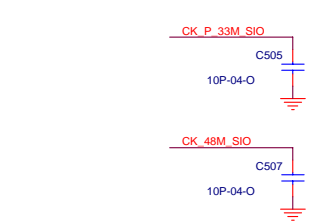
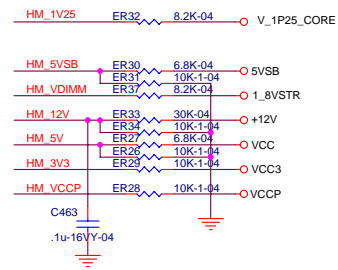
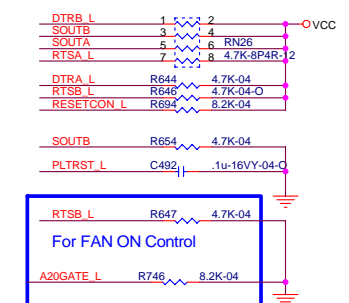
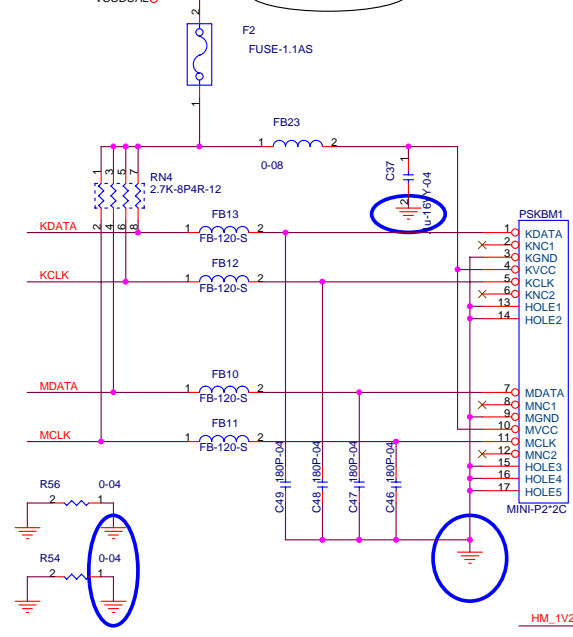
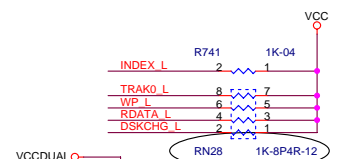
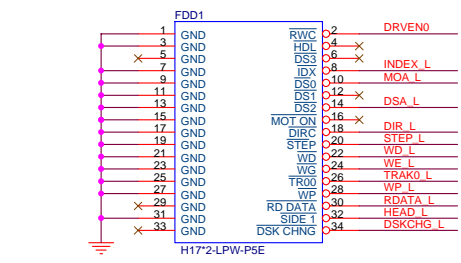


Top Veiw

THERM. SENSING



5/9



FAN PWM = 25% just after boot-up and POST with 8718!

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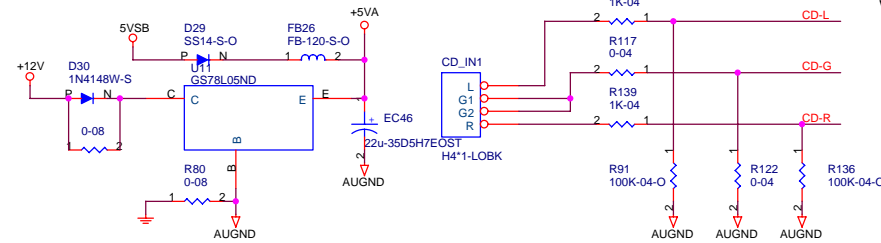
ITE 8712 LPC I/O

Size: Document Number **946GZT-AM** Rev: A

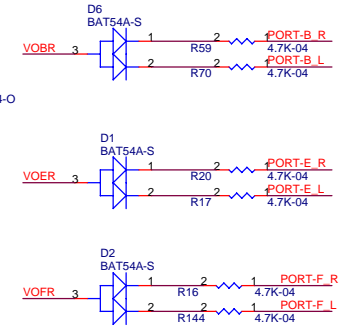
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Placement put on EC

PCR	C25	1	2	1u-25V-O	PORT-C_R
PCL	C66	1	2	1u-25V-O	PORT-C_L
PBR	C65	1	2	1u-25V-O	PORT-B_R
PBL	C80	1	2	1u-25V-O	PORT-B_L

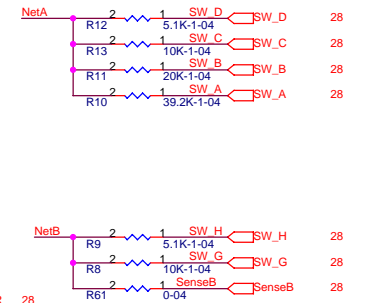


Verfout bias for stereo microphone.



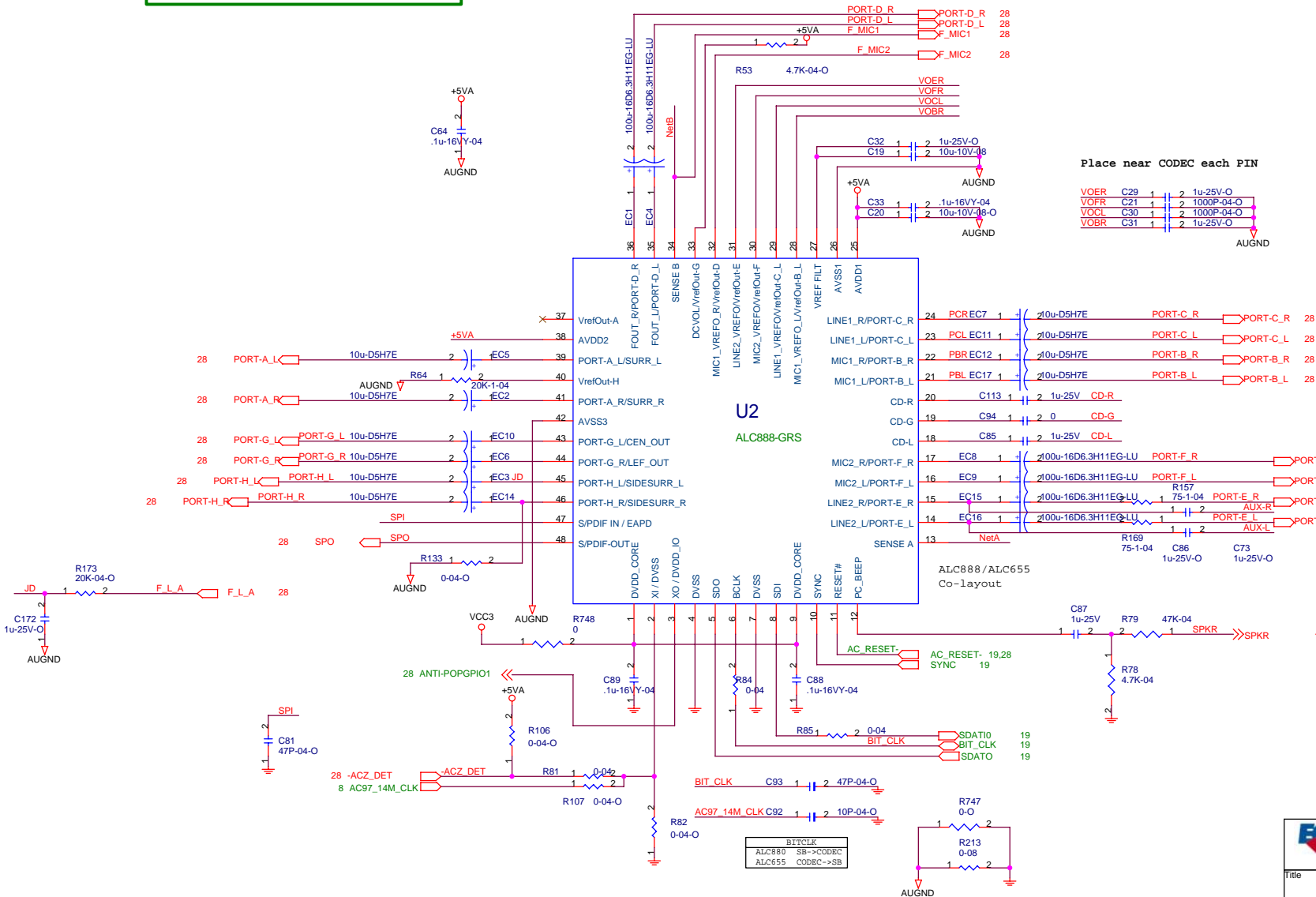
Place near Chip

Resistors Networks

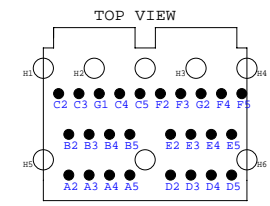
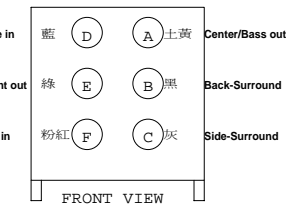
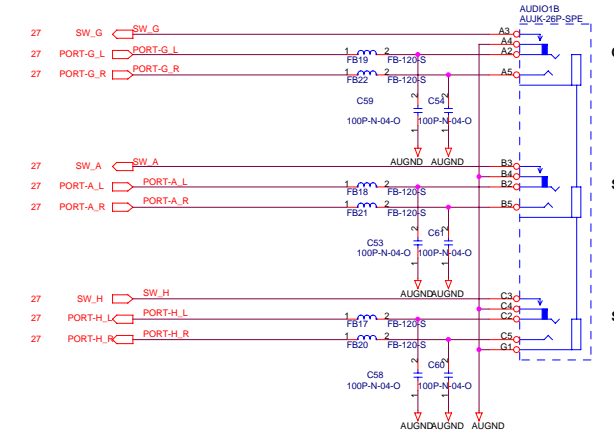
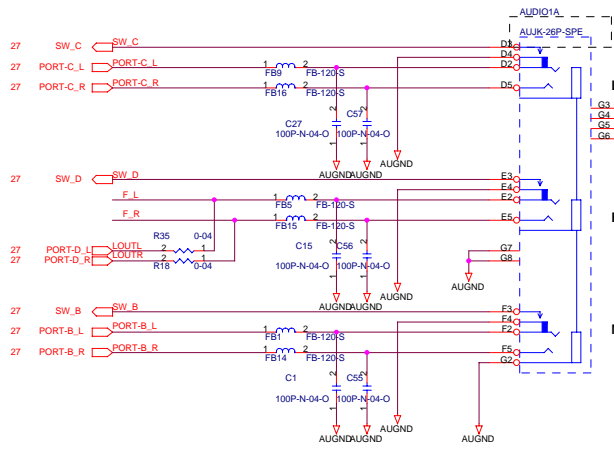


Place near CODEC each PIN

VOER	C29	1	2	1u-25V-O
VOFR	C21	1	2	1000P-04-O
VOCL	C30	1	2	1000P-04-O
VOBR	C31	1	2	1u-25V-O

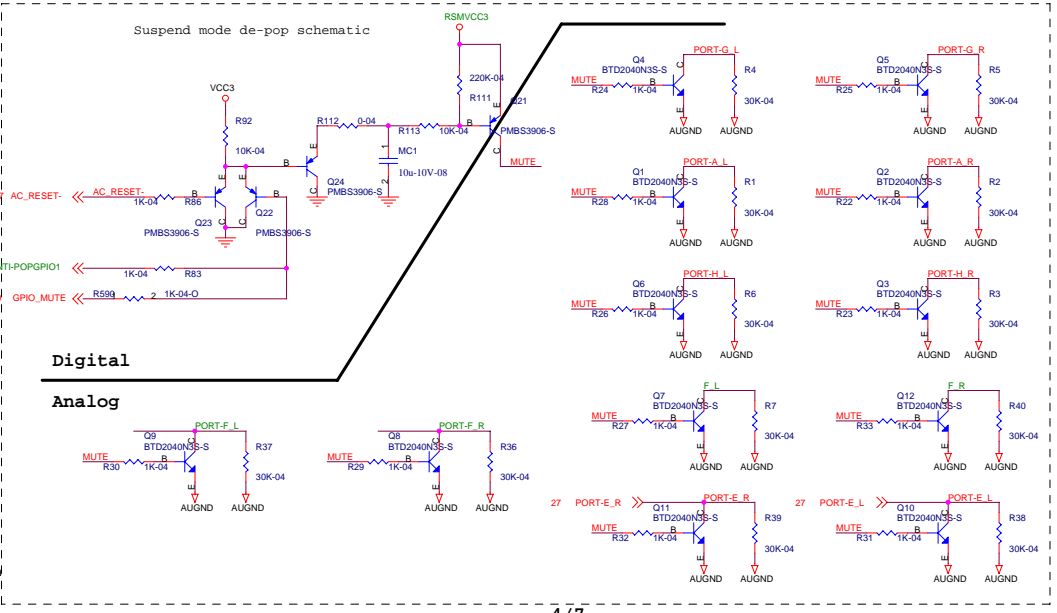
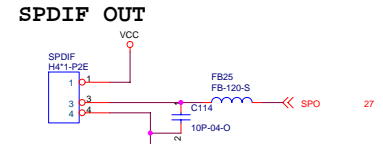
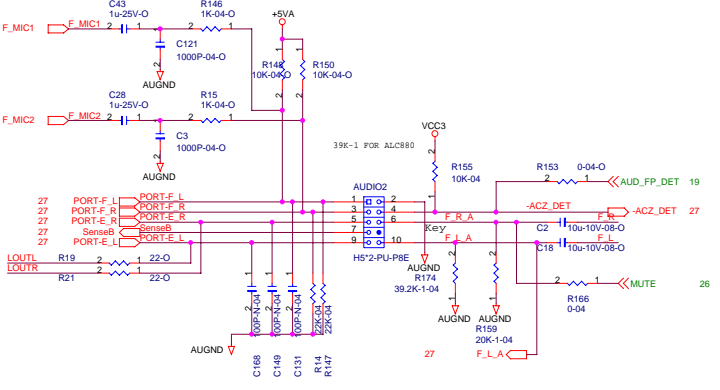


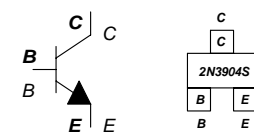
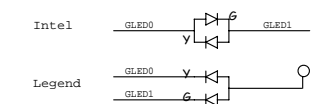
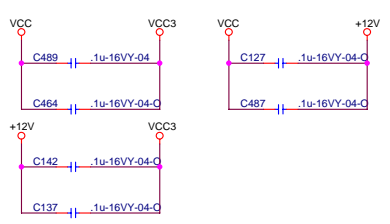
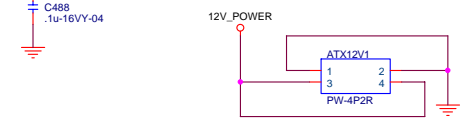
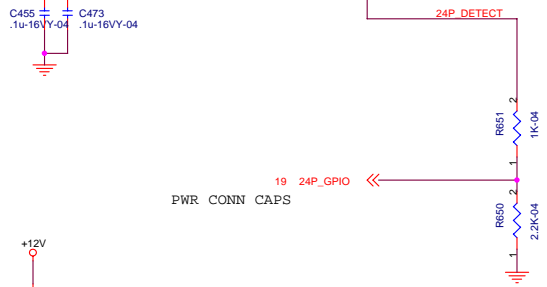
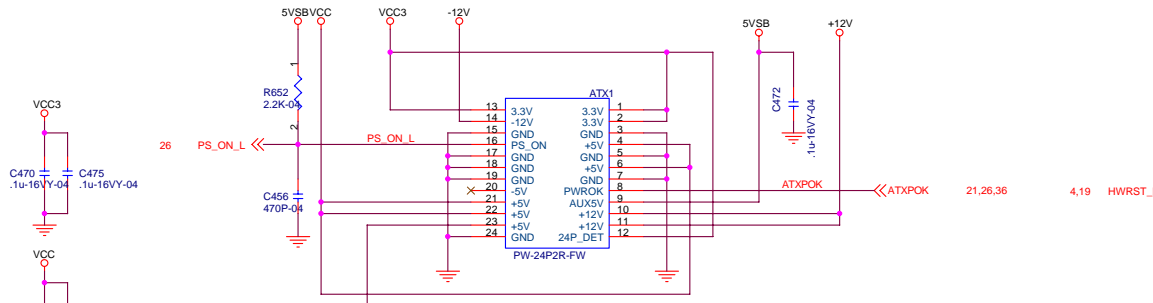
BITCLK	ALC880	SB->CODEC
	ALC655	CODEC->SB



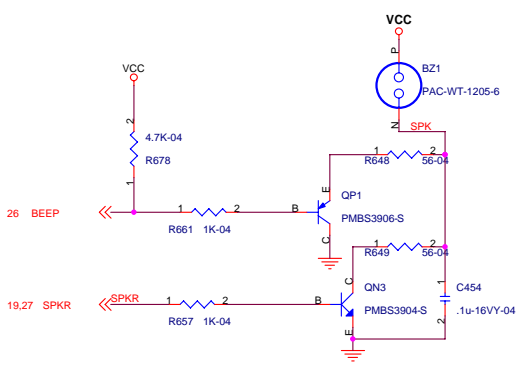
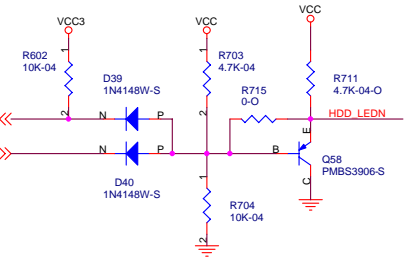
Line in
Front out
Mic in

Center/Bass out
Surround
SIDE Surround
Side-Surround



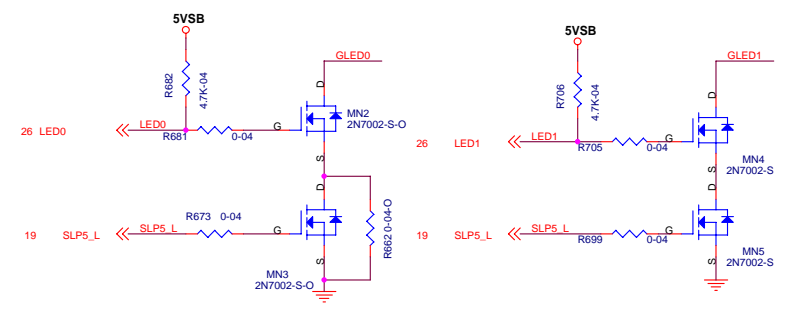
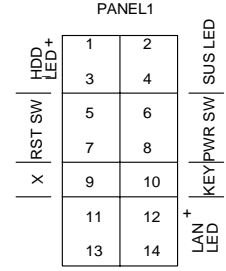
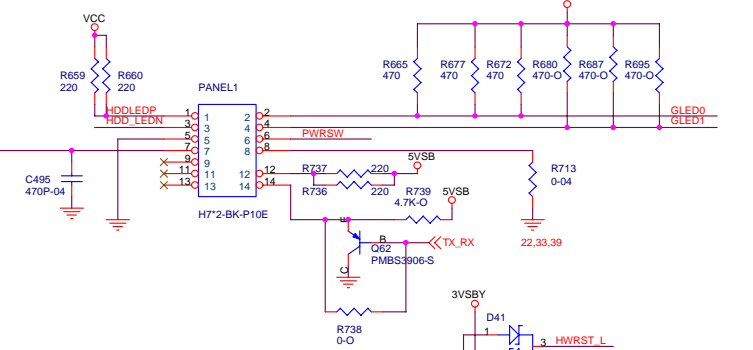


	S0	S1	S3	S4, S5
PANEL1(4, 2)	Green	G-Blinking	Y-Blinking	Dark
LPANEL1(3, 5, 7)	Green	G-Blinking	G-Blinking	Dark
LSPI(1, 2)	Dark	Dark	Light	Dark
SPI(1, 3) (2, 3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH



FOR ACER

Power state LED
 S0 Blue Steady
 S1/S3 Blue Blinking
 S4/S5 Off



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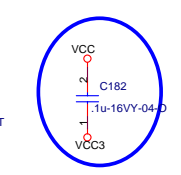
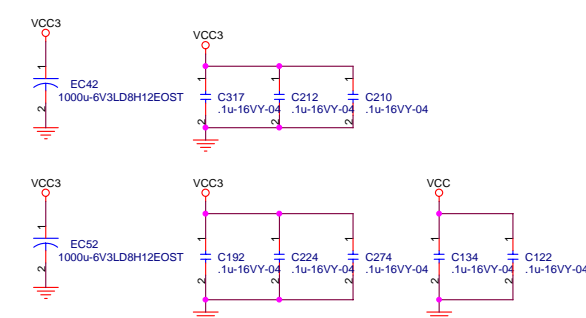
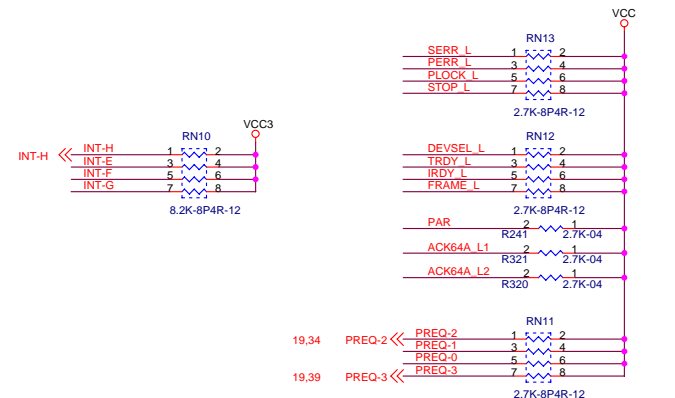
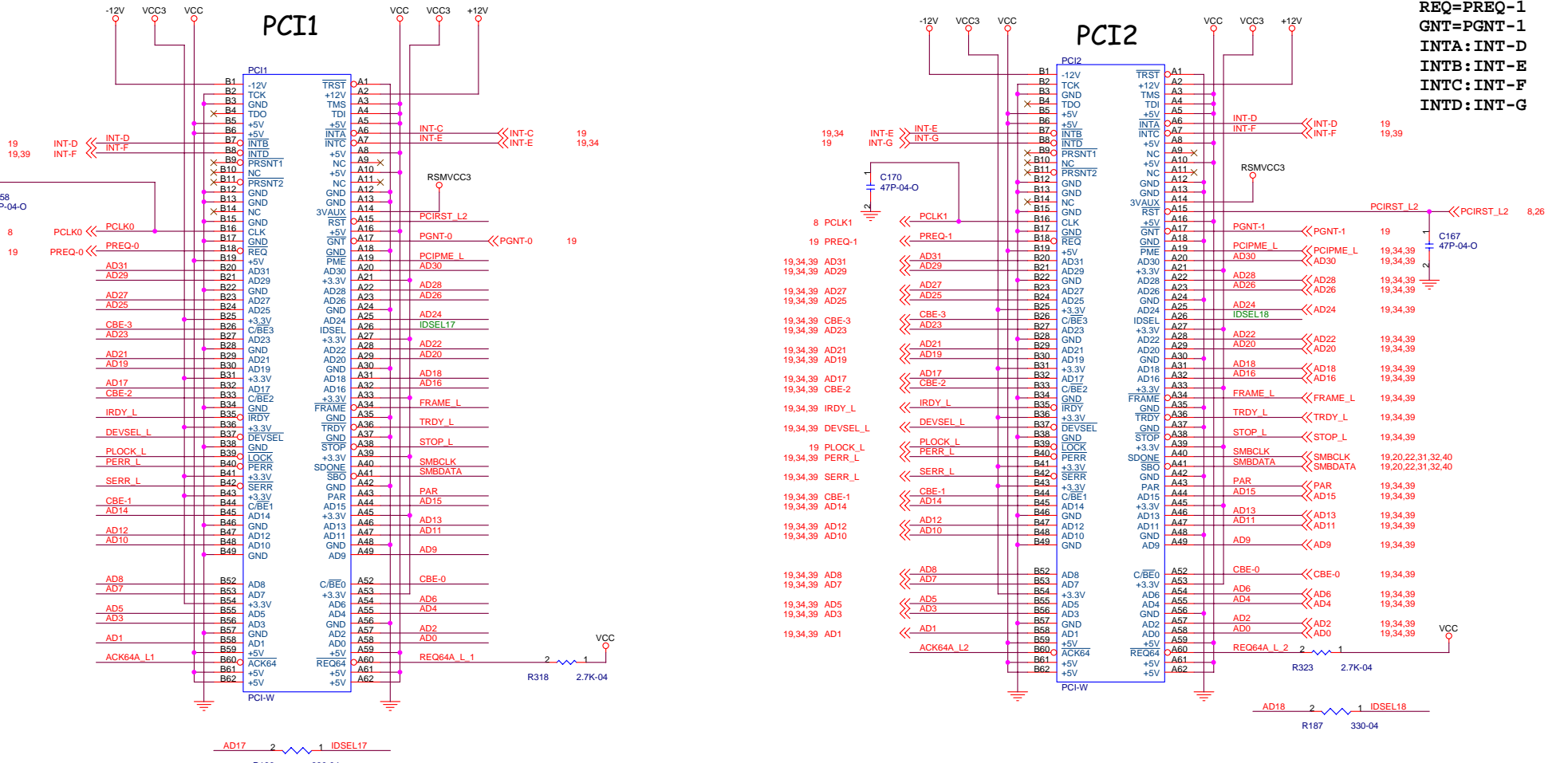
Title: **ATX Power & Front Panel**

Size: Custom Document Number: **946GZT-AM** Rev: A

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CLK=PCK0
 RST=PCIRST_L2
 IDSEL=AD17
 REQ=PREQ-0
 GNT=PGNT-0
 INTA:INT-C
 INTB:INT-D
 INTC:INT-E
 INTD:INT-F

CLK=PCK1
 RST=PCIRST_L2
 IDSEL=AD18
 REQ=PREQ-1
 GNT=PGNT-1
 INTA:INT-D
 INTB:INT-E
 INTC:INT-F
 INTD:INT-G



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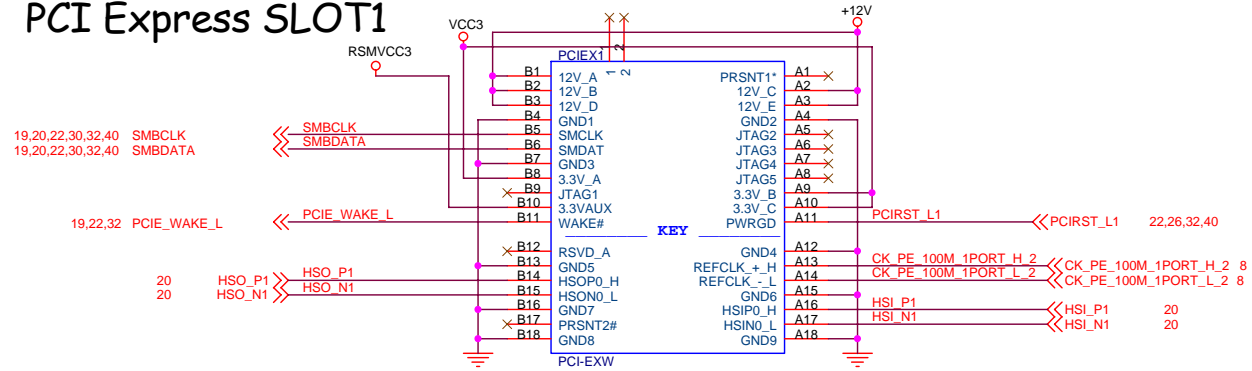
Title: **PCI Slot 1&2**


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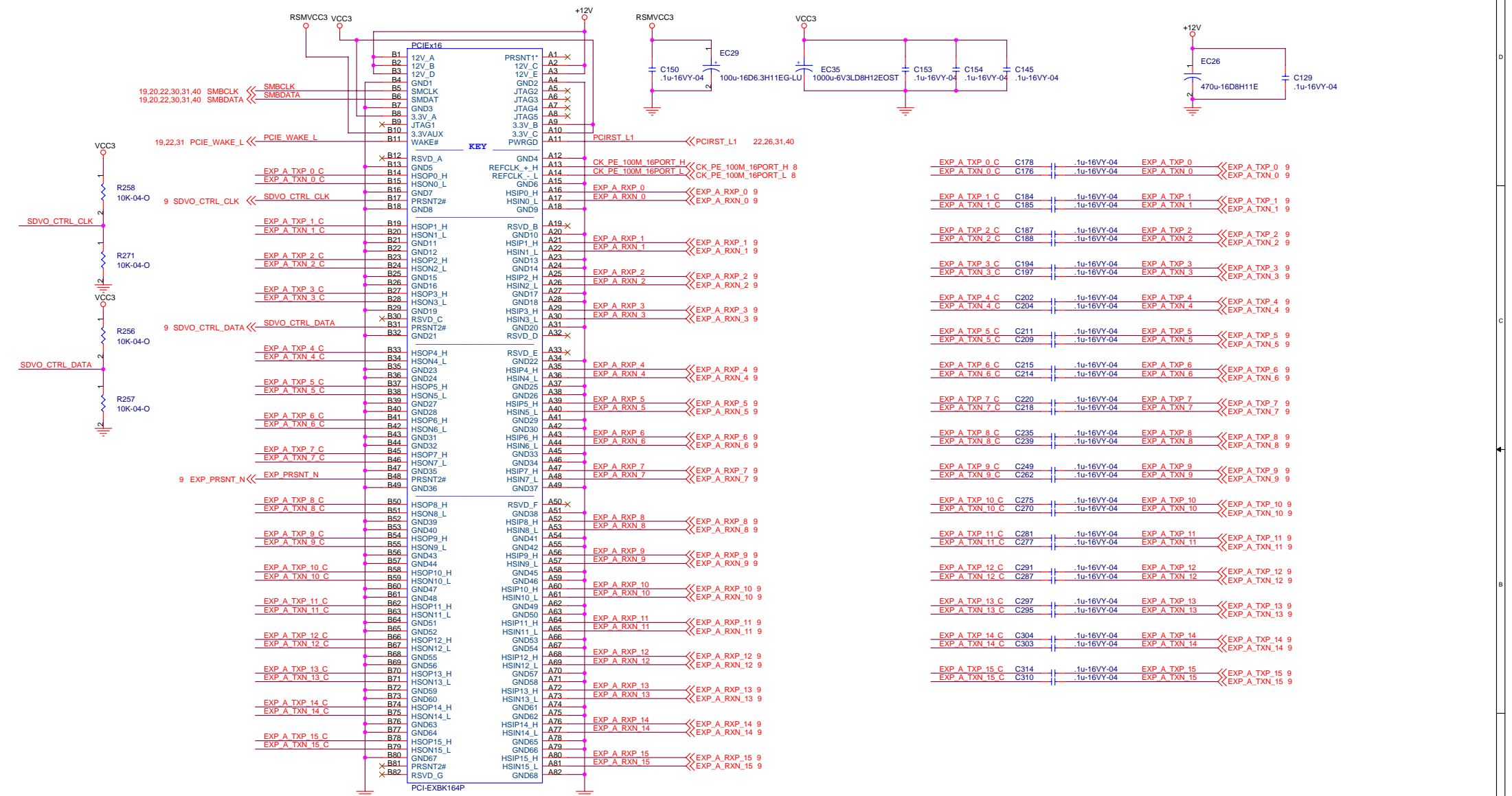
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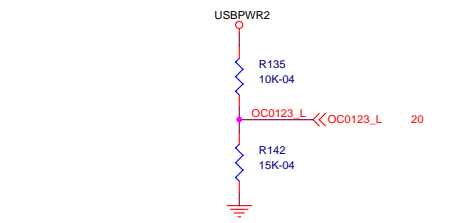
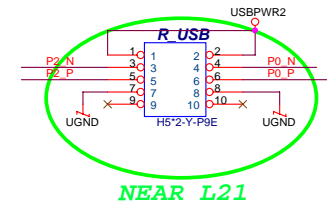
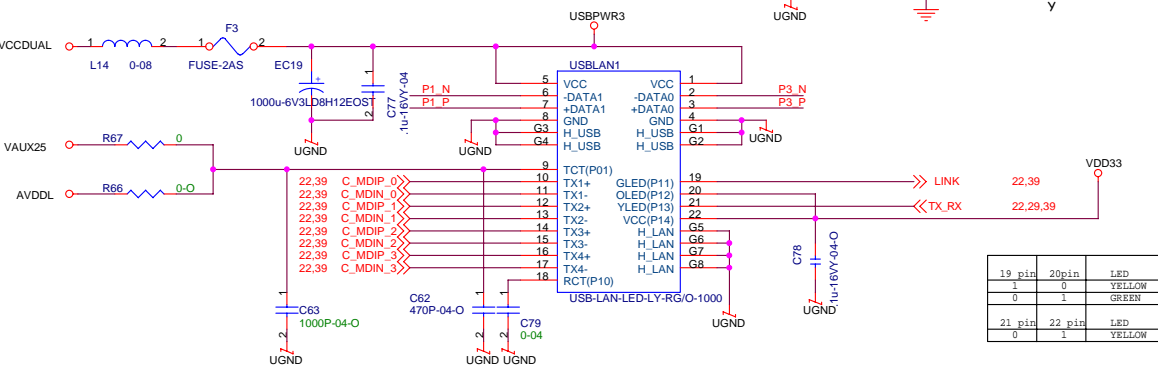
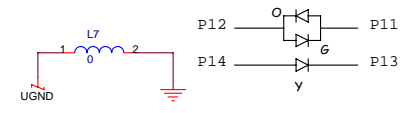
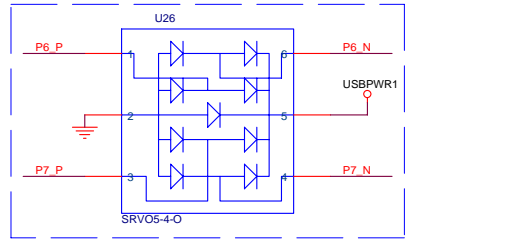
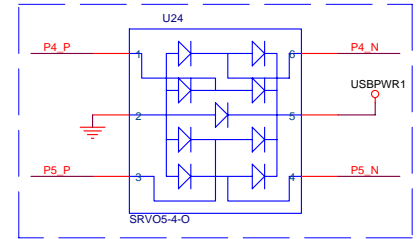
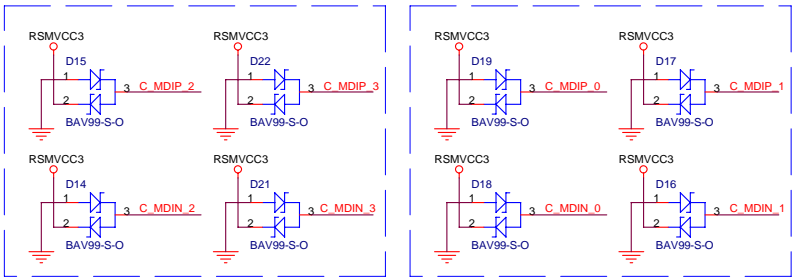
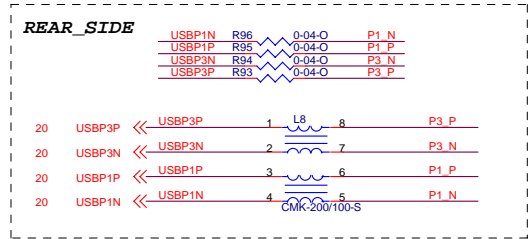
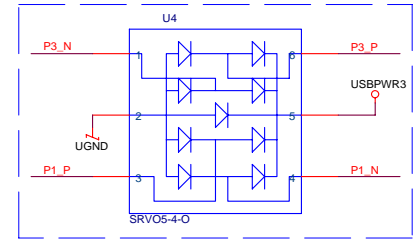
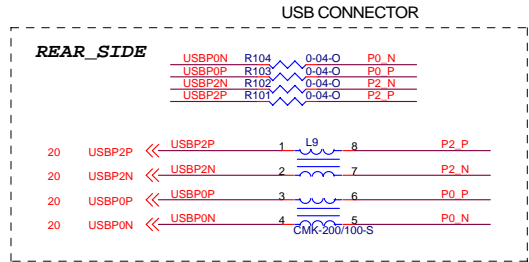
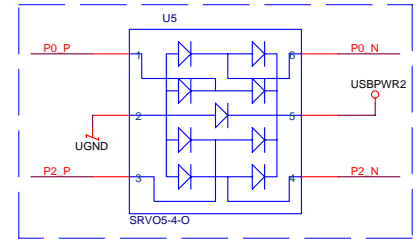
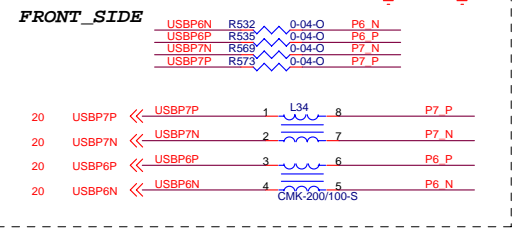
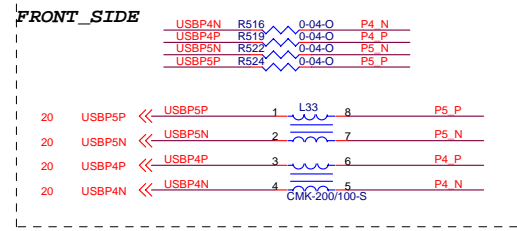
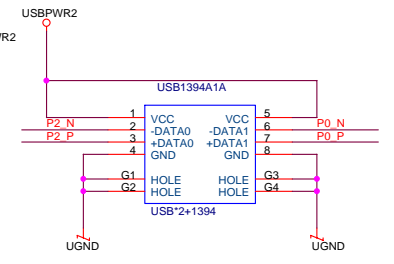
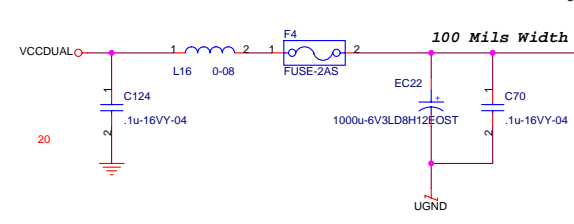
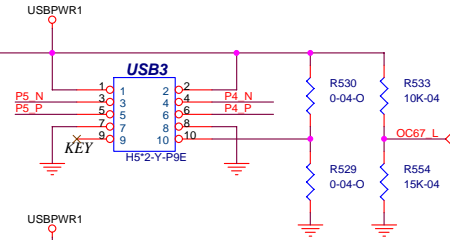
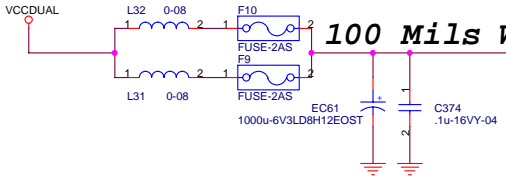
Date: Tuesday, May 23, 2006 Sheet 30 of 44

PCI Express SLOT1



 Elitegroup Computer Systems		
Title PCI Slot 1		
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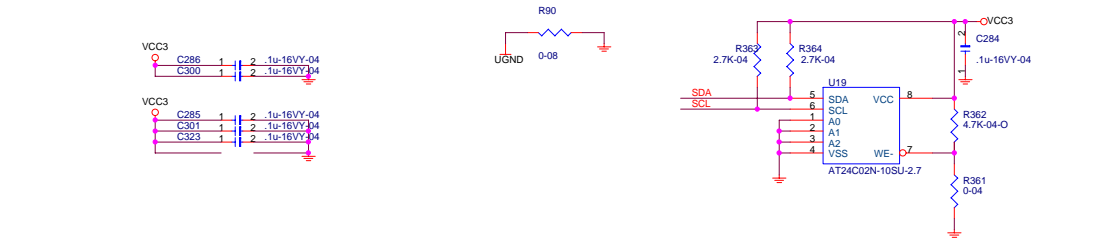
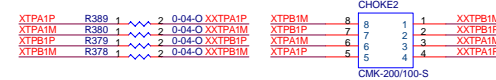
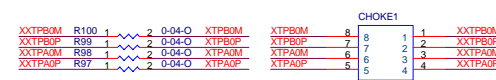
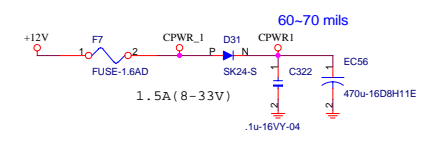
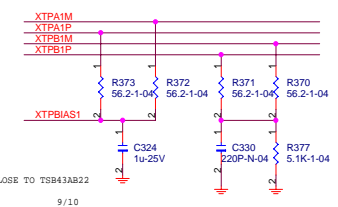
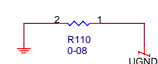
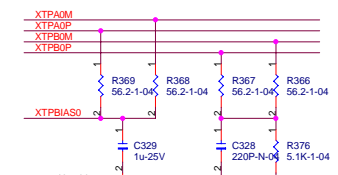
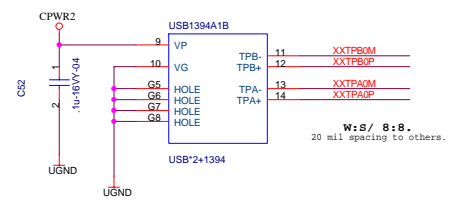
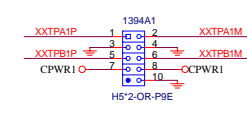
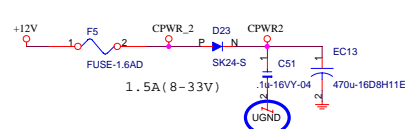
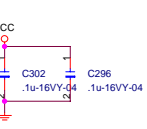
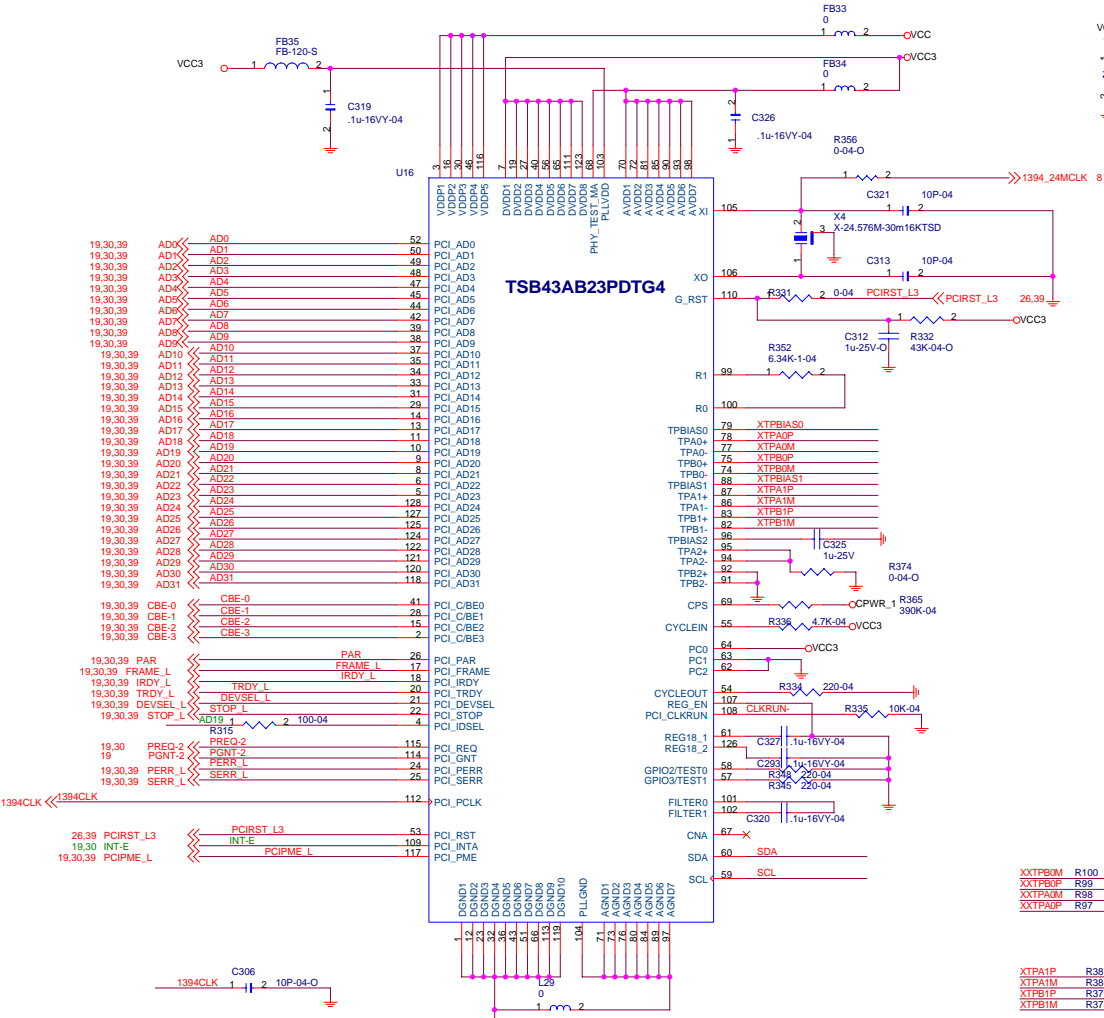
19 pin	20 pin	LED
1	0	YELLOW
0	1	GREEN
21 pin	22 pin	LED
0	1	YELLOW

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Title: **BACK I/O**

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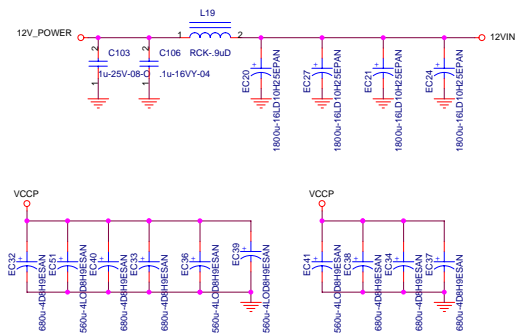
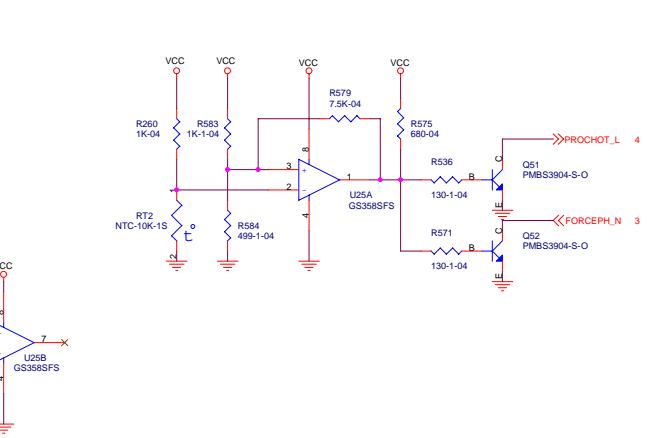
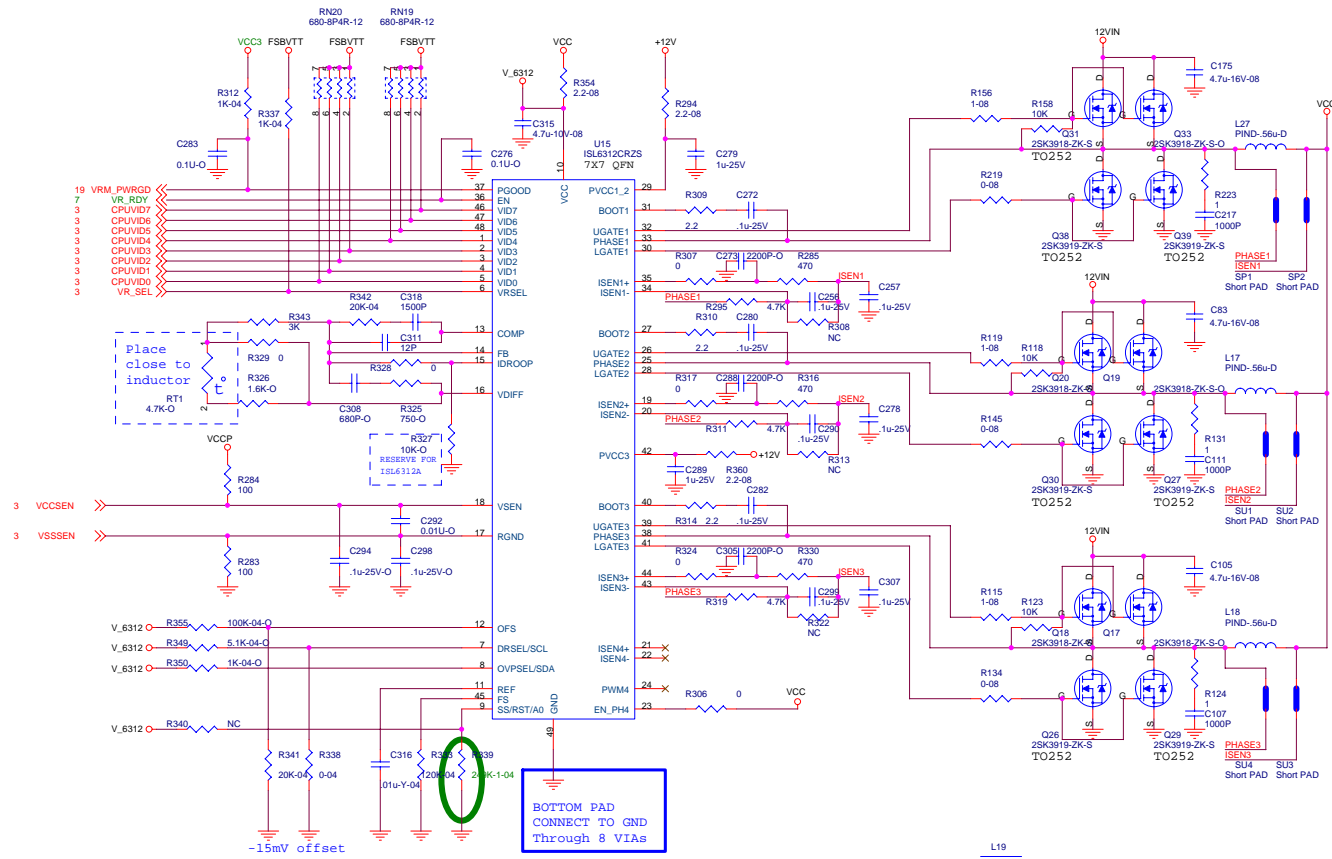
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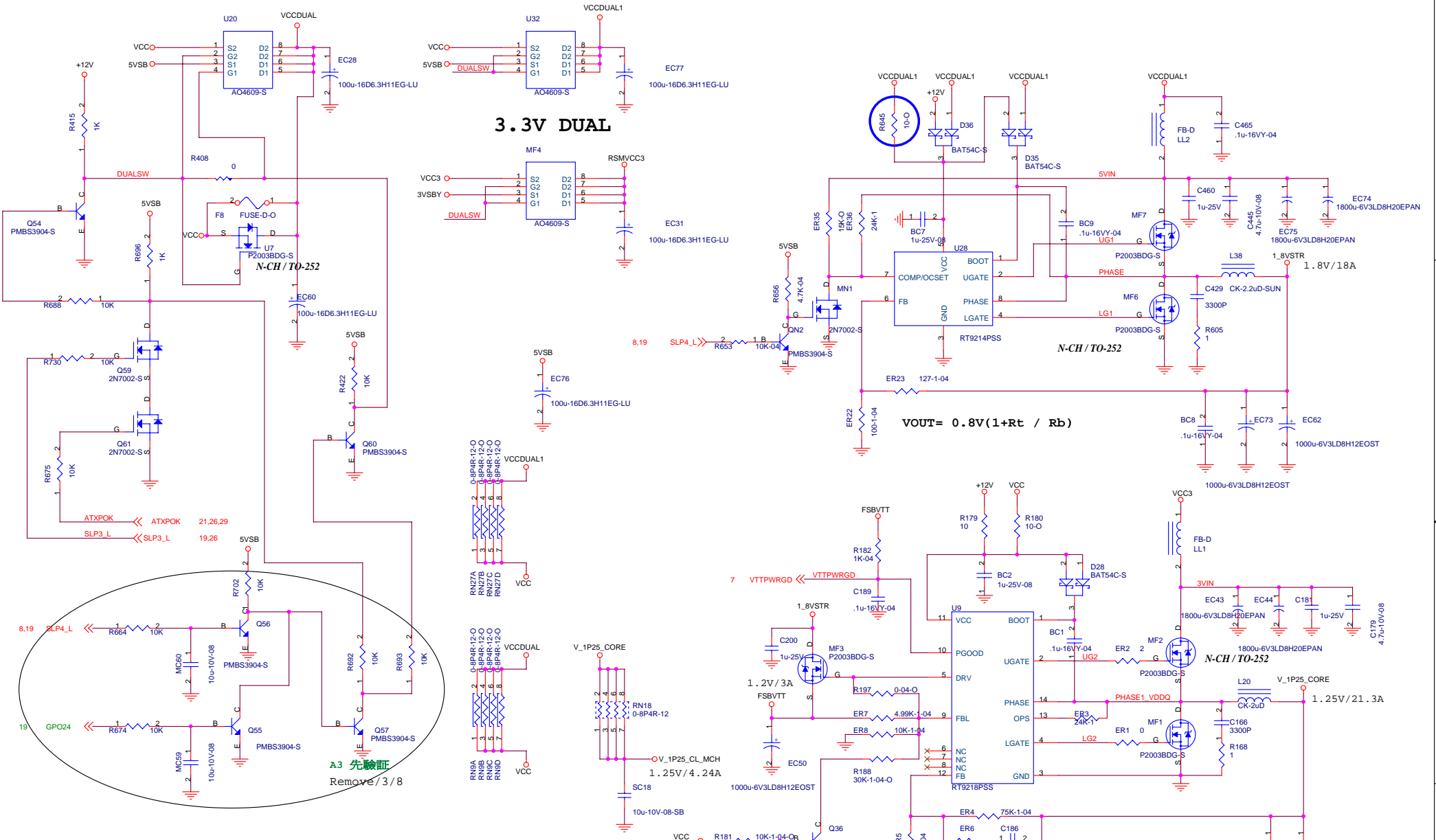


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TI TSB43AB23	
Size	Rev
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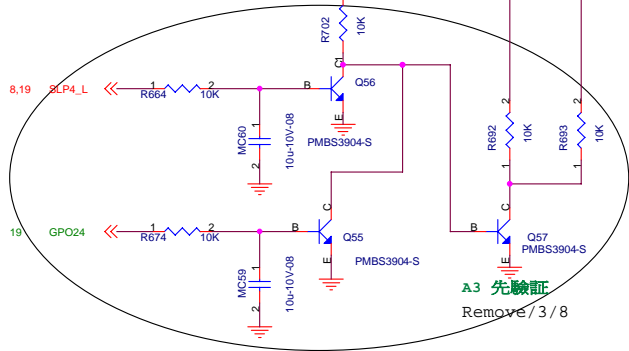
ISL6312/6322CR FOR Intel P4 Broadwater VRD11 POWER CKT - 4 PHASE





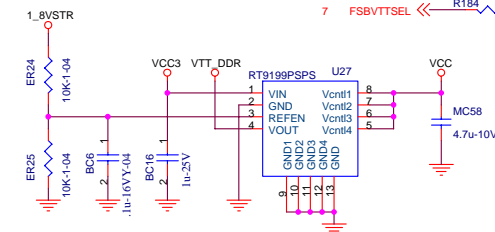
3.3V DUAL

$$V_{OUT} = 0.8V(1 + R_t / R_b)$$



A3 先験証
Remove / 3 / 8

Signal Mode	GPO24	VCCDUAL
S4/S5	0	0(No Power)
S4/S5	1	1(5VSB)



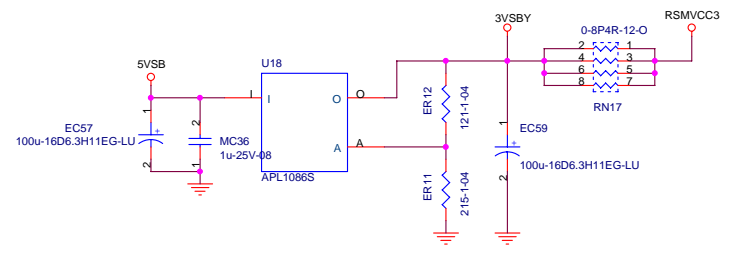
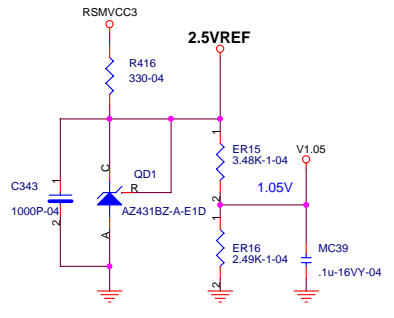
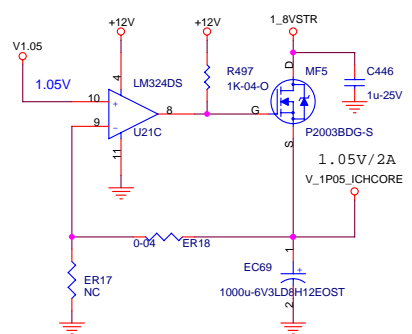
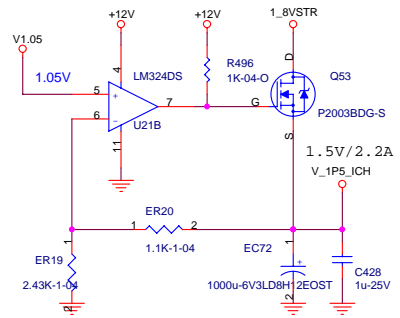
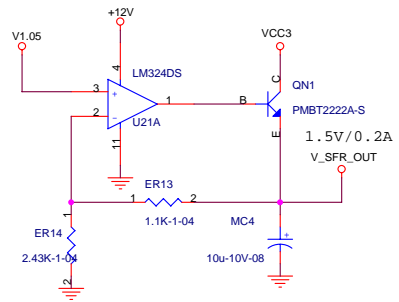
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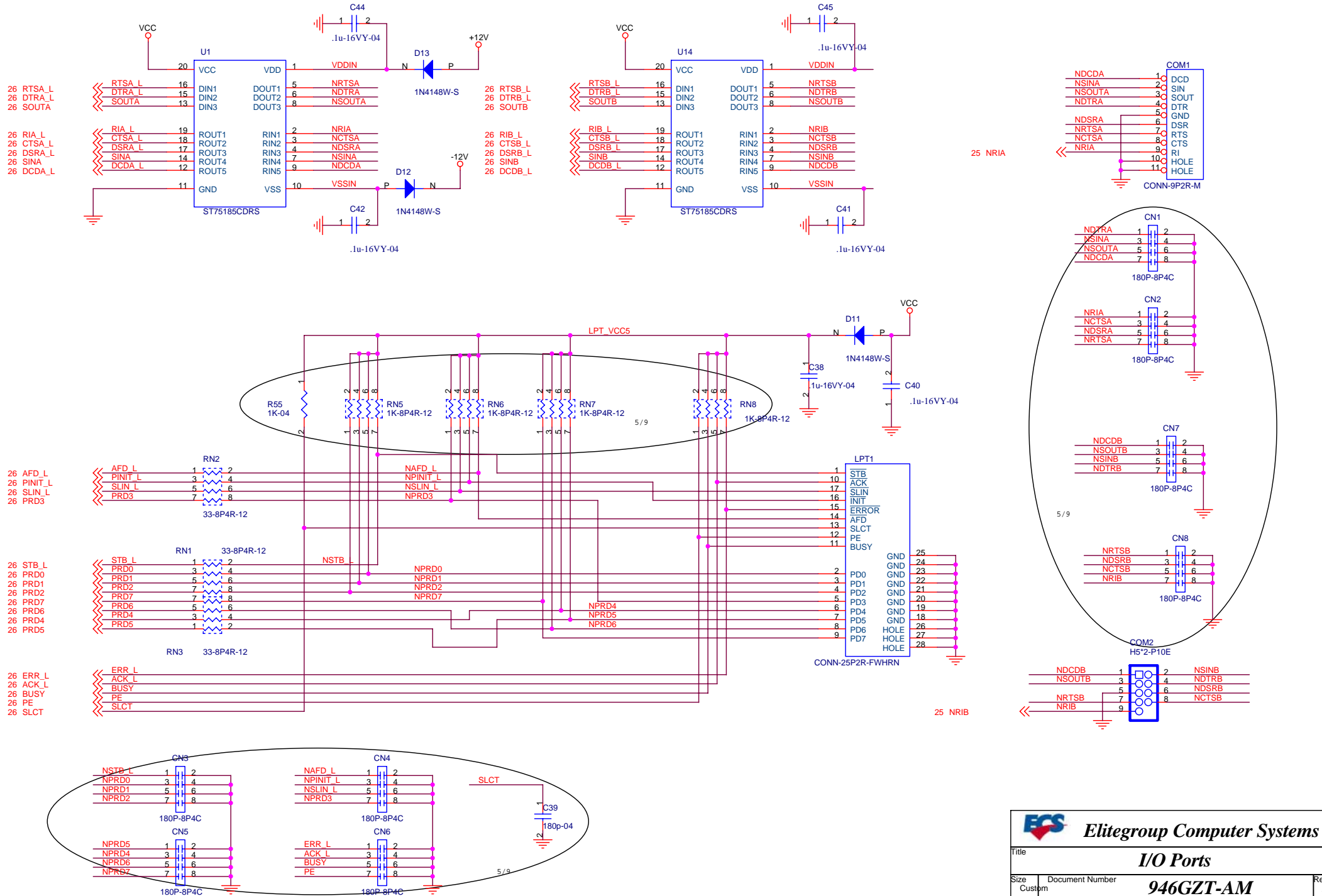
Title: **DDR&System DC-DC**

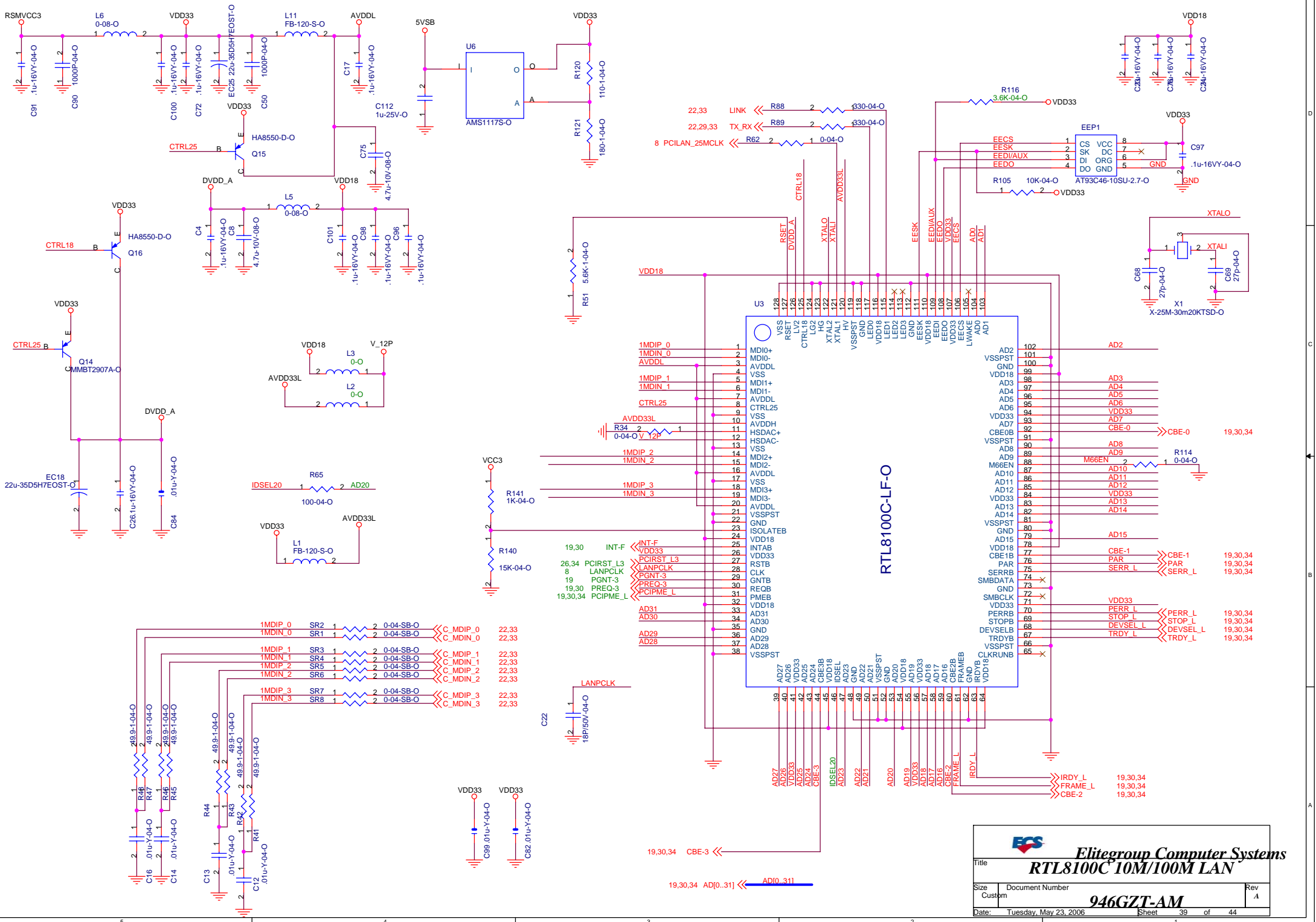
Size: Document Number **946GZT-AM** Rev: A

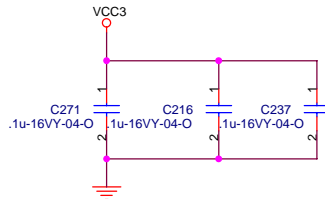
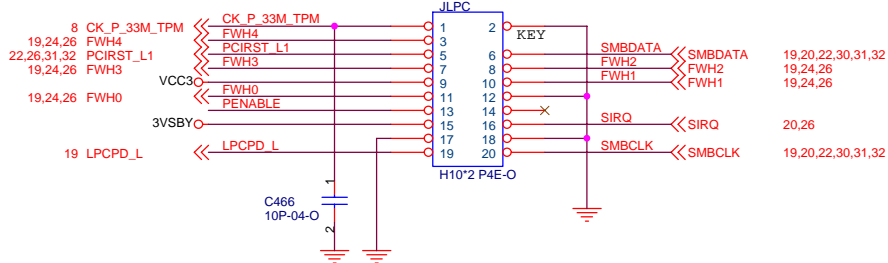
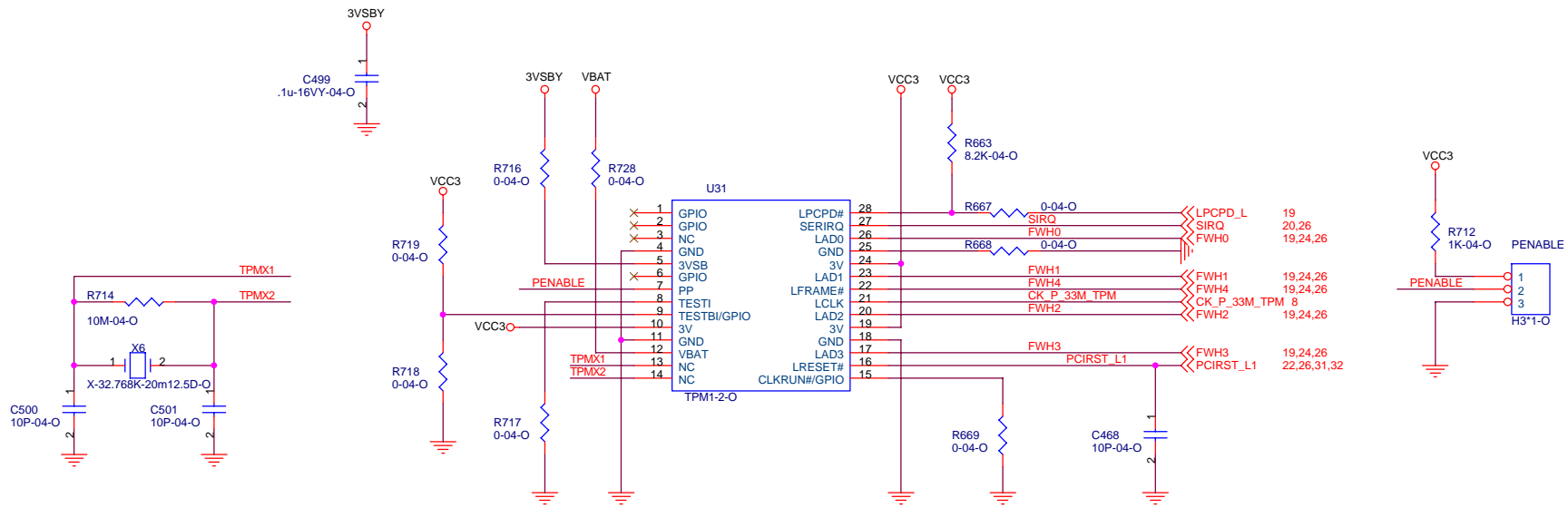
Customer: **946GZT-AM**

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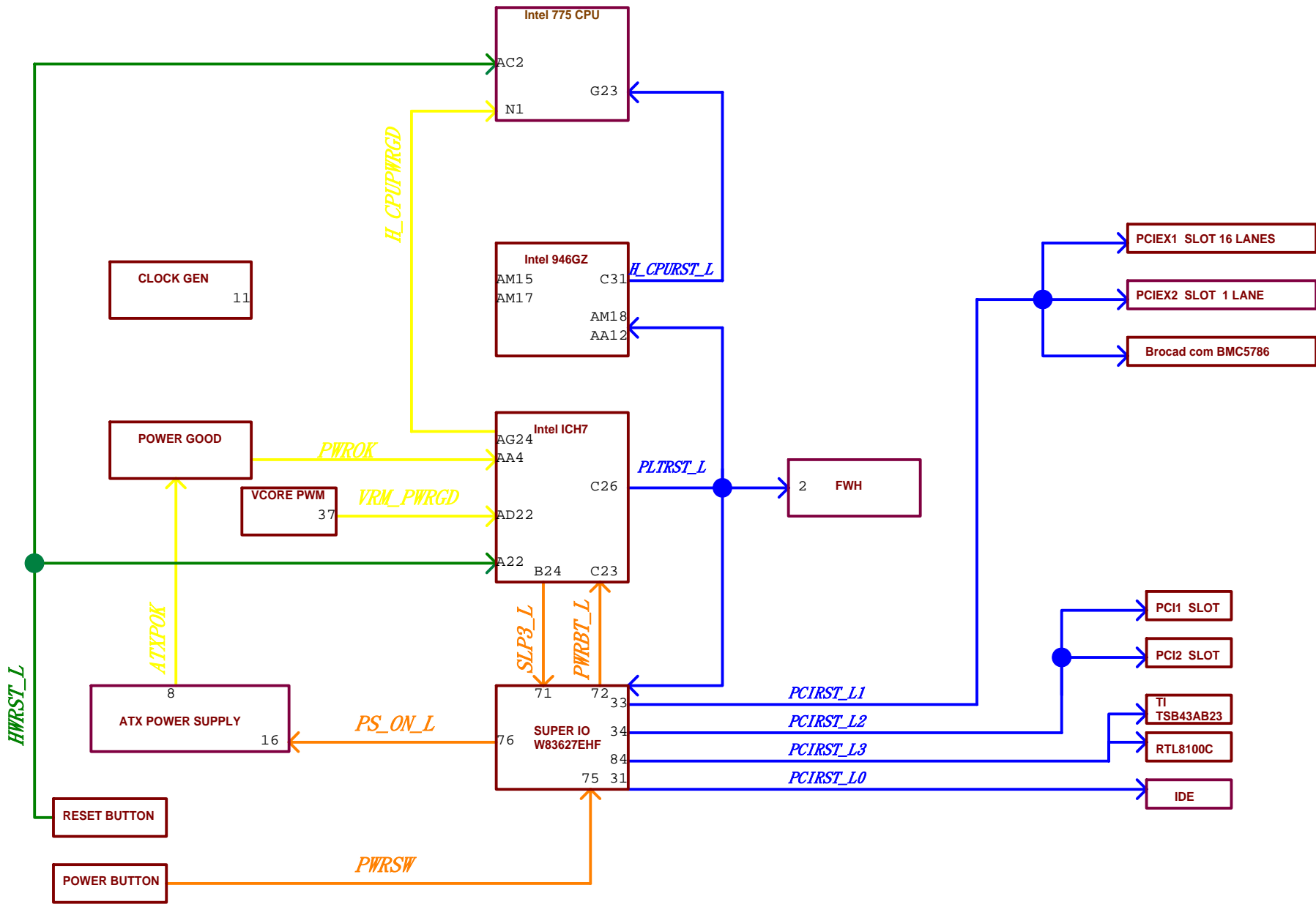
SCH VER	PCB VER	DATE	DESCRIPTION
A	A	2006/05/10	Preliminary release

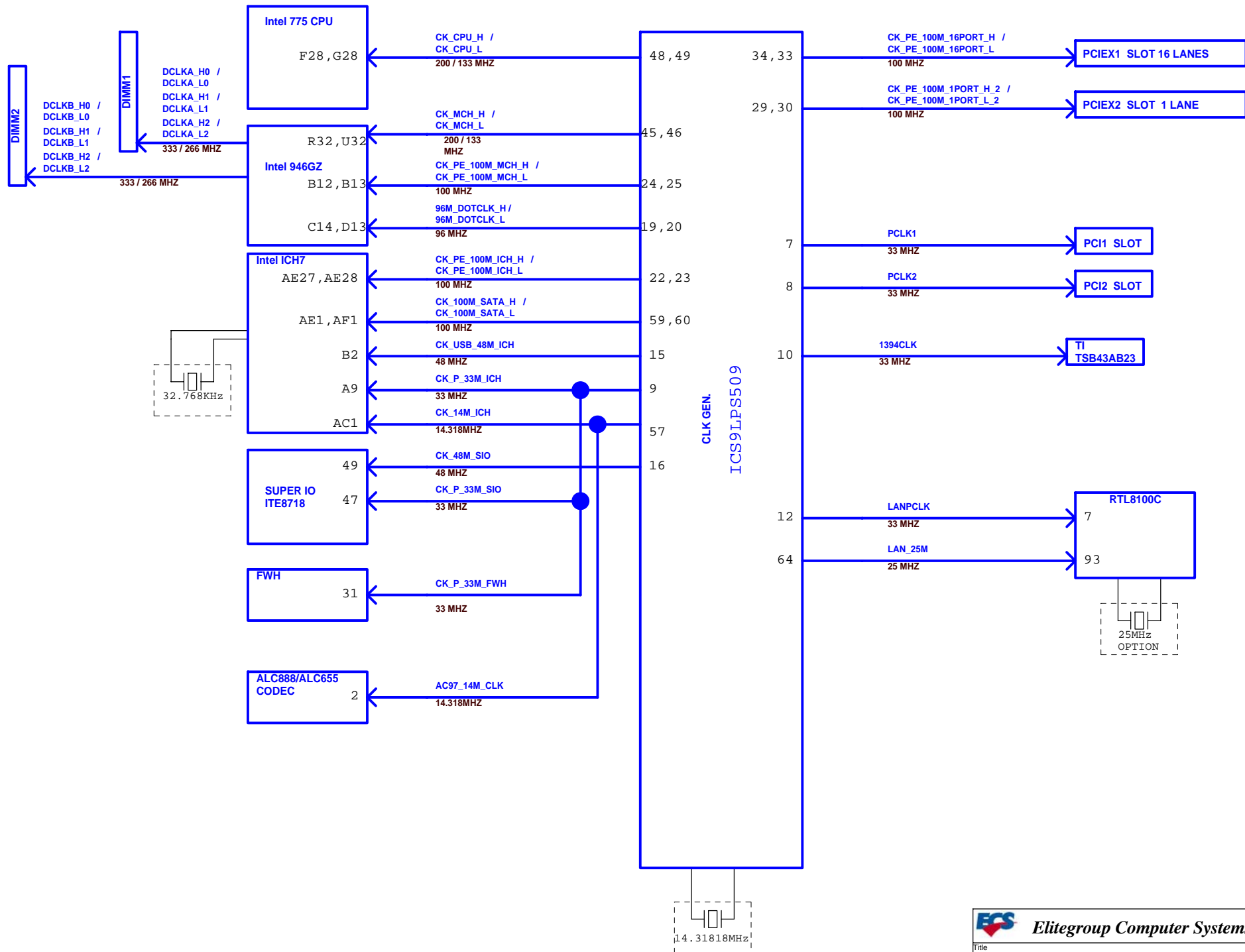
 **Elitegroup Computer Systems**

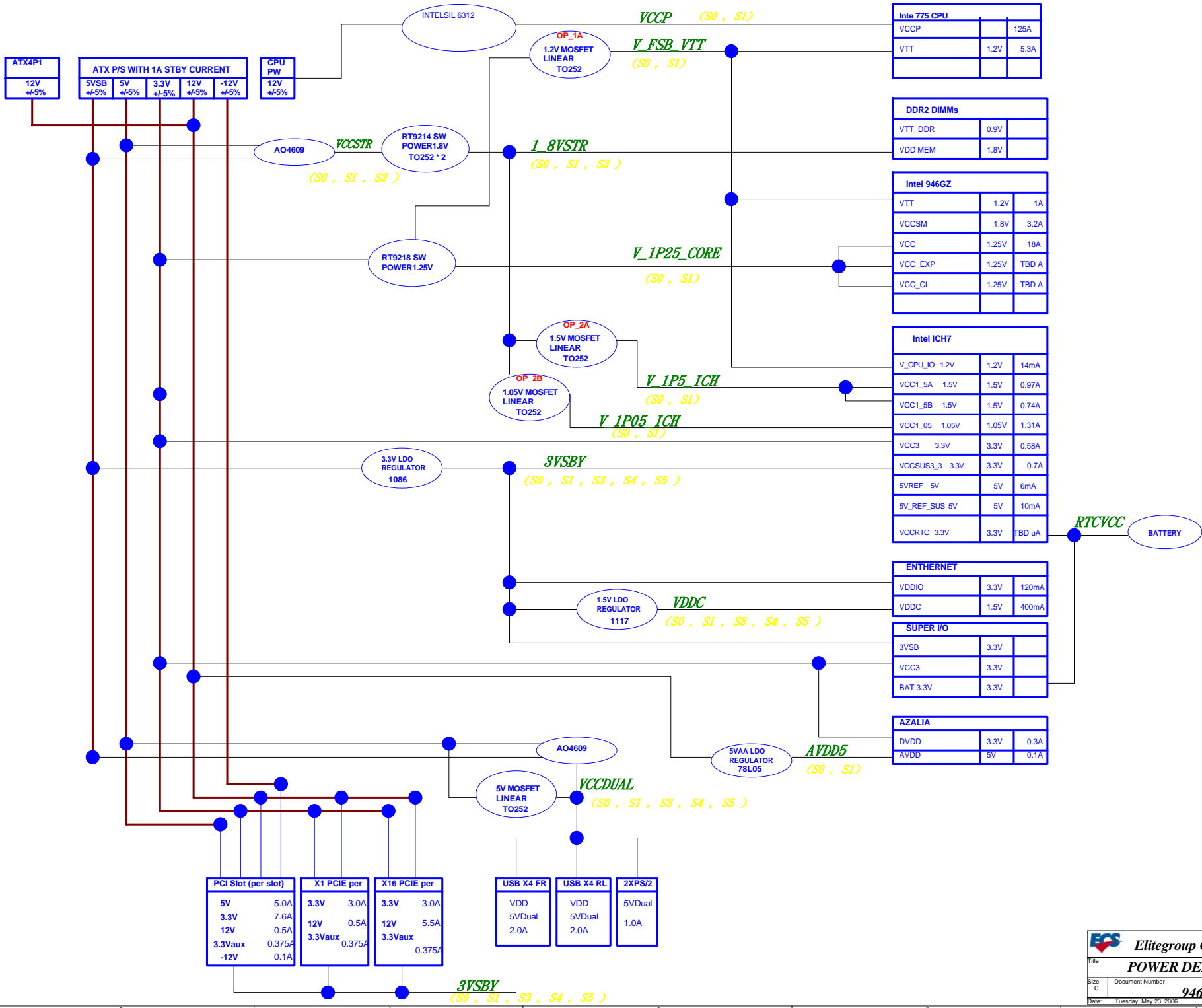
Title: **Change list**

Size: Custom Document Number: **946GZT-AM** Rev: A

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Intel 775 CPU		
VCCP		125A
VTT	1.2V	5.3A

DDR2 DIMMs		
VTT_DDR	0.9V	
VDD MEM	1.8V	

Intel 946GZ		
VTT	1.2V	1A
VCCSM	1.8V	3.2A
VCC	1.25V	18A
VCC_EXP	1.25V	TBD A
VCC_CL	1.25V	TBD A

Intel ICH7			
V_CPU_IO	1.2V	1.2V	14mA
VCC1_5A	1.5V	1.5V	0.97A
VCC1_5B	1.5V	1.5V	0.74A
VCC1_05	1.05V	1.05V	1.31A
VCC3	3.3V	3.3V	0.58A
VCCSUS3_3	3.3V	3.3V	0.7A
5VREF	5V	5V	6mA
5V_REF_SUS	5V	5V	10mA
VCCRTC	3.3V	3.3V	TBD uA

ETHERNET		
VDDIO	3.3V	120mA
VDDC	1.5V	400mA

SUPER I/O		
3VSB	3.3V	
VCC3	3.3V	
BAT 3.3V	3.3V	

AZALIA		
DVDD	3.3V	0.3A
AVDD	5V	0.1A

ATX P/S WITH 1A STBY CURRENT					
12V	5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

CPU PW	
12V	+/-5%

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.375A

X16 PCIE per	
3.3V	3.0A
12V	5.5A
3.3Vaux	0.375A

USB X4 FR	
VDD	5VDual
	2.0A

USB X4 RL	
VDD	5VDual
	2.0A

2XPS/2	
5VDual	1.0A