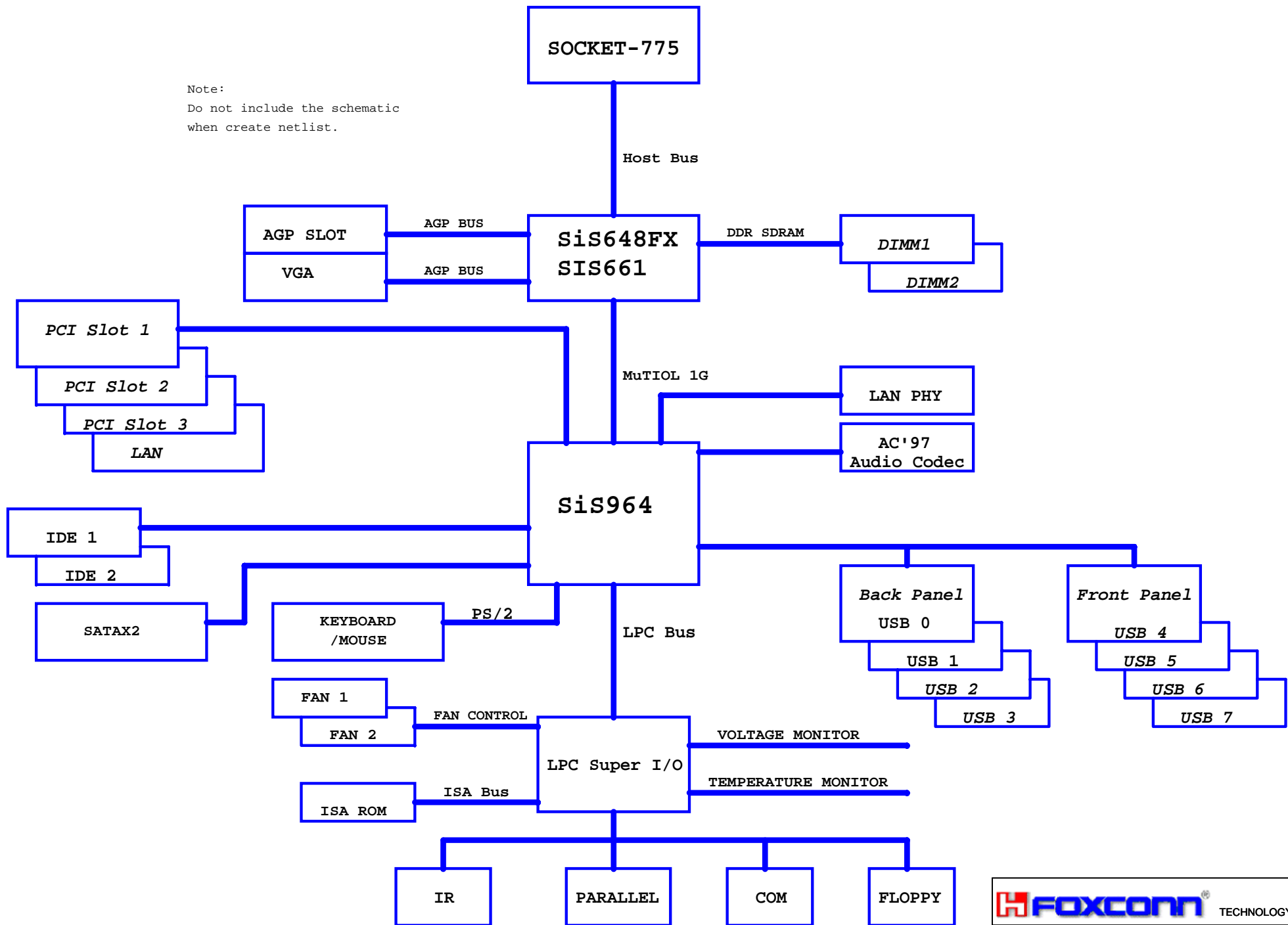
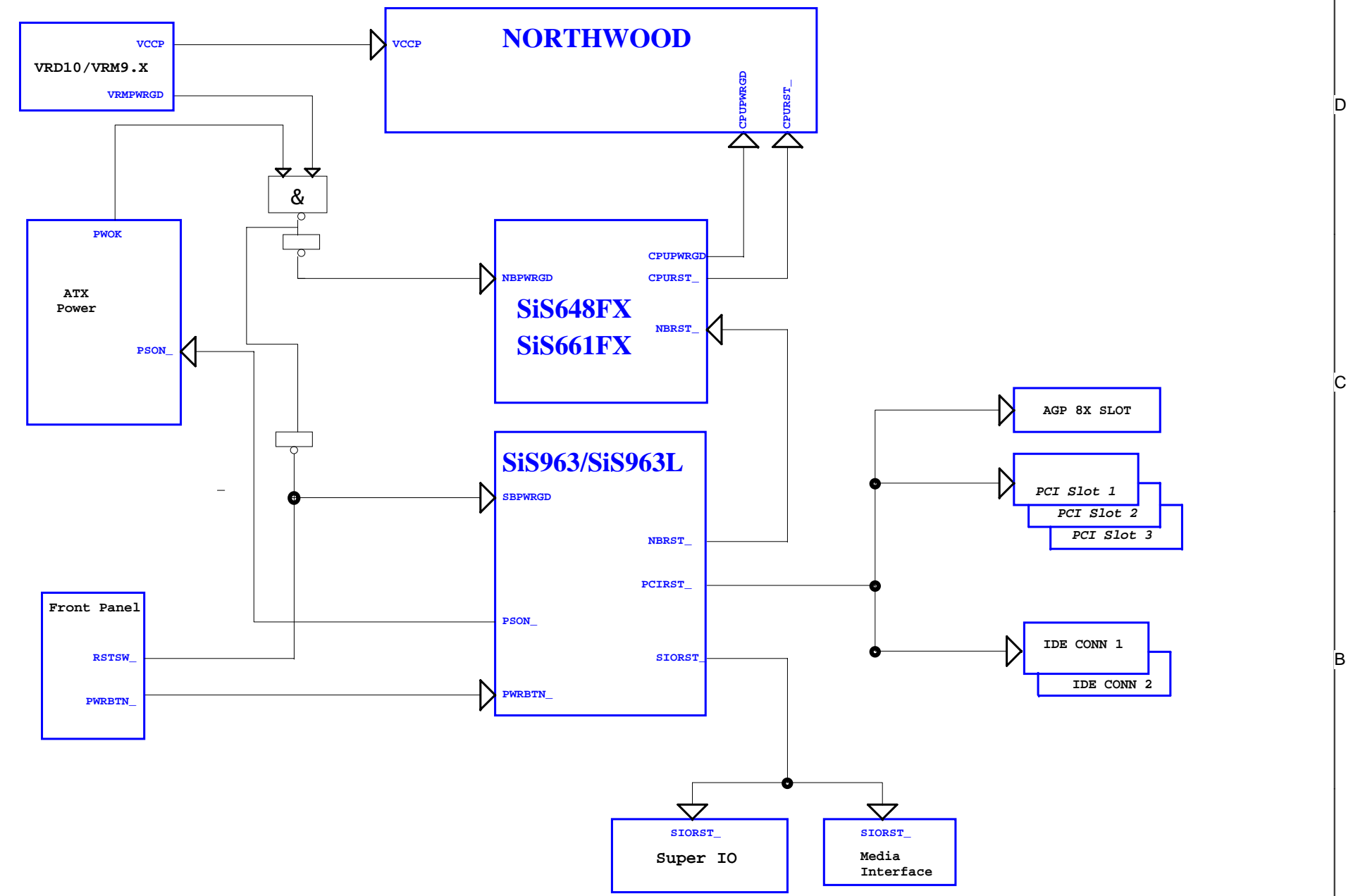
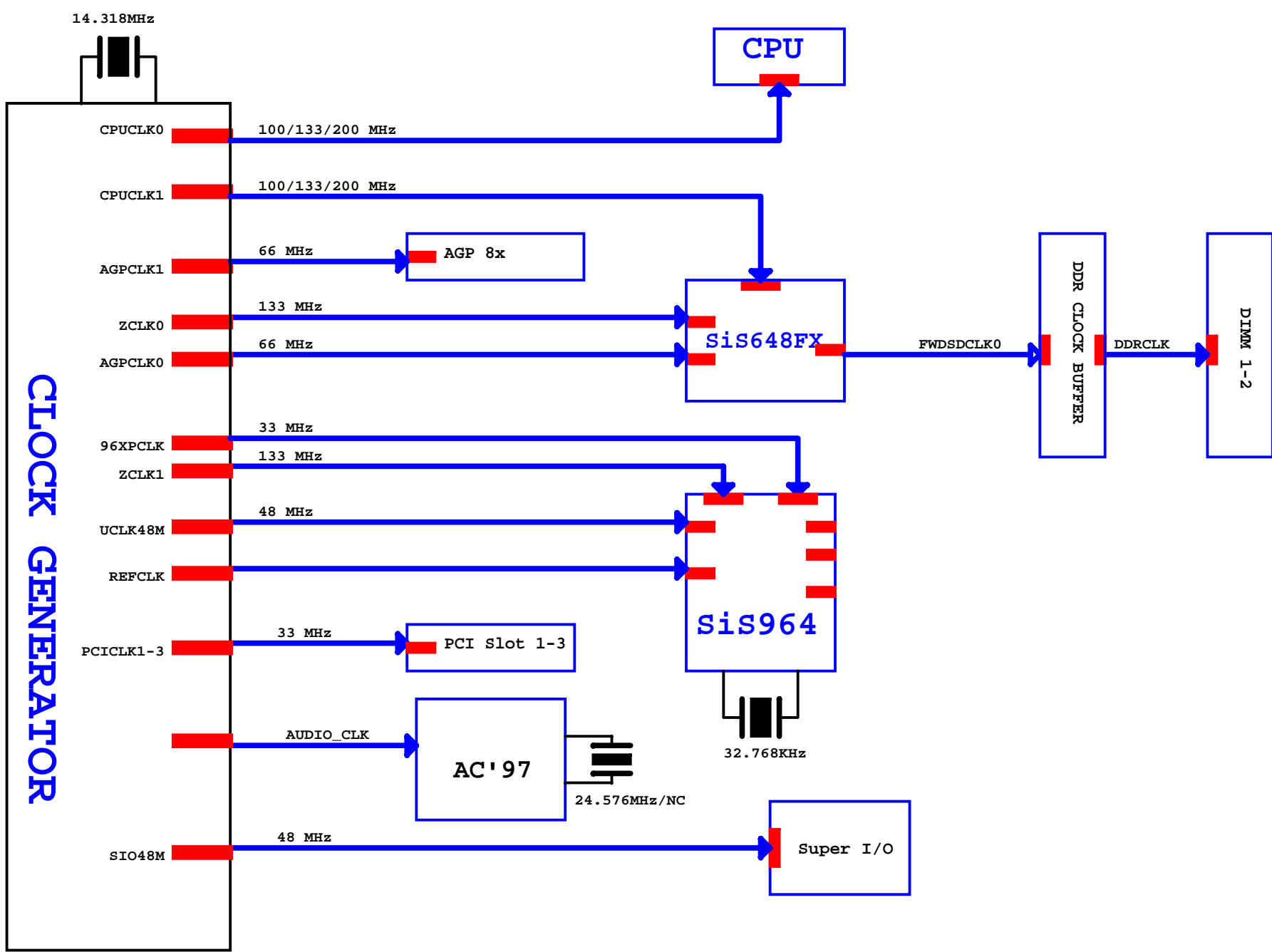
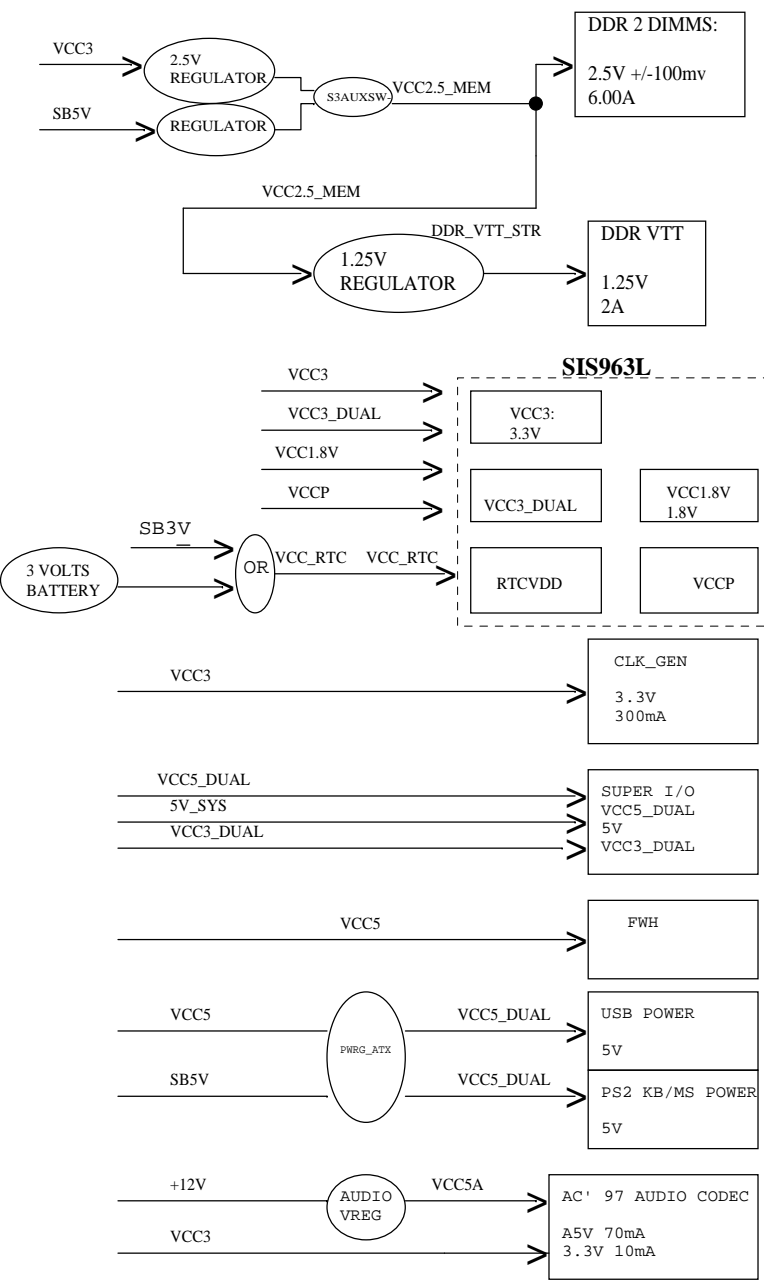
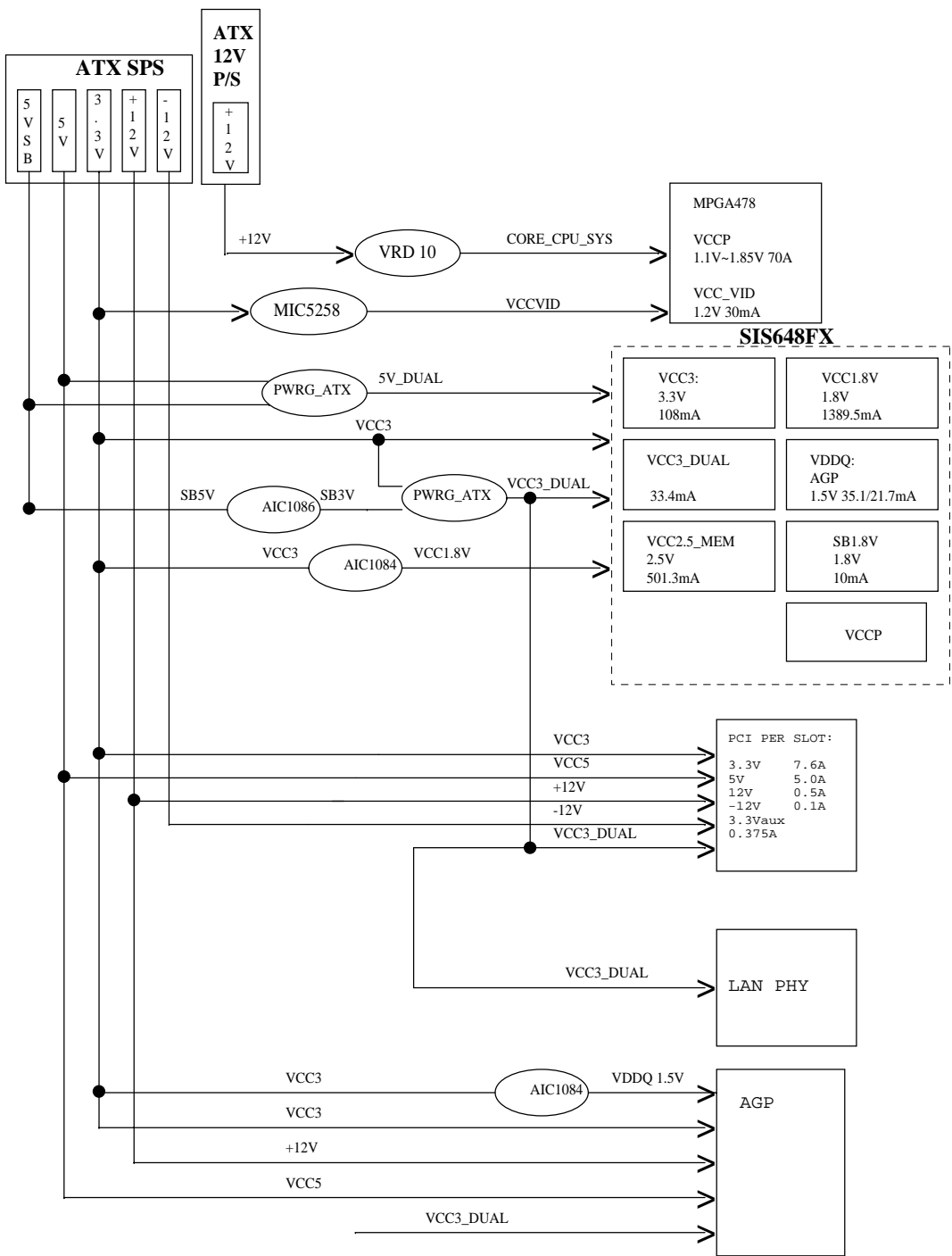


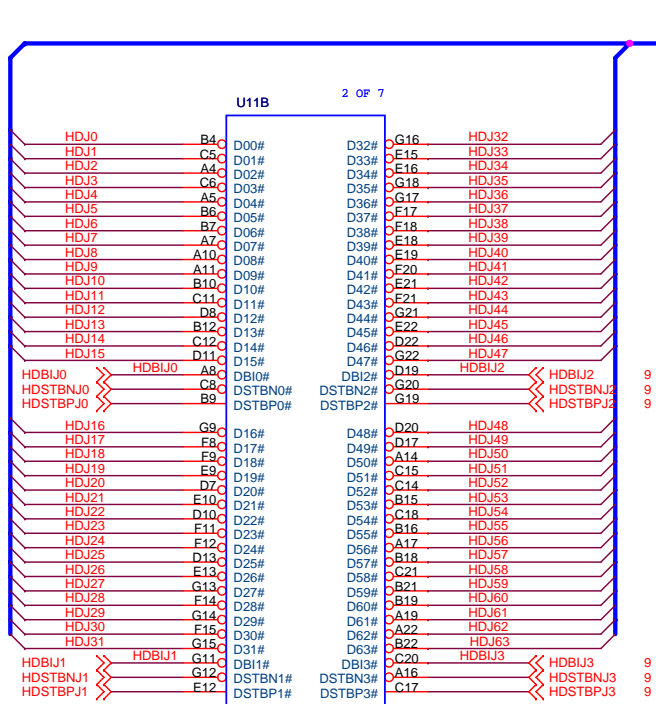
Note:
Do not include the schematic
when create netlist.







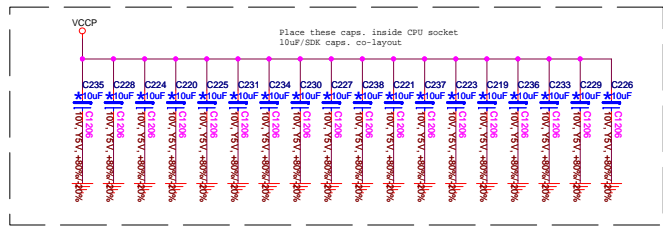




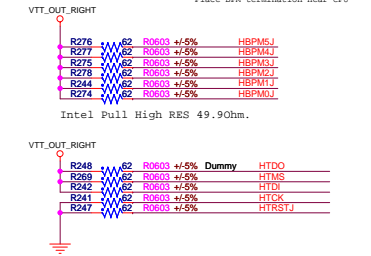
U11E 5 OF 7	
AG22	VCCP1
K29	VCCP2
AM26	VCCP3
AL8	VCCP4
AE12	VCCP5
AE11	VCCP6
W23	VCCP7
W24	VCCP8
W25	VCCP9
T26	VCCP10
Y28	VCCP11
AL18	VCCP12
AG25	VCCP13
W30	VCCP14
Y30	VCCP15
AN14	VCCP16
VCCP17	VCCP17
Y26	VCCP18
AG29	VCCP19
M29	VCCP20
U24	VCCP21
AC27	VCCP22
AM18	VCCP23
AB8	VCCP24
AC26	VCCP25
J8	VCCP26
J28	VCCP27
T30	VCCP28
AM9	VCCP29
AF15	VCCP30
AC8	VCCP31
AE14	VCCP32
N23	VCCP33
W29	VCCP34
U29	VCCP35
AC24	VCCP36
AG24	VCCP37
Y23	VCCP38
AN26	VCCP39
AN25	VCCP40
AN11	VCCP41
AN18	VCCP42
Y27	VCCP43
Y25	VCCP44
AD24	VCCP45
AE23	VCCP46
AE22	VCCP47
AN19	VCCP48
V8	VCCP49
K8	VCCP50
AE21	VCCP51
AM30	VCCP52
AE19	VCCP53
AC30	VCCP54
AE15	VCCP55
M30	VCCP56
K27	VCCP57
M24	VCCP58
AN21	VCCP59
AC28	VCCP60
N25	VCCP61
AE18	VCCP62
W26	VCCP63
AD25	VCCP64
M8	VCCP65
N30	VCCP66
AD26	VCCP67
A126	VCCP68
AM29	VCCP69
M25	VCCP70
M26	VCCP71
L8	VCCP72
U25	VCCP73
V8	VCCP74
A12	VCCP75
AD27	VCCP76
U23	VCCP77
M23	VCCP78
N27	VCCP79
AG29	VCCP80
AM22	VCCP81
K28	VCCP82
U8	VCCP83
AK18	VCCP84
AD8	VCCP85
K24	VCCP86
AH28	VCCP87
AH21	VCCP88
	VCCP89
	VCCP90
	VCCP91
	VCCP92
	VCCP93
	VCCP94
	VCCP95
	VCCP96
	VCCP97
	VCCP98
	VCCP99
	VCCP100

U11F 6 OF 7	
AF9	VCCP185
AH22	VCCP186
AH11	VCCP187
AM14	VCCP188
AH10	VCCP189
AE29	VCCP190
AH27	VCCP191
AG26	VCCP192
AK19	VCCP193
AG15	VCCP194
J24	VCCP195
T24	VCCP196
J13	VCCP197
T28	VCCP198
W28	VCCP199
J25	VCCP200
J27	VCCP201
AG19	VCCP202
AL23	VCCP203
AG25	VCCP204
W4	VCCP205
Y24	VCCP206
AK14	VCCP207
J9	VCCP208
AJ22	VCCP209
AF14	VCCP210
J30	VCCP211
M27	VCCP212
AG18	VCCP213
A48	VCCP214
AH27	VCCP215
A48	VCCP216
AG8	VCCP217
AN9	VCCP218
AD29	VCCP219
W8	VCCP220
AH8	VCCP221
N24	VCCP222
Y27	VCCP223
AN22	VCCP224
K22	VCCP225
J14	VCCP226
AG11	VCCP227
AF19	VCCP228
N8	VCCP229
AM13	VCCP230
AK24	VCCP231
AJ10	VCCP232
AE2	VCCP233
AK4	VCCP234
AJ16	VCCP235
AE2	VCCP236
AE2	VCCP237
AE2	VCCP238
AE2	VCCP239
AE2	VCCP240
AE2	VCCP241
AE2	VCCP242
AE2	VCCP243
AE2	VCCP244
AE2	VCCP245
AE2	VCCP246
AE2	VCCP247
AE2	VCCP248
AE2	VCCP249
AE2	VCCP250
AE2	VCCP251
AE2	VCCP252
AE2	VCCP253
AE2	VCCP254
AE2	VCCP255
AE2	VCCP256
AE2	VCCP257
AE2	VCCP258
AE2	VCCP259
AE2	VCCP260
AE2	VCCP261
AE2	VCCP262
AE2	VCCP263
AE2	VCCP264
AE2	VCCP265
AE2	VCCP266
AE2	VCCP267
AE2	VCCP268
AE2	VCCP269
AE2	VCCP270
AE2	VCCP271
AE2	VCCP272
AE2	VCCP273
AE2	VCCP274
AE2	VCCP275
AE2	VCCP276
AE2	VCCP277
AE2	VCCP278
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AE2	VCCP285
AE2	VCCP286
AE2	VCCP287
AE2	VCCP288
AE2	VCCP289
AE2	VCCP290
AE2	VCCP291
AE2	VCCP292
AE2	VCCP293
AE2	VCCP294
AE2	VCCP295
AE2	VCCP296
AE2	VCCP297
AE2	VCCP298
AE2	VCCP299
AE2	VCCP300

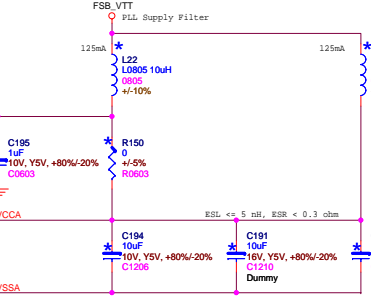
U11G 7 OF 7	
H22	VSS126
H21	VSS127
H20	VSS128
H18	VSS129
H18	VSS130
H17	VSS131
H17	VSS132
H17	VSS133
H17	VSS134
H17	VSS135
H17	VSS136
H17	VSS137
H17	VSS138
H17	VSS139
H17	VSS140
H17	VSS141
H17	VSS142
H17	VSS143
H17	VSS144
H17	VSS145
H17	VSS146
H17	VSS147
H17	VSS148
H17	VSS149
H17	VSS150
H17	VSS151
H17	VSS152
H17	VSS153
H17	VSS154
H17	VSS155
H17	VSS156
H17	VSS157
H17	VSS158
H17	VSS159
H17	VSS160
H17	VSS161
H17	VSS162
H17	VSS163
H17	VSS164
H17	VSS165
H17	VSS166
H17	VSS167
H17	VSS168
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H17	VSS180
H17	VSS181
H17	VSS182
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H17	VSS287
H17	VSS288
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H17	VSS291
H17	VSS292
H17	VSS293
H17	VSS294
H17	VSS295
H17	VSS296
H17	VSS297
H17	VSS298
H17	VSS299
H17	VSS300



note: 7/6-change termination 49.9 to R0702 47

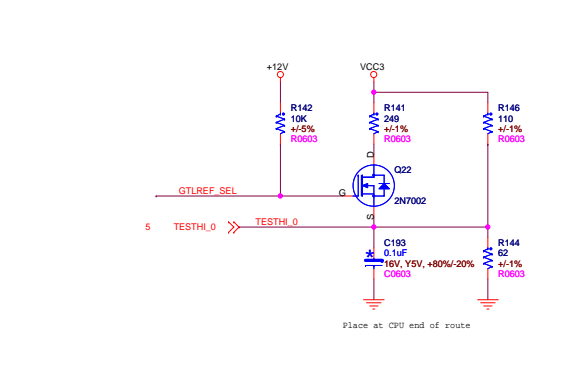


Intel Pull High RES 49.9ohm.

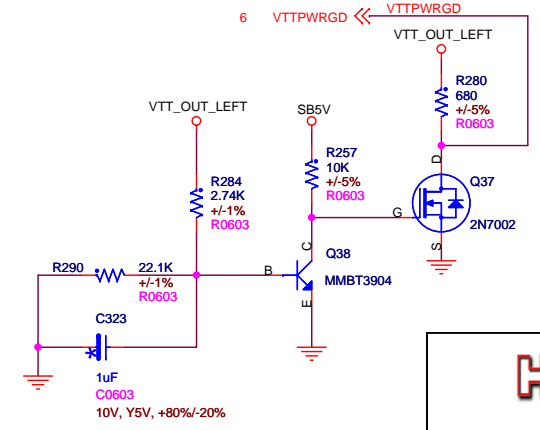
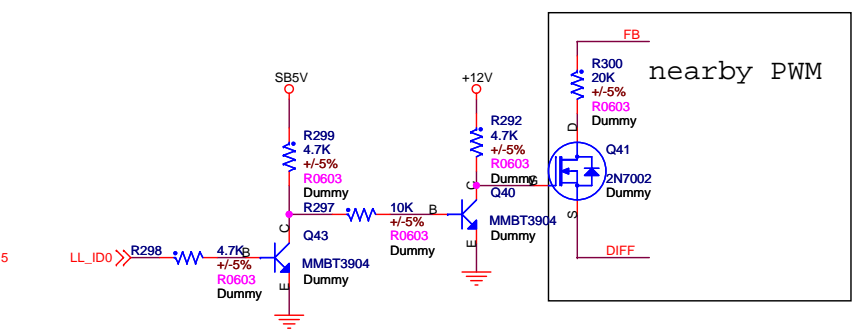
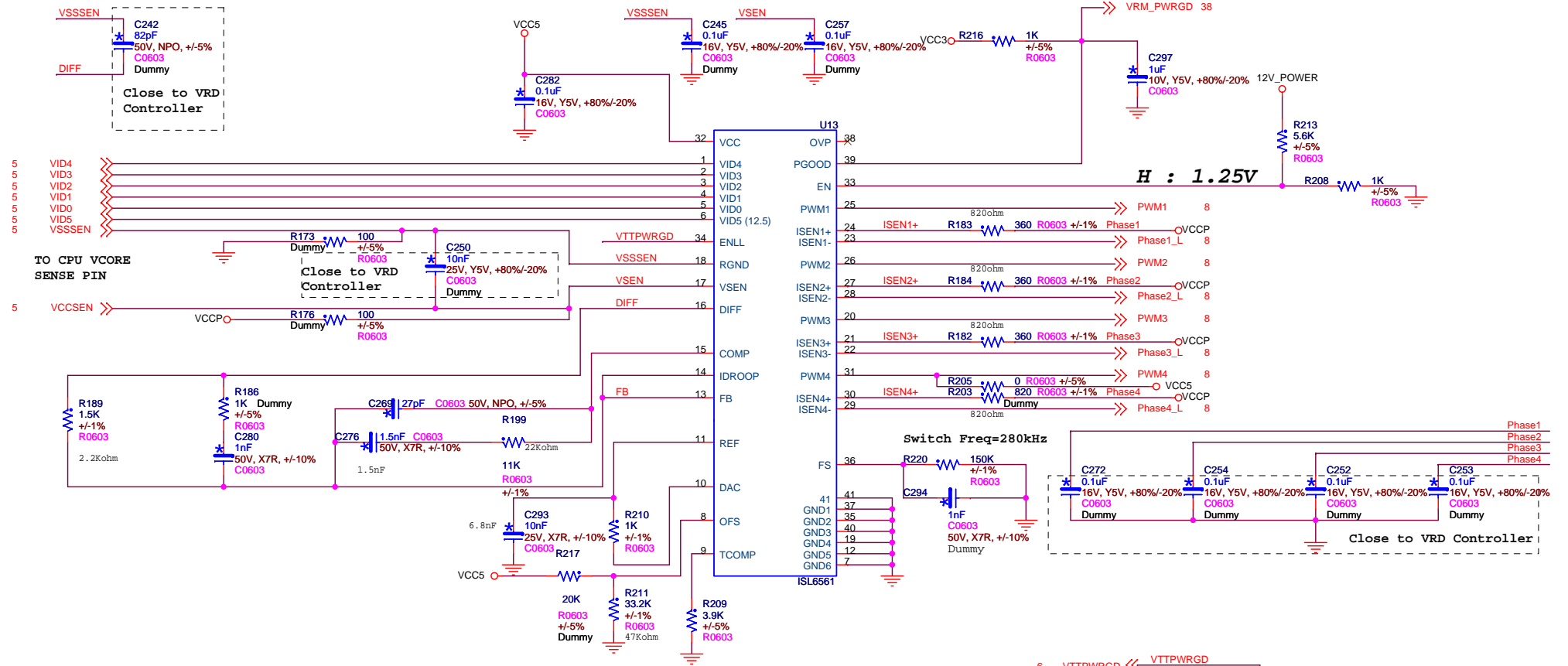



Notes:
 1. Cap. should be within 600 mils of the VCCA and VSSA pins
 2. VCCA route should be parallel and next to VSSA route
 3. Min. 12 mils trace from the filter to the processor pins
 4. The inductors should be close to the cap.

U11D 4 OF 7	
HTCK	AE1
HTDO	AD1
HTMS	AC1
HTRS1J	AG1
	TRST#
	VTT1
	B26
	B30
	B30
	C29
	VTT5
	VTT6
	B27
	VTT8
	C28
	BPM1#
	VTT9
	A28
	VTT10
	A27
	C30
	VTT12
	A30
	VTT13
	C26
	VTT14
	C26
	VTT15
	VTT16
	D27
	VTT17
	VTT18
	VTT19
	D26
	D26
	B26
	D26
	D30
	AM6
	VTT19
	VTT20
	D26
	VTT22
	D30
	VTT23
	VTT24
	VTT25
	VTT26
	VTT27
	VTT28
	VTT29
	VTT30
	VTT31
	VTT32
	VTT33
	VTT34
	VTT35
	VTT36
	VTT37
	VTT38
	VTT39
	VTT40
	VTT41
	VTT42
	VTT43
	VTT44
	VTT45
	VTT46
	VTT47
	VTT48
	VTT49
	VTT50
	VTT51
	VTT52
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	VTT58
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	VTT64
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	VTT97
	VTT98
	VTT99
	VTT100



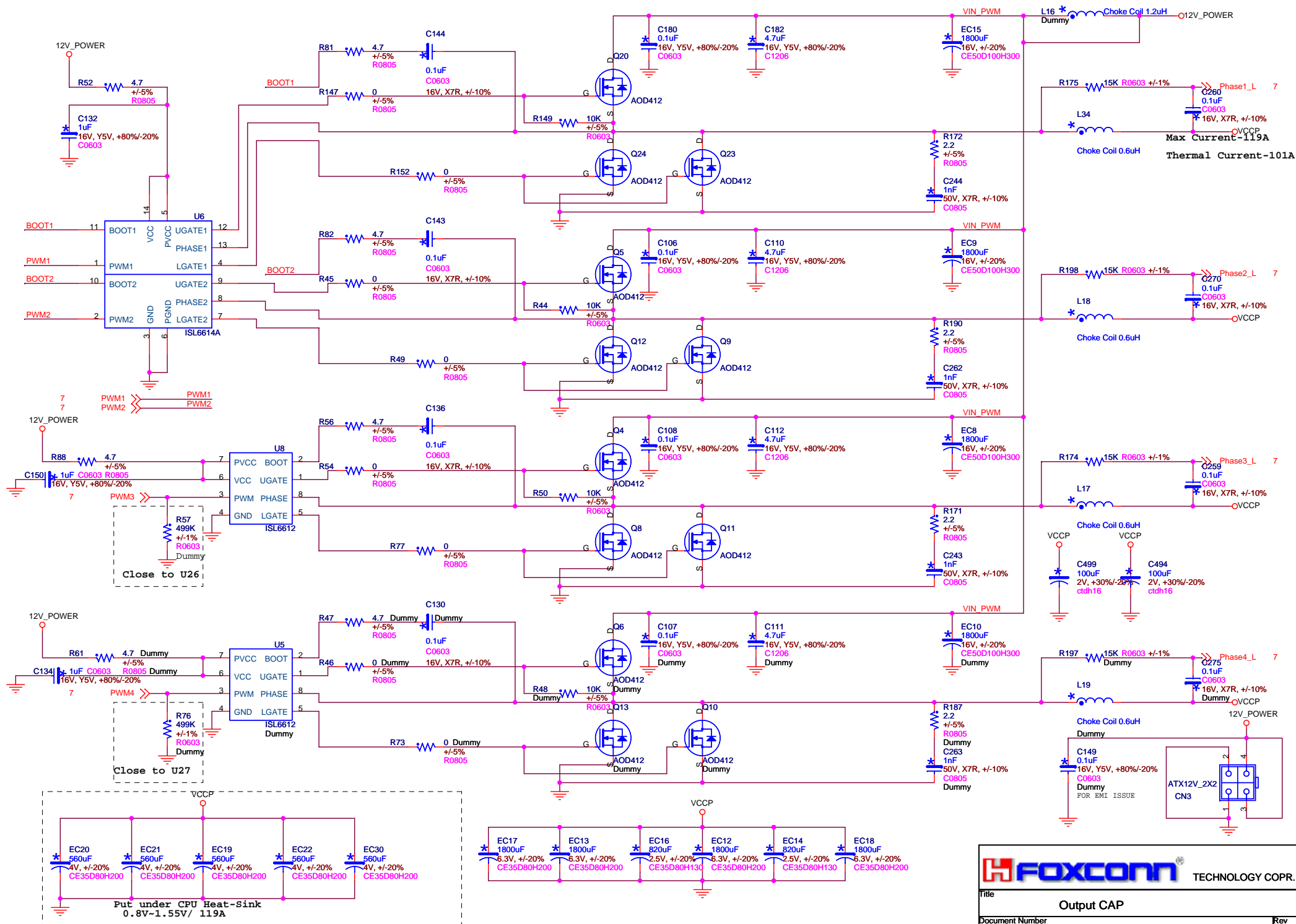
CPU Power Controller Intersil ISL6561 (VRD10.1)





FOXCONN PCEG

Title		
Voltage Regulator Down 10.1		
Size	Document Number	Rev
Custom	648M06	B
Date:	Wednesday, March 16, 2005	Sheet 7 of 41



FOXCONN TECHNOLOGY COPR.

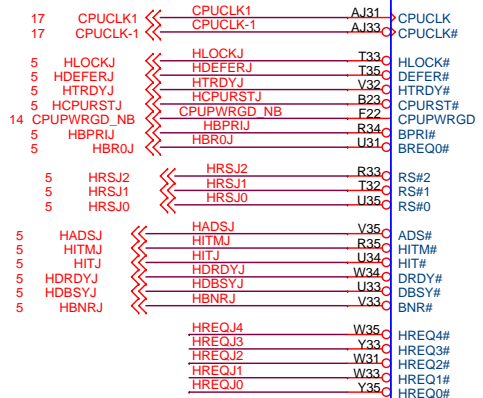
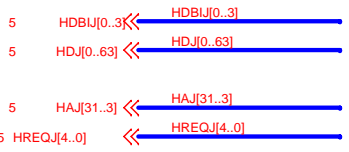
Title: **Output CAP**

Document Number: **648M06**

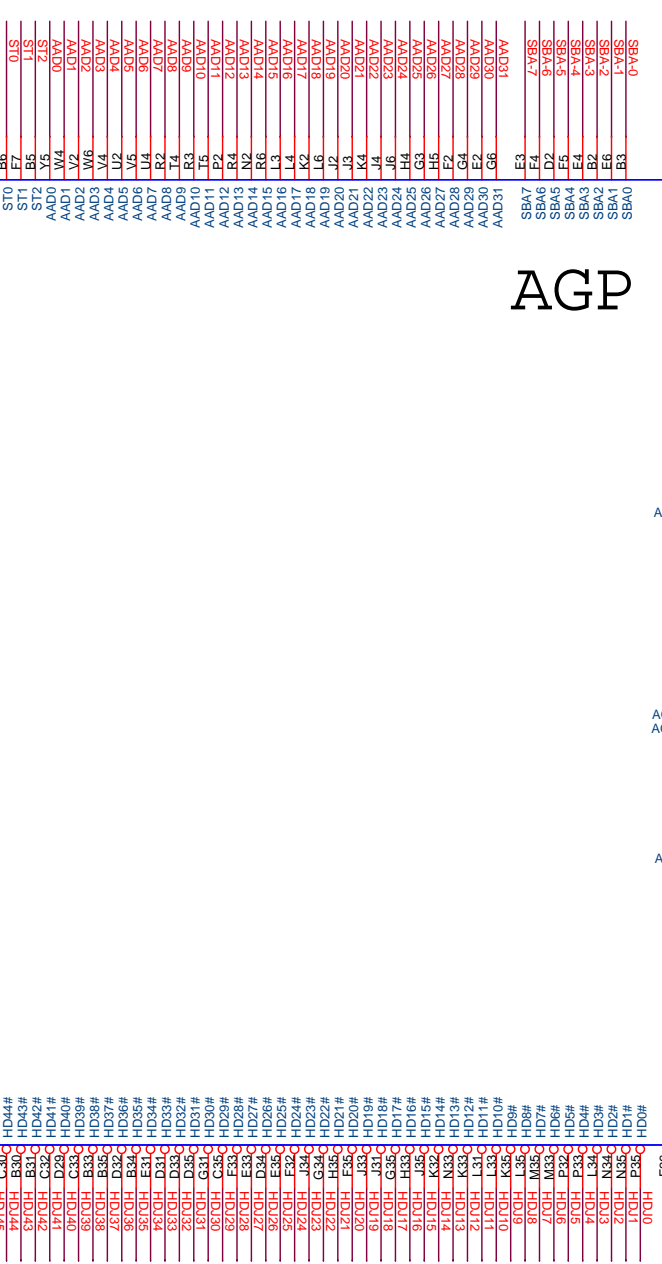
Date: Wednesday, March 16, 2005

Sheet 8 of 41

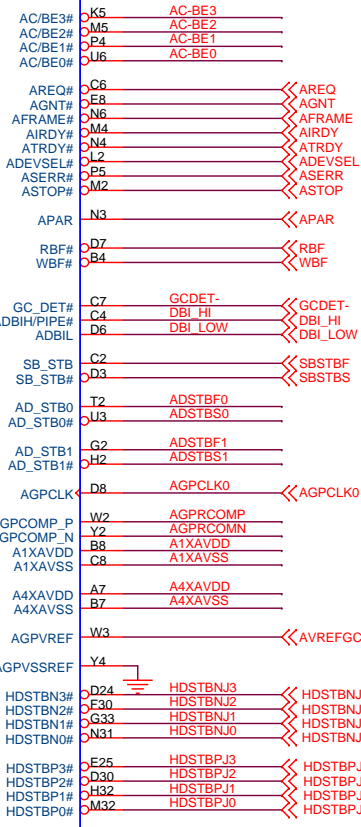
Rev B



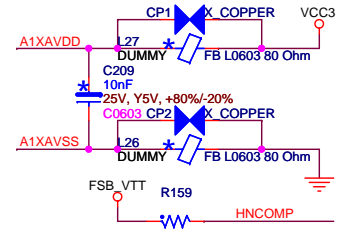
HOST



AGP



648C



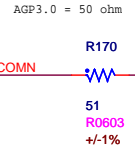
R49 change from 100 to 120

R158

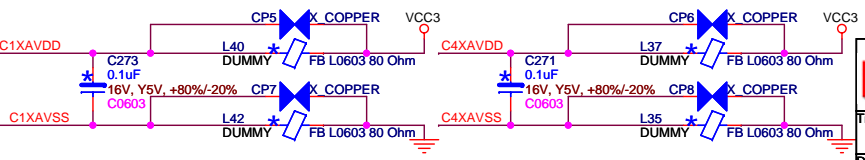
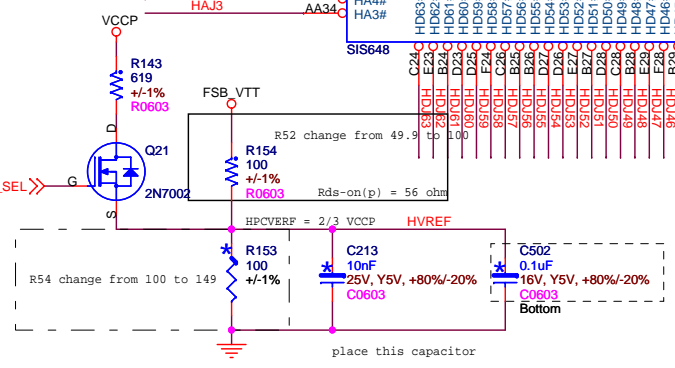
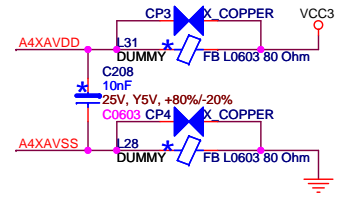
R159

R158

648	14 1%	120 1%
661FX	14 1%	120 1%



BC48, BC49 Change to 0.1uF?



Title: 661FX-1 HOST & AGP

Document Number: 648M06

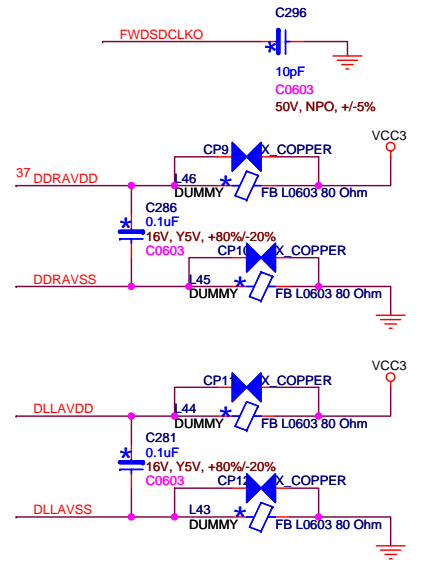
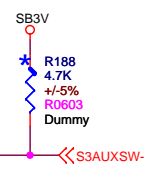
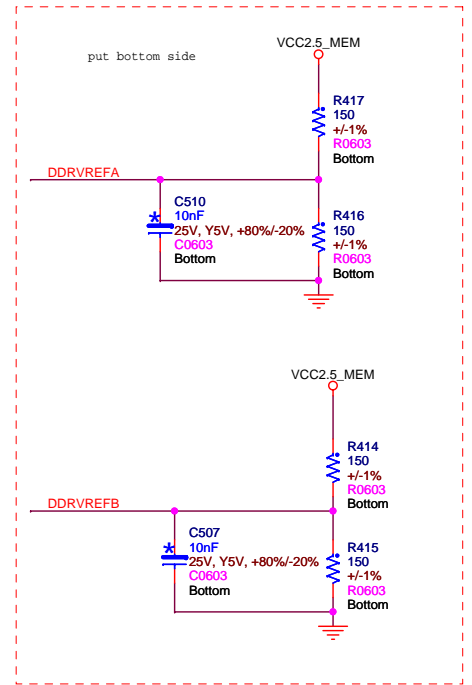
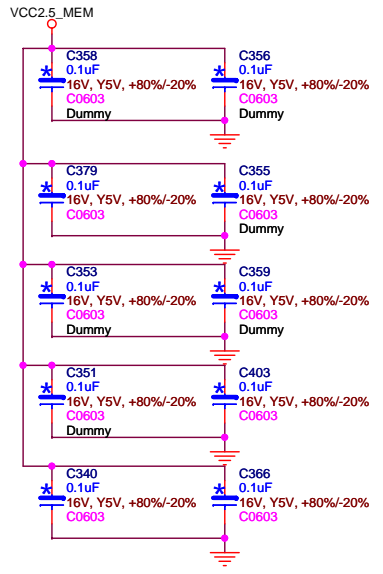
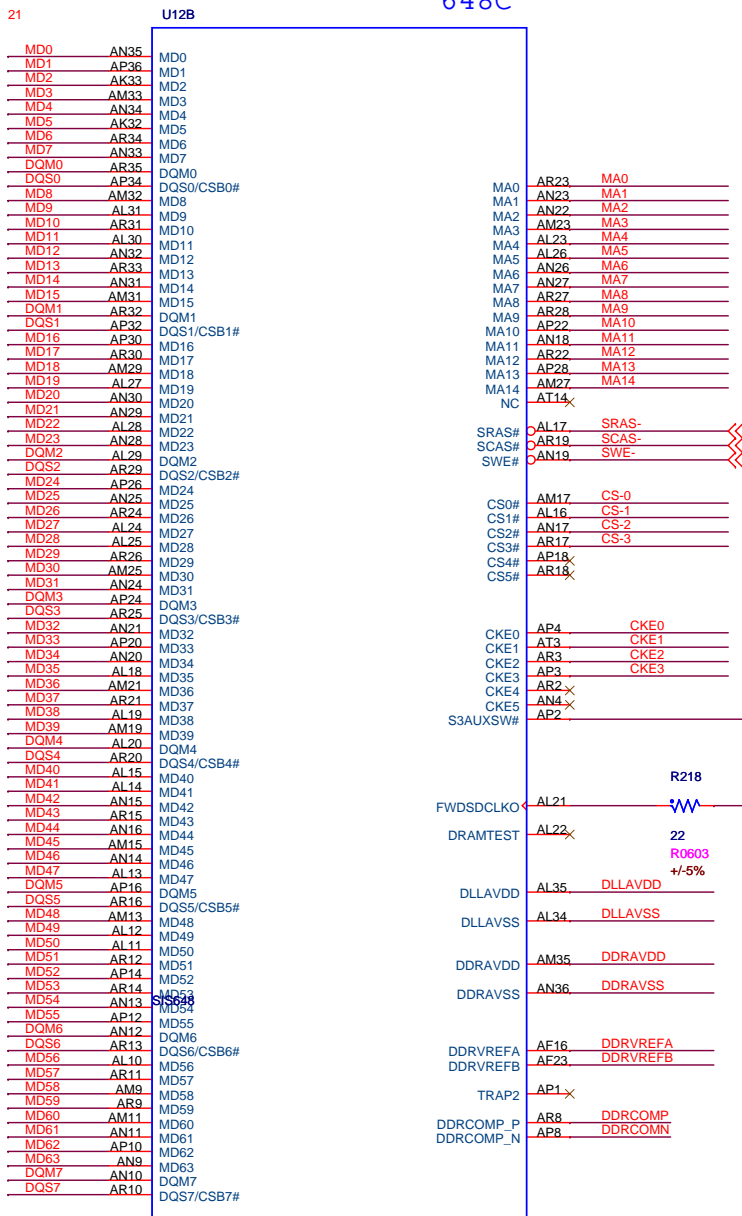
Date: Wednesday, March 16, 2005

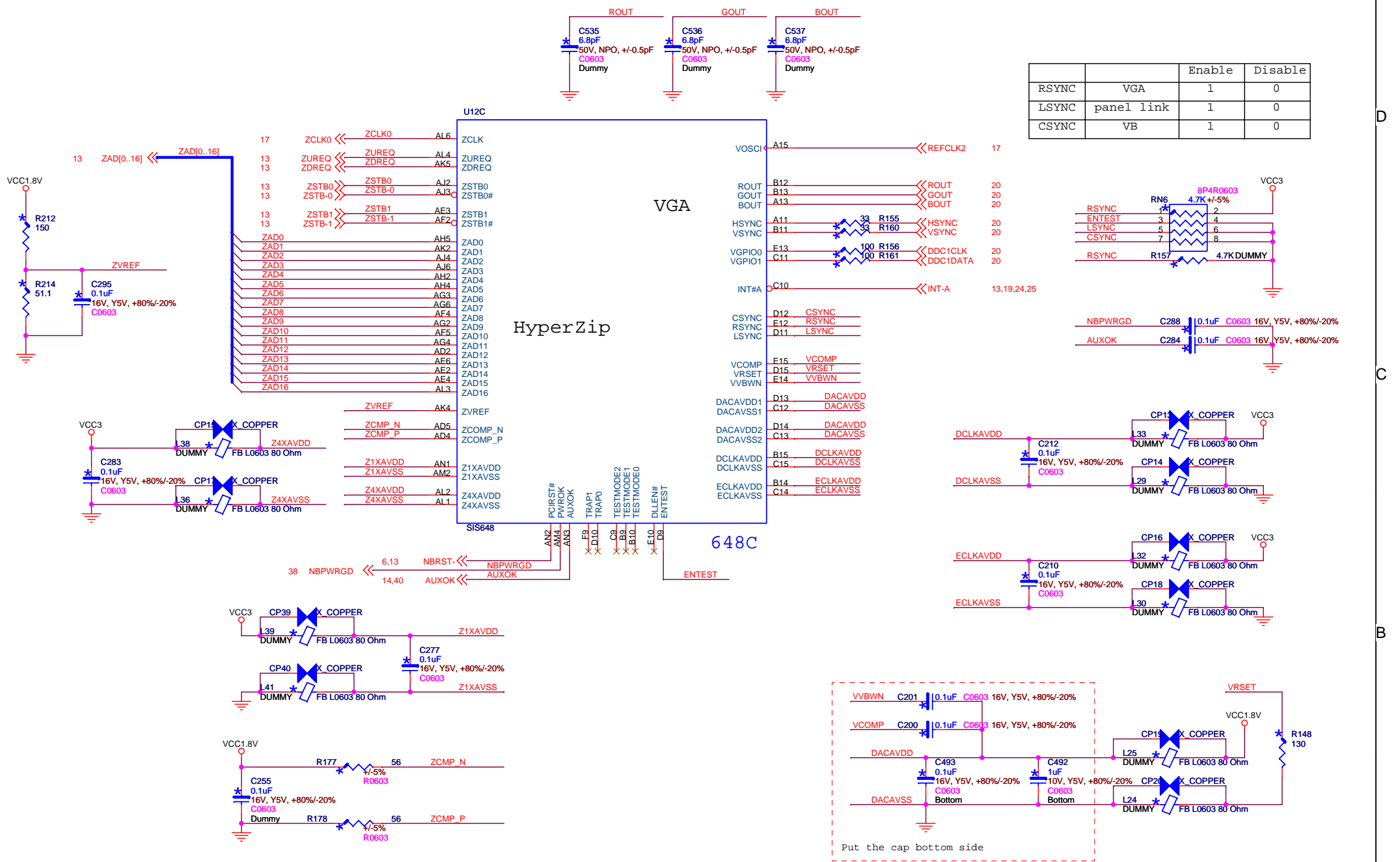
Sheet: 9 of 41

Rev: B

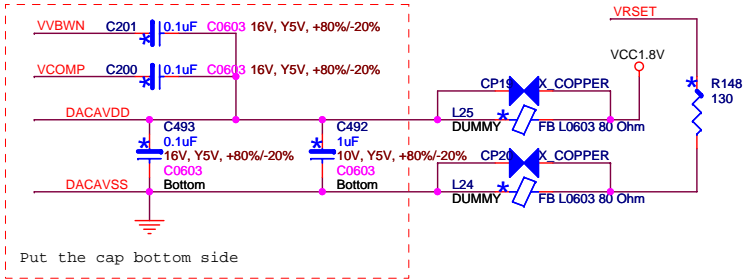
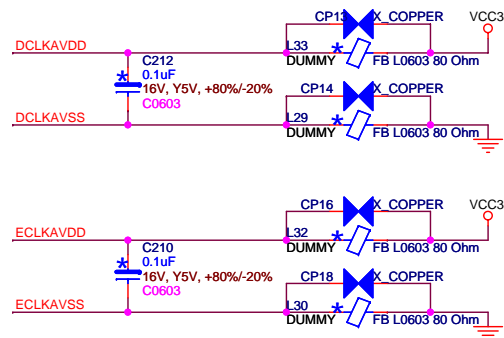
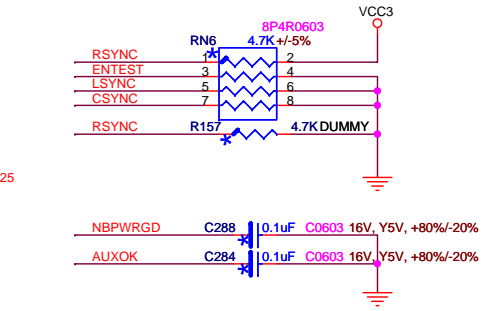
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DQM0..7	DQM0..7	21,23
DQS0..7	DQS0..7	21,23
MA0..14	MA0..14	21,23
CS-0..3	CS-0..3	21,23
CKE0..3	CKE0..3	21

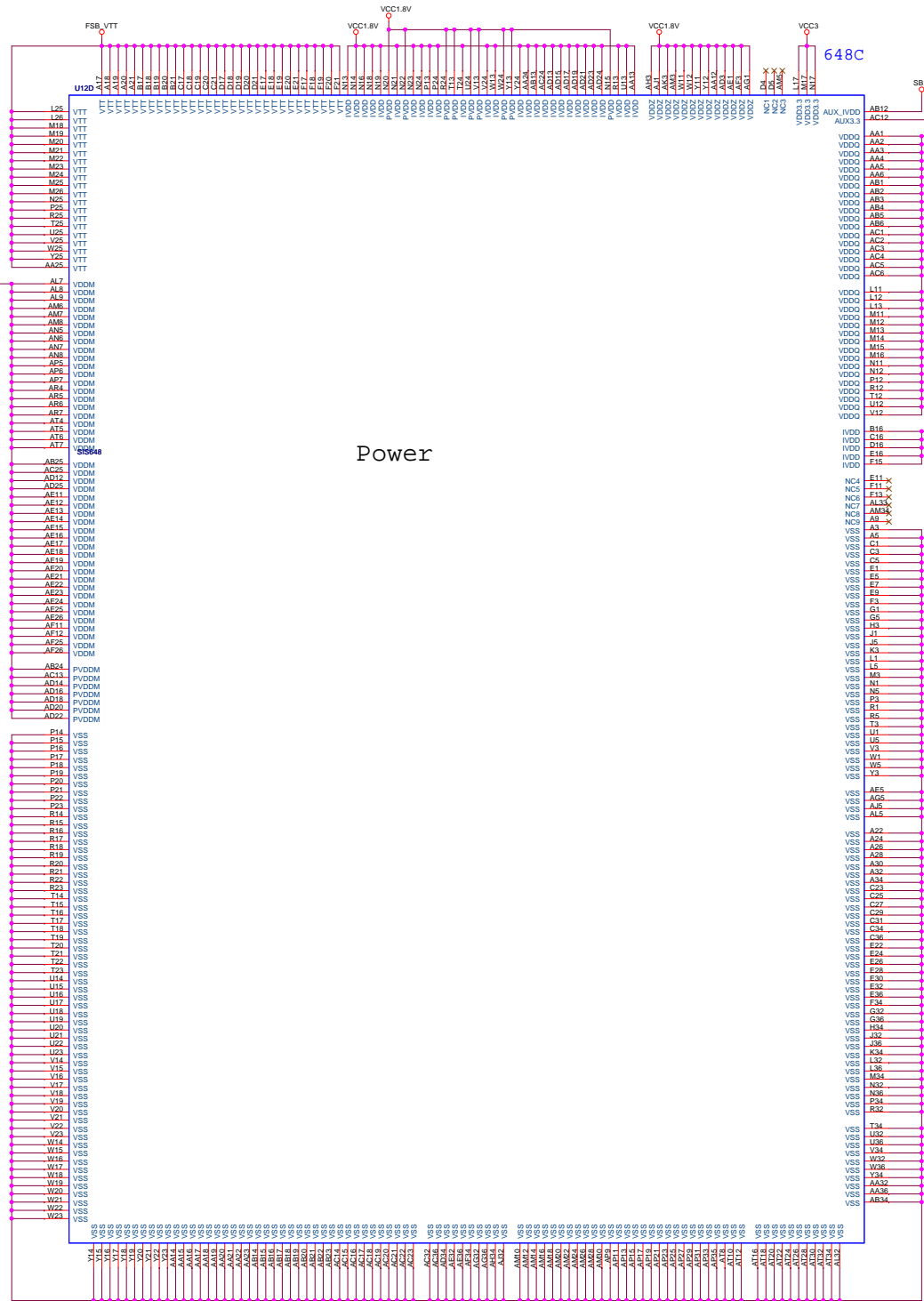
648C



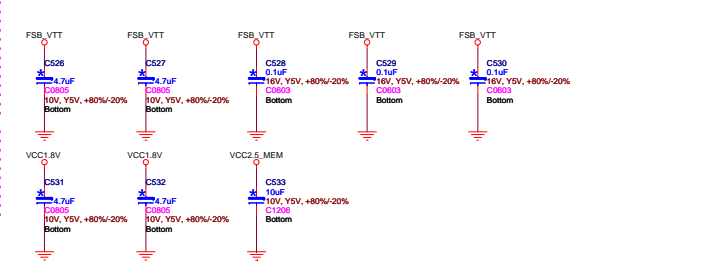
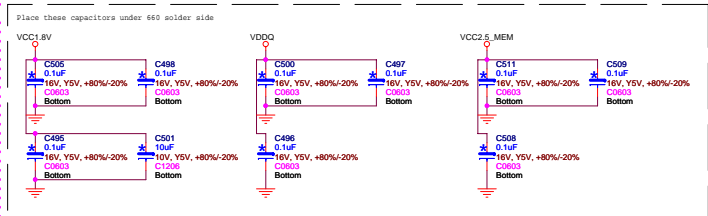
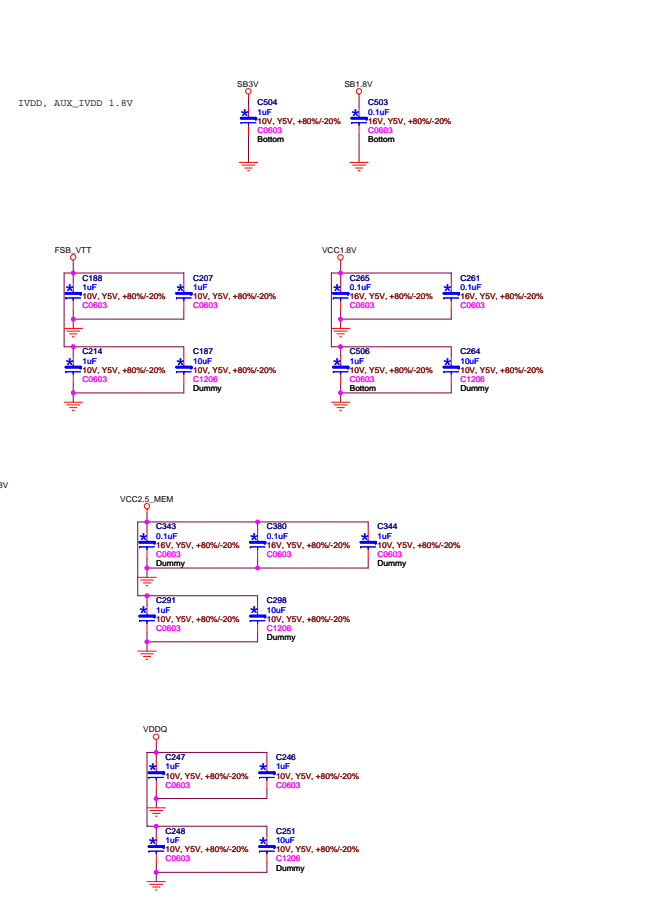


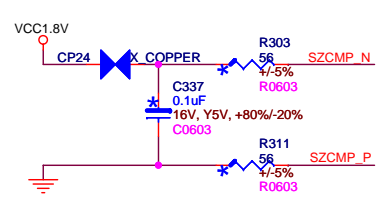
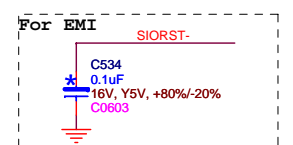
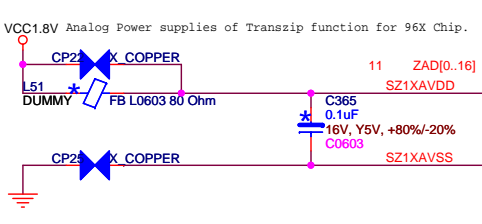
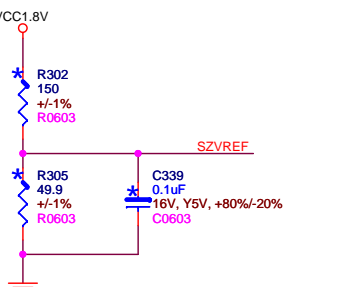
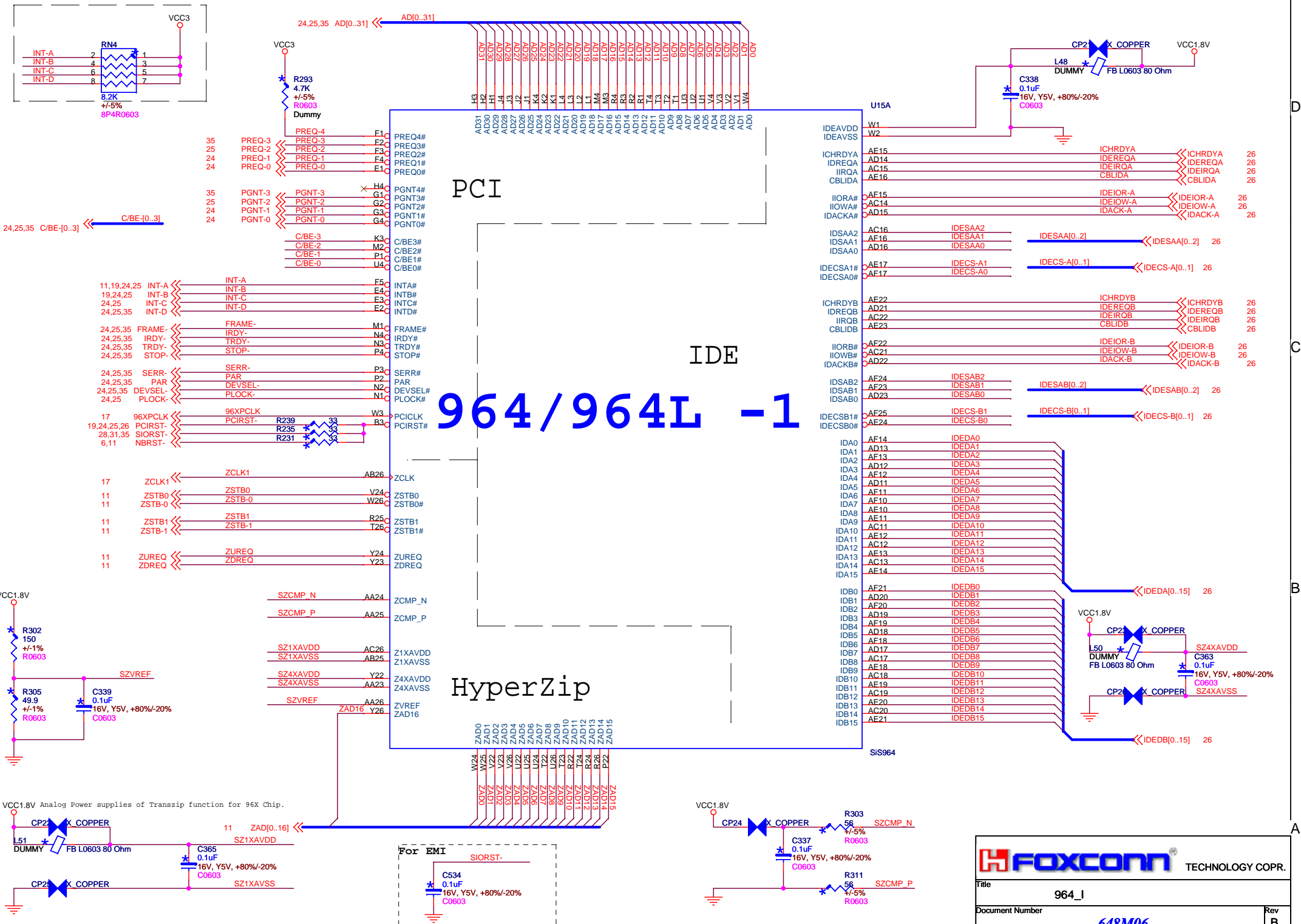
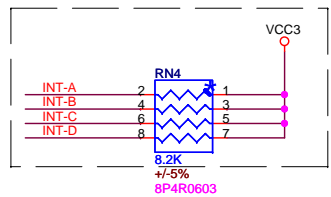
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RSYNC	VGA	1	0
LSYNC	panel link	1	0
CSYNC	VB	1	0

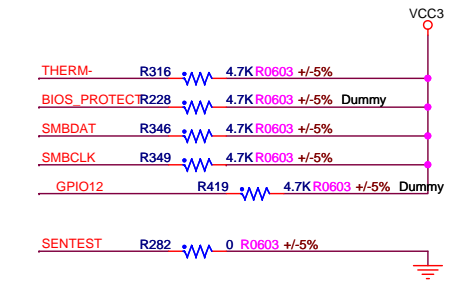
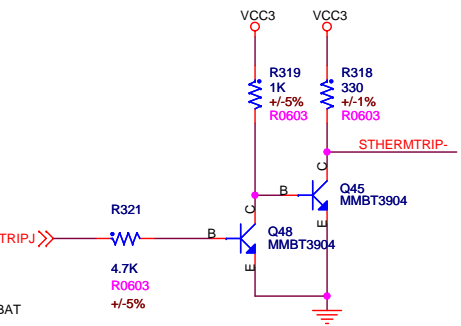
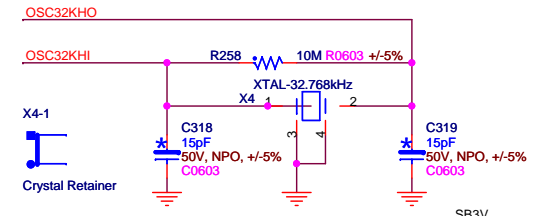
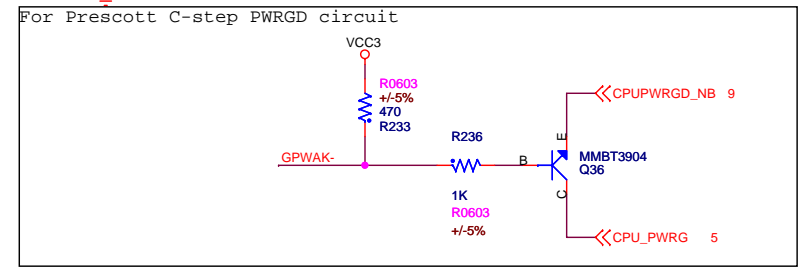
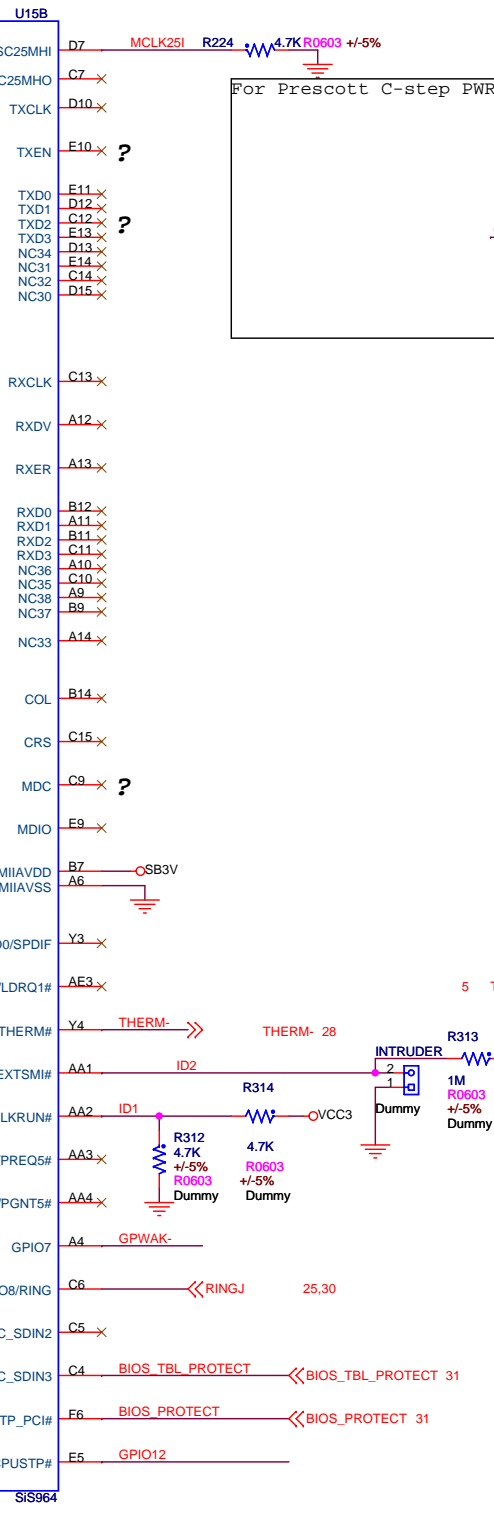
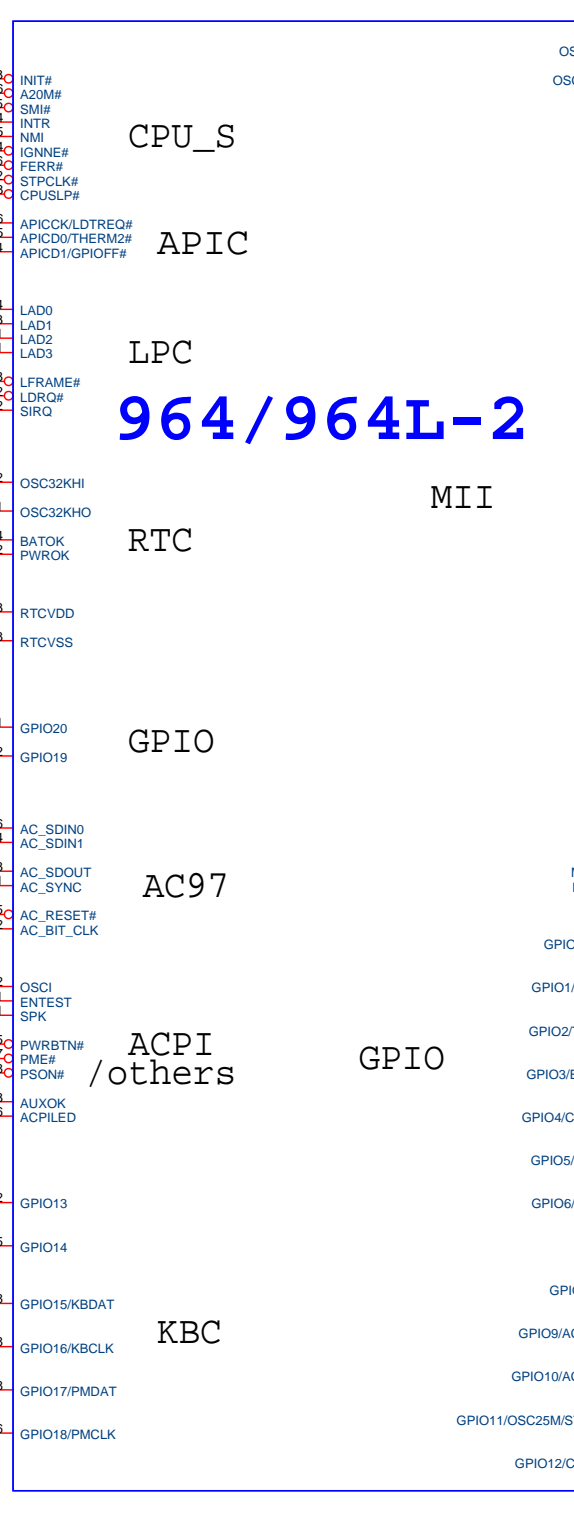
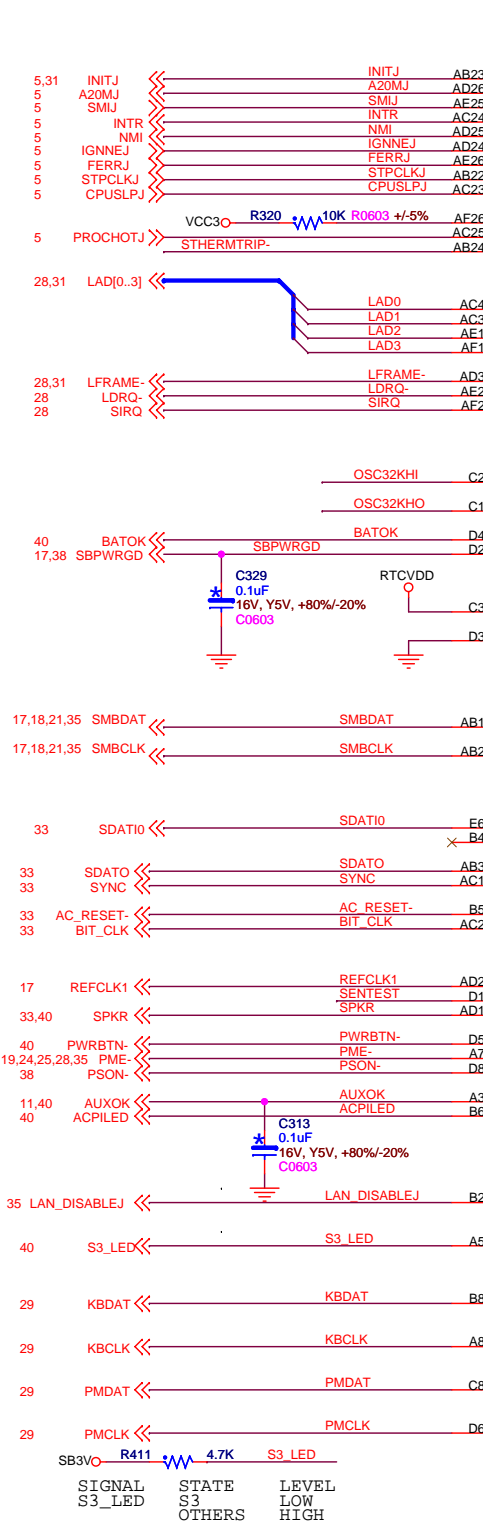


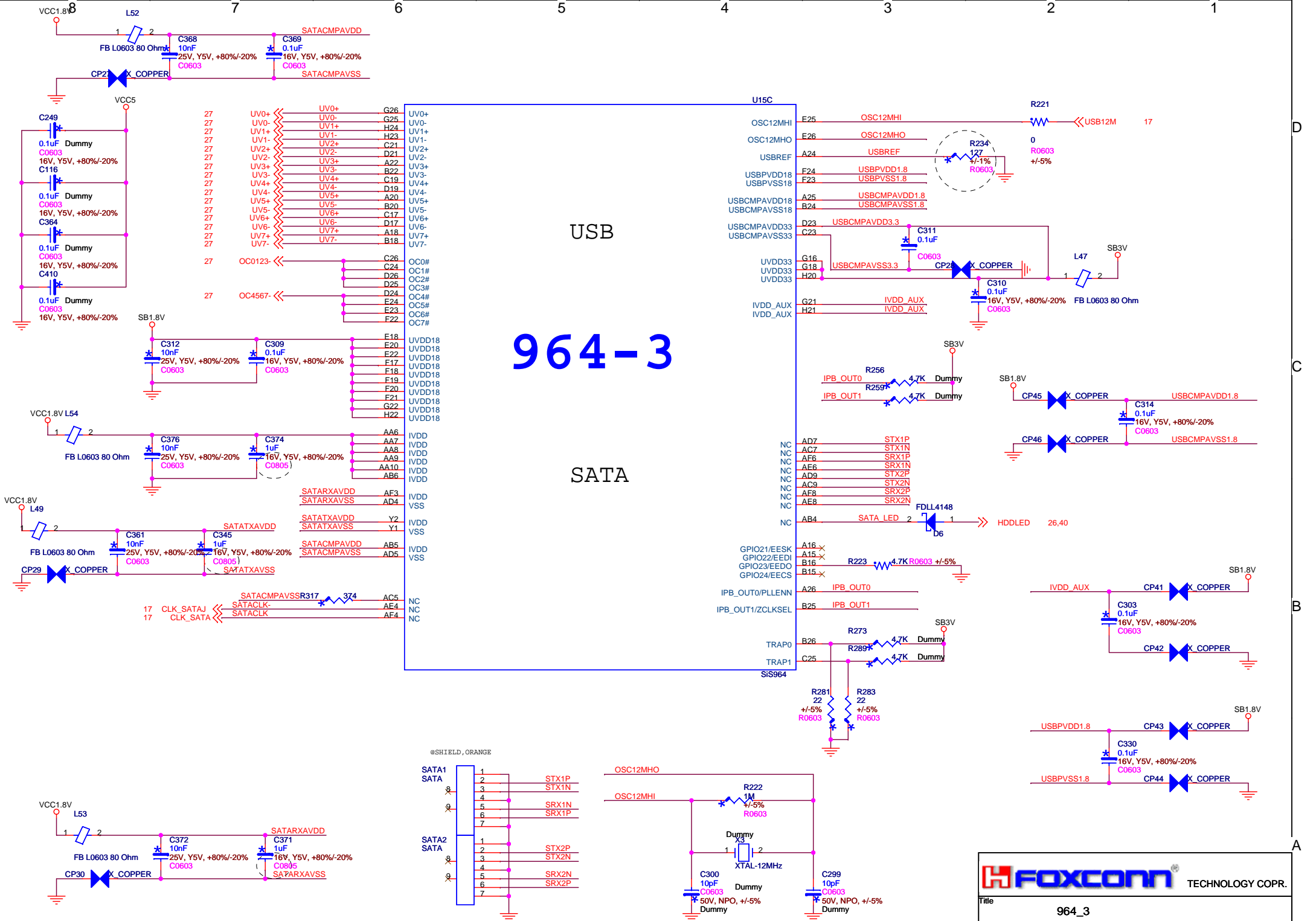


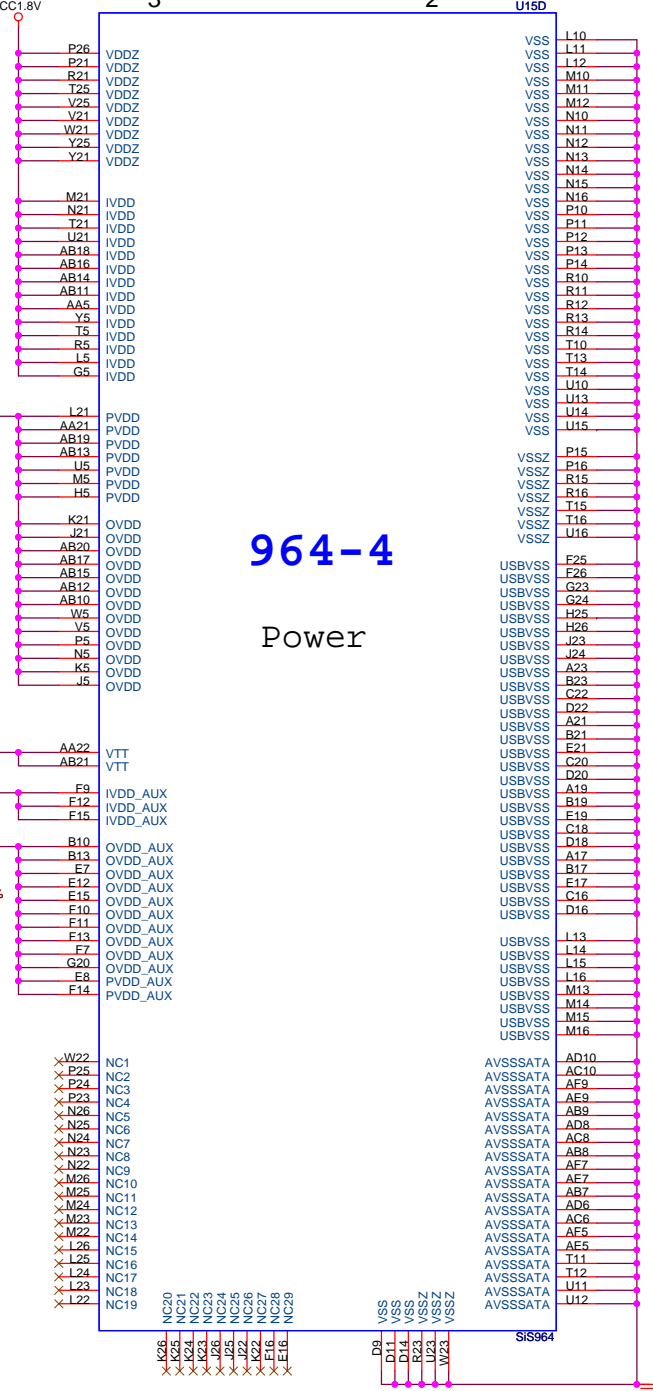
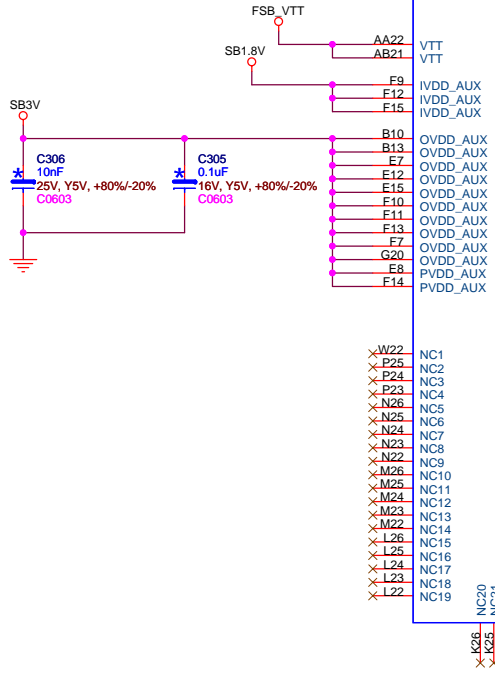
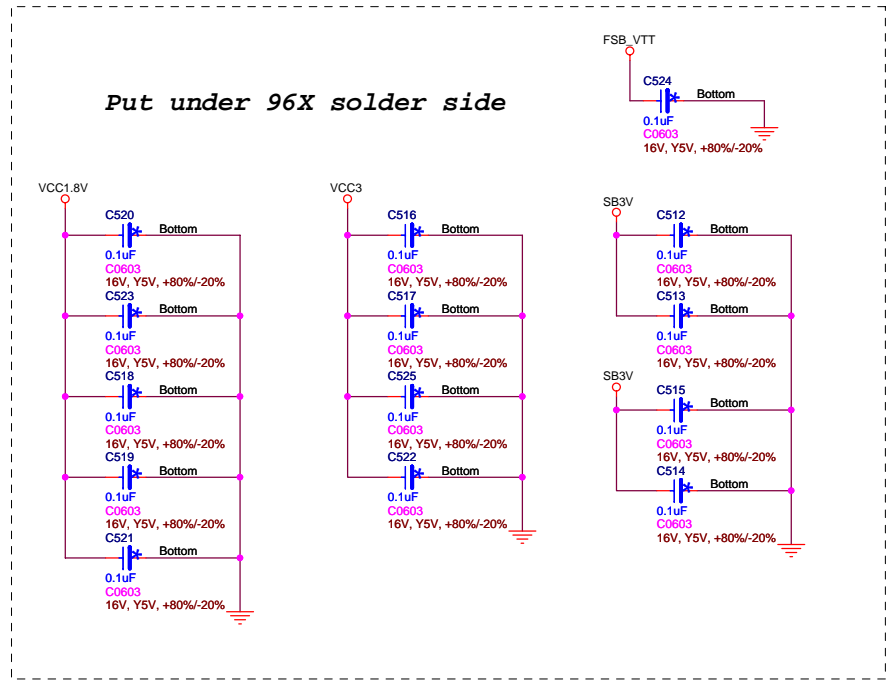
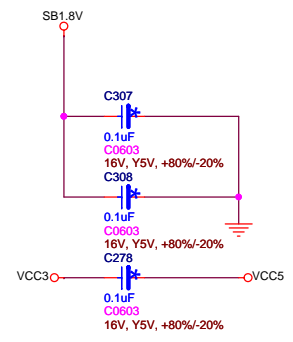
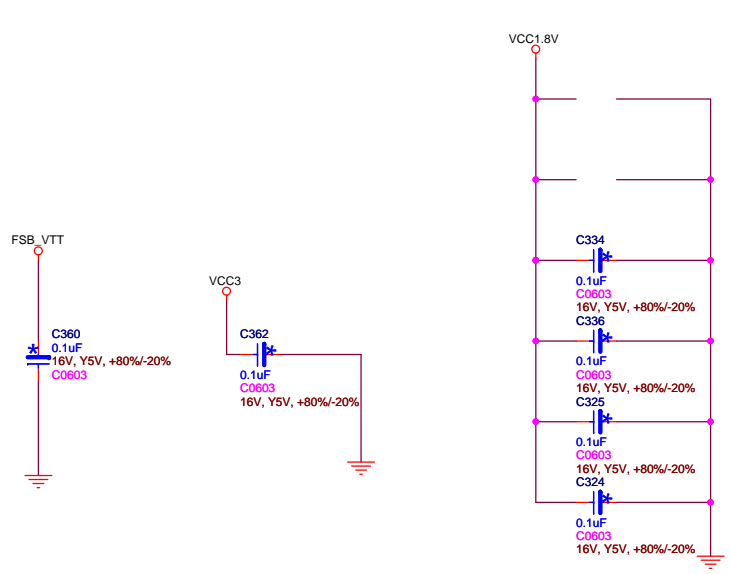
Power



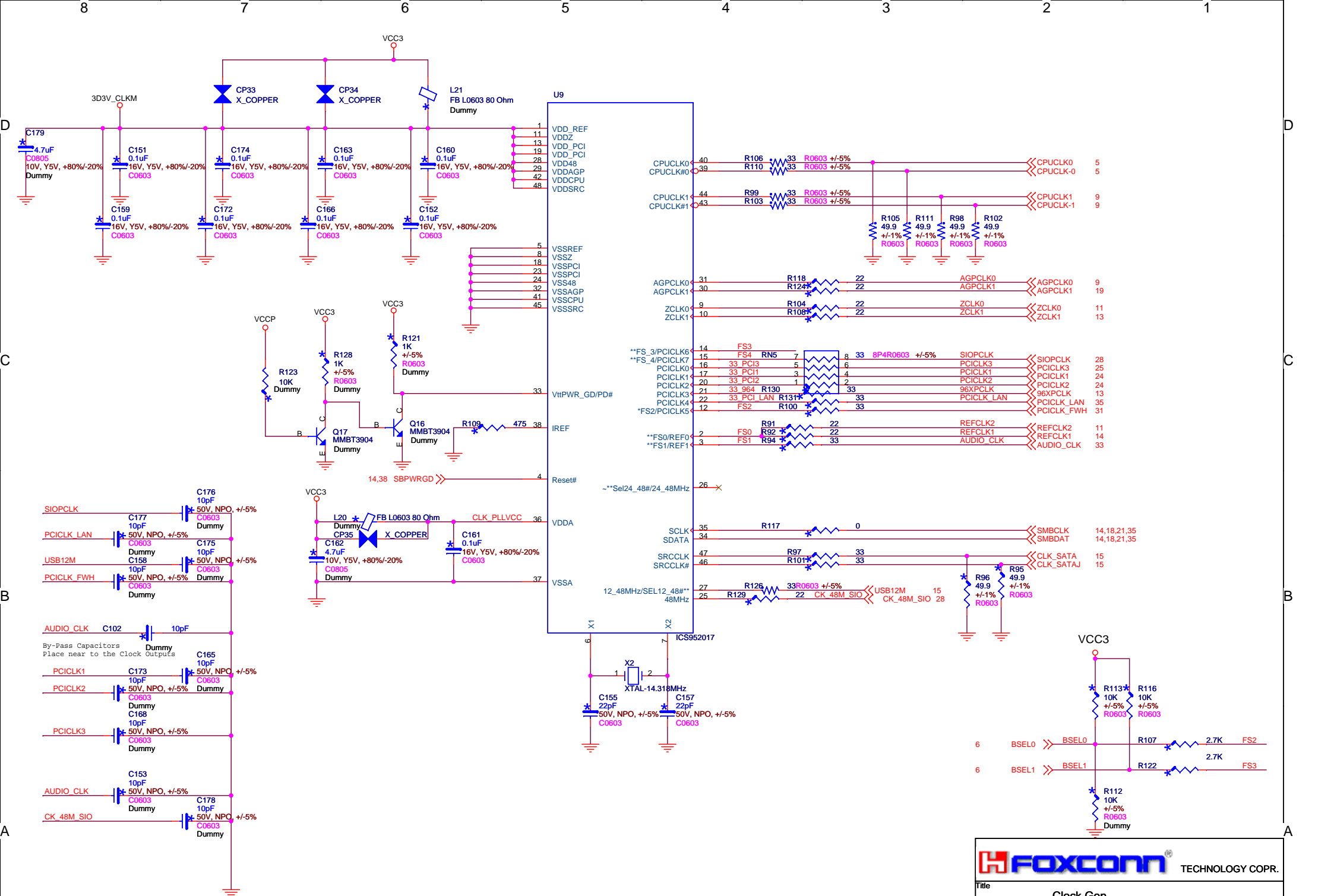


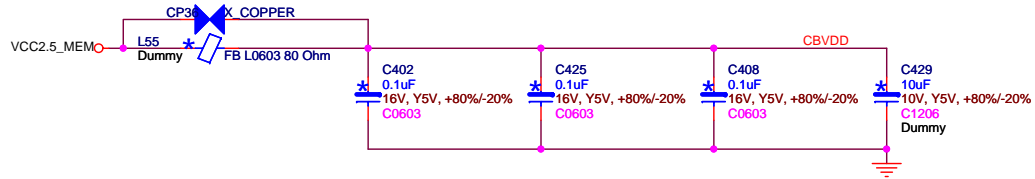




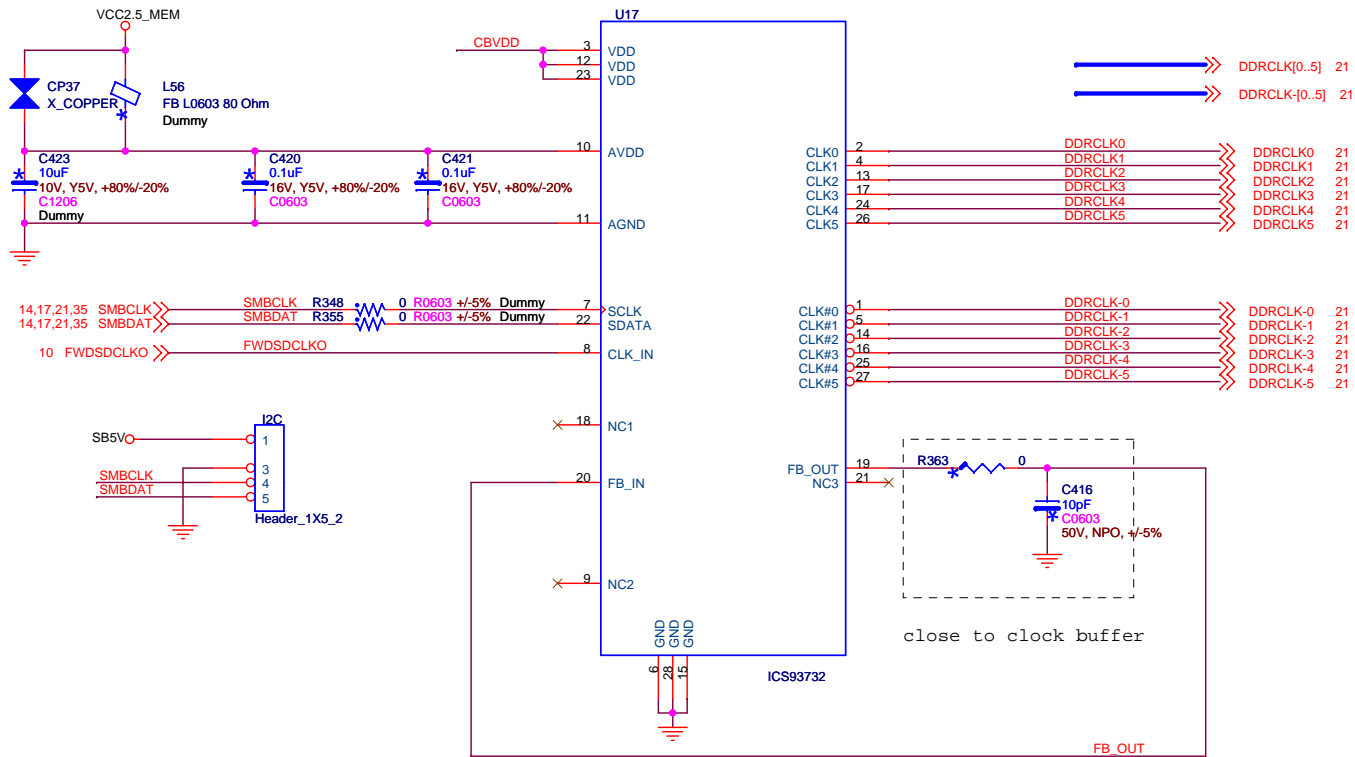


964-4
Power



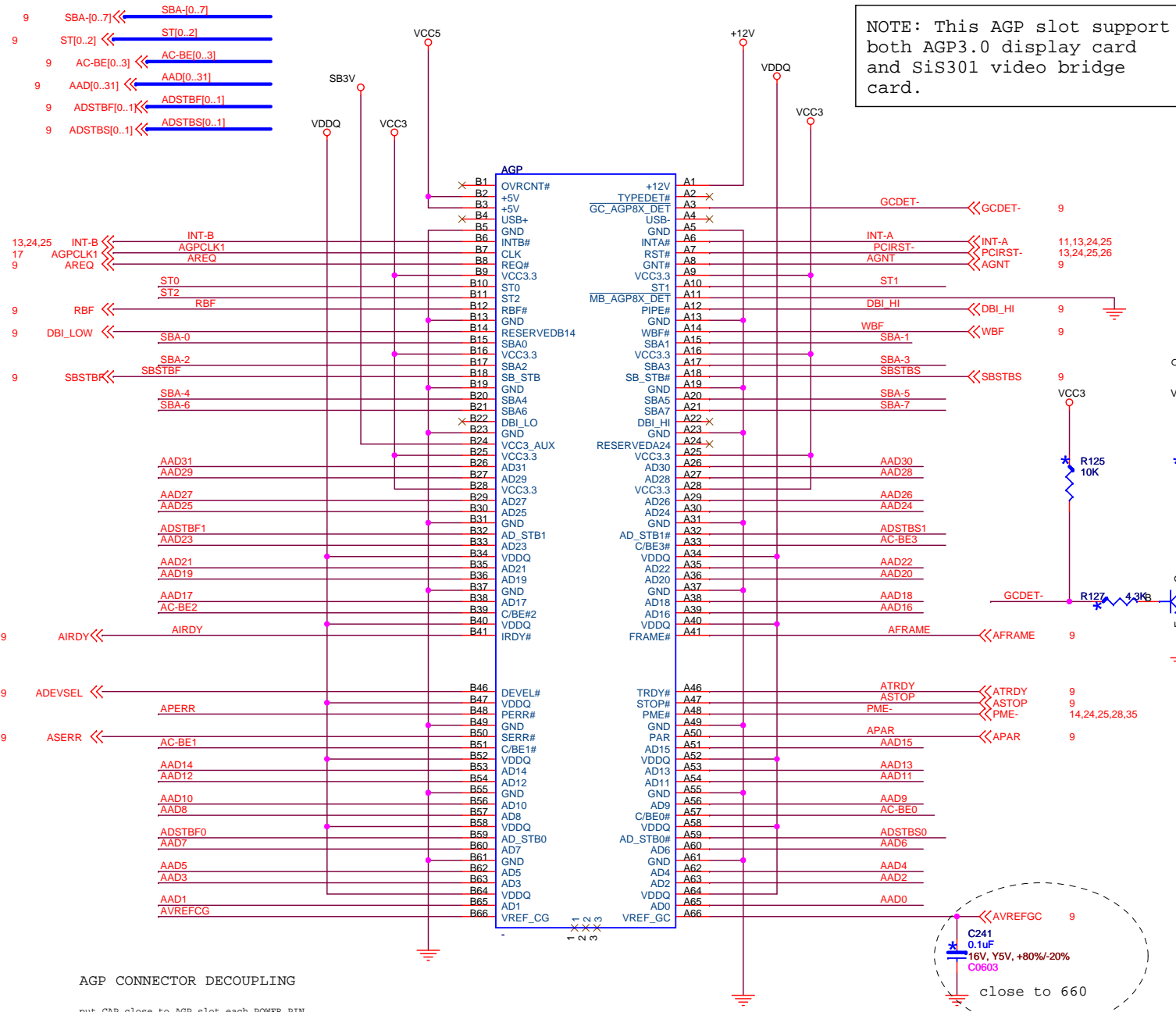


Clock Buffer (DDR)

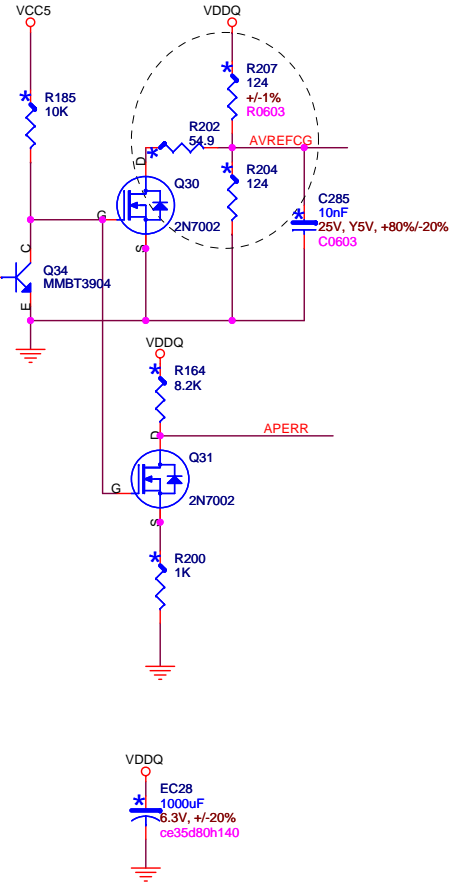
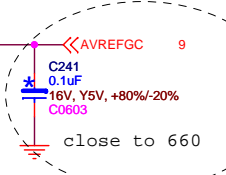


NOTE: This AGP slot support both AGP3.0 display card and SiS301 video bridge card.

GCDET- on card	GCDET-	AVREFCG	APERR
GND	0V	0.35V	0V
OPEN	1.47V	0.75V	1.5V

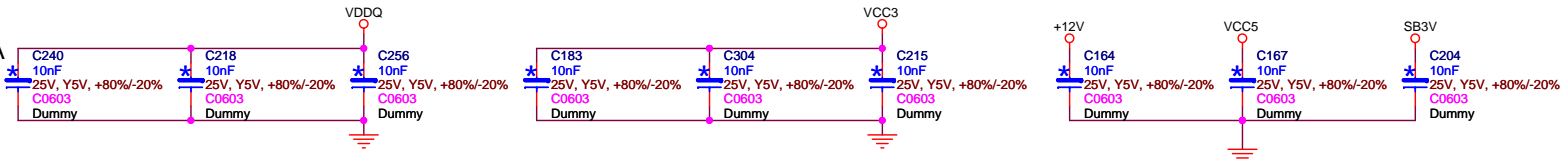


close to AGP SLOT



AGP CONNECTOR DECOUPLING

put CAP close to AGP slot each POWER PIN



FOXCONN TECHNOLOGY COPR.

Title: AGP

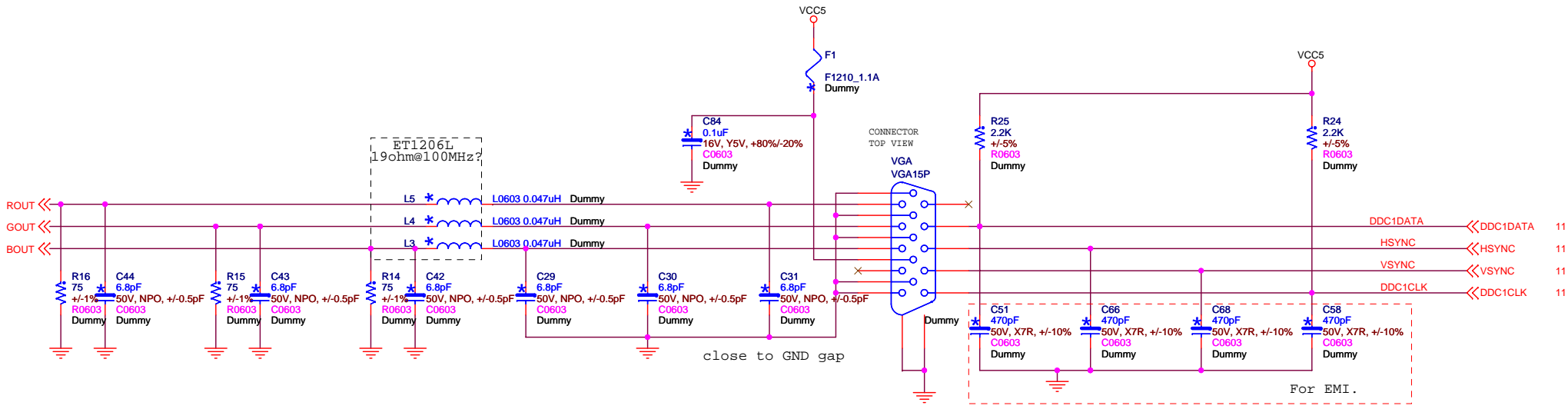
Document Number: 648M06

Date: Wednesday, March 16, 2005

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Rev B

VGA CONNECTOR



10,23 MD[0..63] << MD[0..63]
 10,23 MA[0..14] << MA[0..14]
 10,23 DQM[0..7] << DQM[0..7]
 10,23 DQS[0..7] << DQS[0..7]

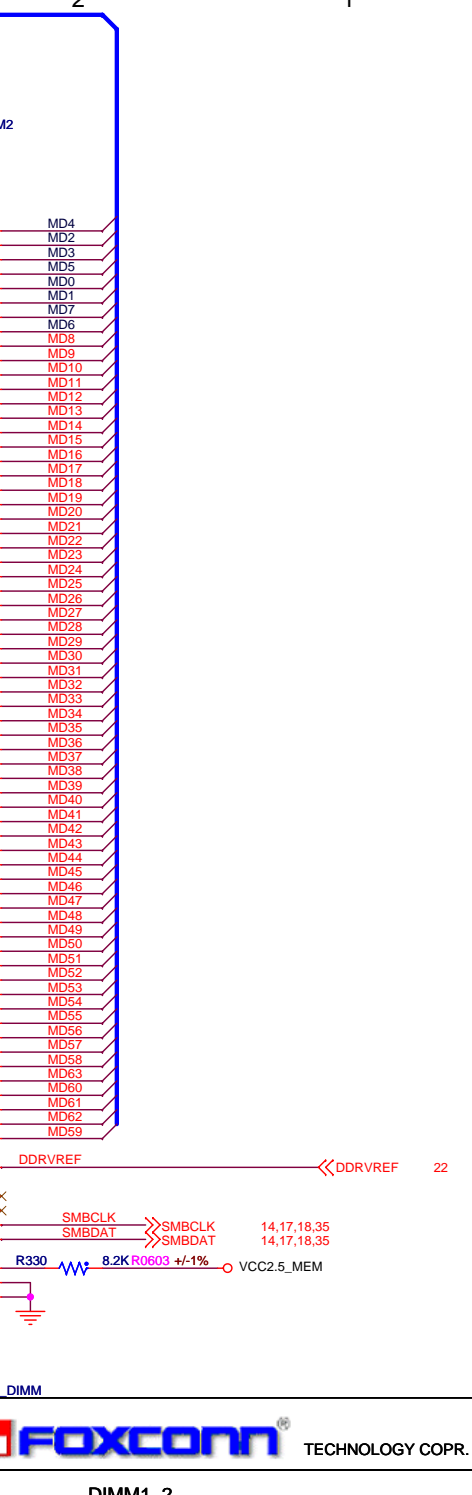
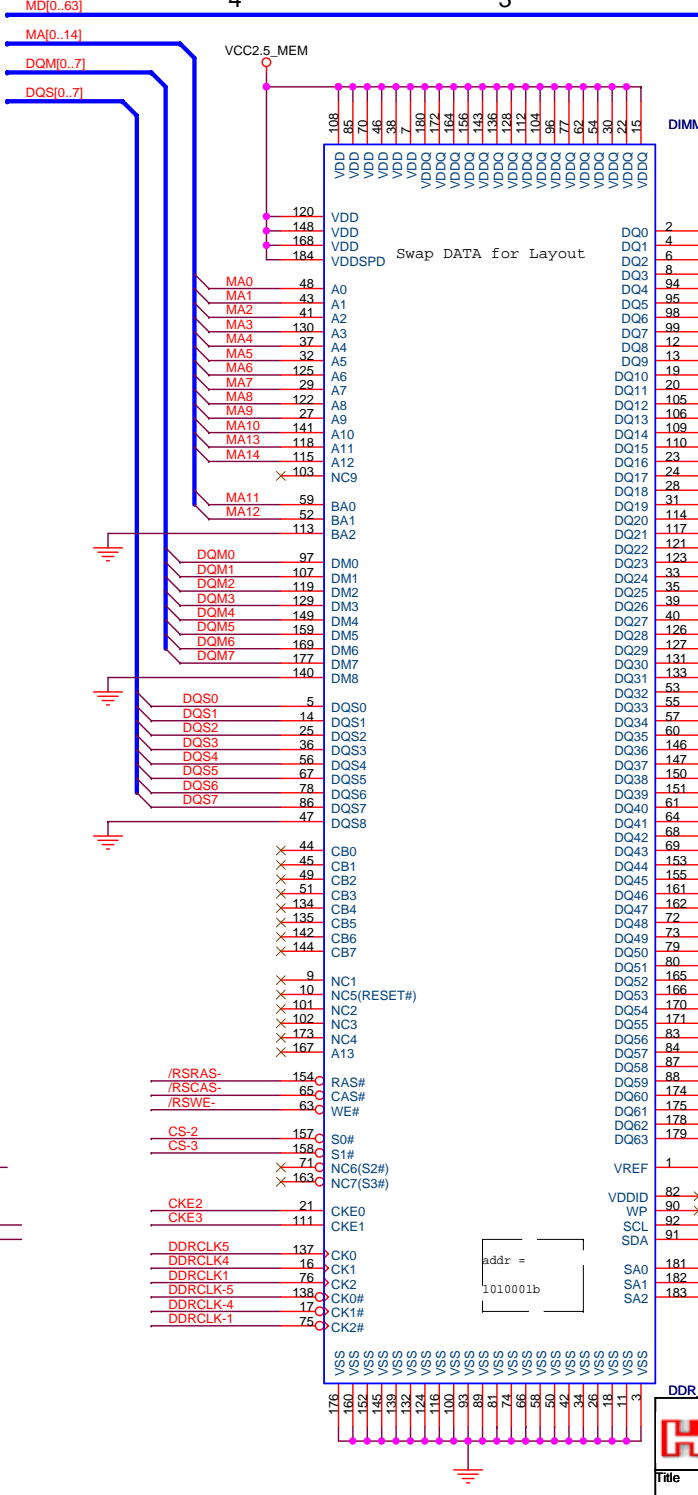
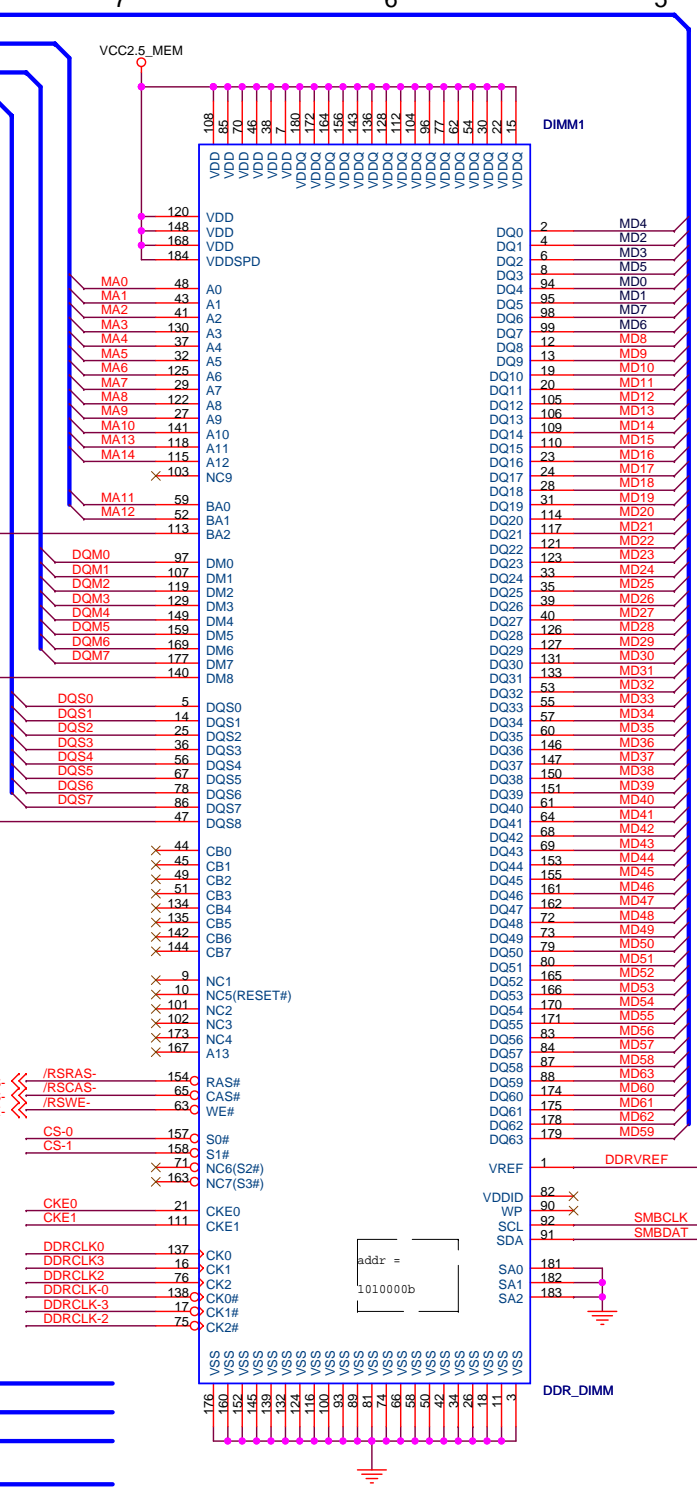
NOTE:
 VDDID IS A TRAP ON THE DIMM
 MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD1=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

10,23 CS-[0..3] << CS-[0..3]
 10 CKE[0..3] << CKE[0..3]
 18 DDRCLK[0..5] << DDRCLK[0..5]
 18 DDRCLK[0..5] << DDRCLK[0..5]

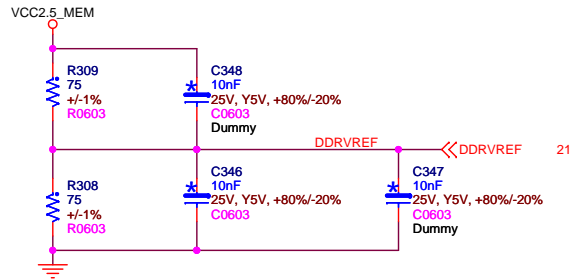


Title DIMM1, 2

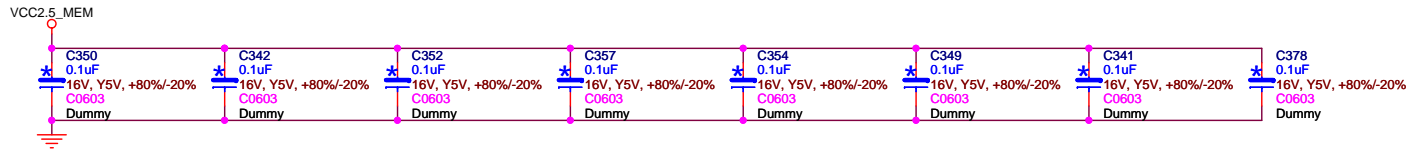
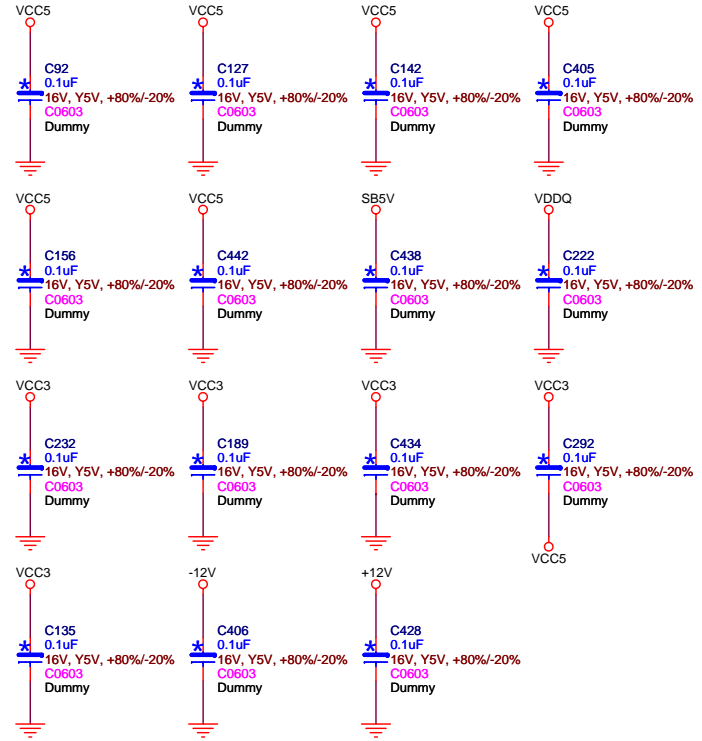
Document Number 648M06

Date: Wednesday, March 16, 2005 Sheet 21 of 41

DDRVREF GEN. & DECOUPLING



EMI



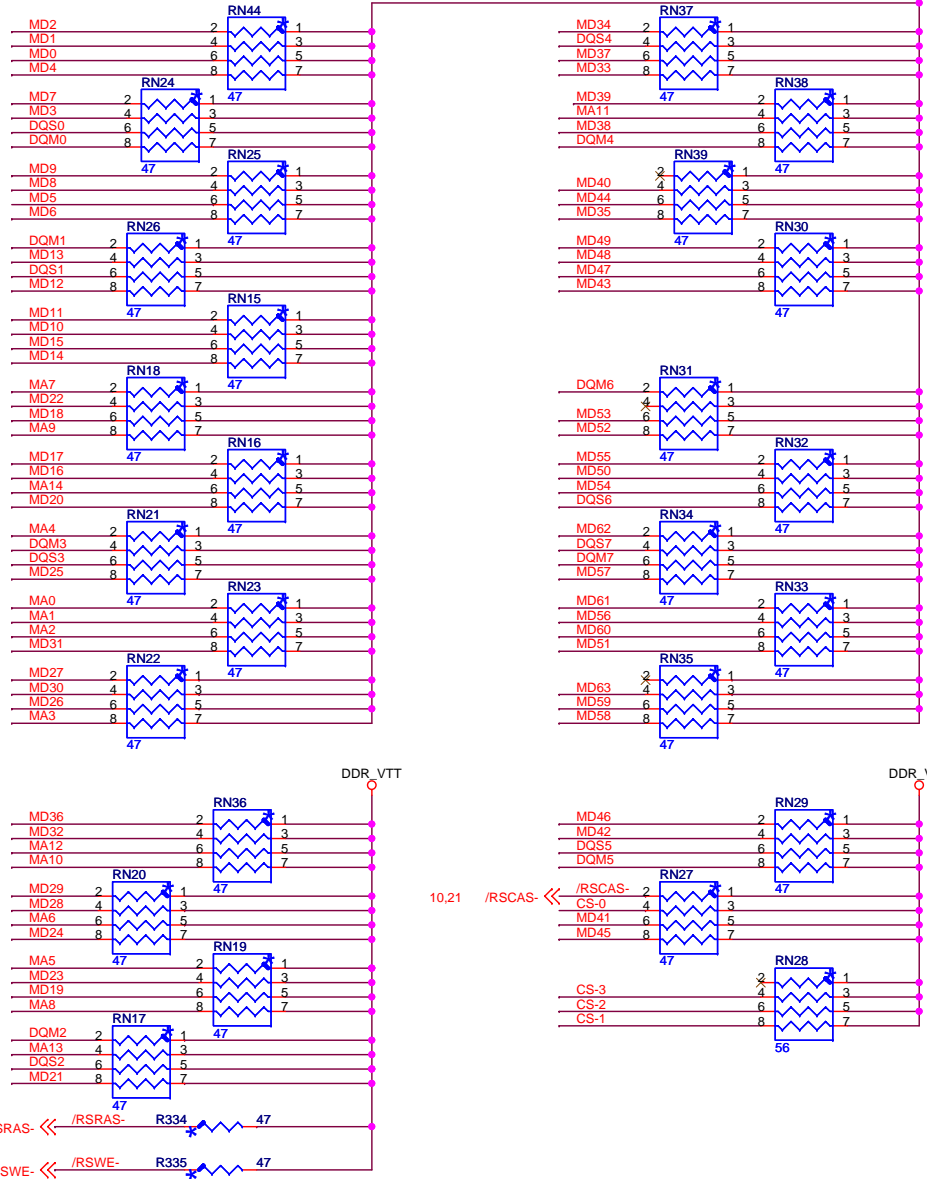
SSTL-2 Termination Resistors

MD[0..63]	10,21
DQM[0..7]	10,21
DQS[0..7]	10,21
MA[0..14]	10,21
CS-[0..3]	10,21

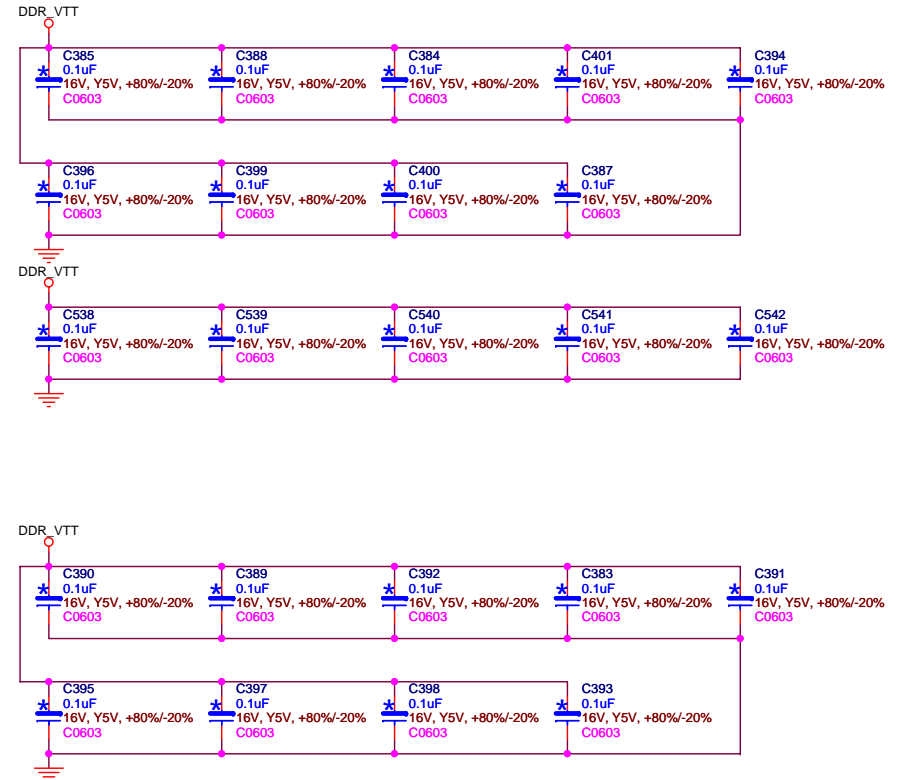
	SDR	R _S	bDDR	R _S	R _{tt}
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	10	33
MA/Control	LV-CMOS	10	SSTL-2	0	33
CS	LV-CMOS	0	SSTL-2	0	47
VKE	DD 3.3V		DD 2.5V		

Termination change 56ohm

DDR_VTT



DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs



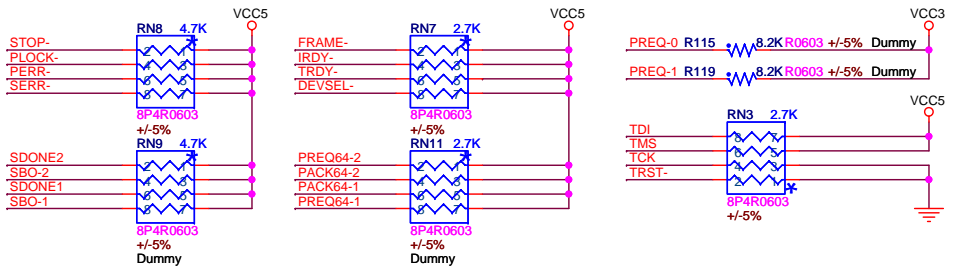
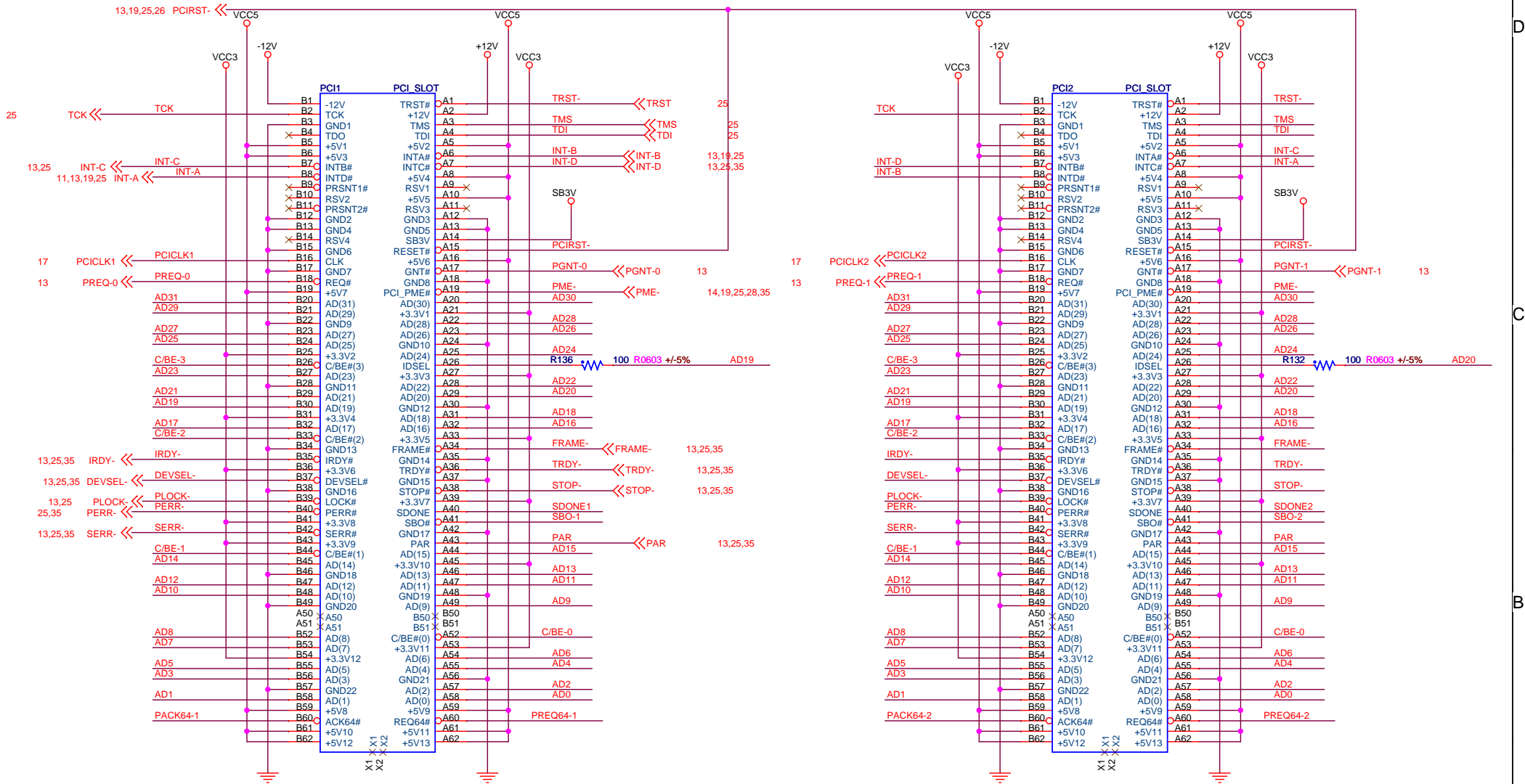
10,21	/RSRAS- << /RSRAS-	R334	47
10,21	/RSWE- << /RSWE-	R335	47

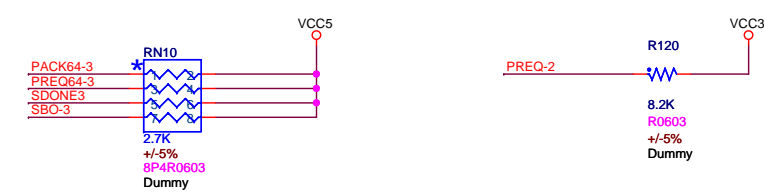
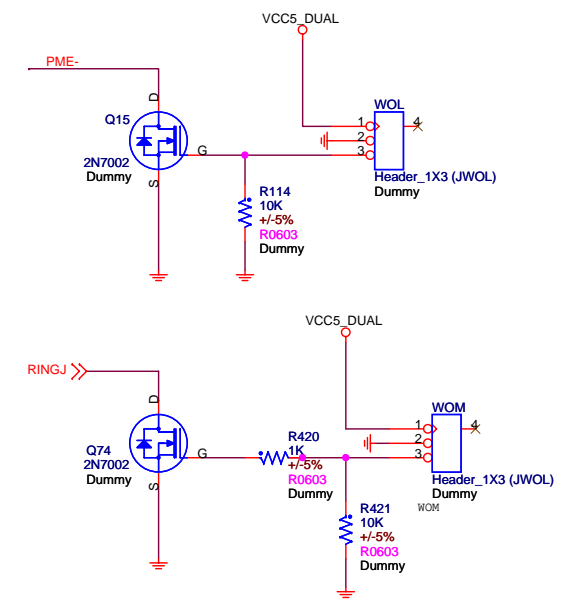
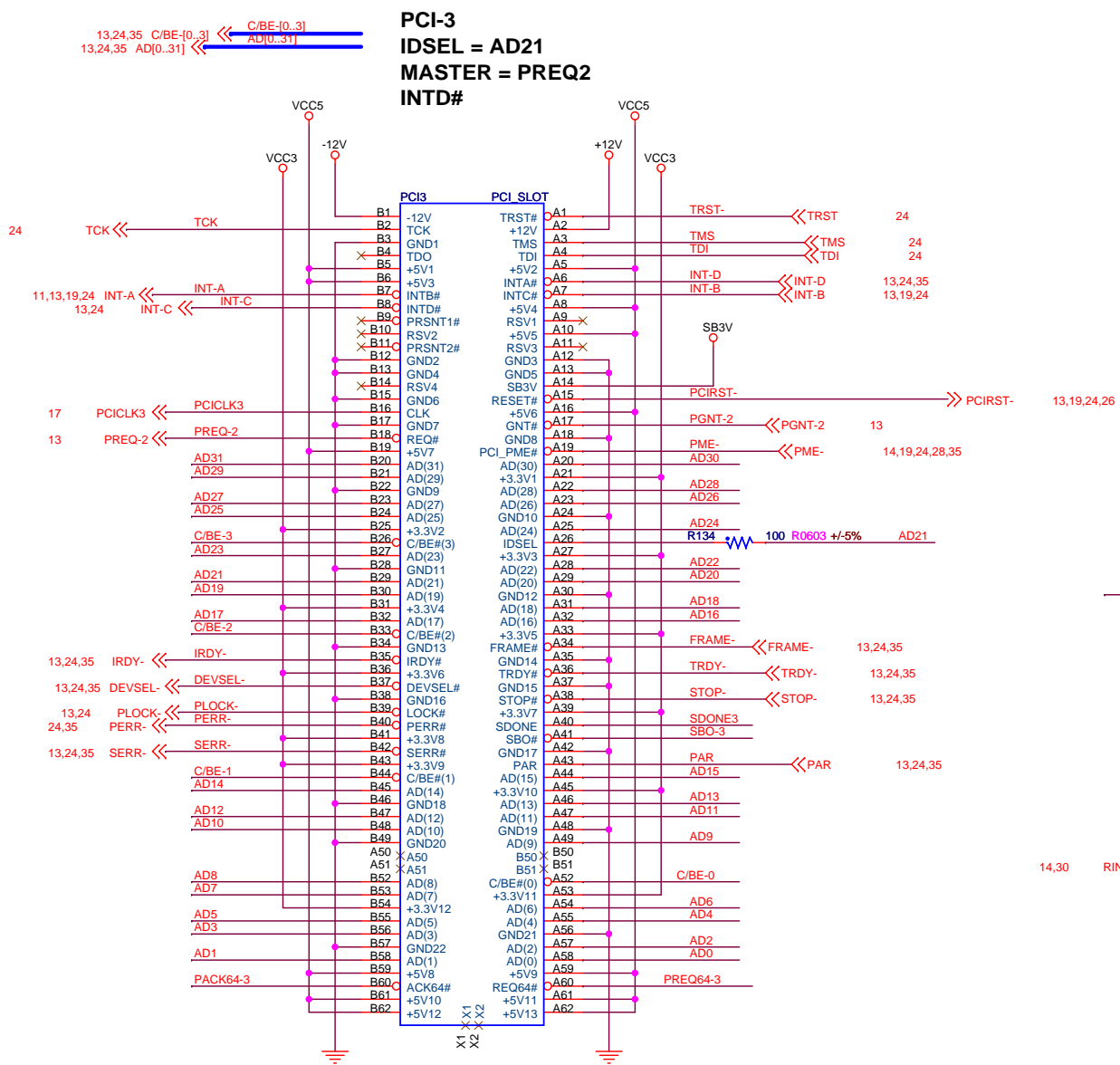


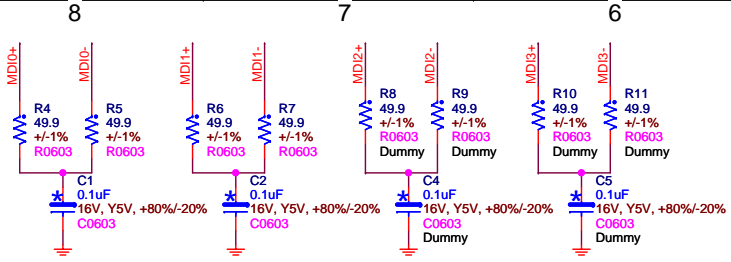
PCI-1
IDSEL = AD19
MASTER = PREQ0
INTB#

PCI Slot 1 & 2

PCI-2
IDSEL = AD20
MASTER = PREQ1
INTC#

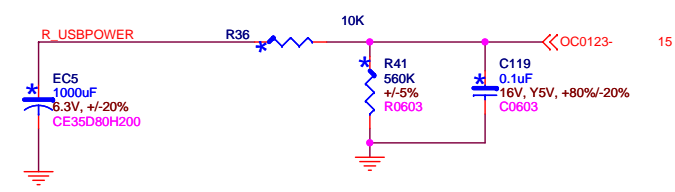
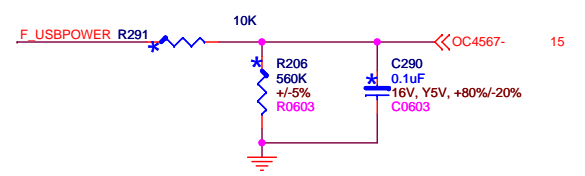
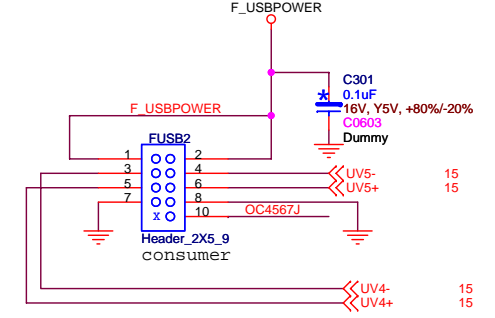
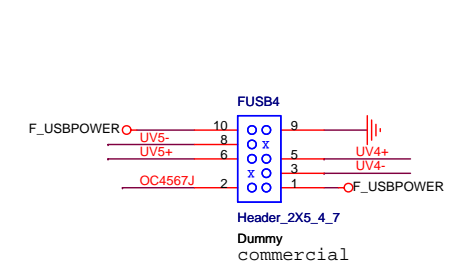
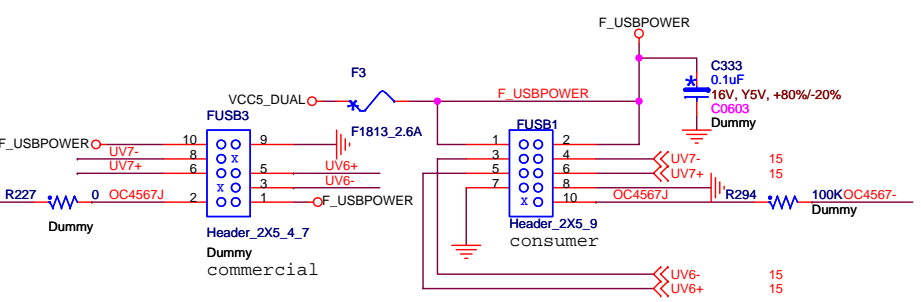
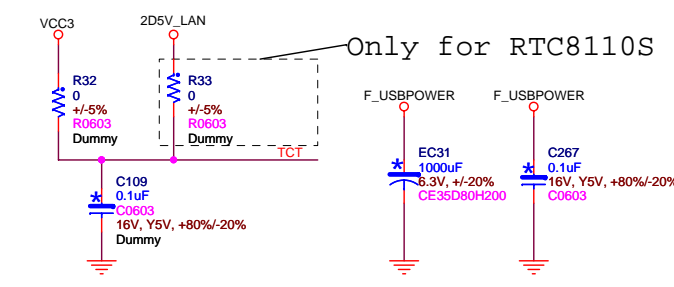
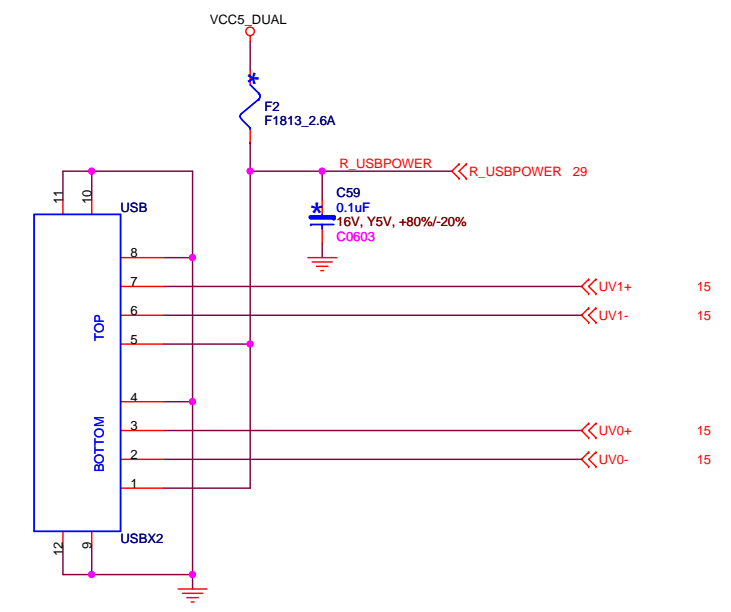
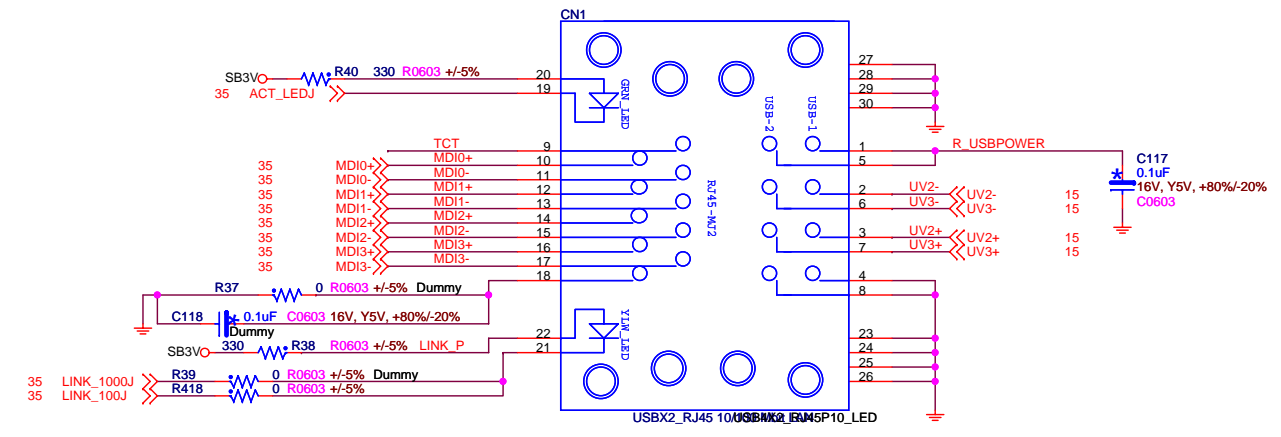


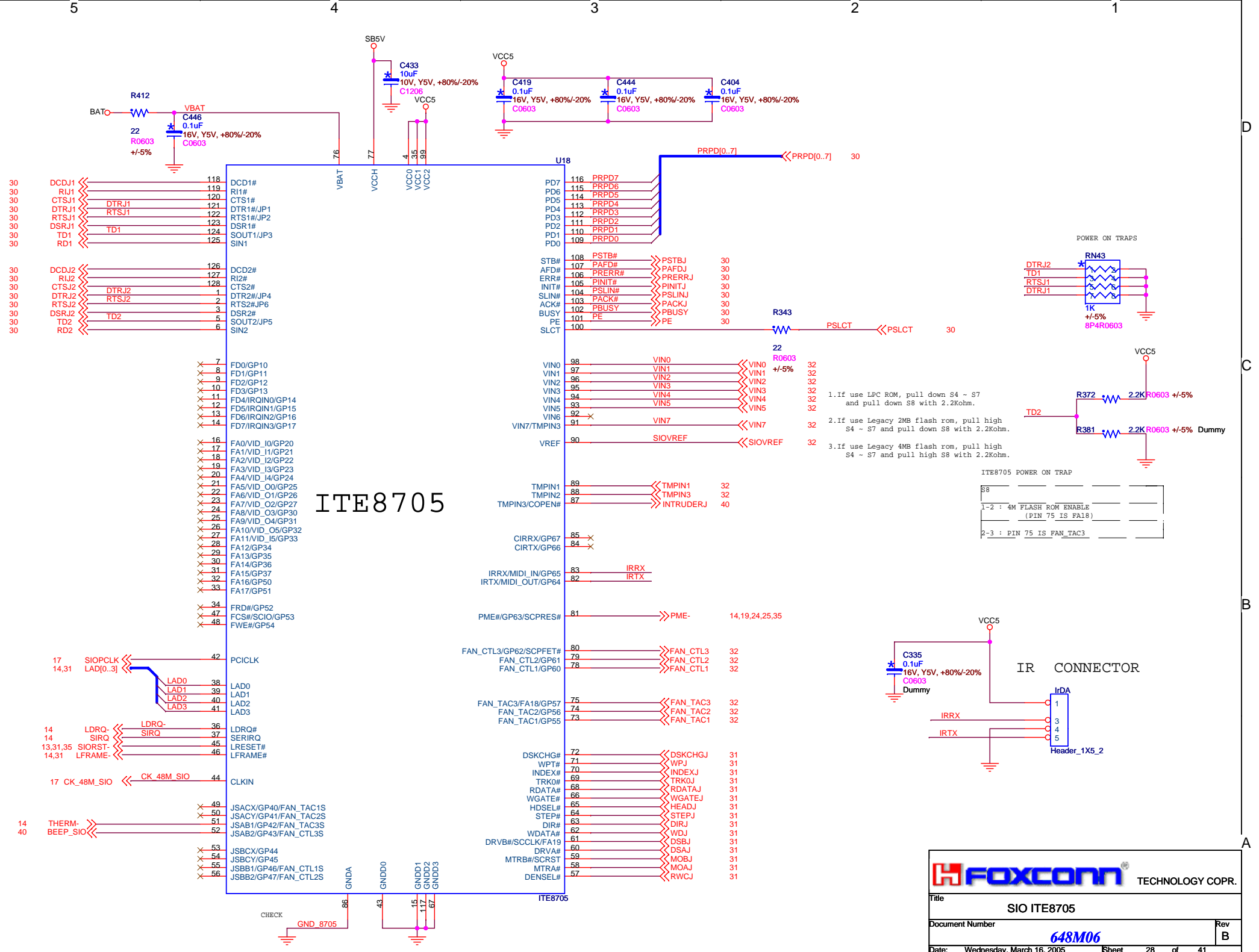




1Gbit Green = on , Yellow = off
 100Mbit Green = off , Yellow = on
 10Mbit Green = off , Yellow = off

G-bit = JFM31U1A-01UBW





ITE8705

D

D

C

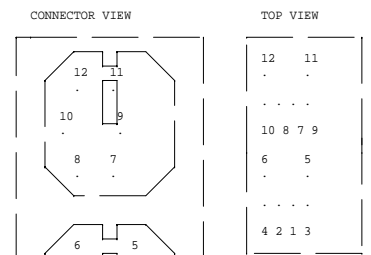
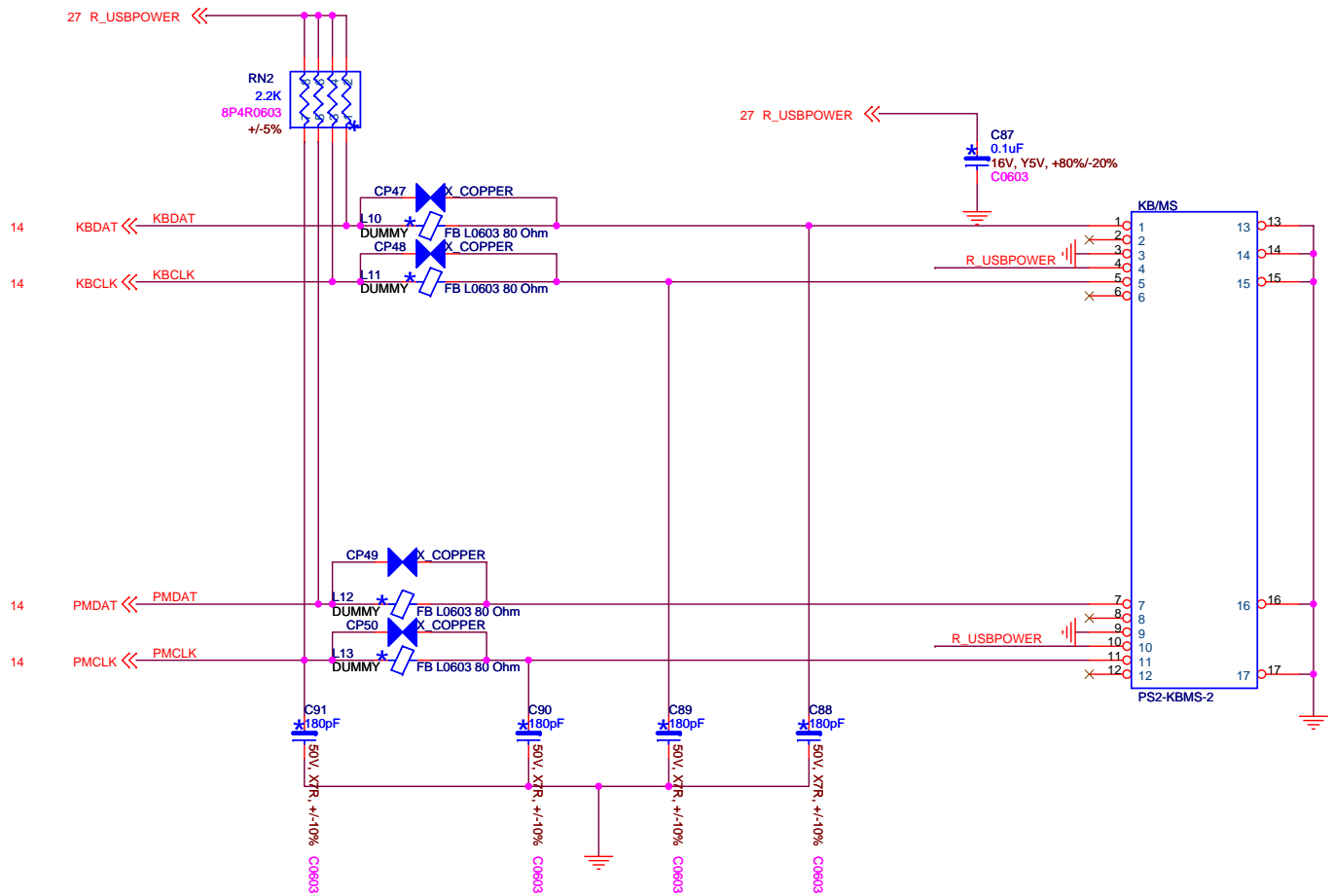
C

B

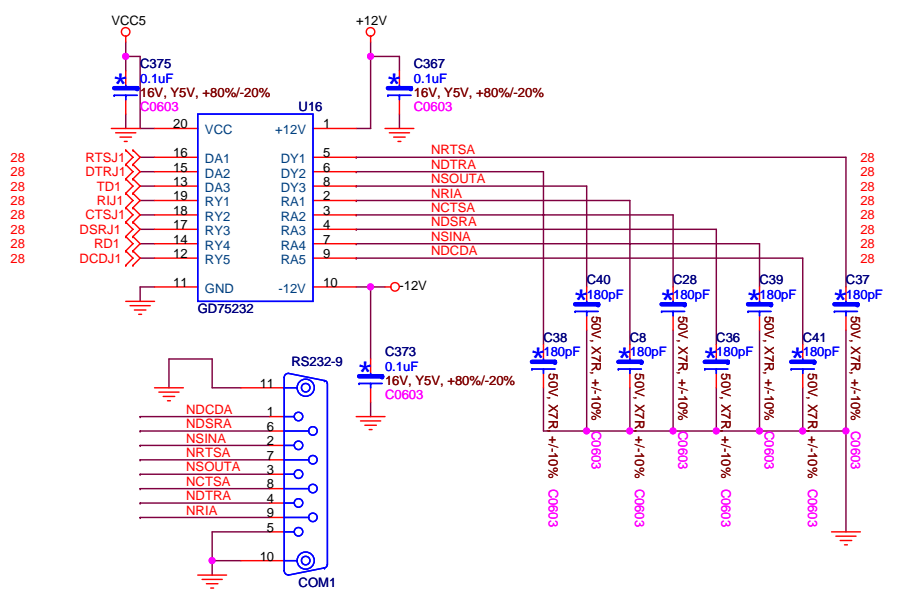
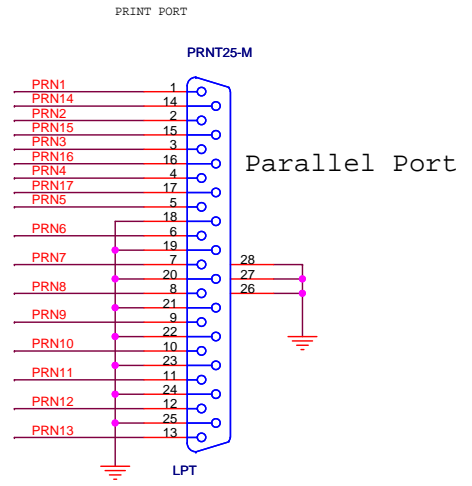
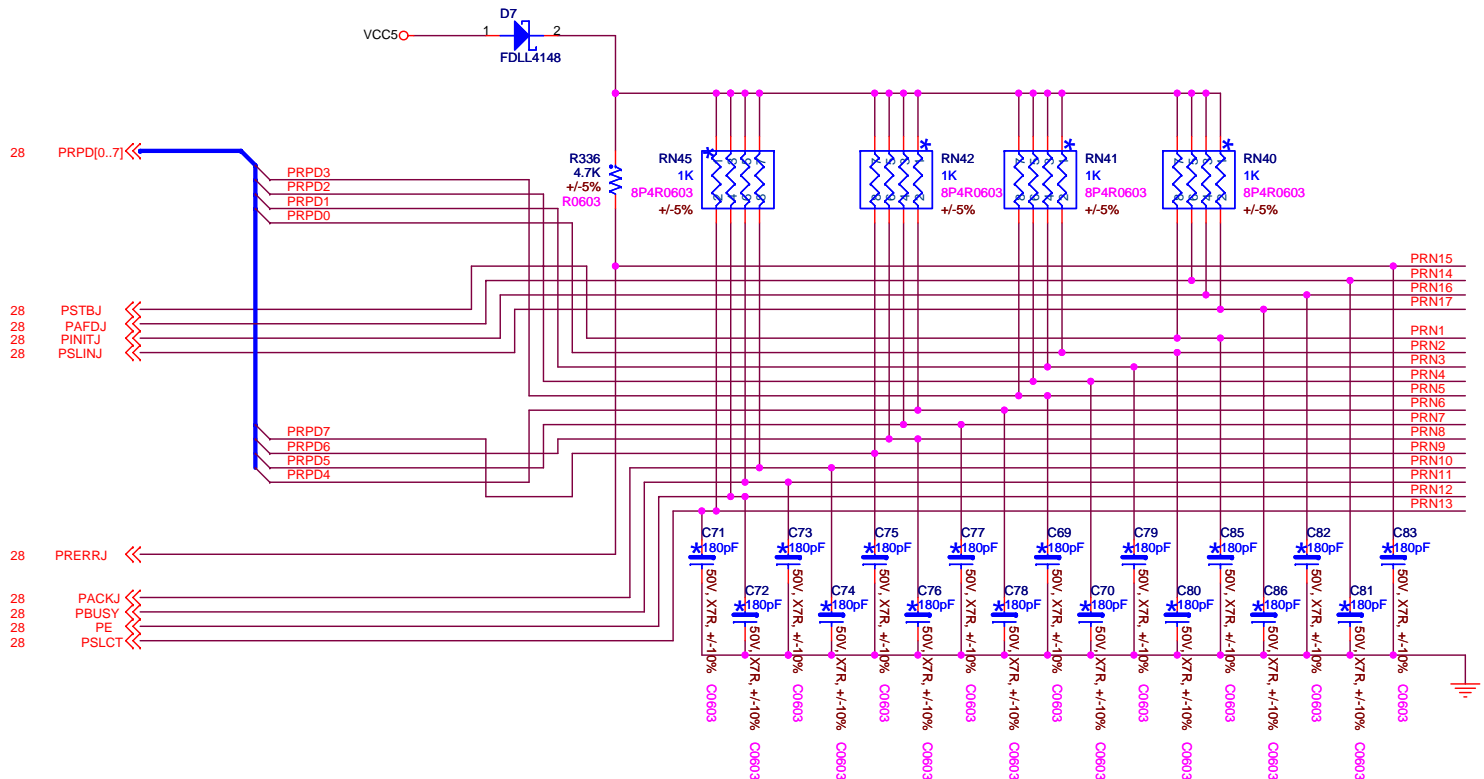
B

A

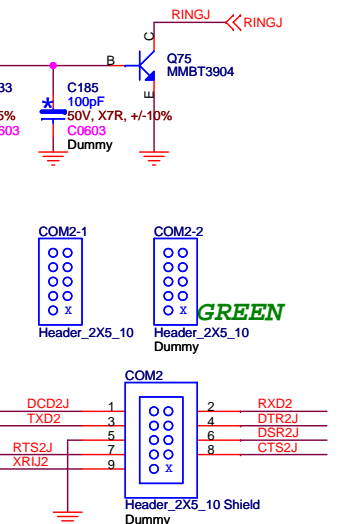
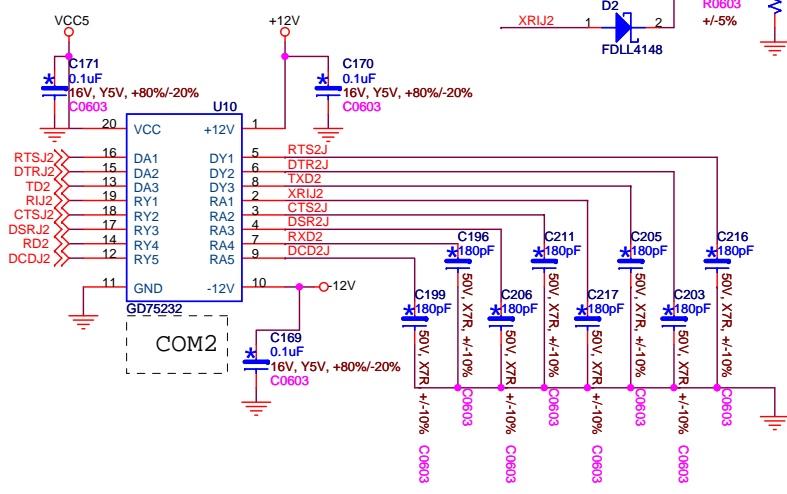
A

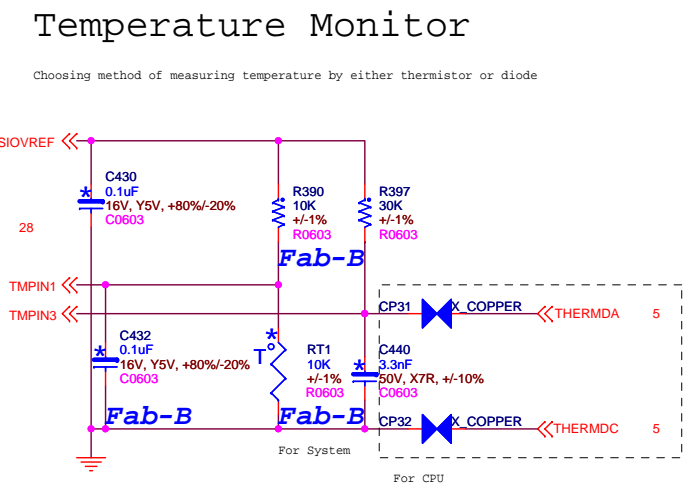
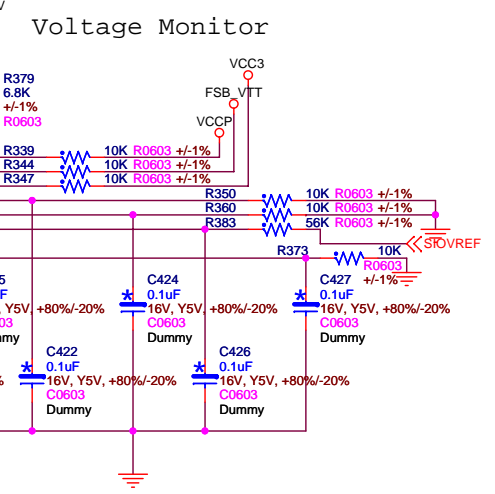
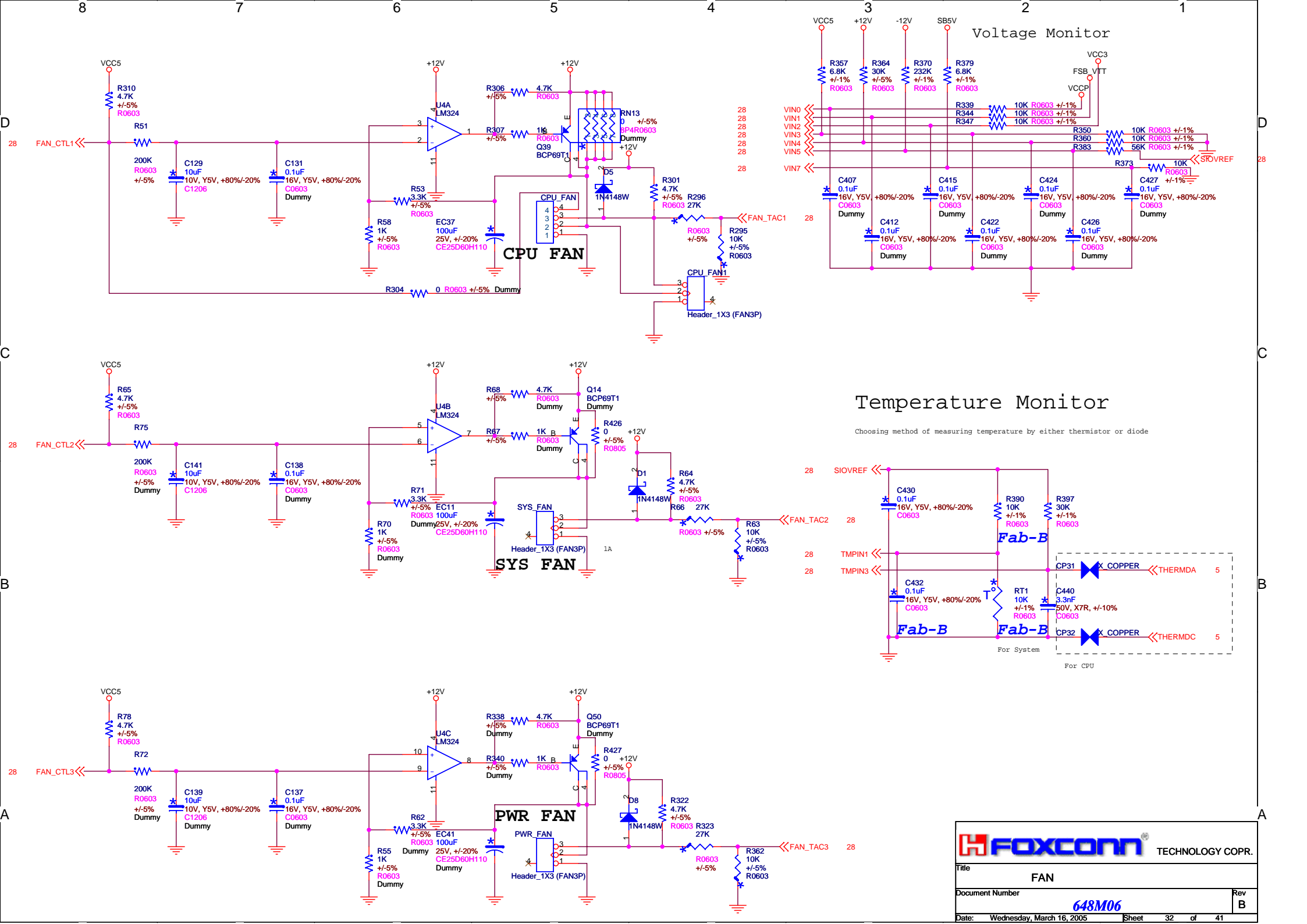


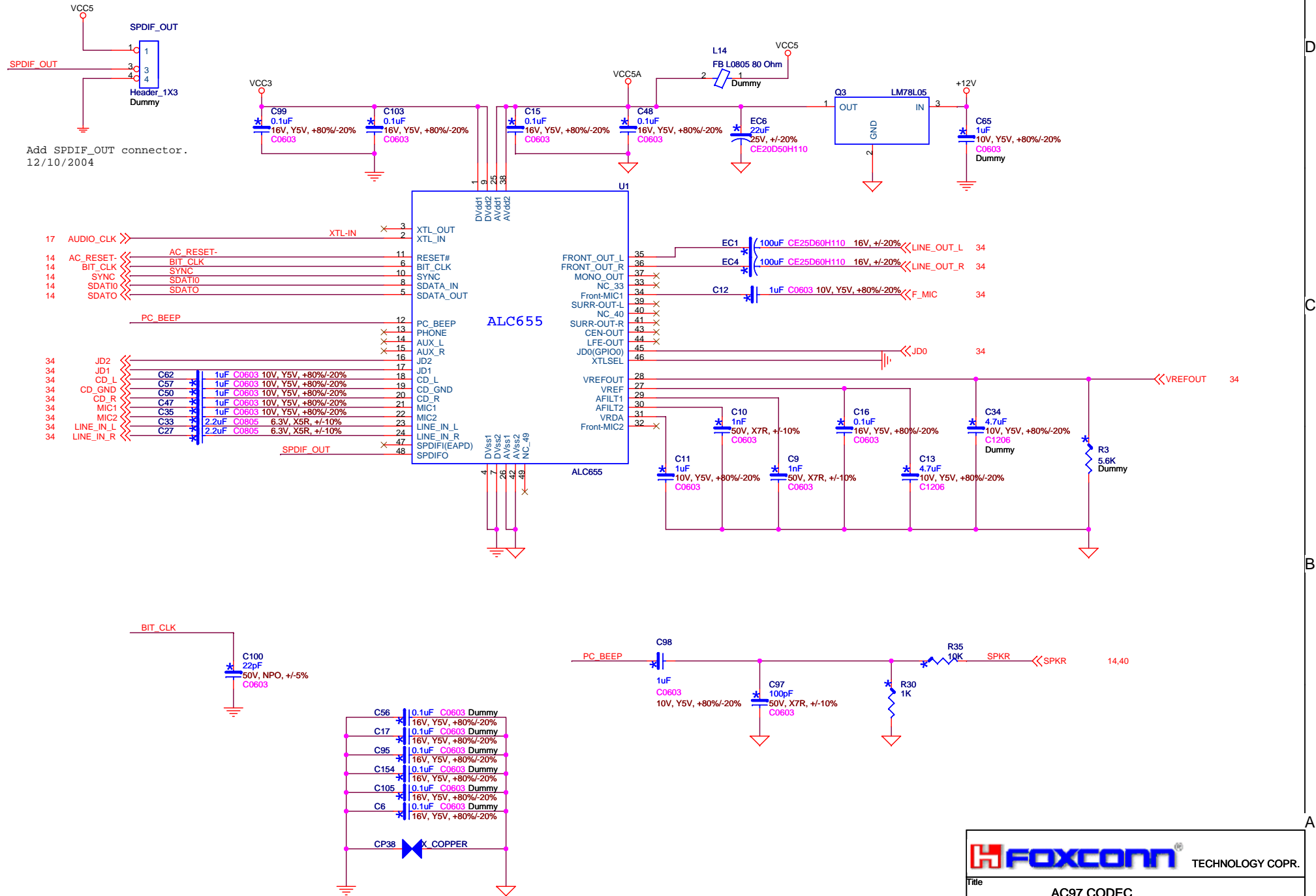
NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.



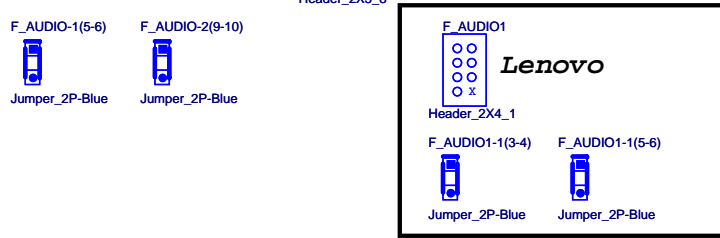
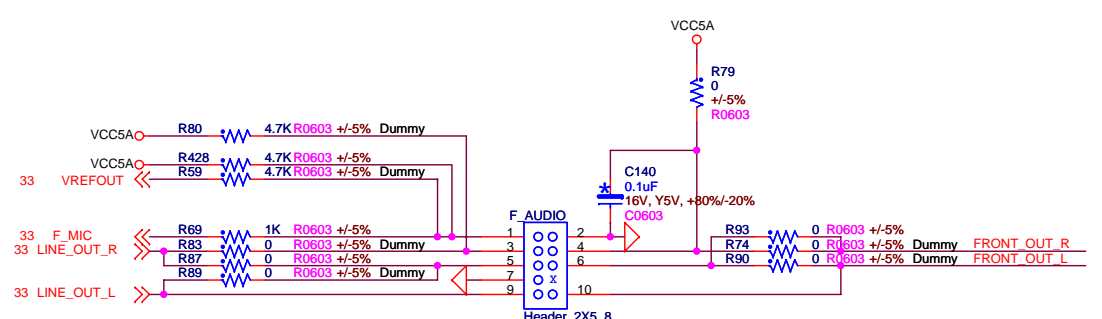
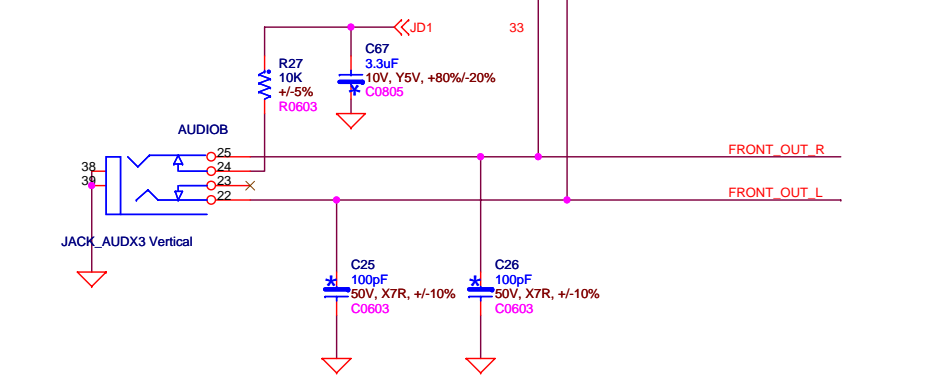
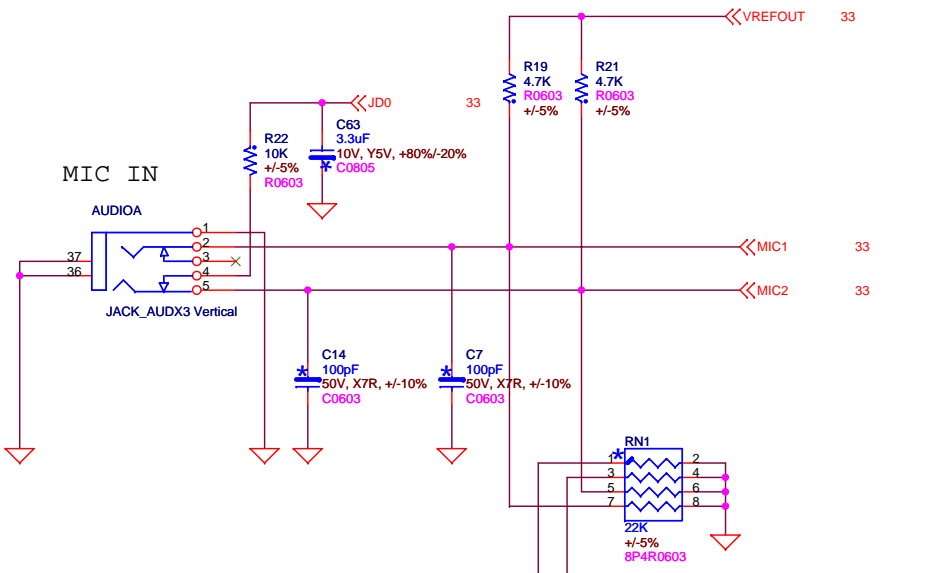
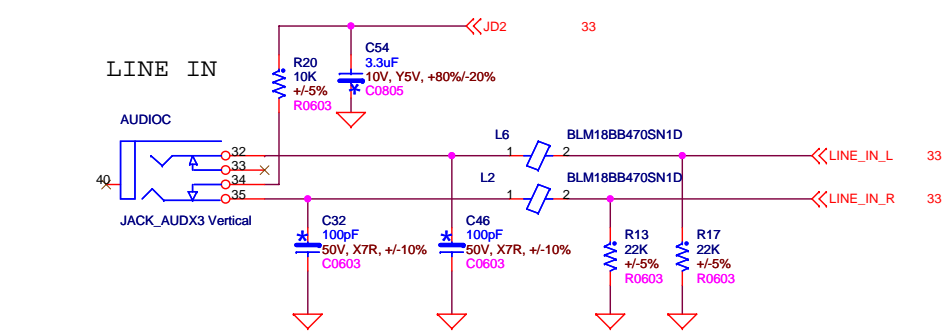
Serial Port








Add SPDIF_OUT connector.
12/10/2004



27 LINK_1000J >>
 27 LINK_100J >>
 27 ACT_LEDJ >>

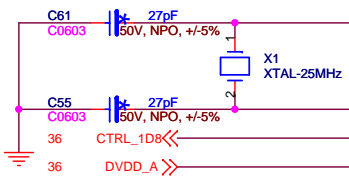
PCI-3
IDSEL = AD24
MASTER = PREQ3
INTD#

 **USE 6/8/6**
WIDTH/SPACE/WIDTH FOR
LAN

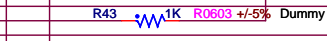
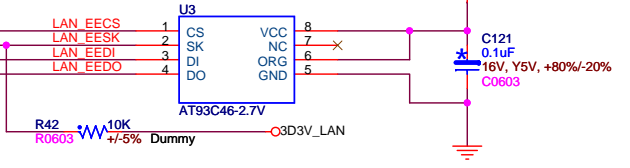
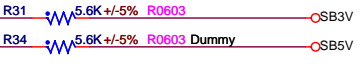
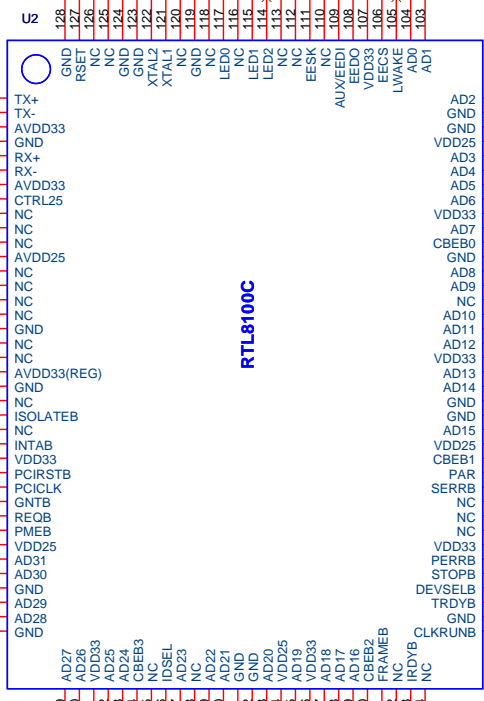
27 MDI0+ >>
 27 MDI0- >>
 27 MDI1+ >>
 27 MDI1- >>
 36 CTRL_2D5 <<
 AVDDH ○
 36 V_12P >>
 27 MDI2+ >>
 27 MDI2- >>
 27 MDI3+ >>
 27 MDI3- >>
 1D8V_LAN ○
 13,24,25 INT-D >>
 3D3V_LAN ○
 13,28,31 SIORST- >>
 17 PCI_CLK LAN >>
 13 PGNT-3 >>
 13 PREQ-3 >>
 14,19,24,25,28 PME- >>
 1D8V_LAN ○

13,24,25 ADJ[31..0] <<

13,24,25 C/BE-3 <<



LAN DISABLE(By disabling LAN clock)

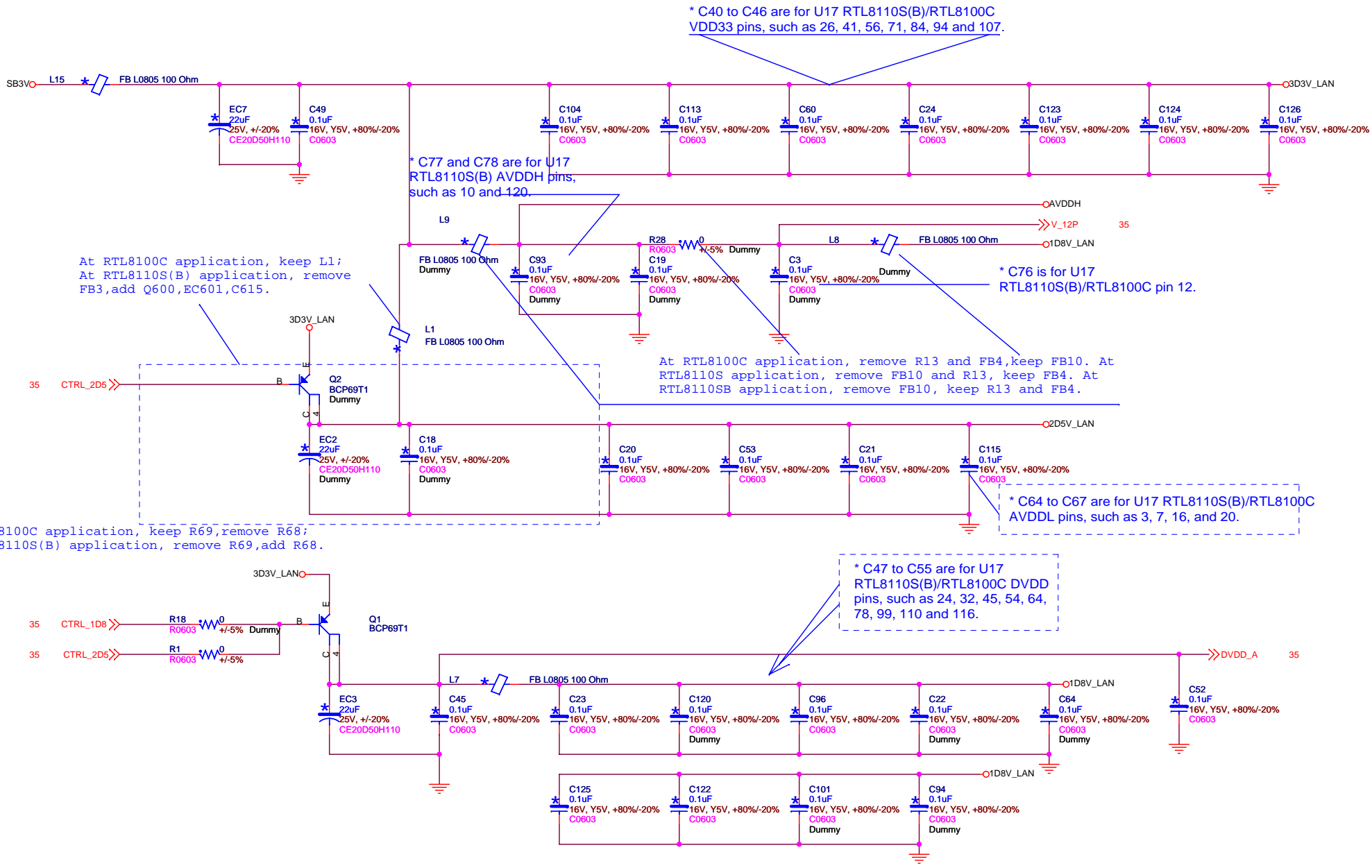


FOXCONN TECHNOLOGY COPR.

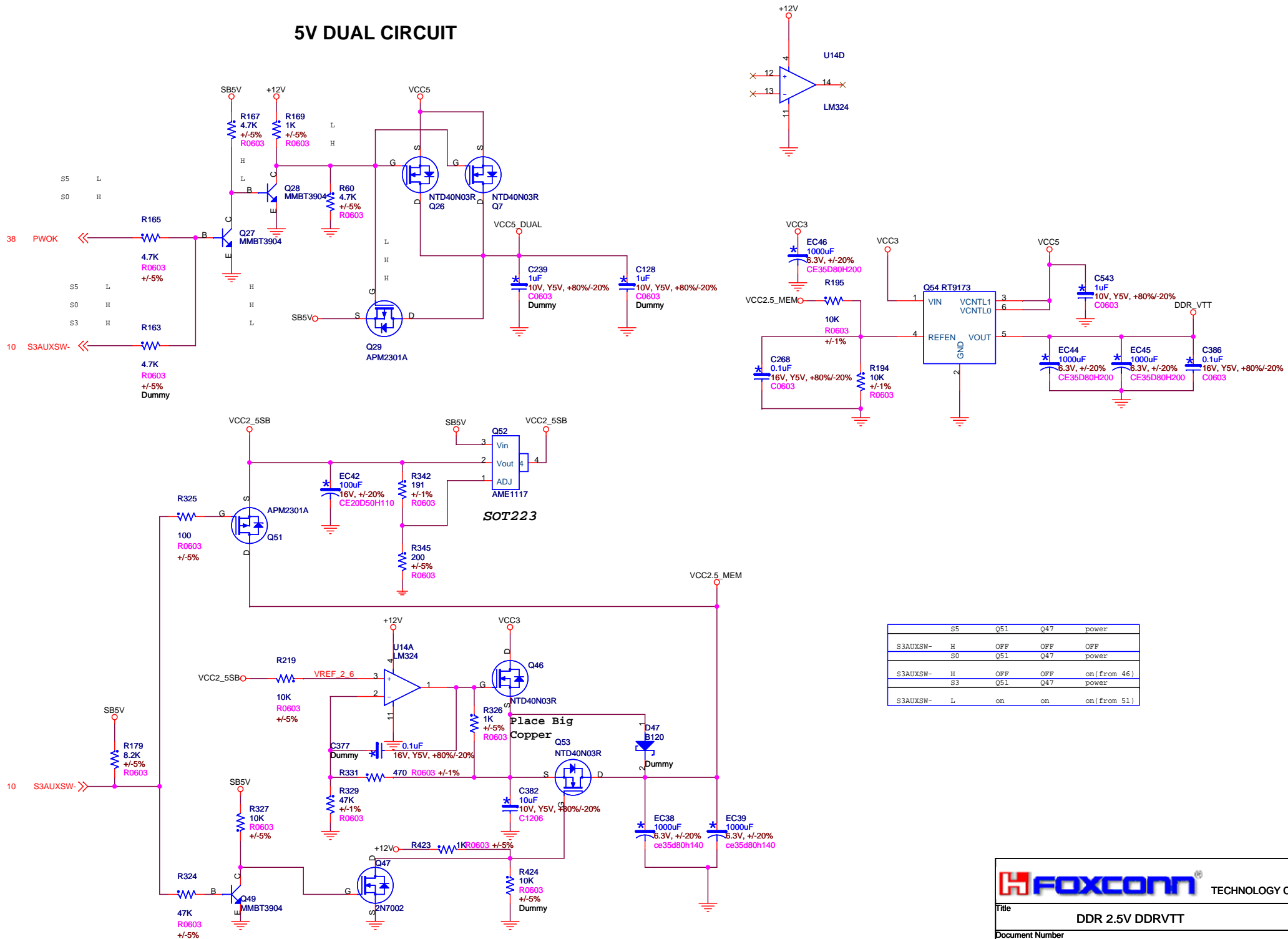
Title: SB3V, SB1.8V, VCC1.8V, VDDQ

Document Number: 648M06 Rev B

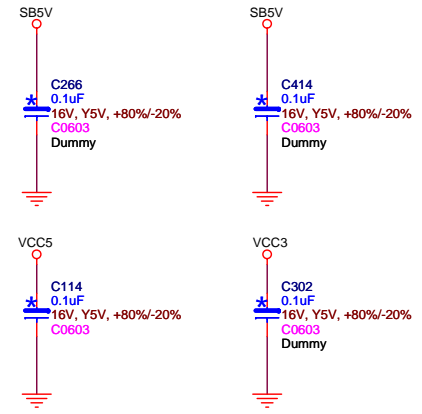
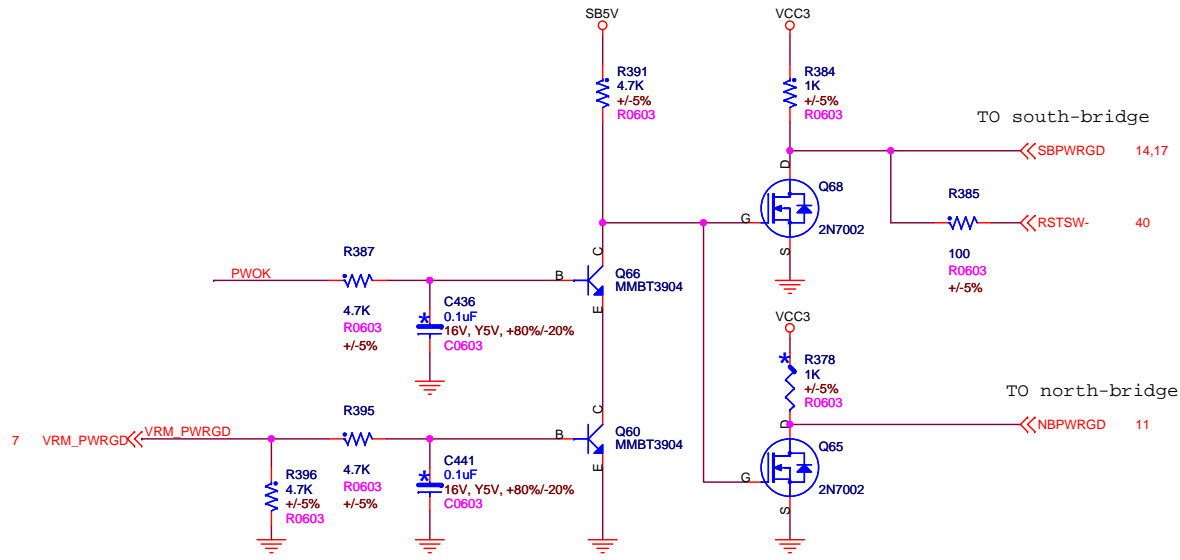
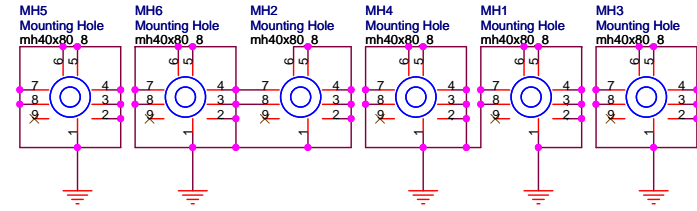
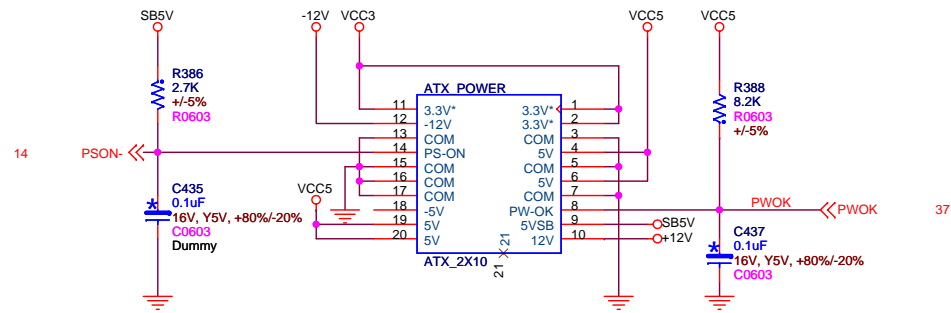
Date: Wednesday, March 16, 2005 Sheet 35 of 41



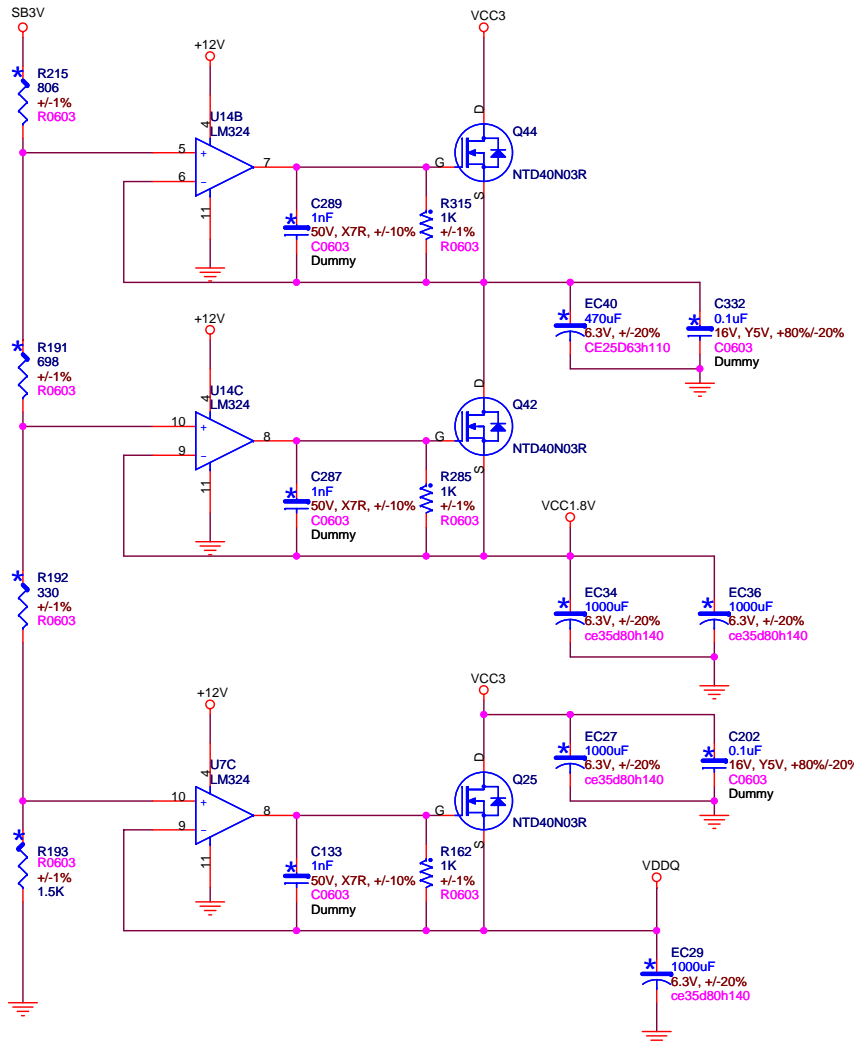
5V DUAL CIRCUIT



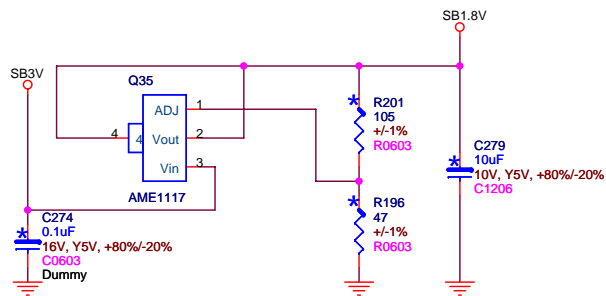
	S5	Q51	Q47	power
S3AUXSW-	H	OFF	OFF	OFF
S0	H	OFF	OFF	power
S3AUXSW-	H	OFF	OFF	on (from 46)
S3	H	ON	ON	power
S3AUXSW-	L	on	on	on (from 51)



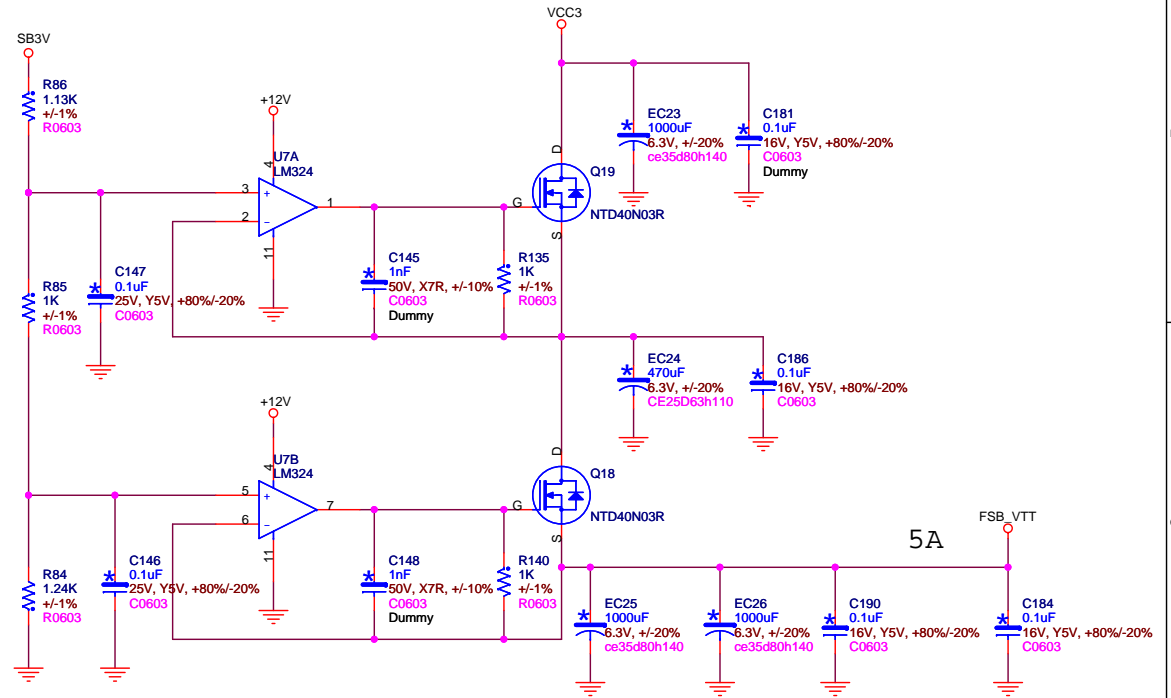
VCC1.8V and VDDQ



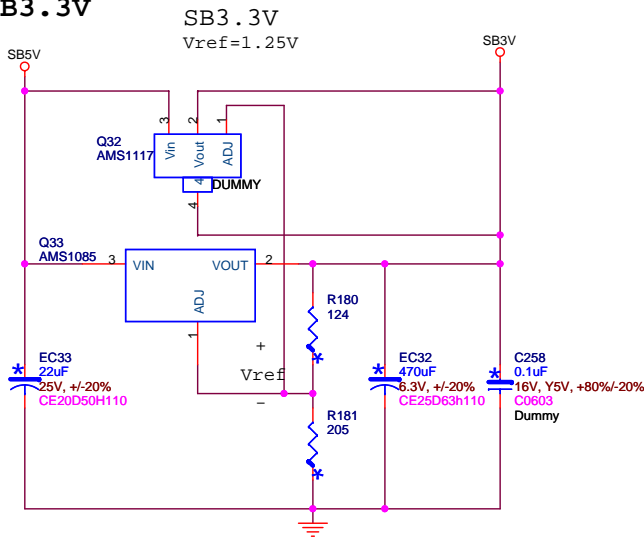
SB1.8V for 964

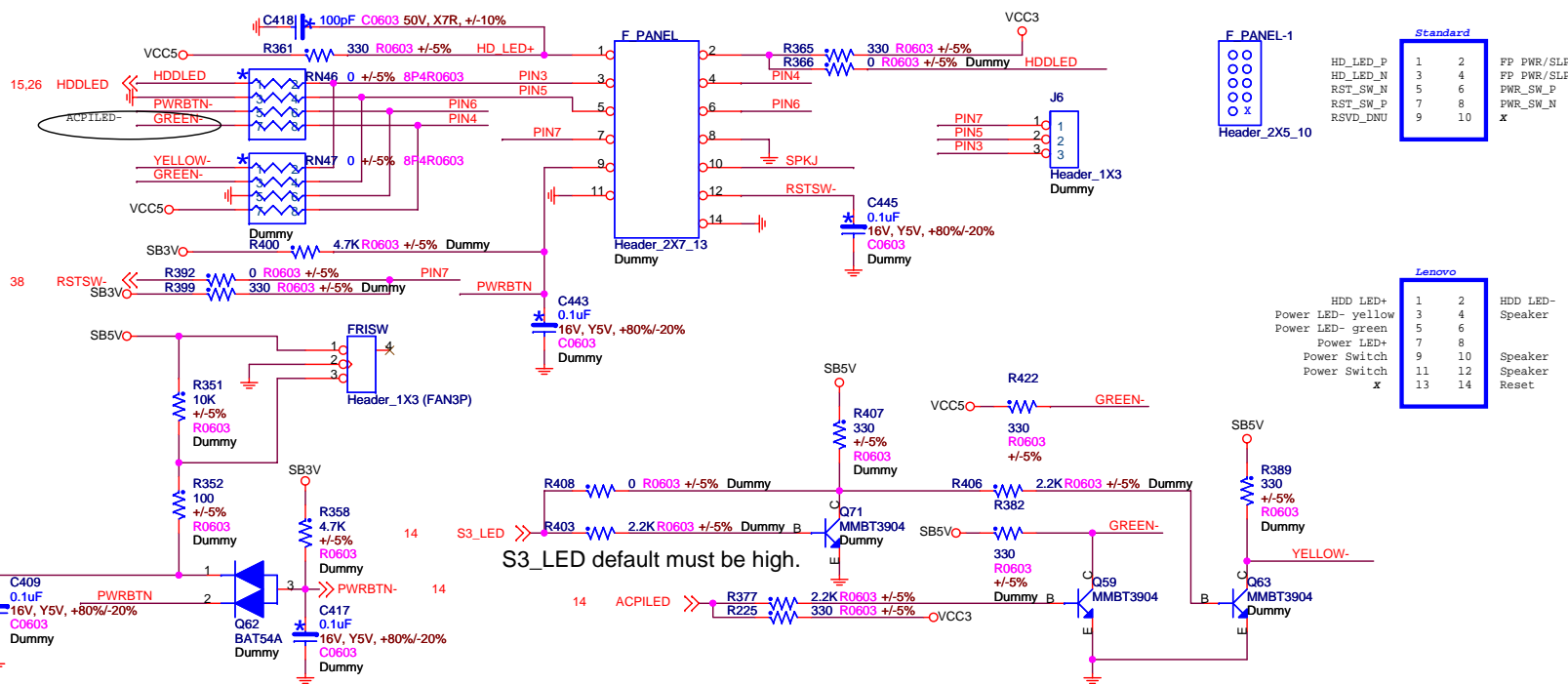


FSB_VTT



SB3.3V





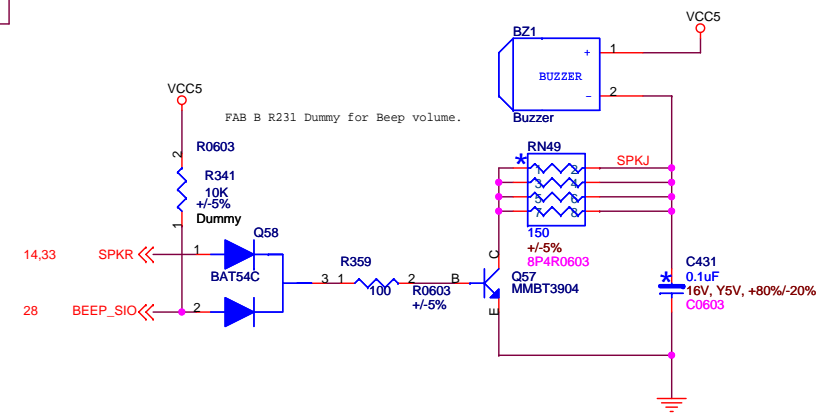
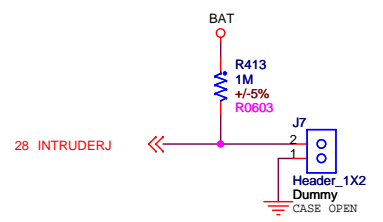
Standard		FP PWR/SLP	
HD_LED_P	1 2	FP PWR/SLP	
HD_LED_N	3 4	FP PWR/SLP	
RST_SW_N	5 6	PWR_SW_P	
RST_SW_P	7 8	PWR_SW_N	
RSVD_DNU	9 10	x	

Lenovo		HDD LED-	
HDD LED+	1 2	HDD LED-	Speaker
Power LED- yellow	3 4	Power LED- green	Speaker
Power LED+	5 6	Power Switch	Speaker
Power Switch	7 8	Power Switch	Reset
Power Switch	9 10	x	
Power Switch	11 12		
Power Switch	13 14		

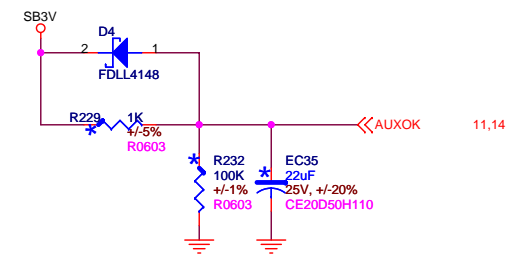
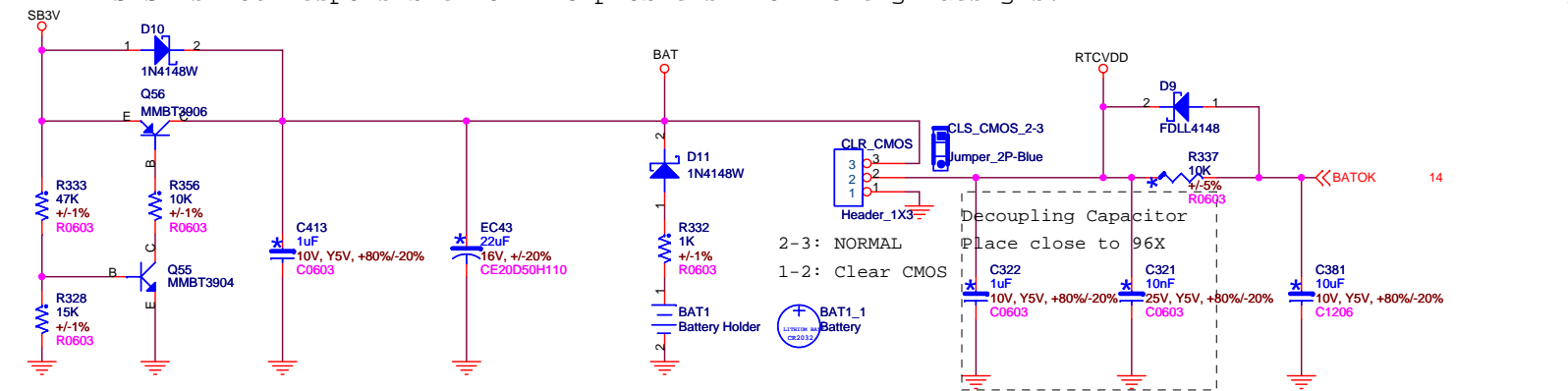
S0: Green LED is on;
 S1: Green LED is blinking;
 S3: Green LED is off;
 S4: Green LED is off;
 S5: Green LED is off.

S0: Green LED is on;
 S1: Green LED is blinking;
 S3: Yellow LED is on;
 S4: All LED are off;
 S5: All LED are off.

S3_LED default must be high.



RTC
 NOTE!
 1.The RTCVDD is 3V
 2.Decoupling capacitor must be close to 96X RTCVDD pin.
 3.RTC circuit must strictly follow SiS's recommended design
 SiS is not responsible for RTC problems from foreign designs.





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