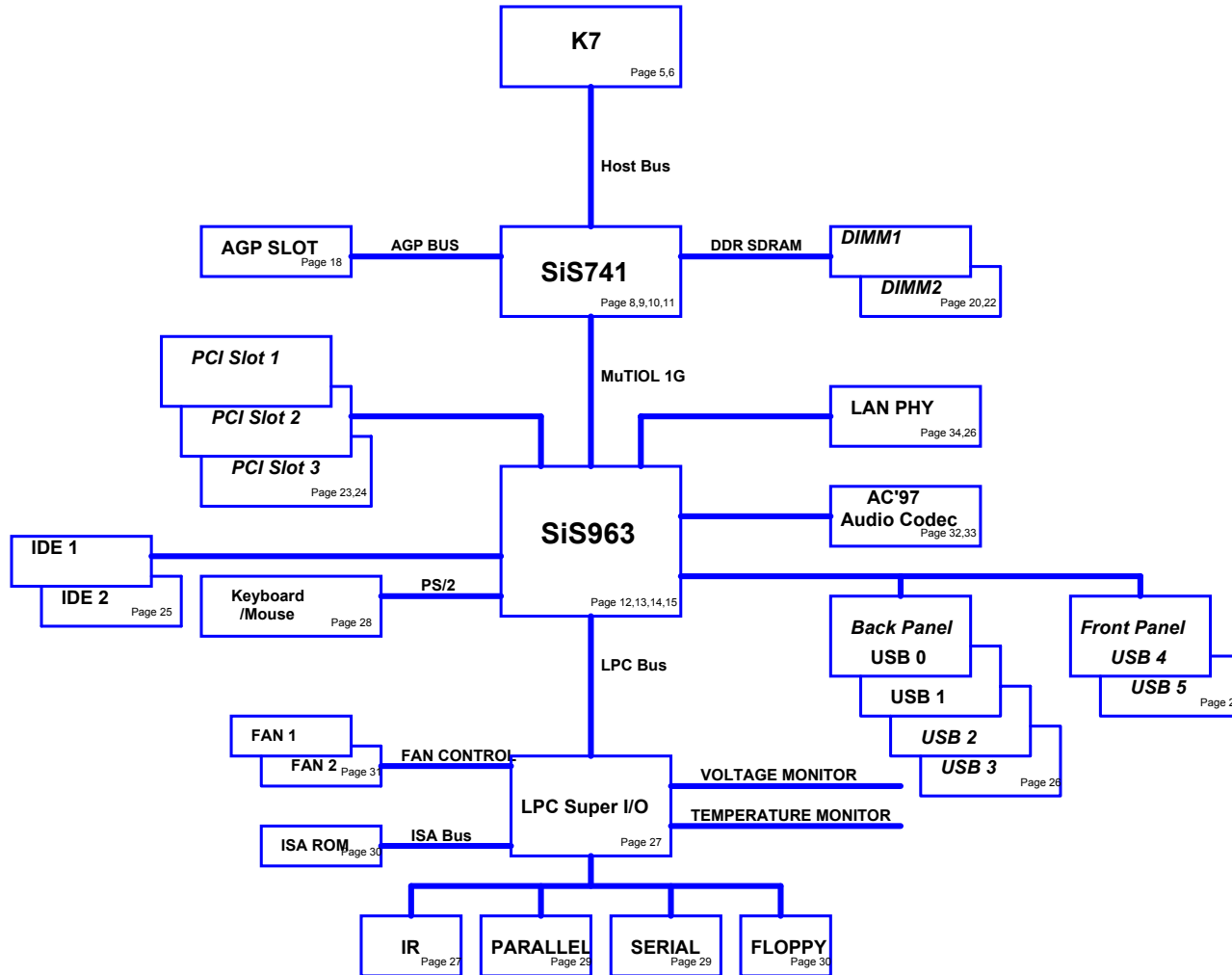


# Topology

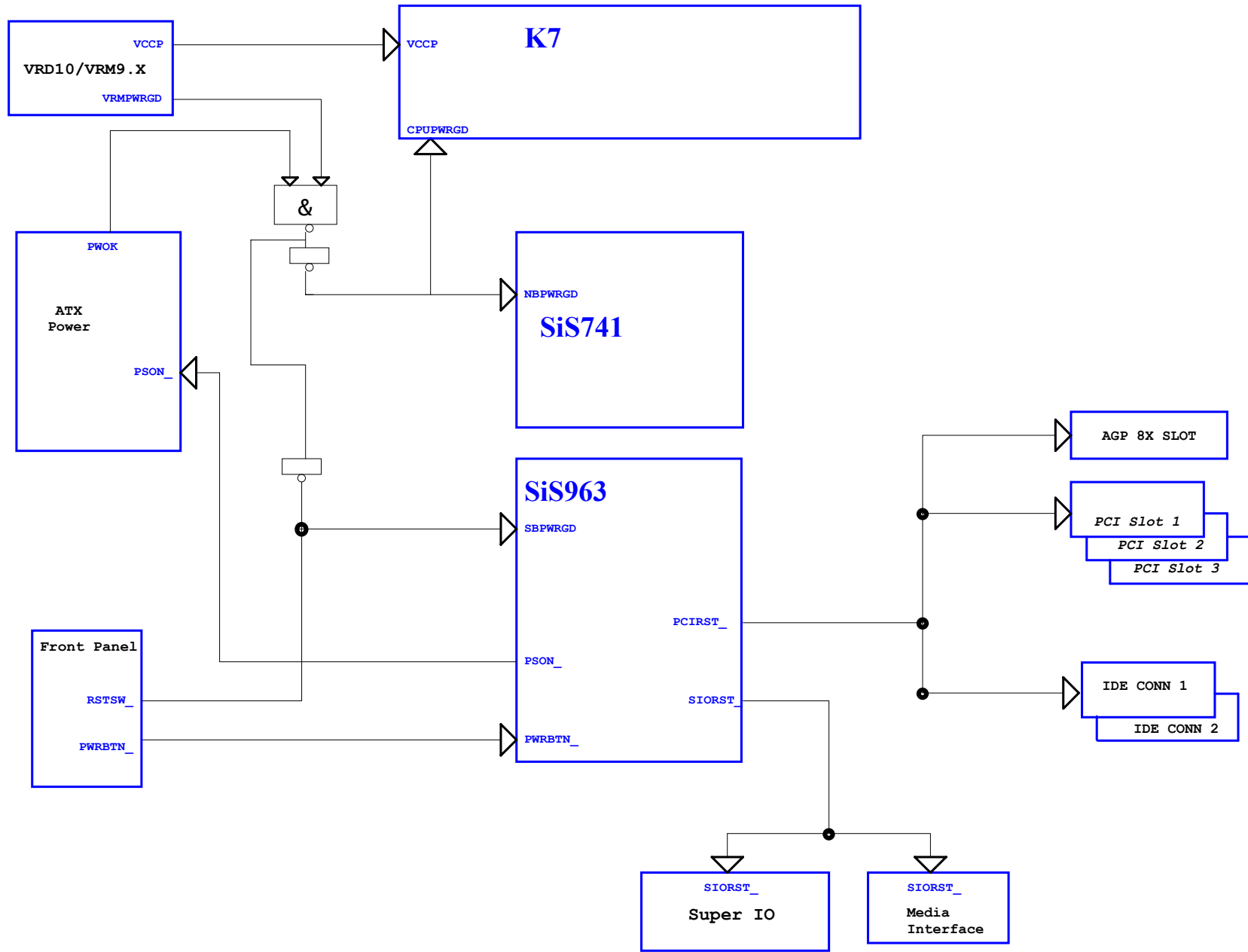


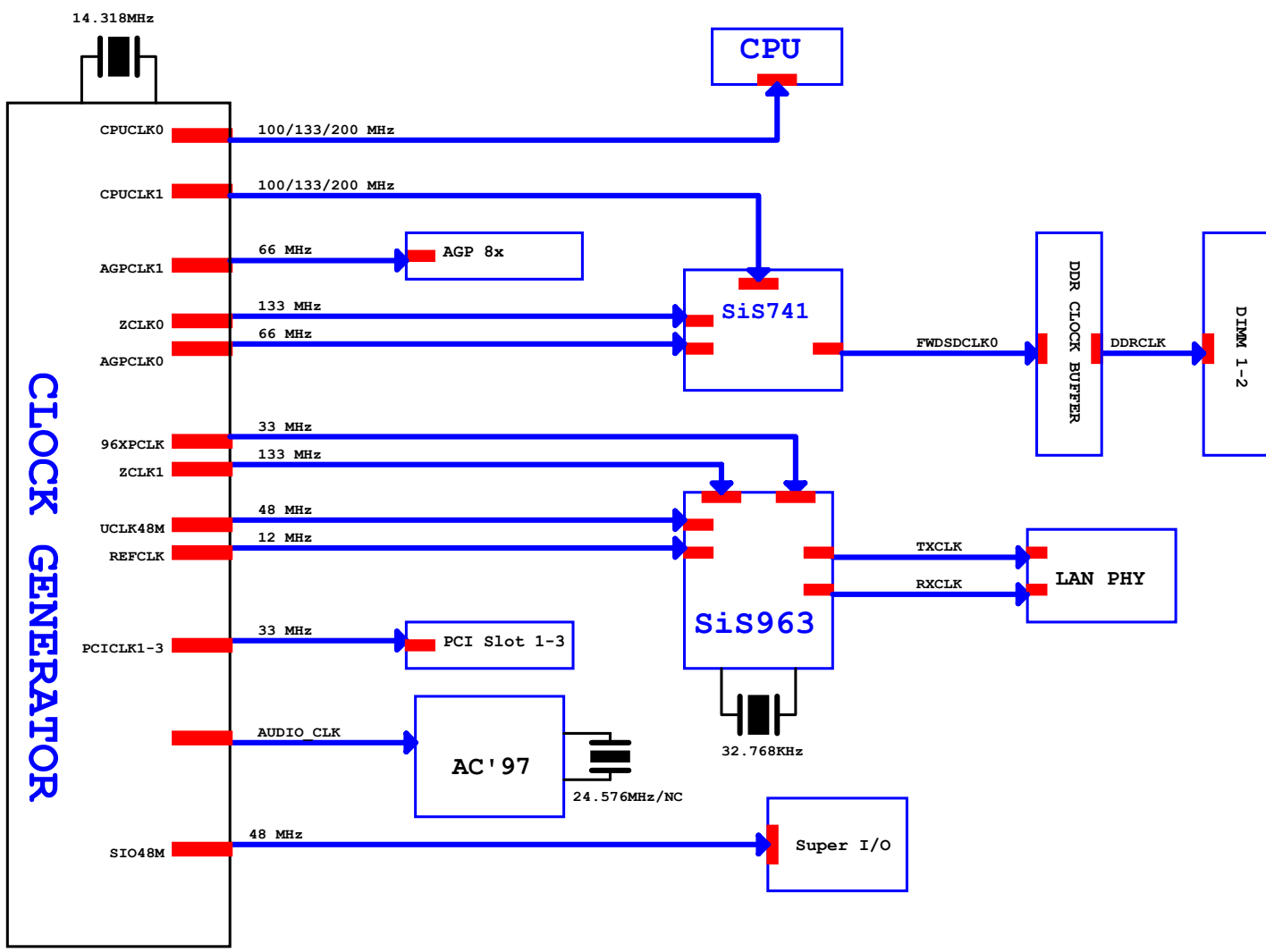
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A1	FIRST RELEASE	06/07/04	

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Page 9.	741-2 DDR
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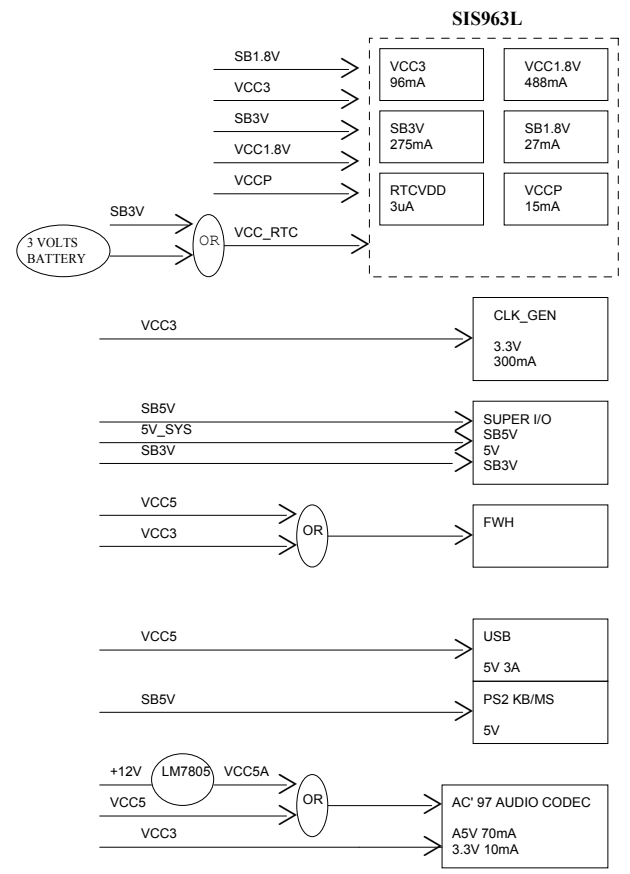
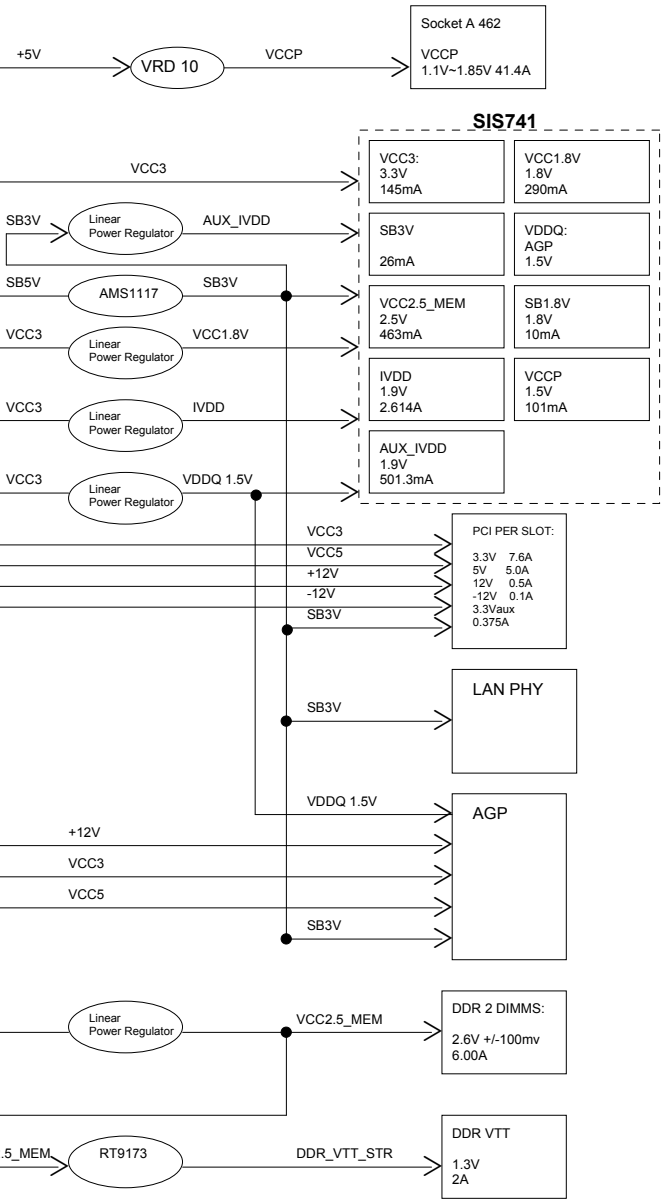
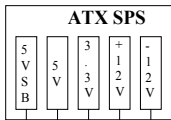


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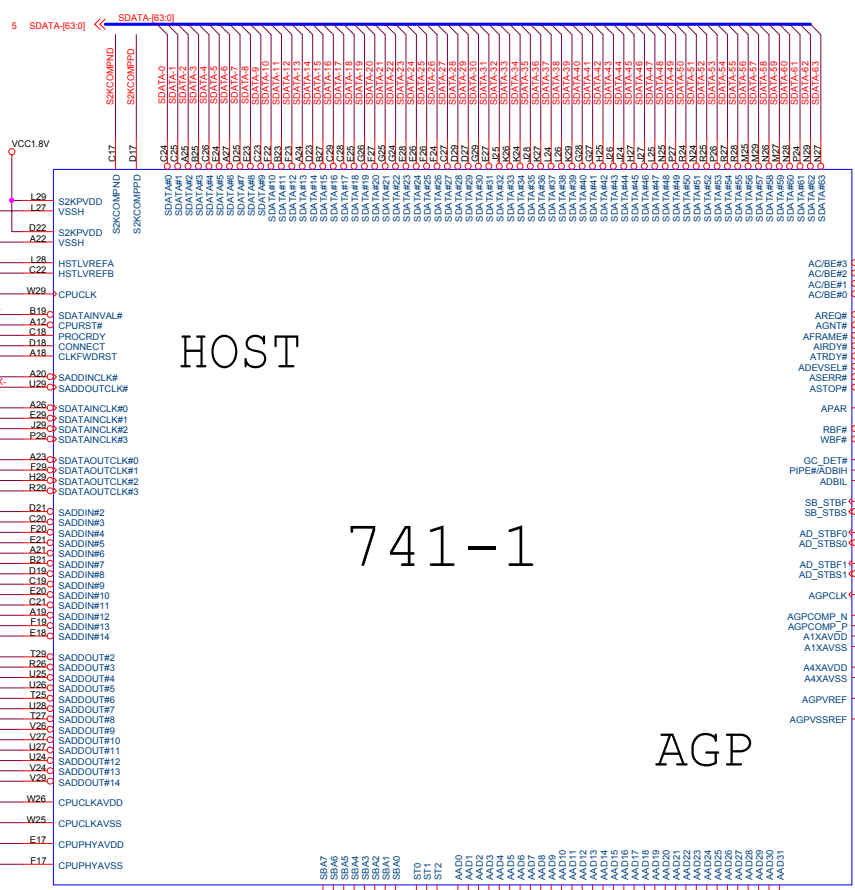
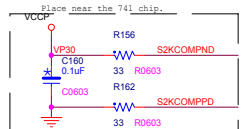
Title <b>Clock Distribution</b>		
Size C	Document Number <b>741M01C</b>	Rev A
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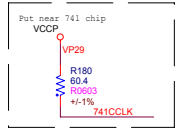
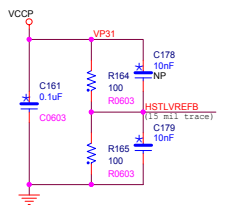
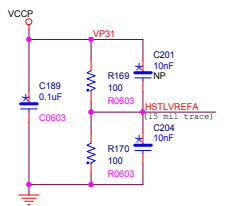
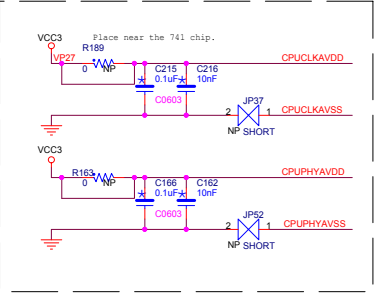
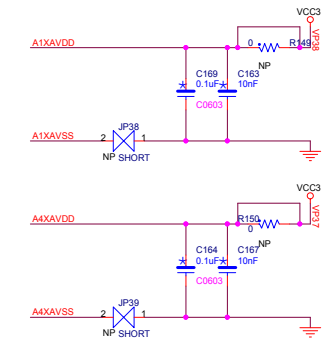
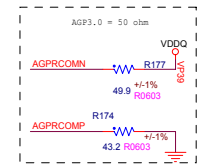
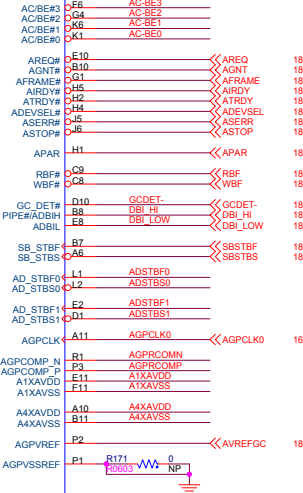




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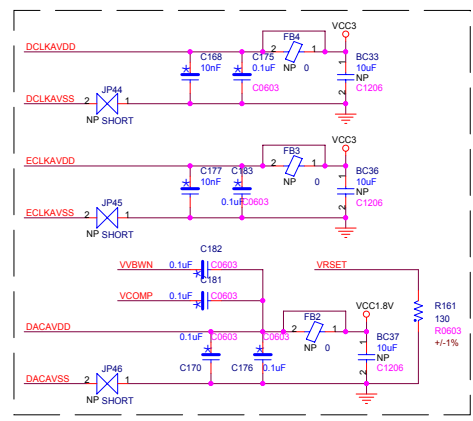
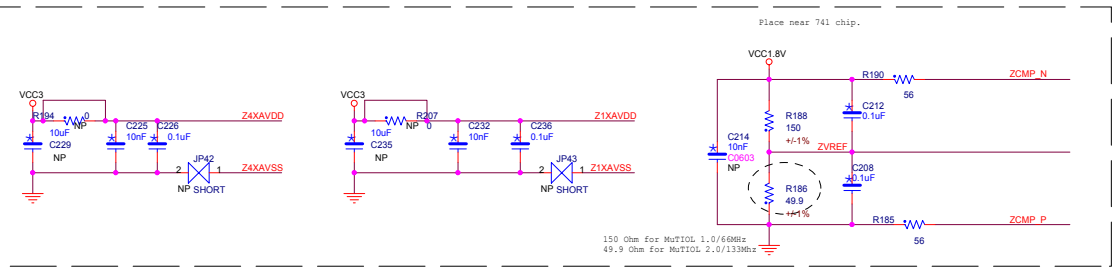
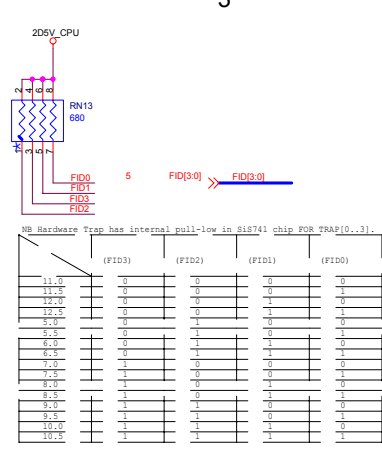
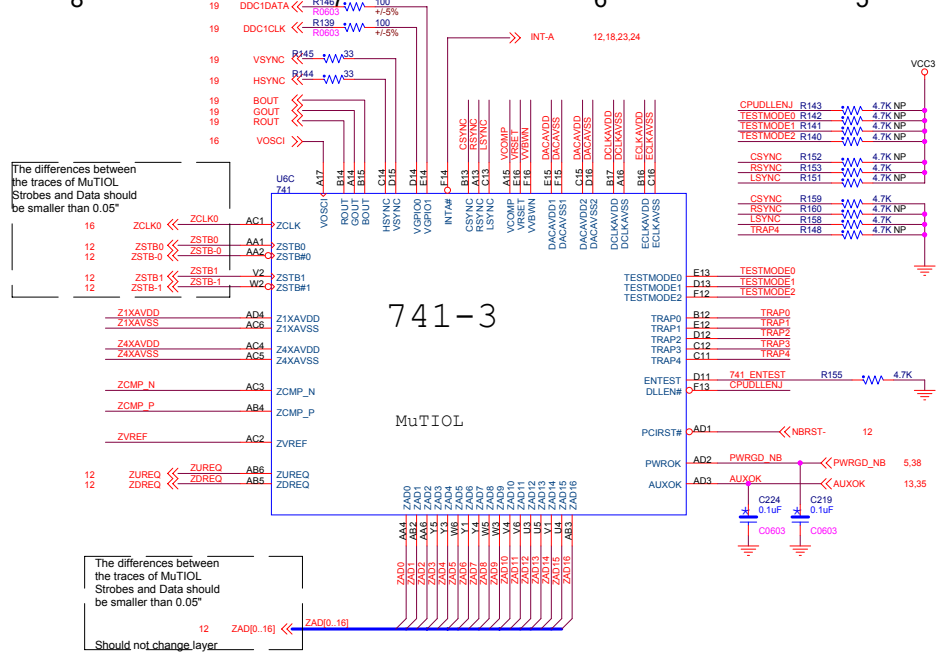
741-1

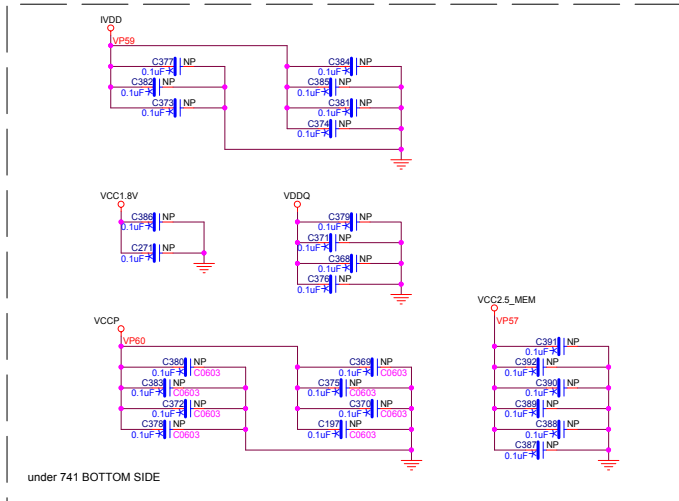
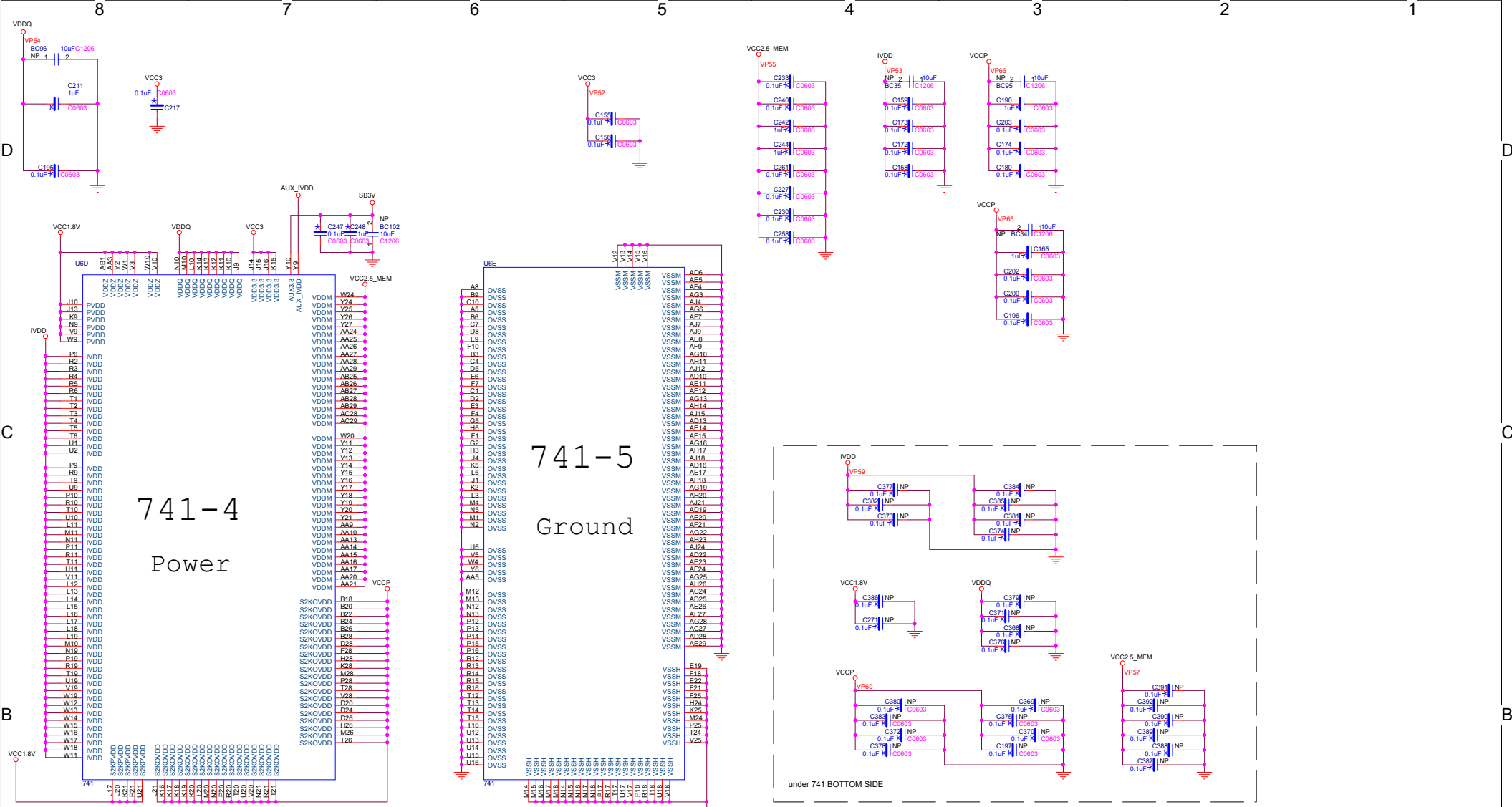
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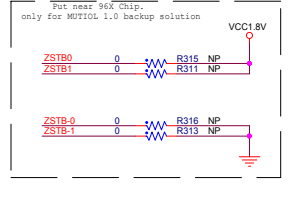
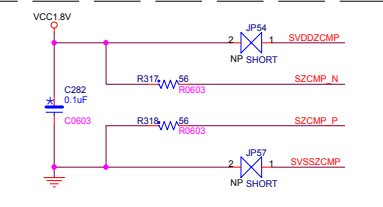
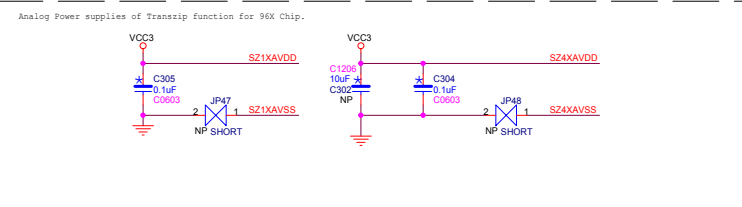
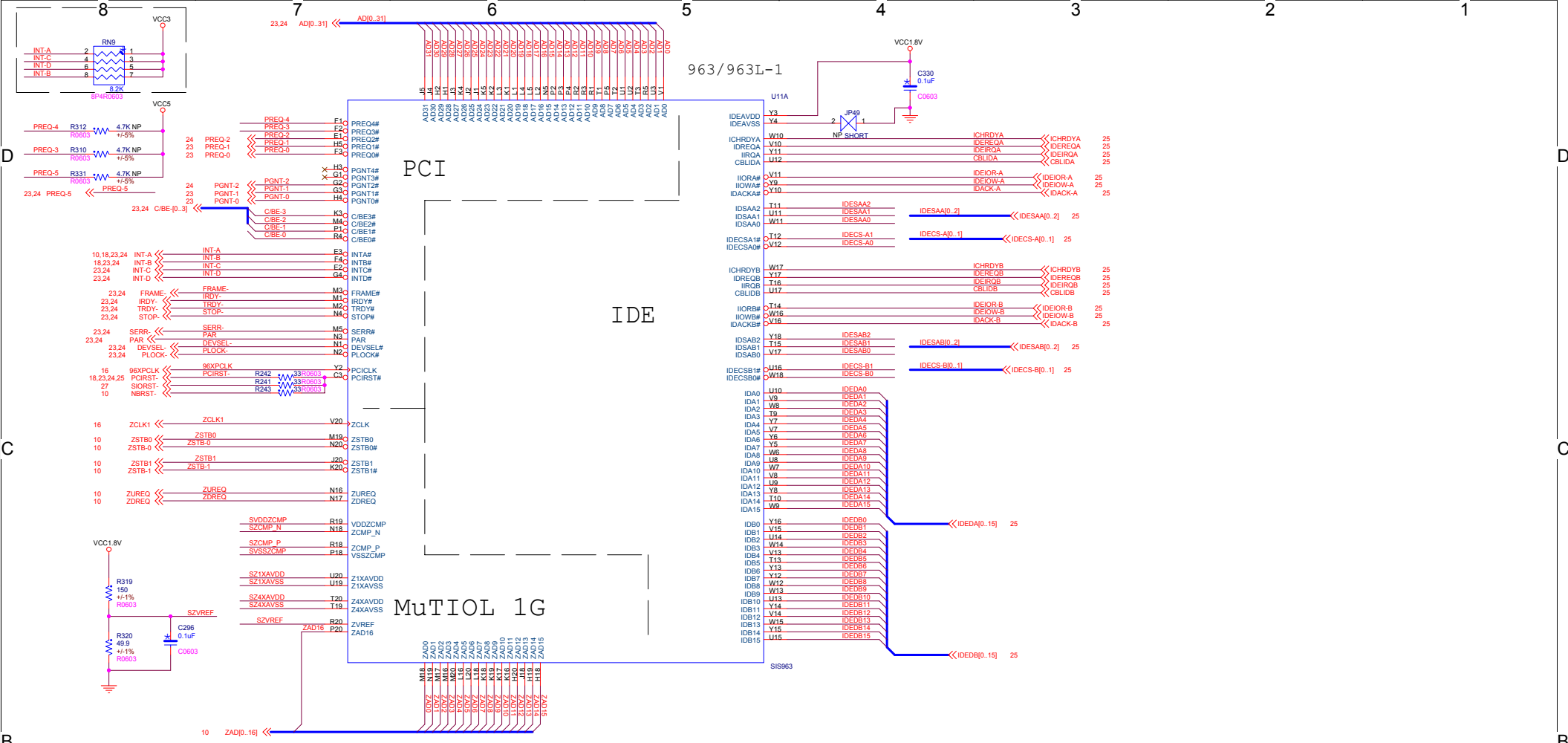


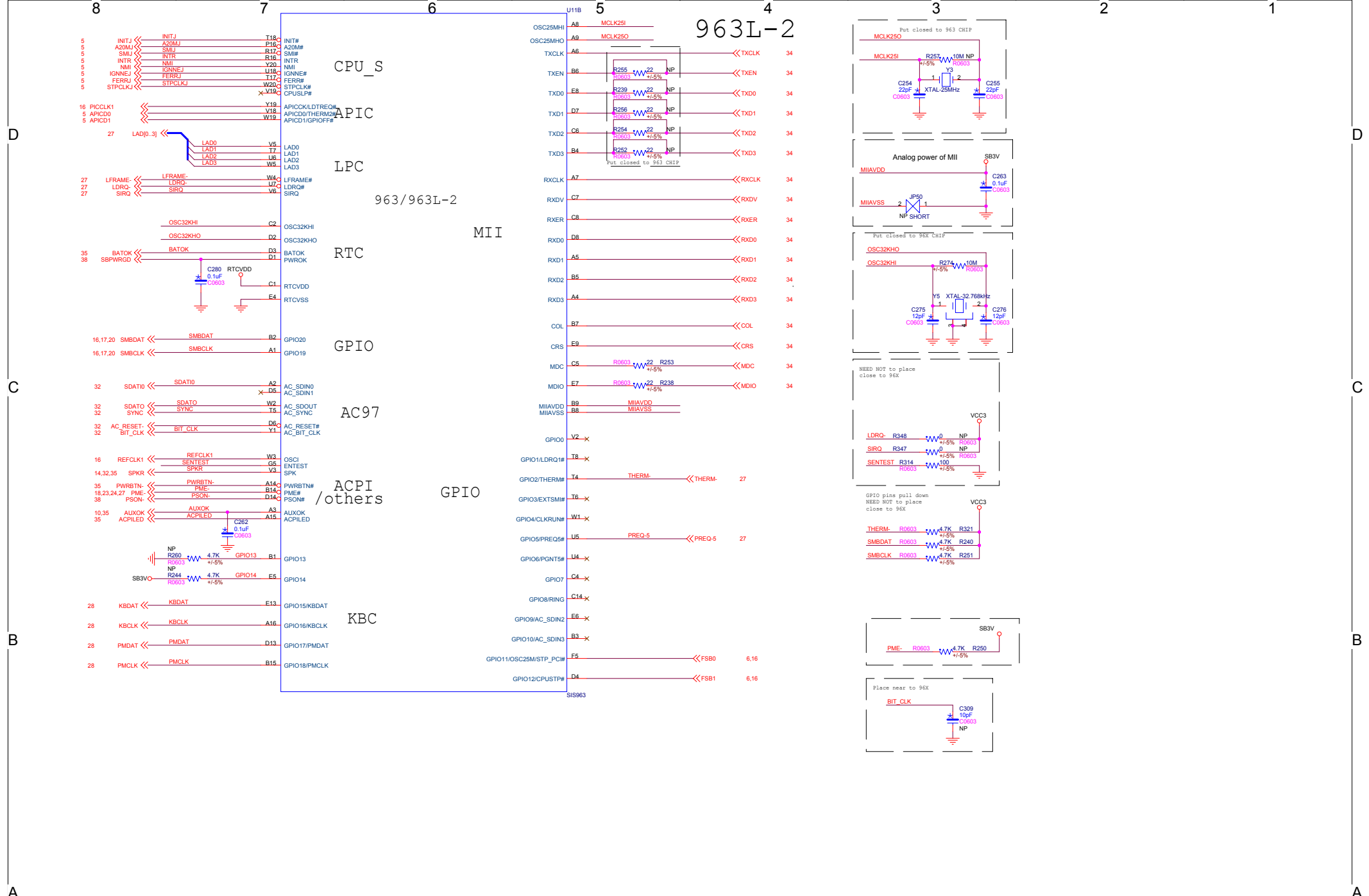




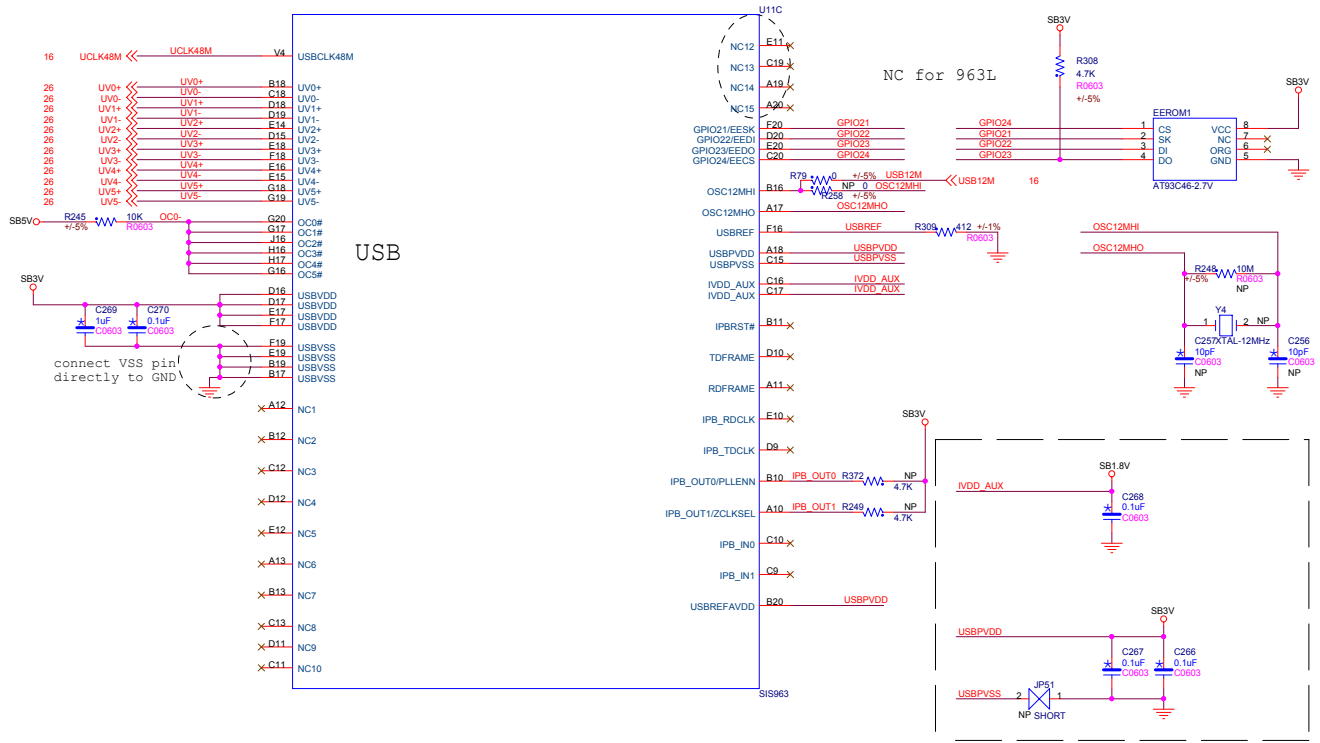




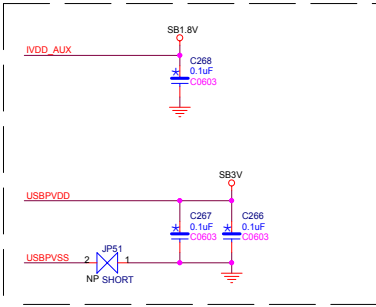




963/963L-3



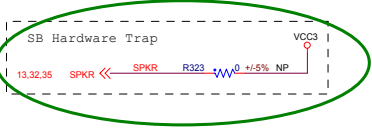
USB

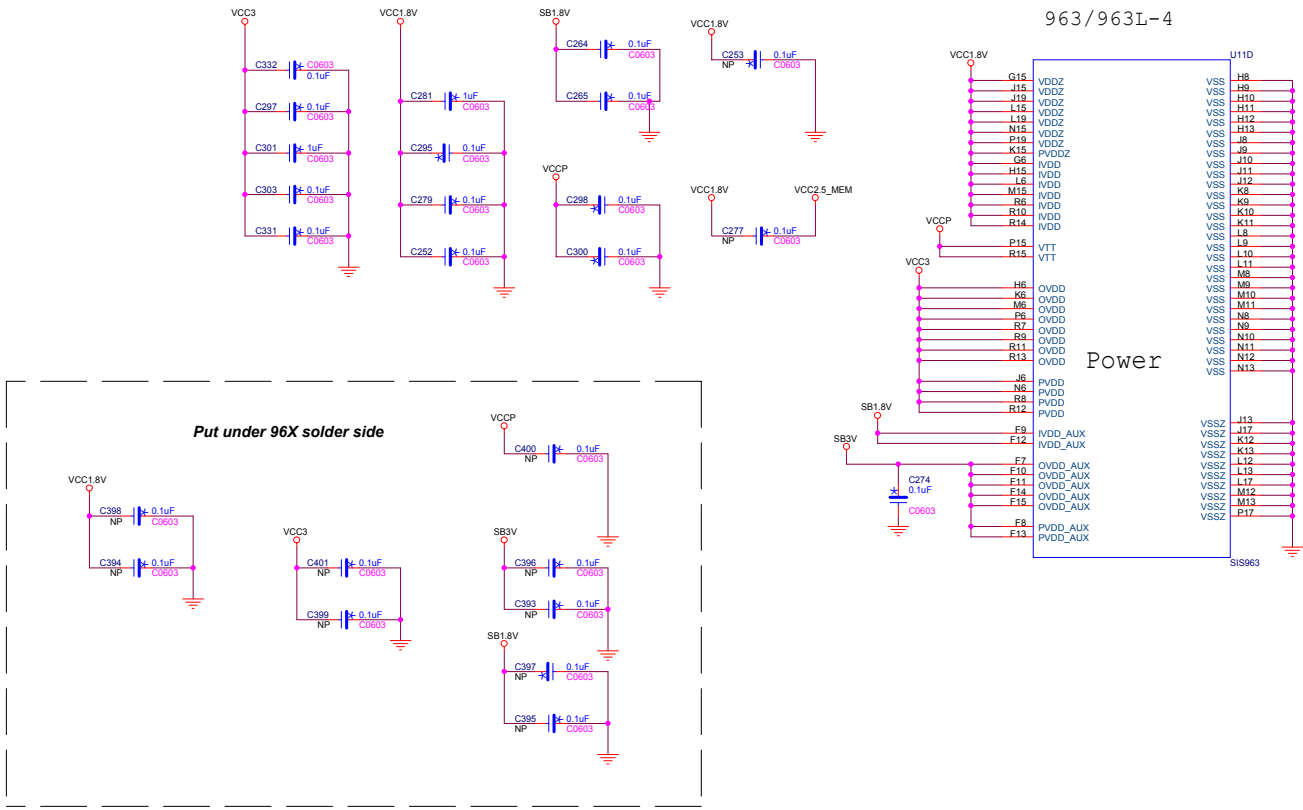


NC for 963L

connect VSS pin directly to GND

	0	1	Default	Internal pull-low (30-50K Ohm)
SPKR (LPC addr mapping)	disable	enable	R169 un-stuff	yes
SDA70 (Trap from)	ROM	PCI AD	R170 un-stuff	yes
OC4- (SB debug mode)	enable	disable	R171 un-stuff	NO





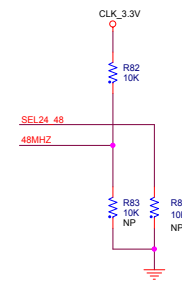
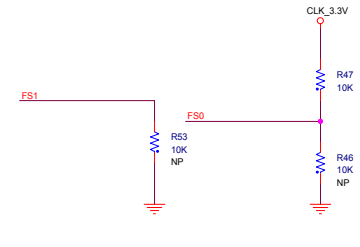
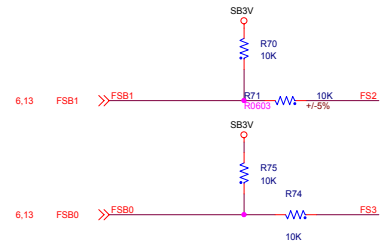
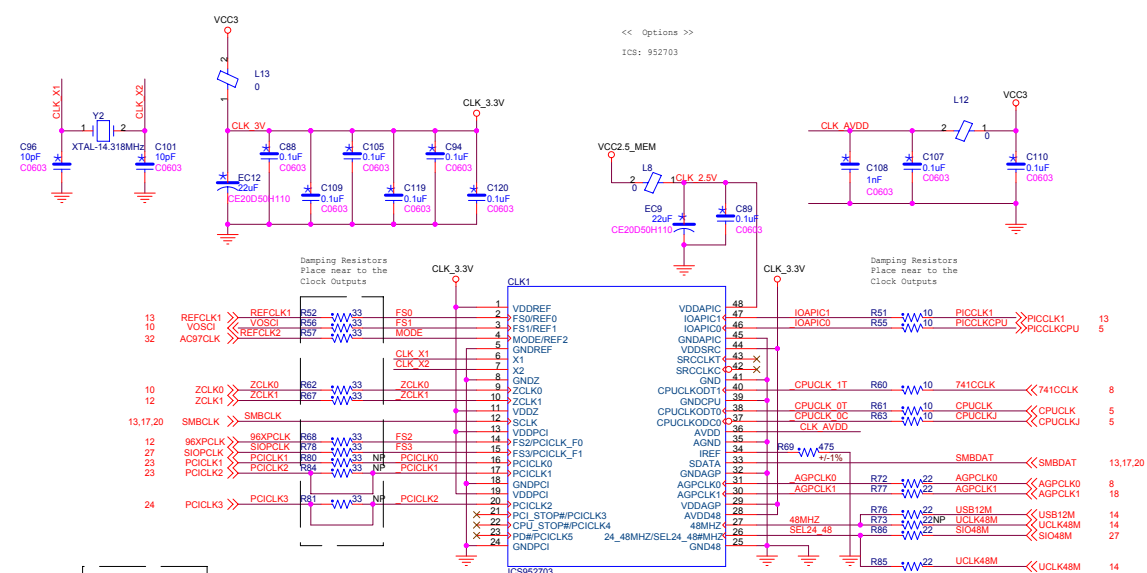
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Title **963-4 POWER**

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# Main Clock Generator



Different clock generator with different frequency define table

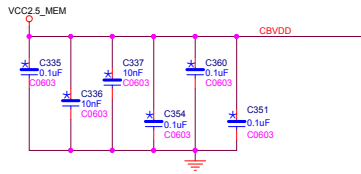
S18 741 CLOCK ( ICS952703 )					S18 741 CLOCK ( ICS952703 )				
(Bit4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	SAVA (MHz)
0	0	0	0	0	200	133.33	66.67	33.33	100
0	0	0	0	1	200	133.33	66.67	33.33	100
0	0	0	0	1	200.99	133.99	67	33.5	100.5
0	0	0	1	1	190	126.67	63.33	31.67	95
0	0	1	0	0	100	133.33	66.67	33.33	100
0	0	1	0	1	100	133.33	66.67	33.33	100
0	0	1	1	0	100.99	134.65	67.33	33.66	100.99
0	0	1	1	1	95	126.67	63.33	31.67	95
0	1	0	0	0	160	133.33	66.67	33.33	100
0	1	0	0	1	166.66	138.88	69.44	34.72	104.16
0	1	0	1	0	161.58	134.65	67.33	33.66	100.99
0	1	0	1	1	152	126.67	63.33	31.67	95
0	1	1	0	0	133.33	133.33	66.67	33.33	100
0	1	1	0	1	133.33	133.33	66.67	33.33	100
0	1	1	1	0	133.99	133.99	67	33.5	100.49
0	1	1	1	1	126.66	126.66	63.33	31.67	95

S18 741 CLOCK ( ICS952703 )					S18 741 CLOCK ( ICS952703 )				
(Bit4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	SAVA (MHz)
1	0	0	0	0	206	137.33	68.67	34.33	103
1	0	0	0	1	210	140	70	35	105
1	0	0	1	0	214	142.67	71.33	35.67	107
1	0	0	1	1	218	145.33	72.67	36.33	109
1	0	1	0	0	103	137.33	68.67	34.33	103
1	0	1	0	1	105	140	70	35	105
1	0	1	1	0	107	142.67	71.33	35.67	107
1	0	1	1	1	109	145.33	72.67	36.33	109
1	1	0	0	0	164.8	137.33	68.67	34.33	103
1	1	0	0	1	168	140	70	35	105
1	1	0	1	0	171.2	142.67	71.33	35.67	107
1	1	0	1	1	174.4	145.33	72.67	36.33	109
1	1	1	0	0	137.33	137.33	68.67	34.33	103
1	1	1	0	1	140	140	70	35	105
1	1	1	1	0	142.67	142.67	71.34	35.67	107
1	1	1	1	1	145.33	145.33	72.67	36.33	109



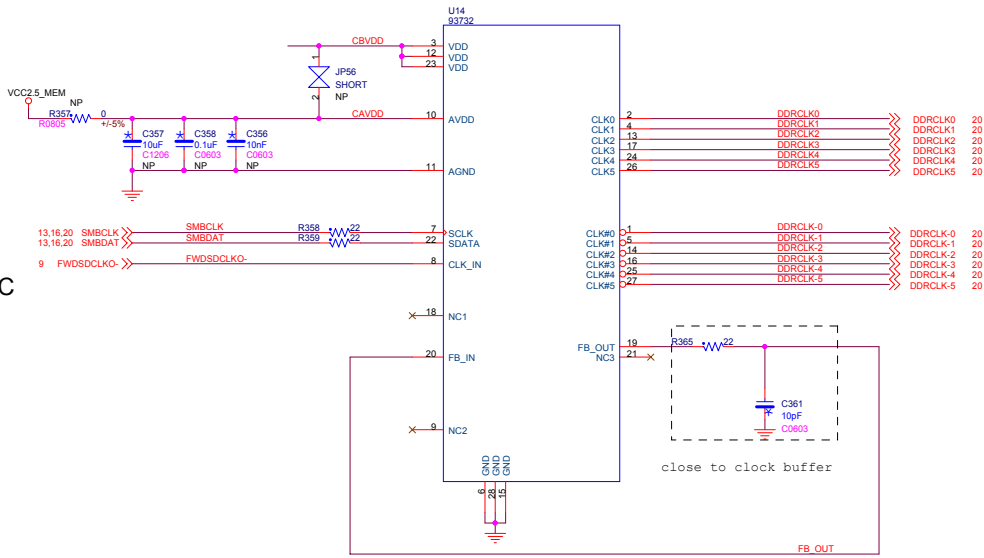
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==> DDRCLK[0..5] 20  
 ==> DDRCLK[0..5] 20

### Clock Buffer (DDR)

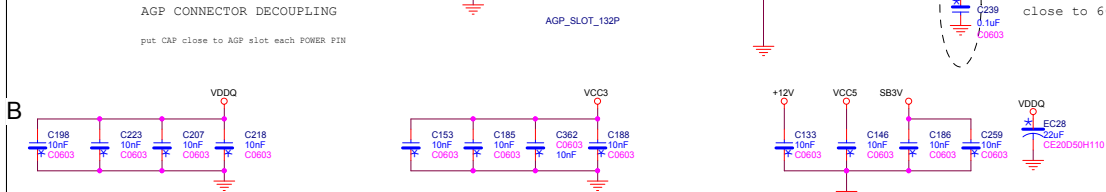
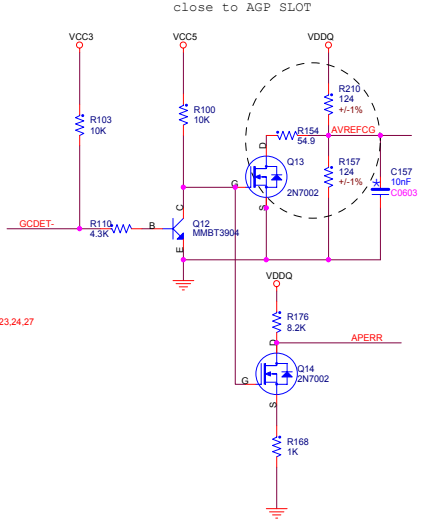
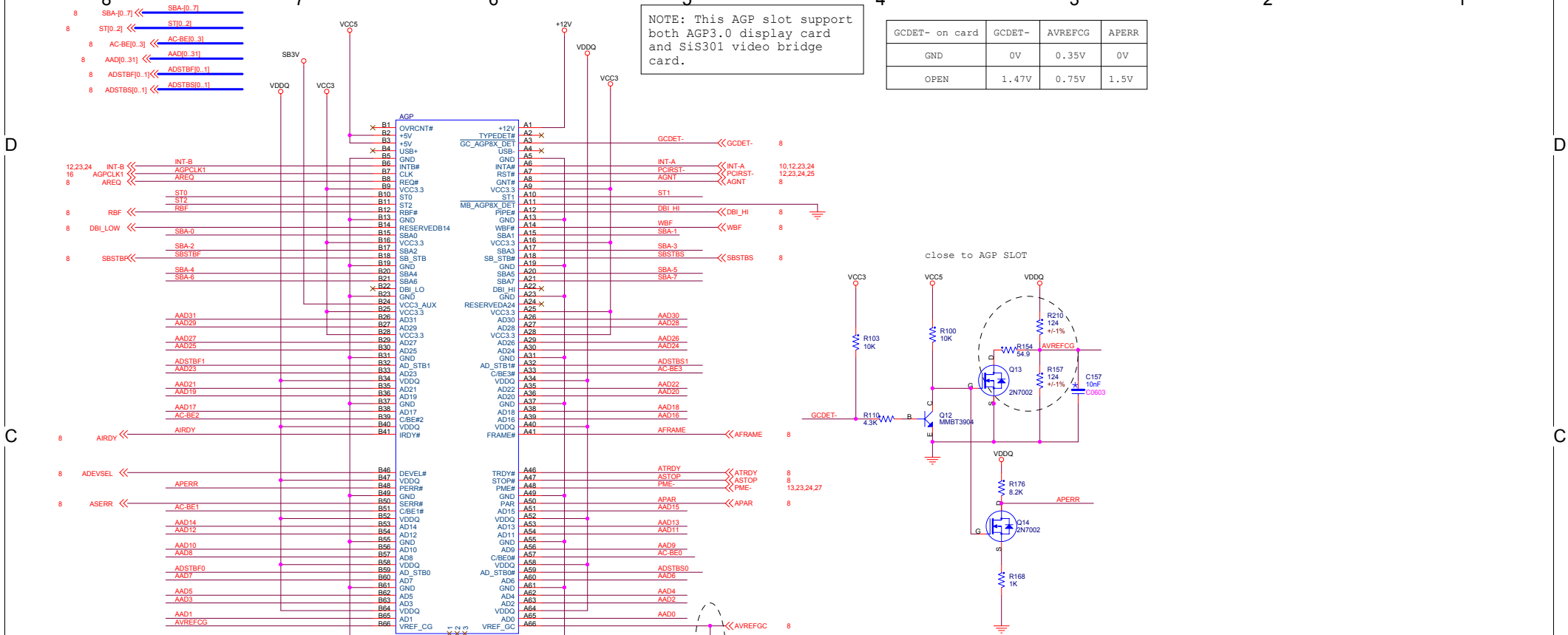


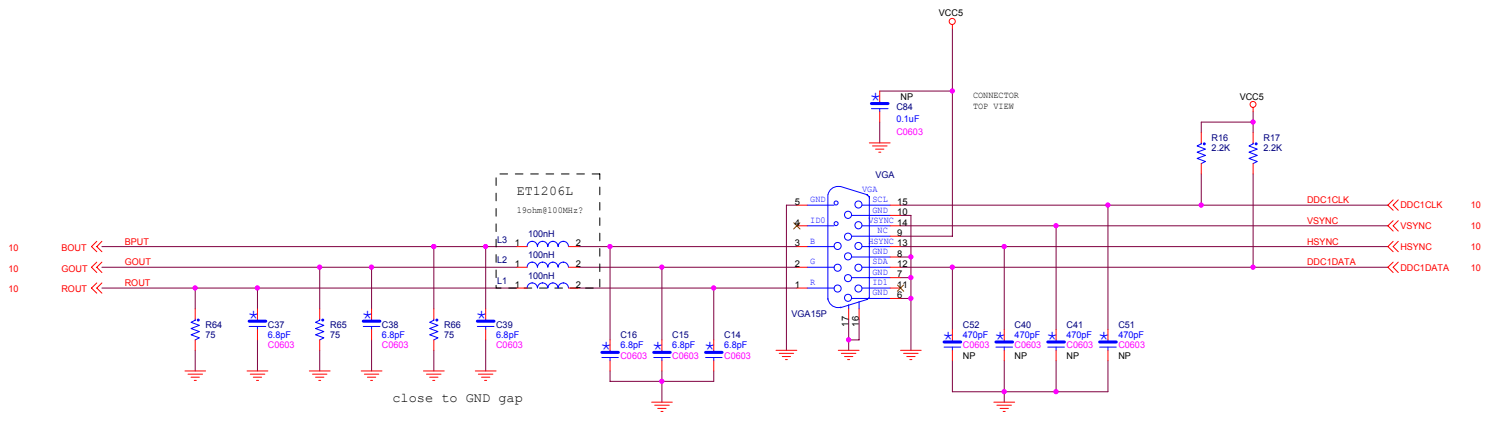
close to clock buffer



NOTE: This AGP slot support both AGP3.0 display card and SiS301 video bridge card.

GCDET- on card	GCDET-	AVREFCG	APERR
GND	0V	0.35V	0V
OPEN	1.47V	0.75V	1.5V





close to GND gap



Title			VGA Connector
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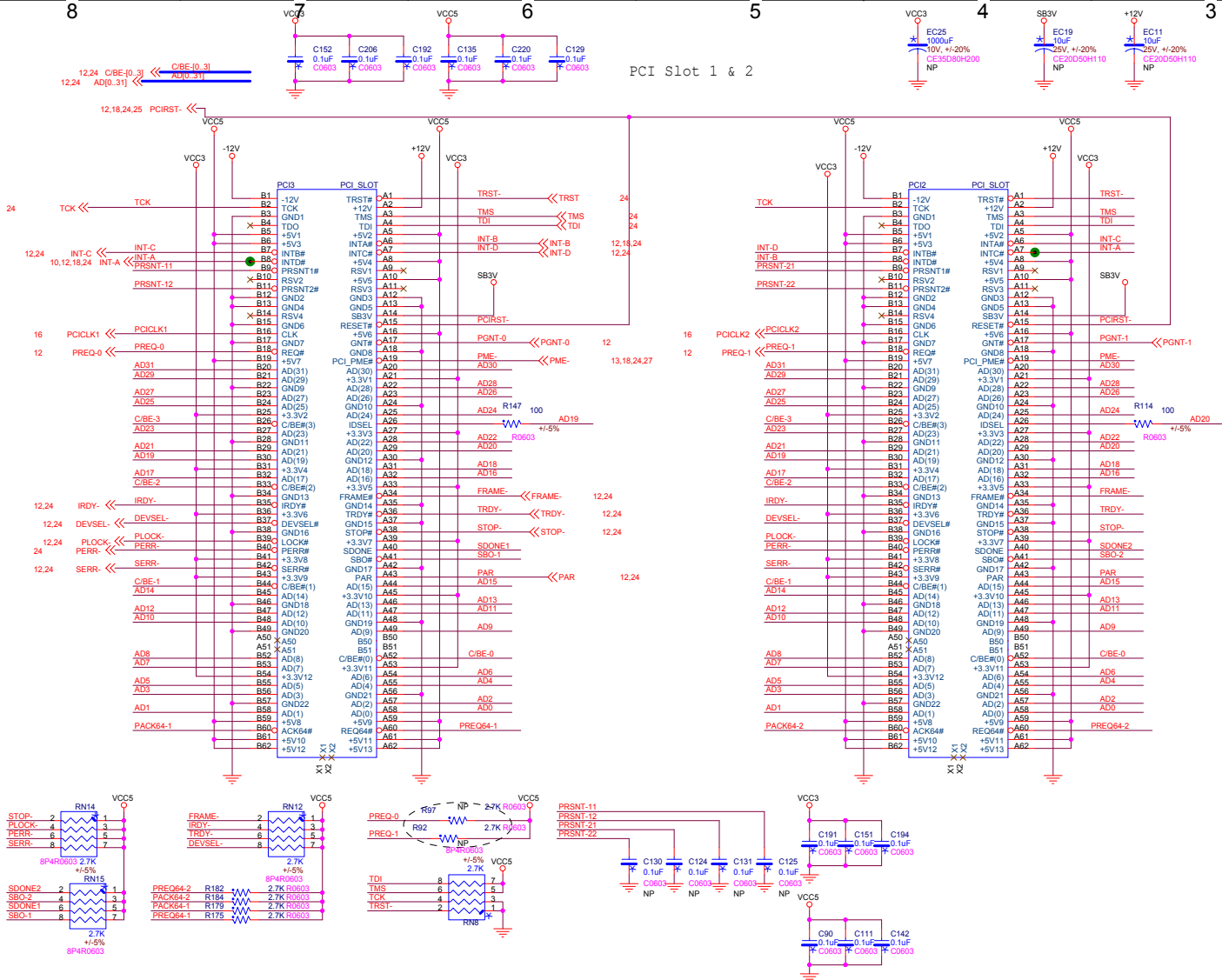
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FOXCONN PCEG

Title		
Blank		
Size	Document Number	Rev
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Date:	Monday, June 07, 2004	Sheet 1 of 40

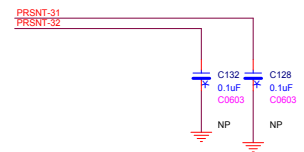
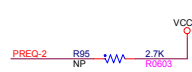
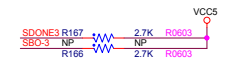
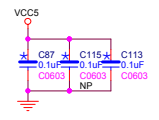
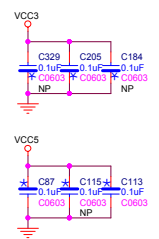
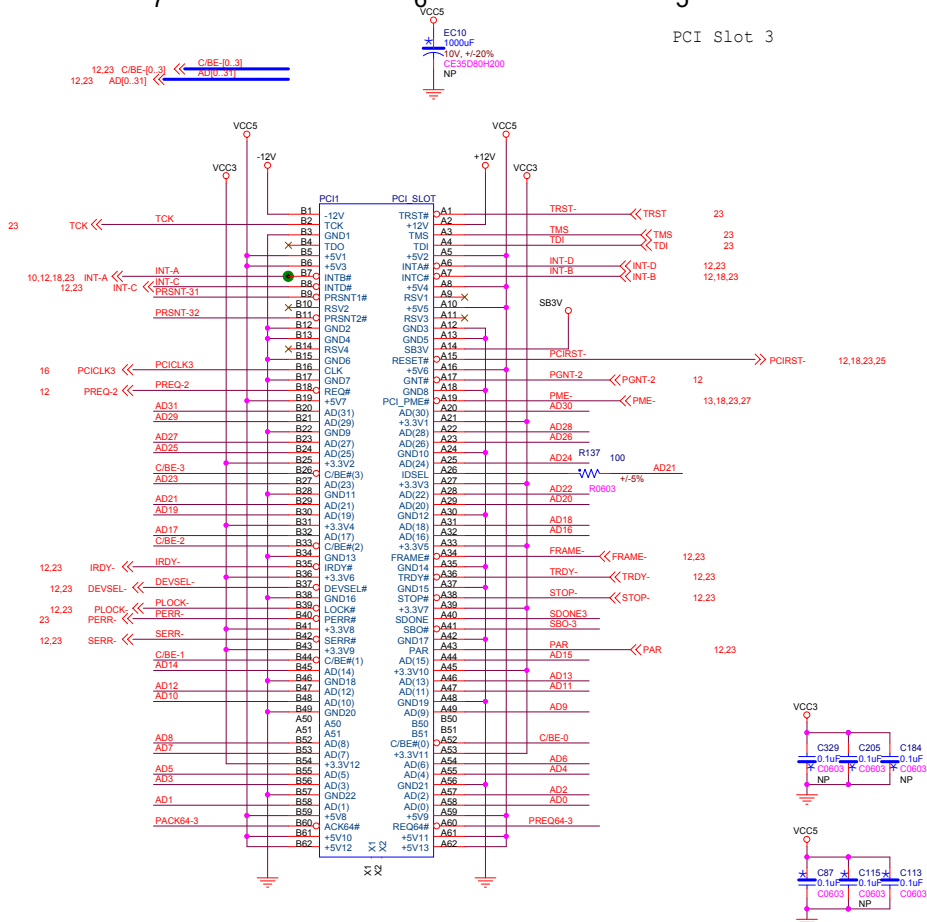




PCI Slot 1 & 2

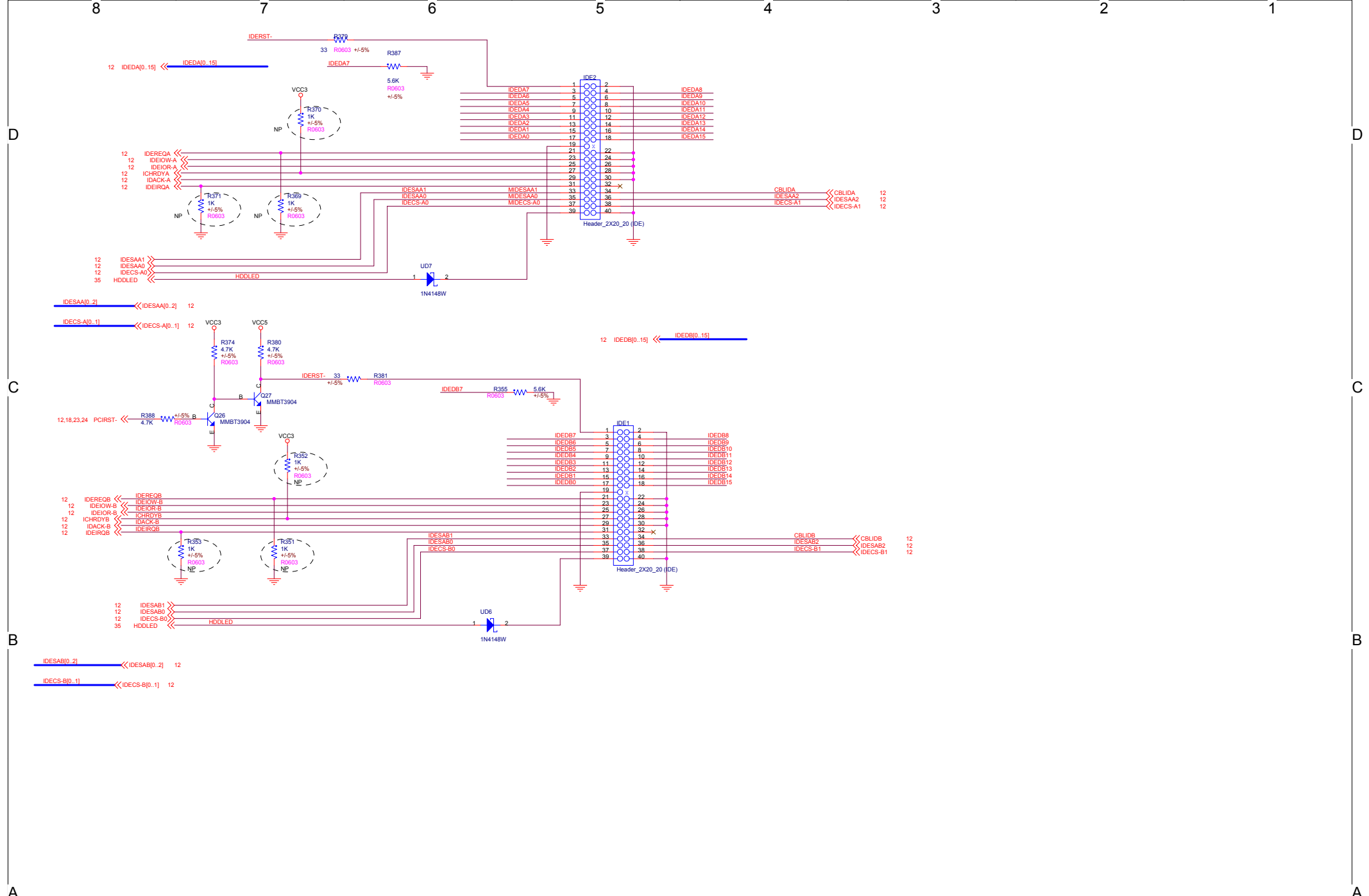


PCI Slot 3



Title <b>PCI 3</b>		
Size	Document Number <b>741M01C</b>	Rev <b>A</b>
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Title <b>IDE</b>		
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D

D

C

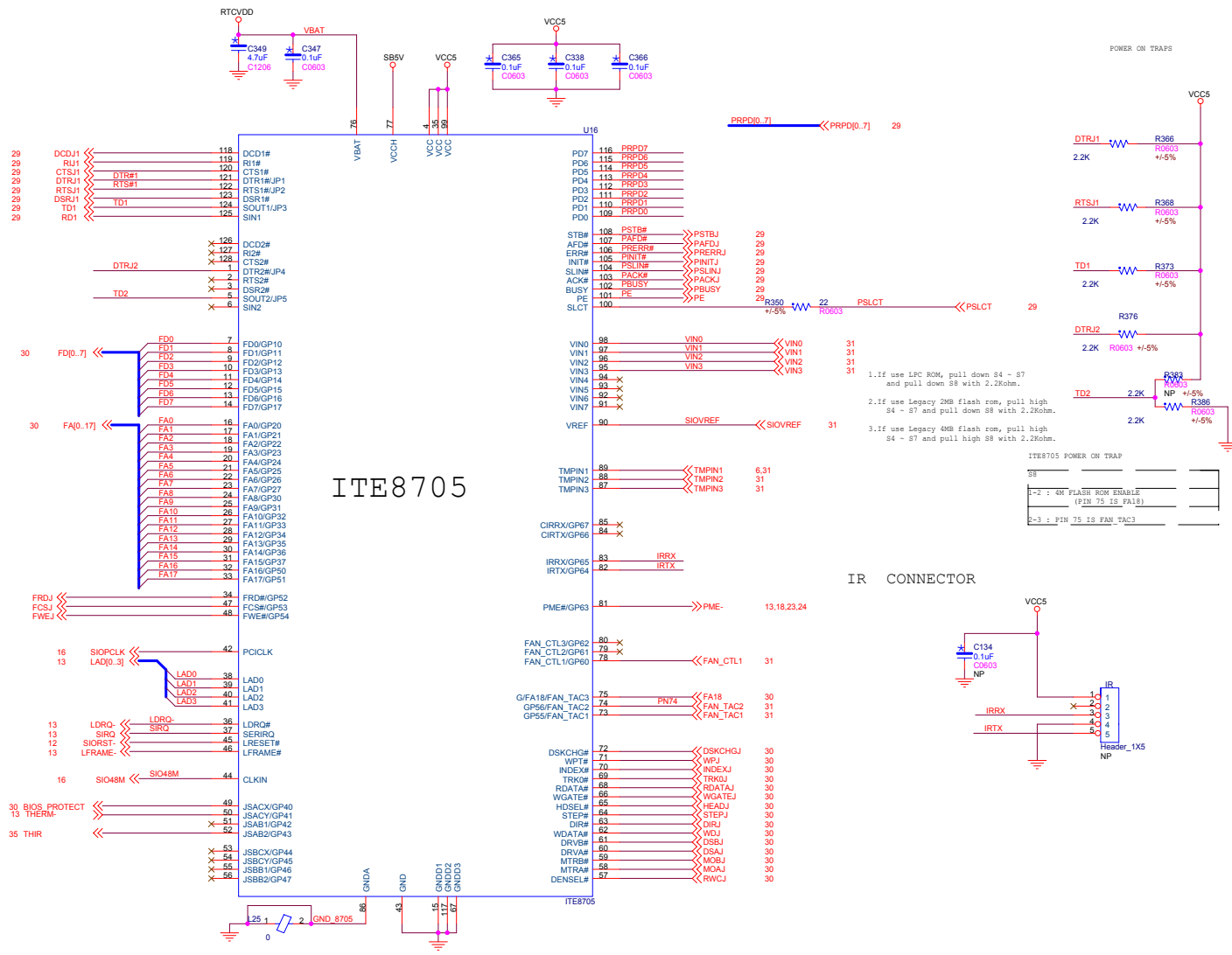
C

B

B

A

A

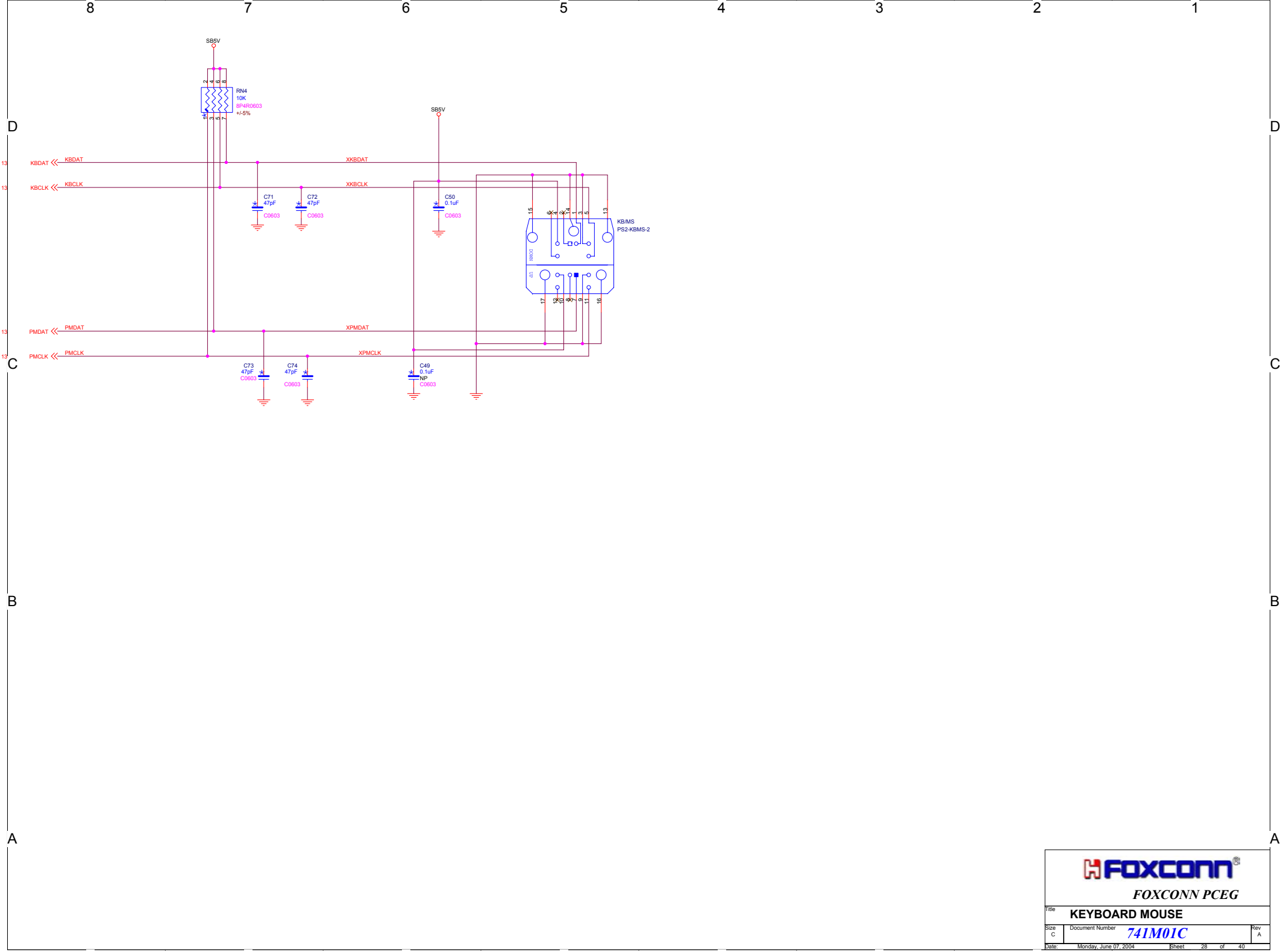


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 FOXCONN PCEG

Title: **ITE8705**

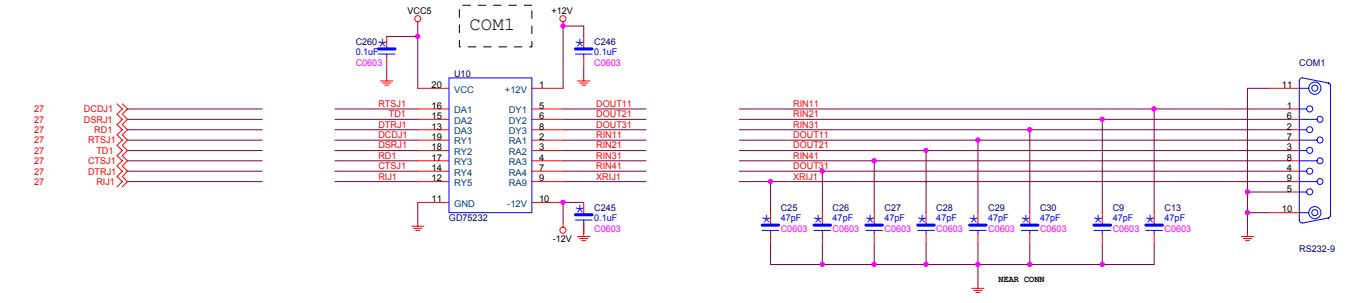
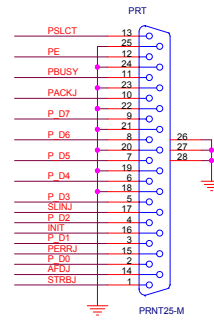
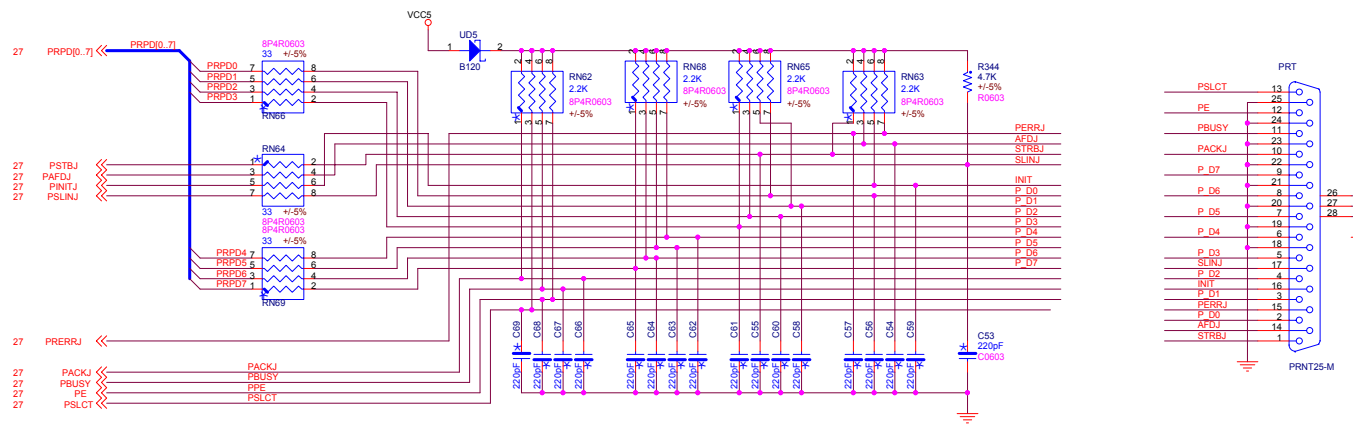
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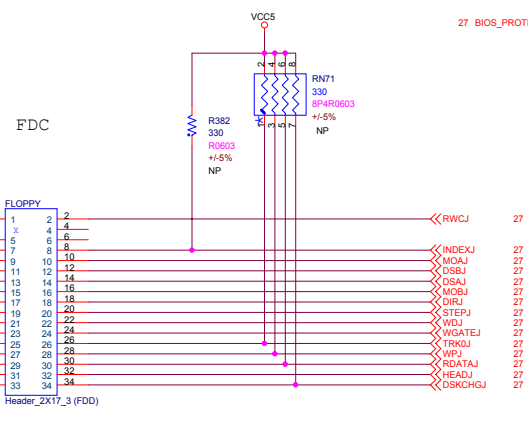
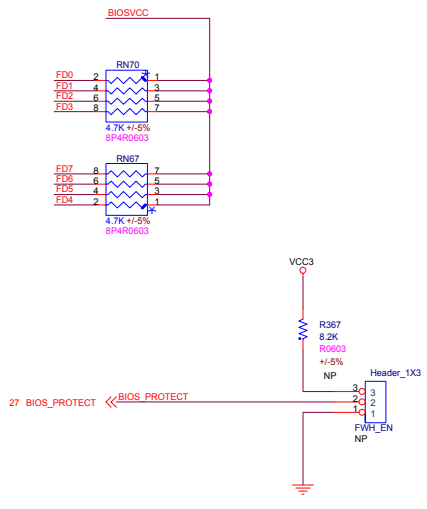
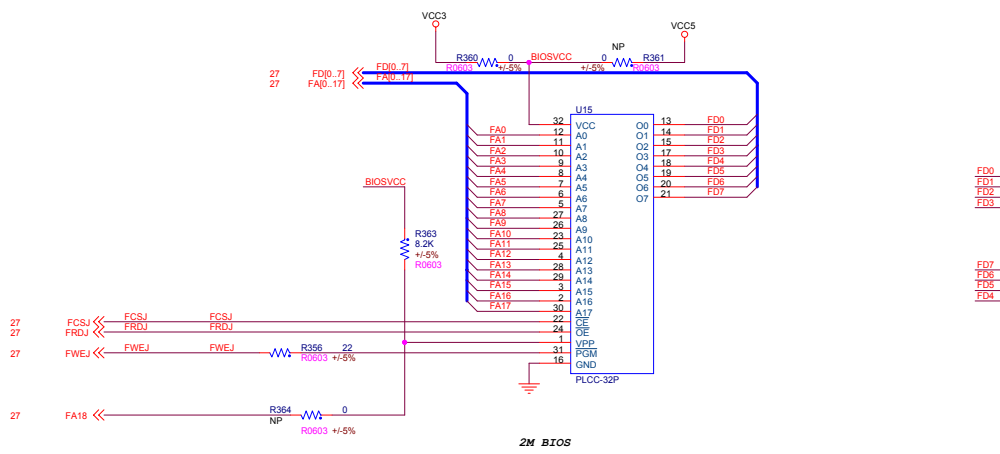


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Title <b>KEYBOARD MOUSE</b>		
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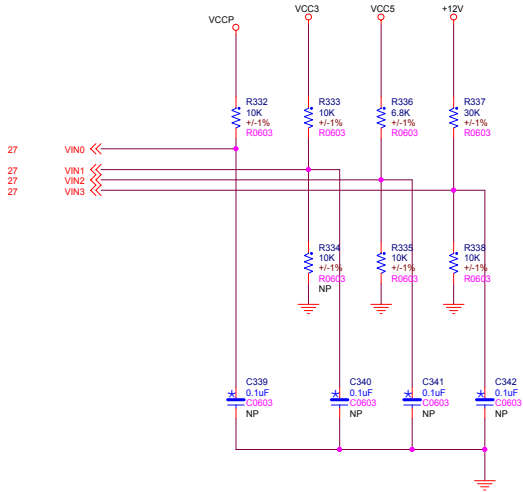


ISA INTERFACE ROM

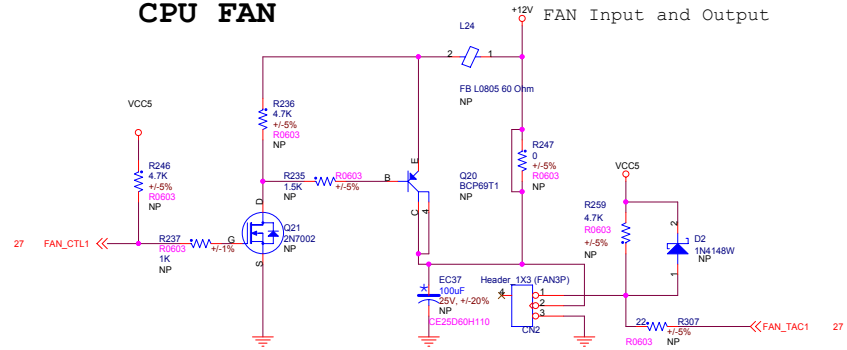


Title <b>BIOS/FLOPPY</b>		
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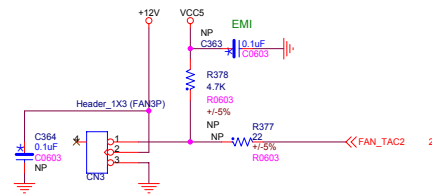
### Voltage Monitor



### CPU FAN

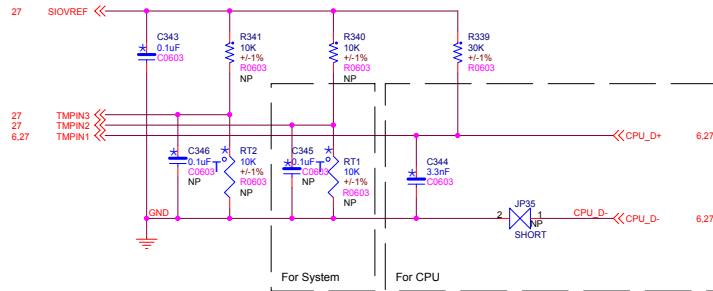


### SYSTEM FAN

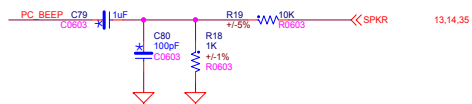
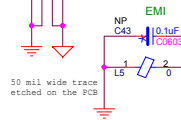
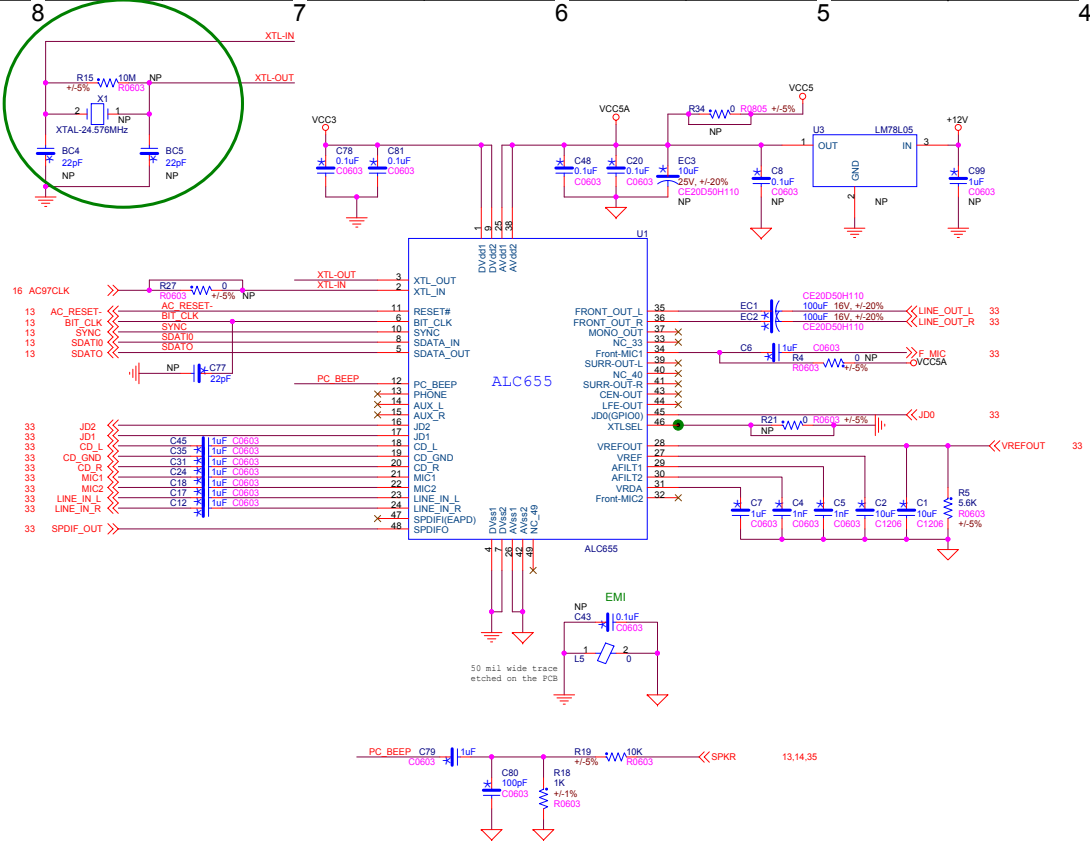


### Temperature Monitor

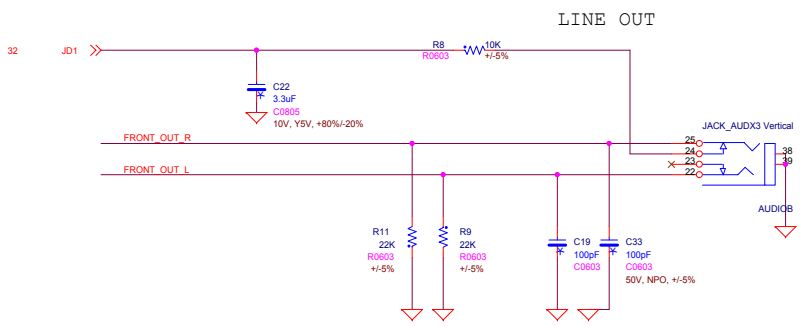
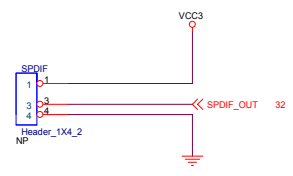
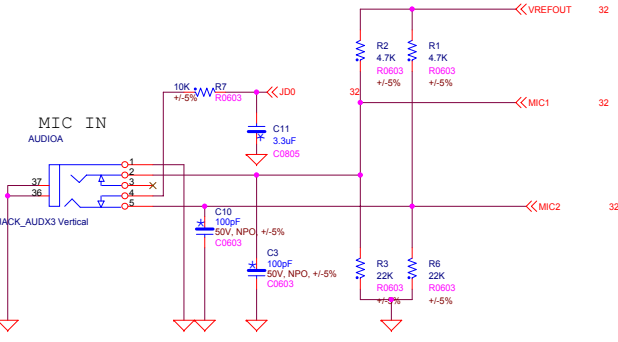
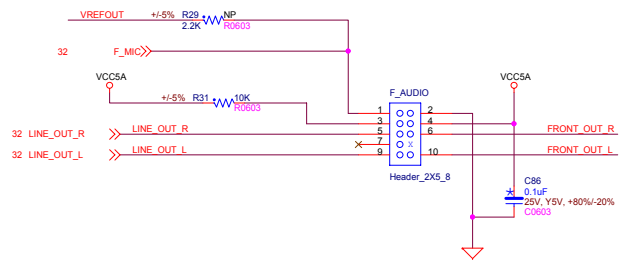
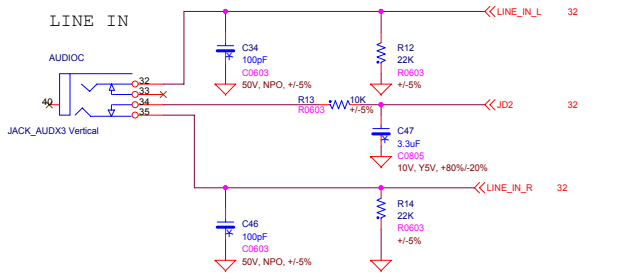
Choosing method of measuring temperature by either thermistor or diode

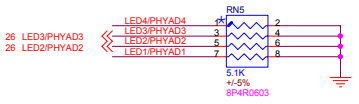
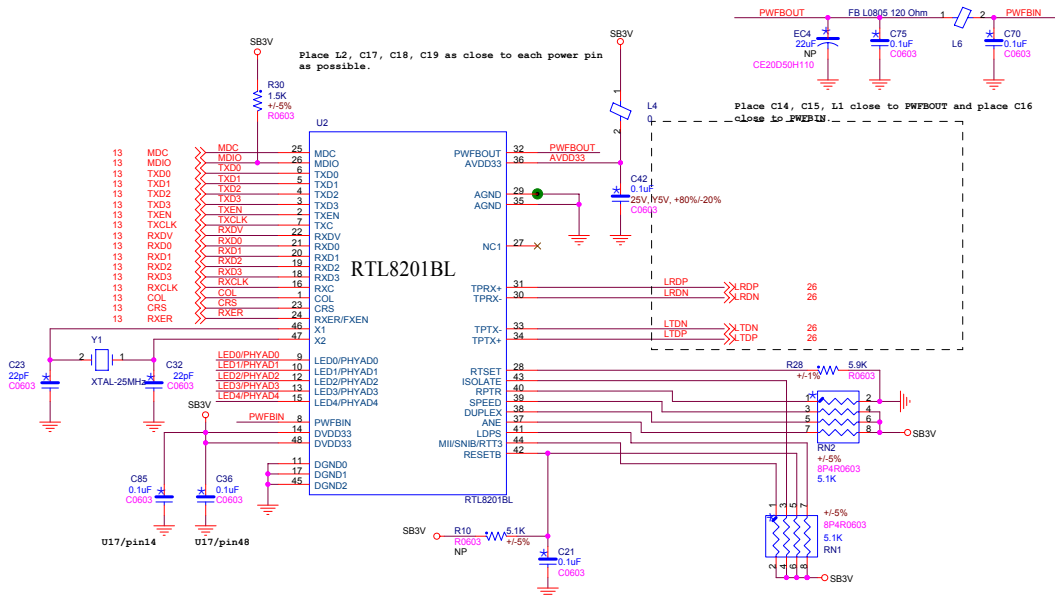


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26 LED0/PHYAD0 << LED0/PHYAD0 R20 SB3V  
5.1K R0803 +/-5%

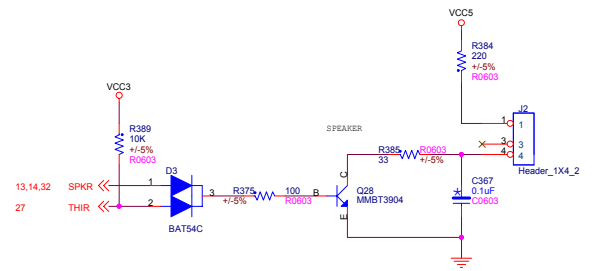
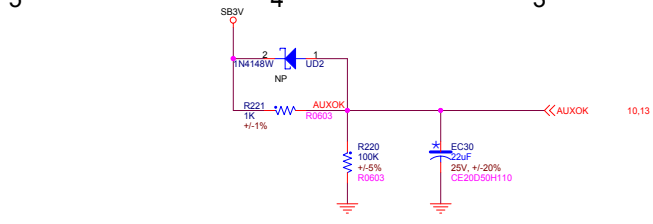
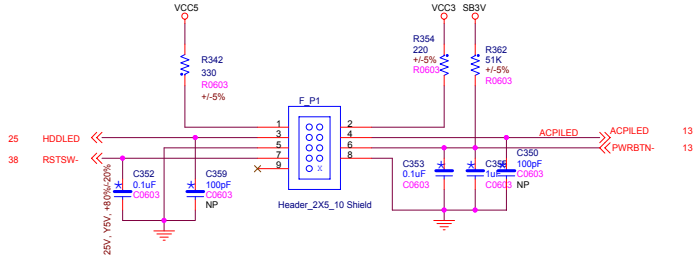
This schematic sets PHY address to 00001b.  
You could set PHY address from 00001b to 11111b.  
But the LED polarity must matches the respective  
PHYAD setting. Refer to datasheet's detailed  
description.

LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

**Hardware Configuration network:**

1. This configuration shows  
Enable: Auto negotiation, Full duplex, 100Mbps,  
Link Down Power Saving, MII interface  
Disable: Isolate, Repeater mode
2. These seven configuration pins could be connected to VDD or GND directly.

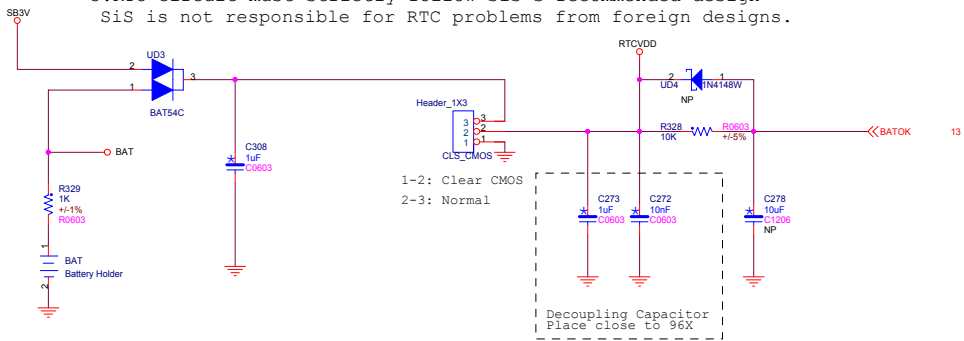




RTC

NOTE!

- 1.The RTCVDD is 3V
  - 2.Decoupling capacitor must be close to 96X RTCVDD pin.
  - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.



Header\_1X3  
3  
2  
1  
CLS\_CMOS

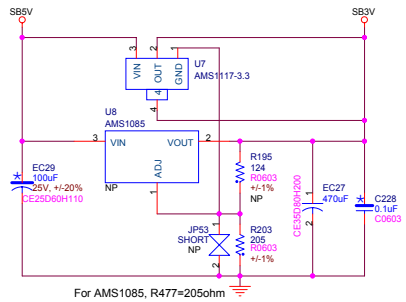
1-2: Clear CMOS  
2-3: Normal

Decoupling Capacitor  
Place close to 96X

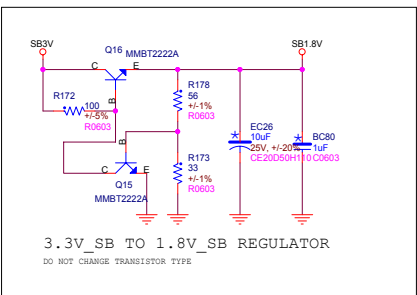


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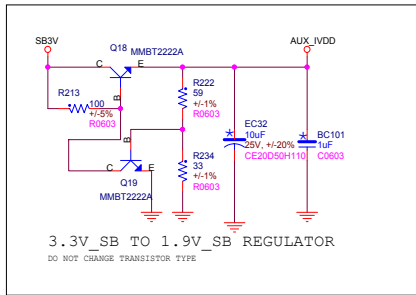
Title <b>POWER BTN/RTC Batt</b>		
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SB1.8V for 963  
for SB1.8V current 67mA (max)



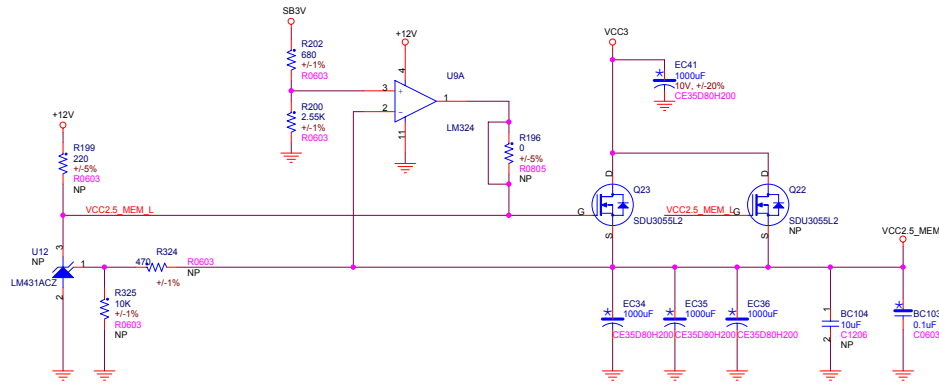
change the EC119 footprint from CE25D60 to CE20D50.



8 7 6 5 4 3 2 1

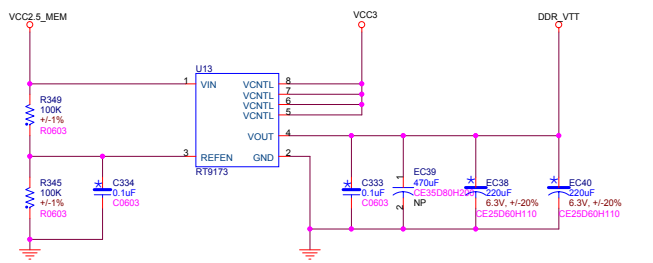
D

D



C

C



B

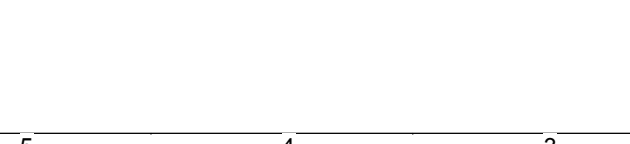
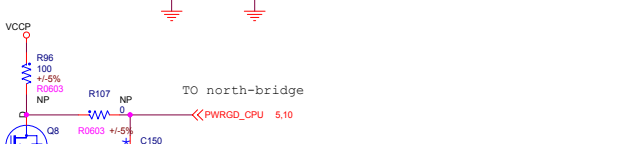
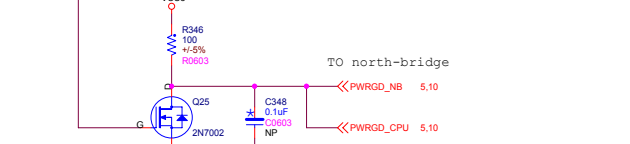
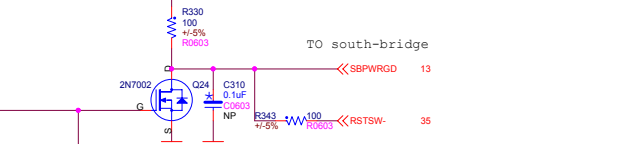
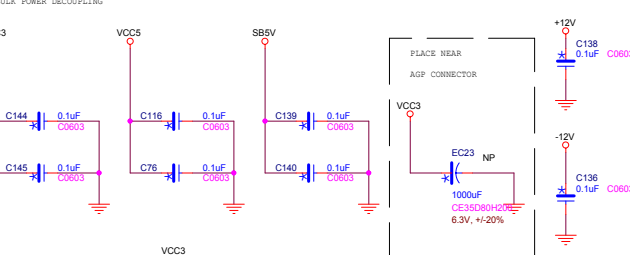
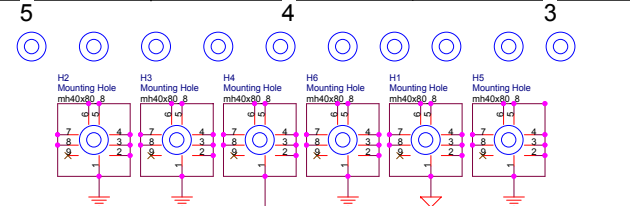
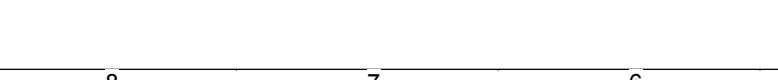
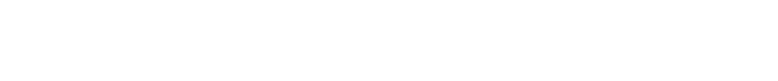
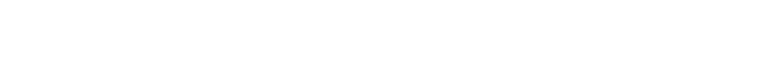
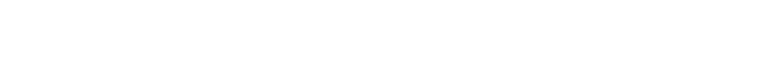
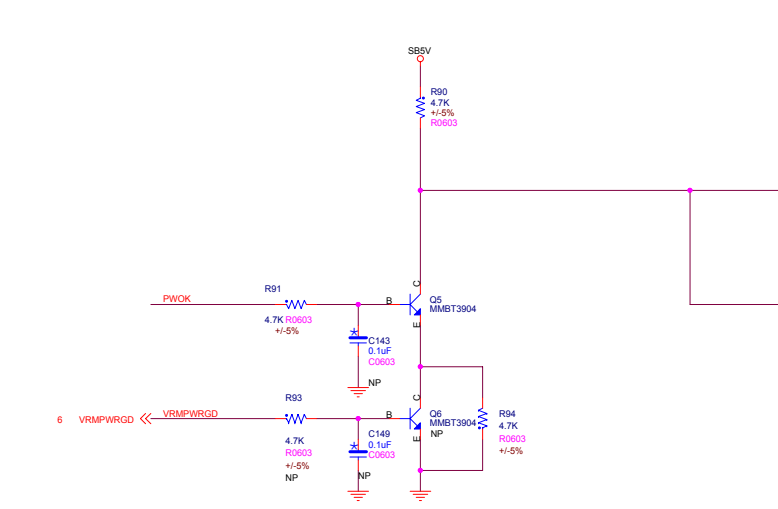
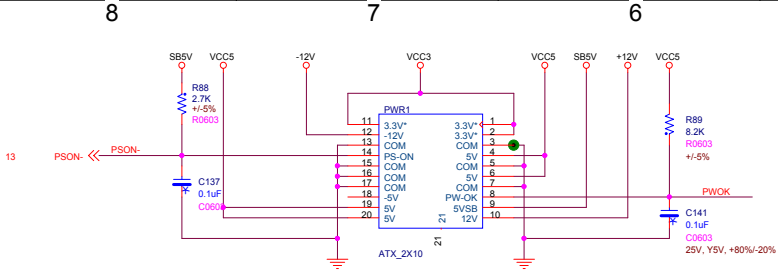
B

A

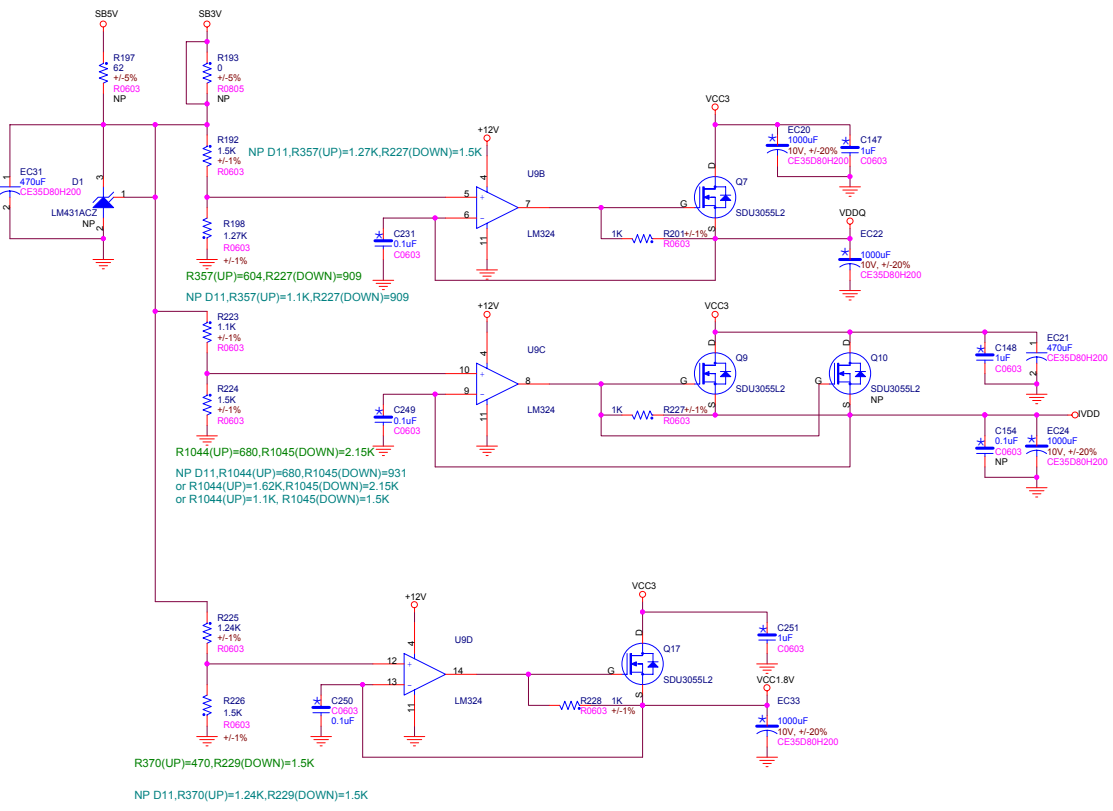
A



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4

3

2

1

D

D

C

C

B

B

A

A



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