

Foxconn Precision Co. Inc.

848M02 Schematic

Fab A

Date: 2004/6/25

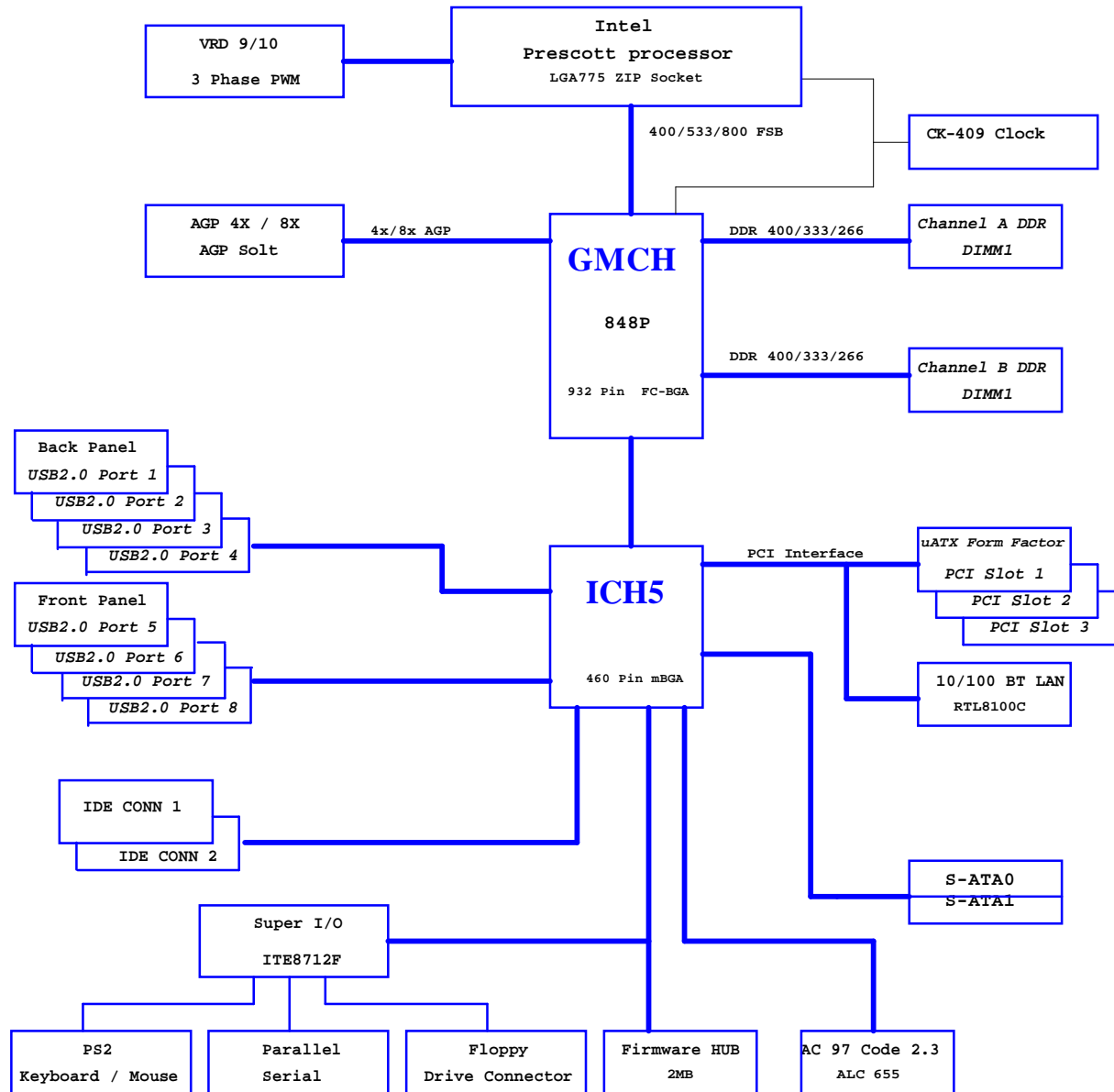
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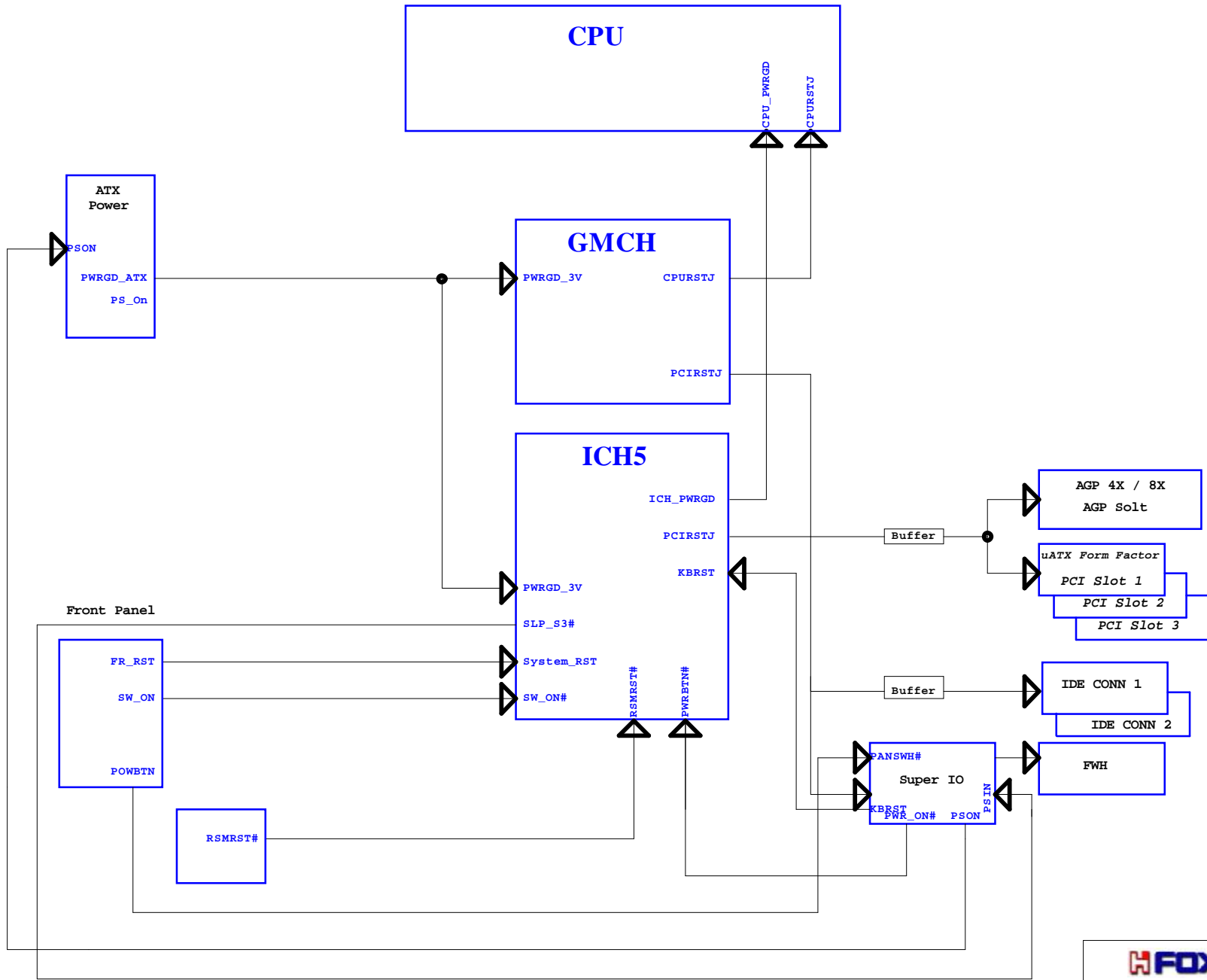
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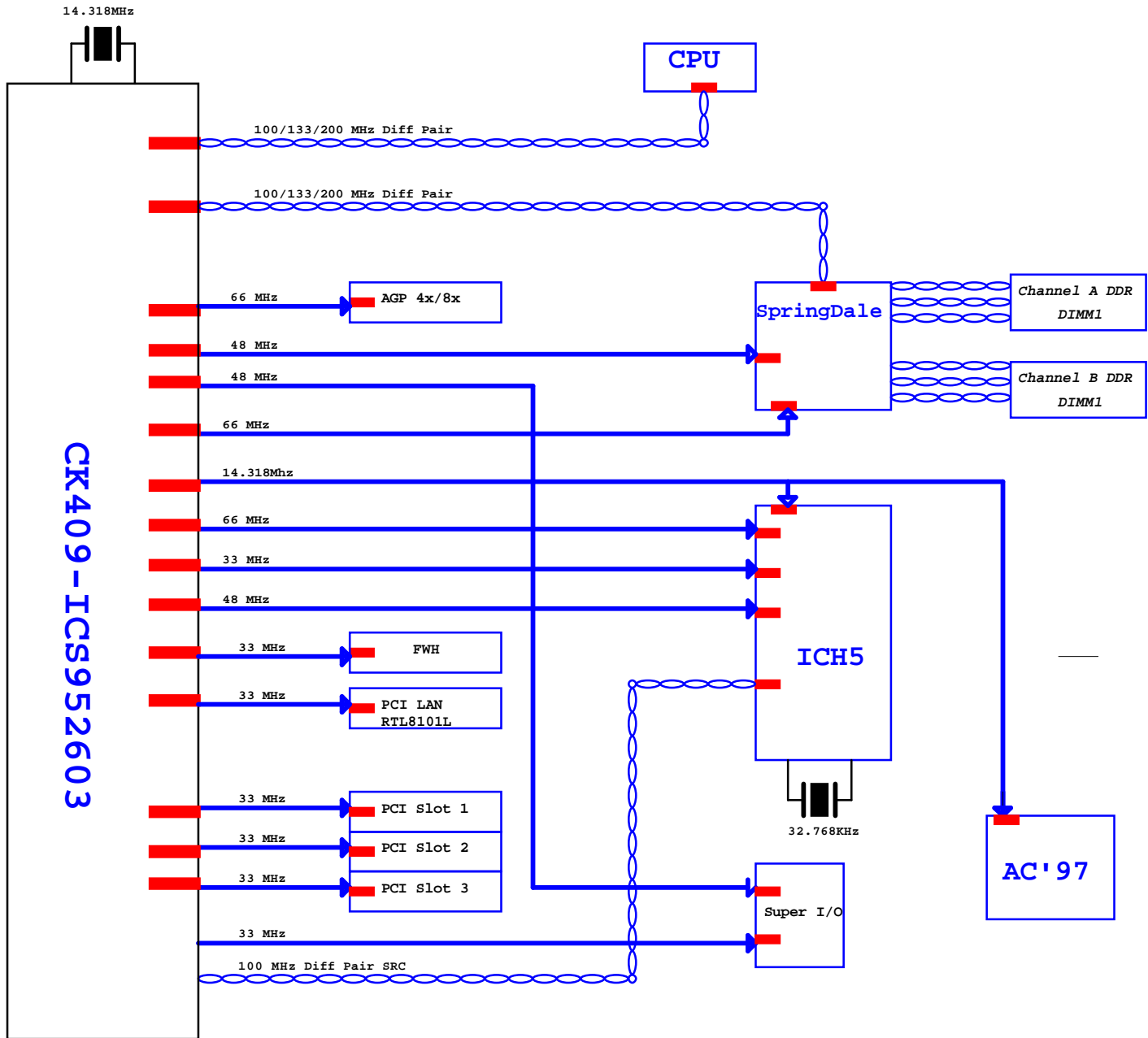


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Title: **Reset Map**

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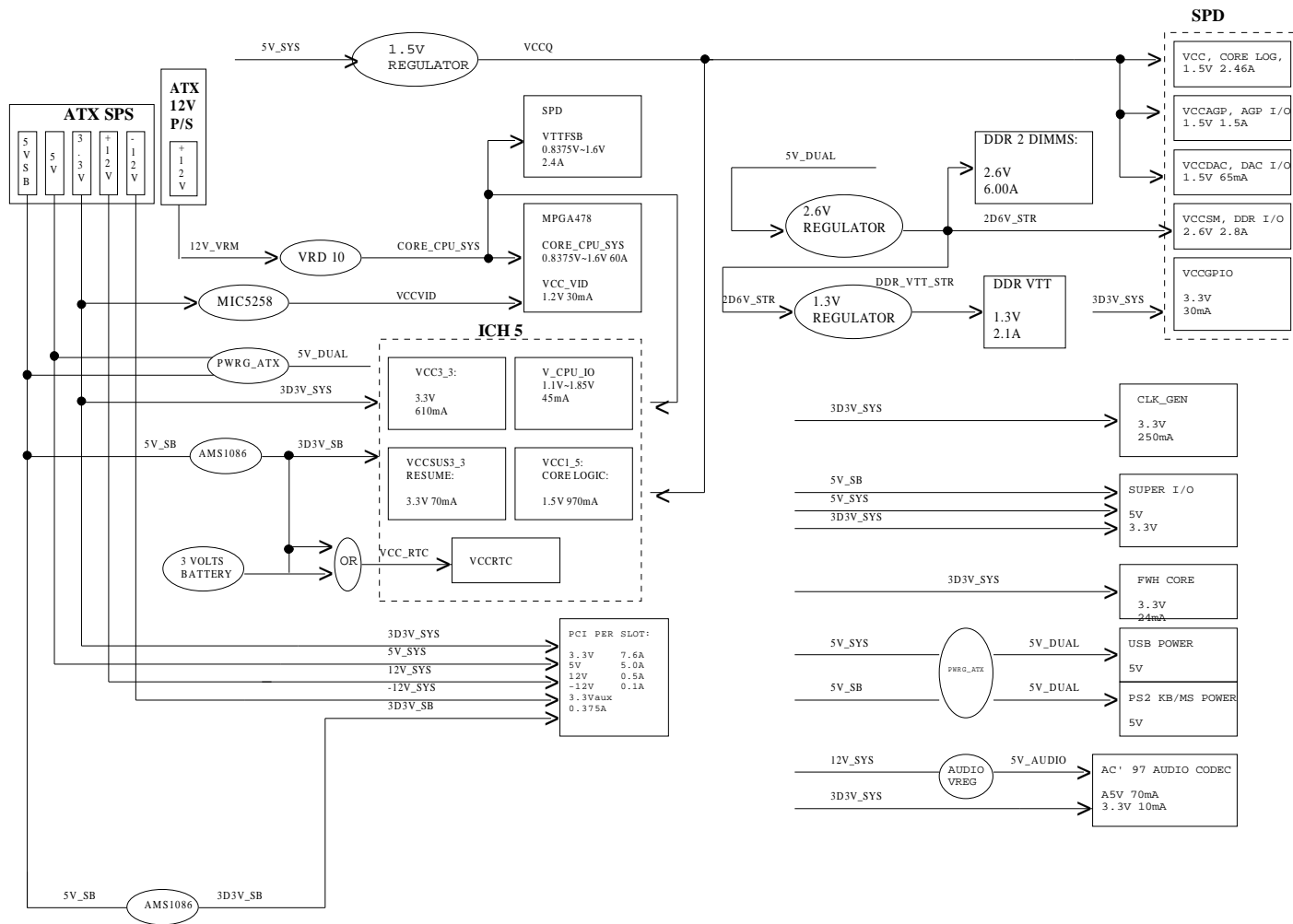


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Title: **Clock Distribution**

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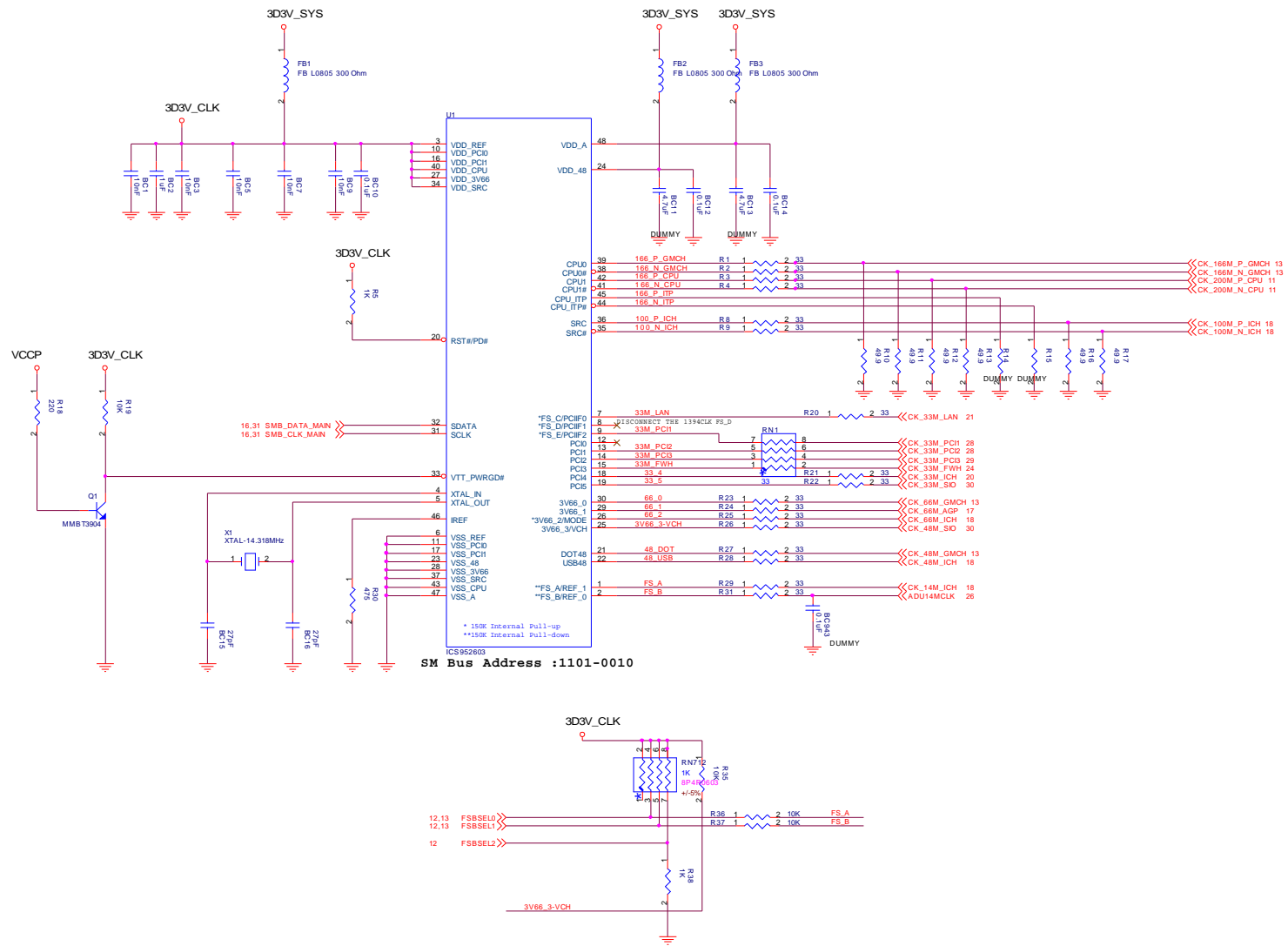


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Title: **Power Delivery Map**

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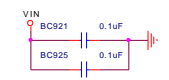
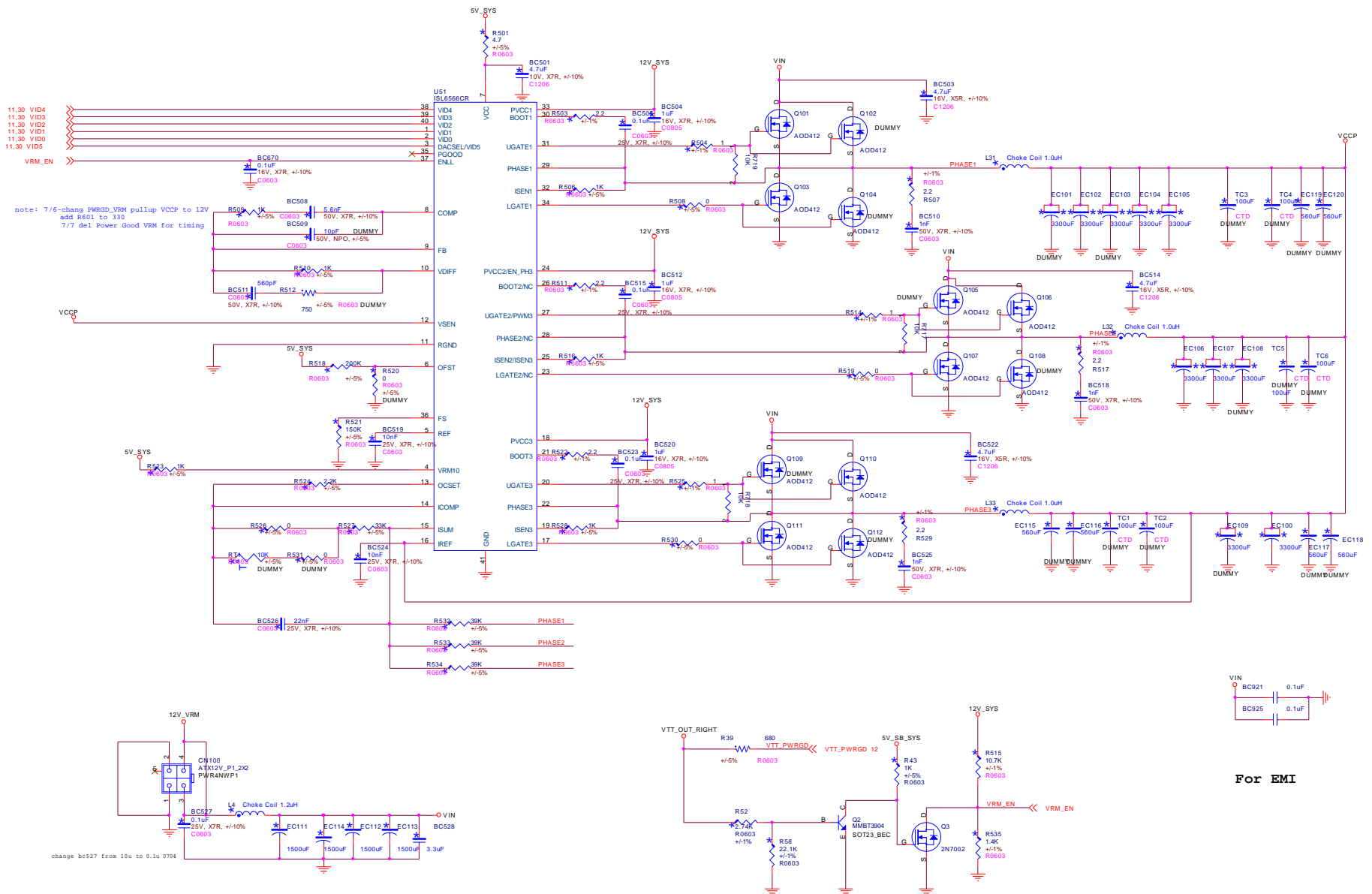
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File		Clock Generator CK-409	
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11.30 VID4
11.30 VID3
11.30 VID2
11.30 VID1
11.30 VID0
11.30 VID5

note: 7/6-chang PWRGD_VRM pullup VCCP to 12V
add R601 to 330
7/7 del Power Good VRM for timing



For EMI

change bc527 from 10u to 0.1u 0704

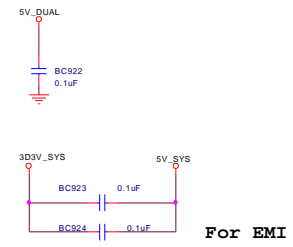
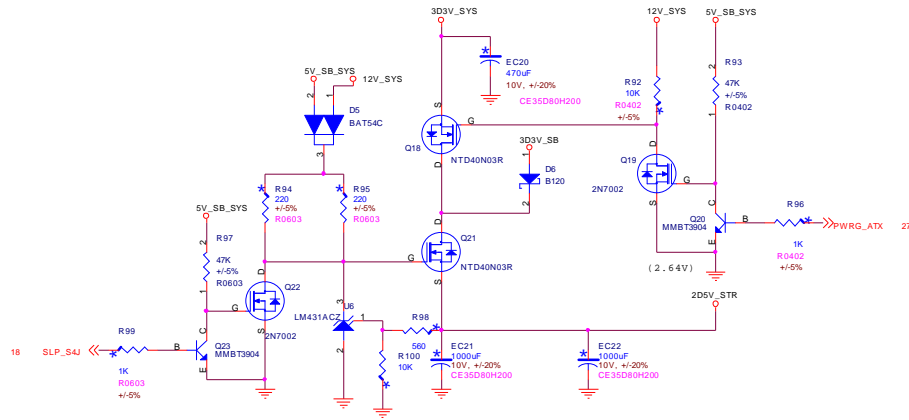
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Title: **VRD10.1**

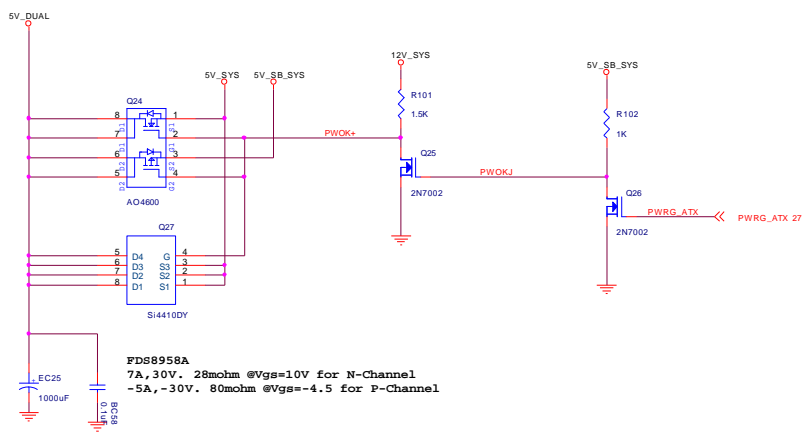
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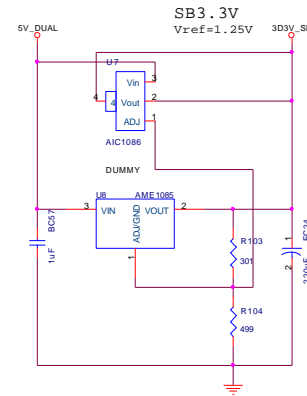
2D5V_STR Regulator



5V_DUAL Circuit



3D3V_SV Regulator



IF USE 1086 DUMMY R103 CHANGE THE R104 TO 0 OHM

$$V_{out} = V_{ref}(1 + R2/R1) + I_{adj}R2$$

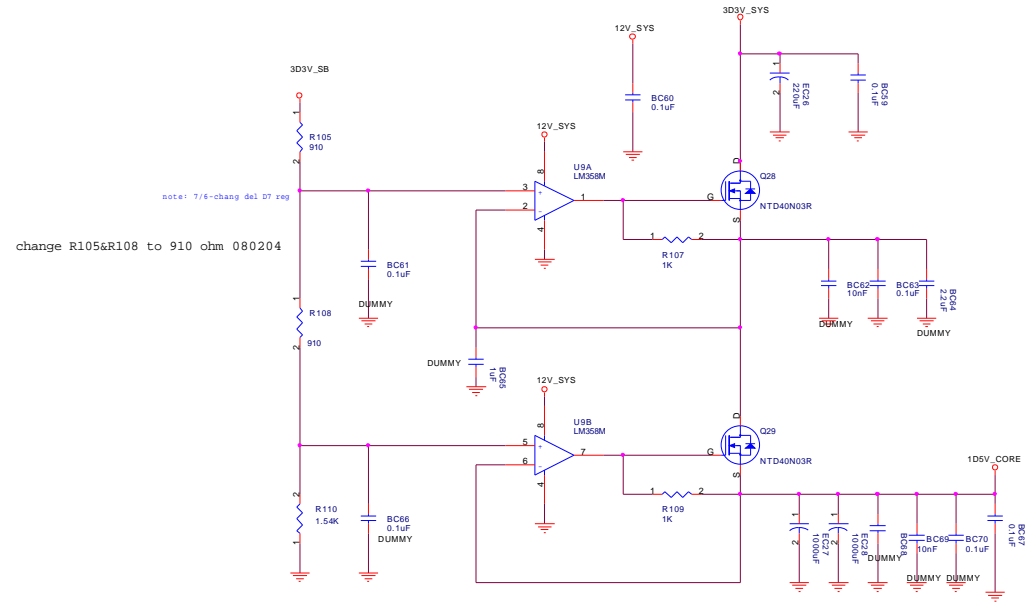
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V




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Title		Power 2.5V-5VDUAL-3.3SB	
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1D5V_CORE Regulator



PROCHOTJ Signal

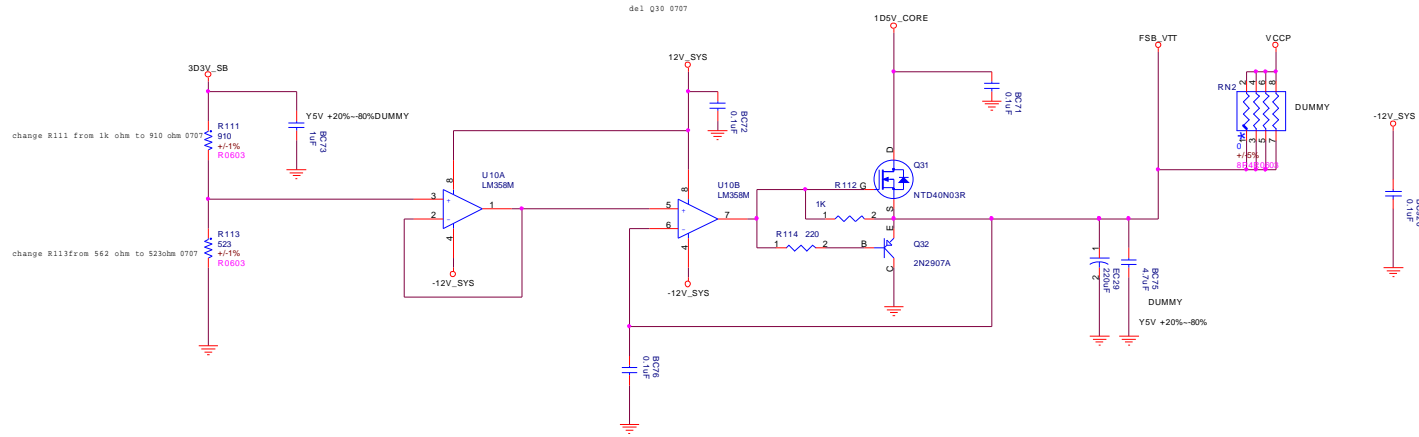
	
FOXCONN PCEG	
Title Power 1.5V	
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FSB_VTT Regulator

PSC=1.2V

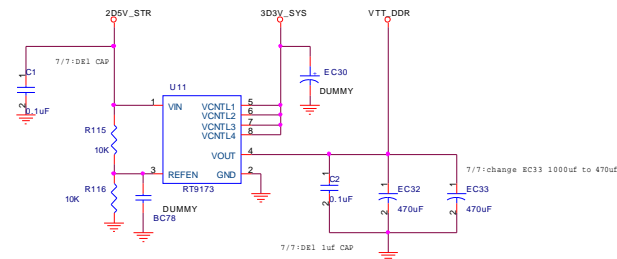
GMCH VTT Source 1.6A and Sink 600mA


change Q30 2M3904 to MMBT3904 FOR FOOTPRINT 0705

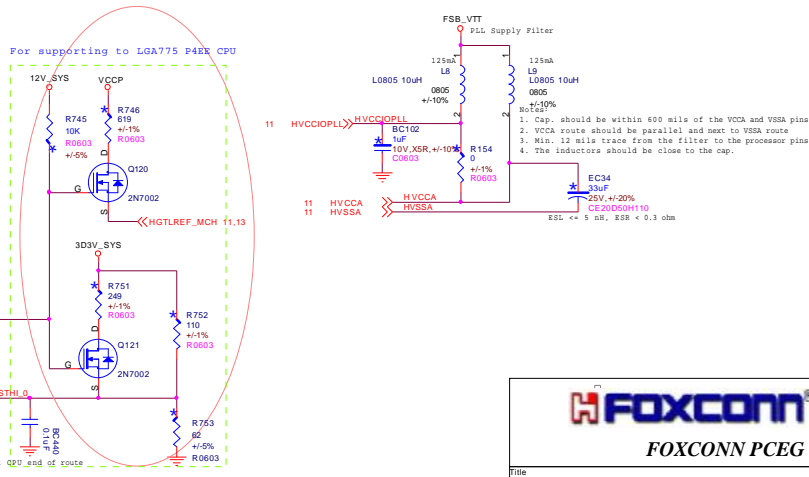
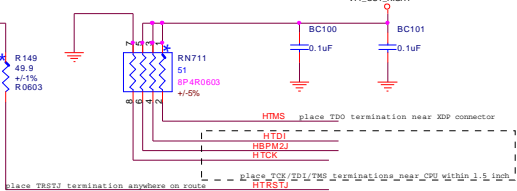
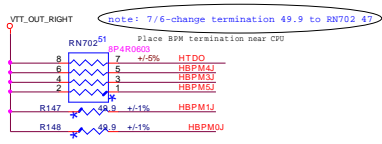
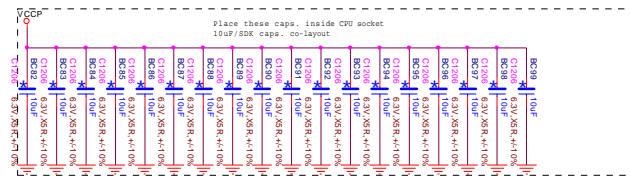
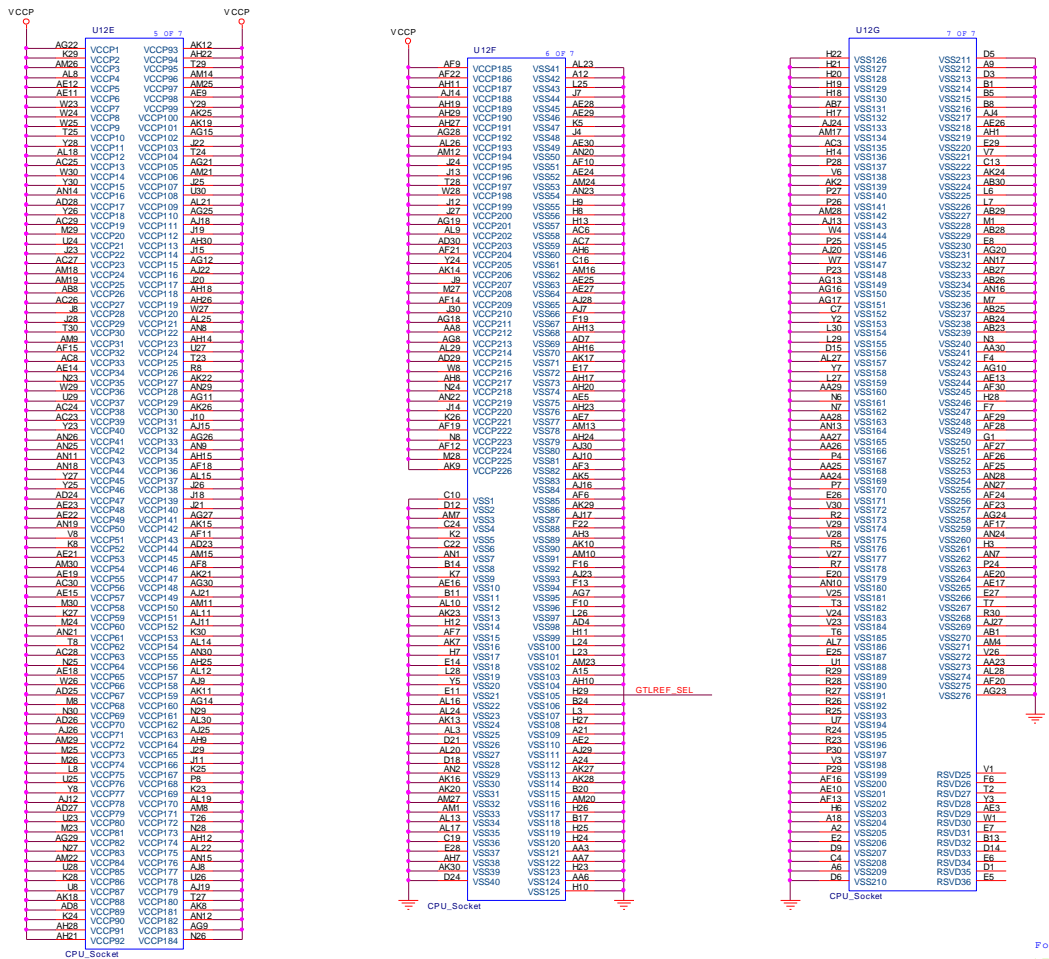


VTT_DDR Regulator

DEL THE BOOTSELECT CIRCUIT FOR ADAPTING TO THE 775CPU DESIGNGUIDE 0705



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Power 1.25V-GMCH VTT	
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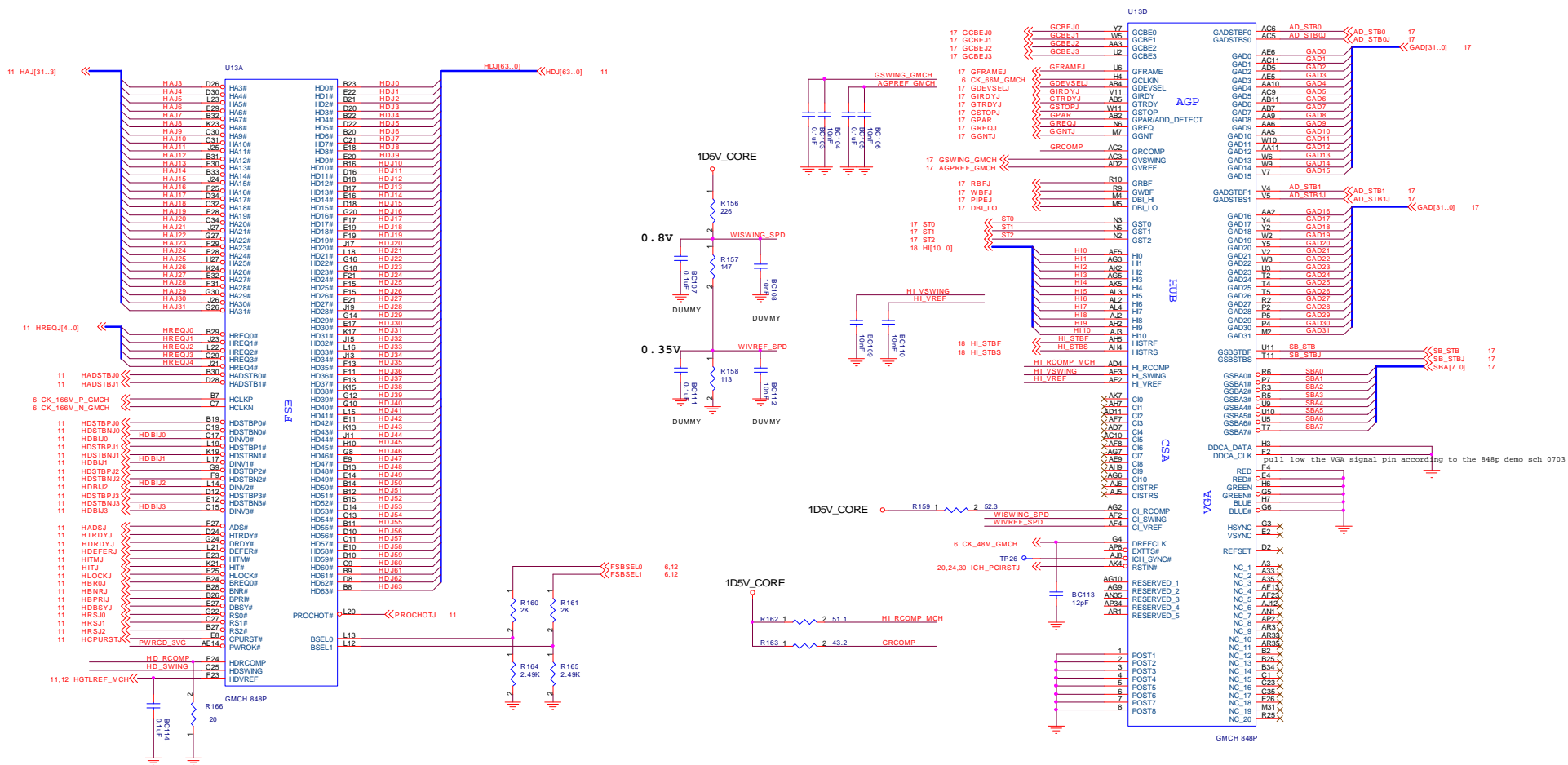


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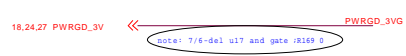
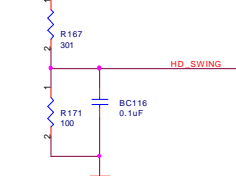
File: **LGA775-2**

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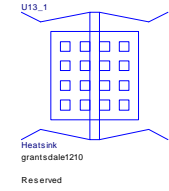


Ver A to Ver B RD_SMI32 update GMCH_VTT replace with VCCP
 18.2427 PWRGD_3V
 note: 7/6-del u17 and gate r169 0



Pin Name	Pin #	Decoupling cap
VTTFSB	A15	0.22uF
VTTFSB	A21	0.47uF
VCC_DDR	E35	0.47uF
VCC_DDR	R35	0.22uF
VCCA_DDR	AL35	0.1uF
VCCA_DDR	AA35	0.1uF
VCC_DDR	AR31	0.1uF
VCC_DDR	AR21	0.22uF
VCC_DDR	AR15	0.1uF
VCC_AGP	AG1	0.1uF
VCC_AGP	Y1	0.1uF

BaseOn Intel WN29 Update

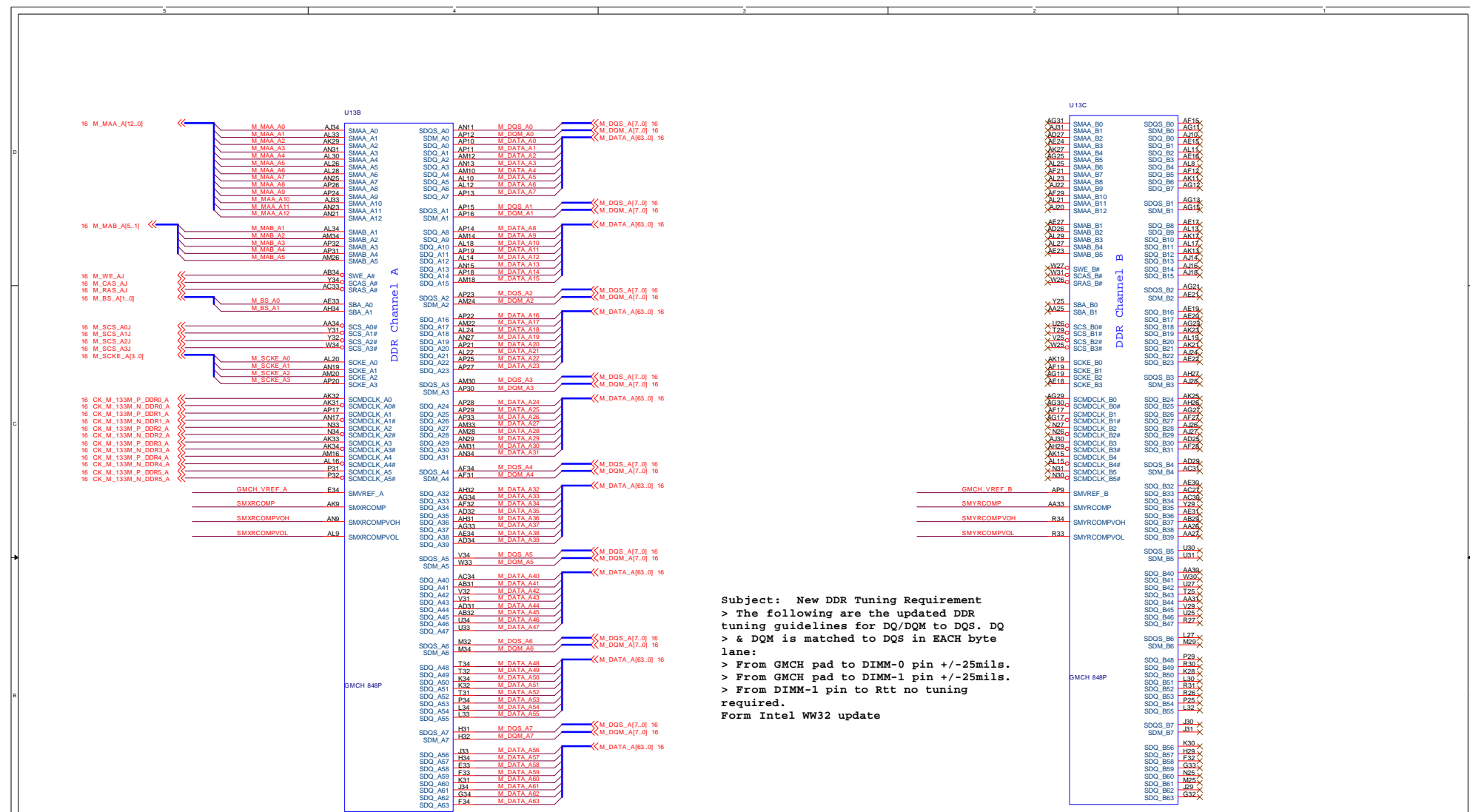


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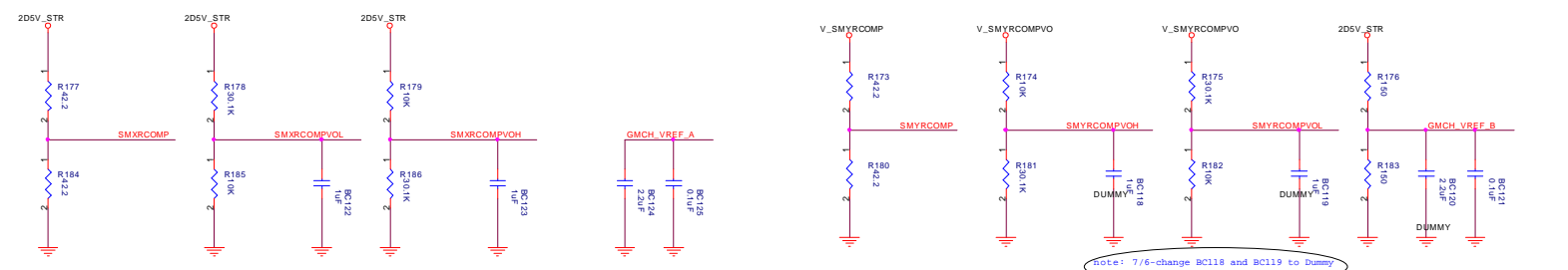
GMCH-1

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Subject: New DDR Tuning Requirement
 > The following are the updated DDR tuning guidelines for DQ/DQM to DQS. DQ > & DQM is matched to DQS in EACH byte lane:
 > From GMCH pad to DIMM-0 pin +/-25mils.
 > From GMCH pad to DIMM-1 pin +/-25mils.
 > From DIMM-1 pin to Rtt no tuning required.
 Form Intel WW32 update

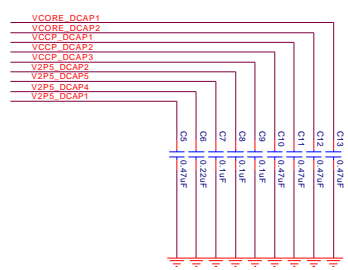
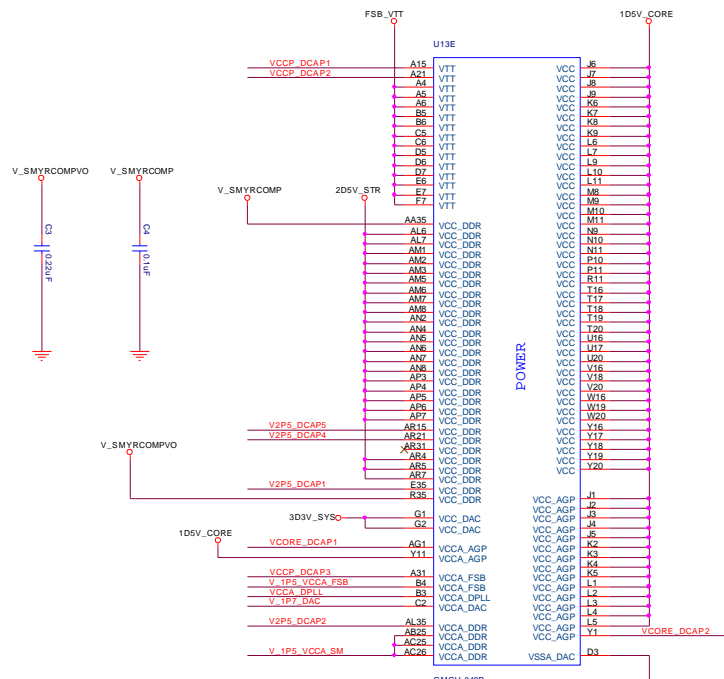


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GMCH-2

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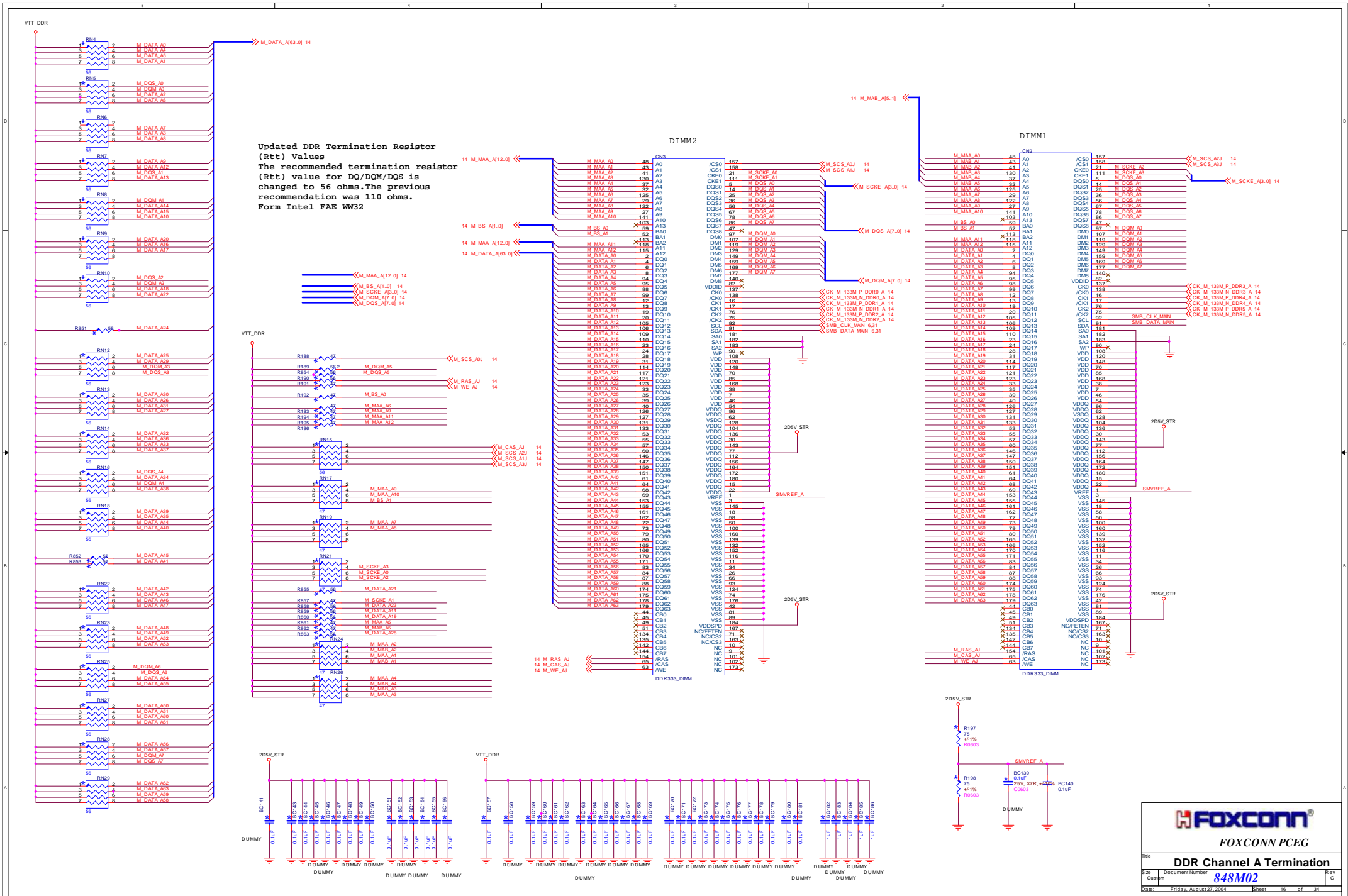


Subject: GMCH Vtt Clarification
 The GMCH VTT regulator is required to be capable of sinking 600mA of current in addition to sourcing 1.6A of current in normal operation. Sinking 600mA of current is a new requirement for the Springdale platform regardless if a Northwood or Prescott processor is installed. The reason why the GMCH VTT VR must be able to sink 600mA is because there will be times when the GMCH VTT VR's output will be set to a voltage lower than the VRD 10's output. The difference in voltage will cause current to be driven from the VRD to the GMCH VTT regulator. If the GMCH VTT VR doesn't have the capability to sink the current, damage to the GMCH can occur. In order to meet this requirement, Intel is using a P-FET in an SOT-23 footprint on the GMCH VTT voltage regulator. The back driven current will be sunk into the ground plane through this P-FET without causing damage to the Springdale GMCH. Update from Intel WW34 MOV

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Updated DDR Termination Resistor (Rtt) Values
The recommended termination resistor (Rtt) value for DQ/DQM/DQS is changed to 56 ohms. The previous recommendation was 110 ohms.
Form Interm FAE WW32

VTT_DDR


25V_STR

DIMM2

DDR333_DIMM

DIMM1

DDR333_DIMM

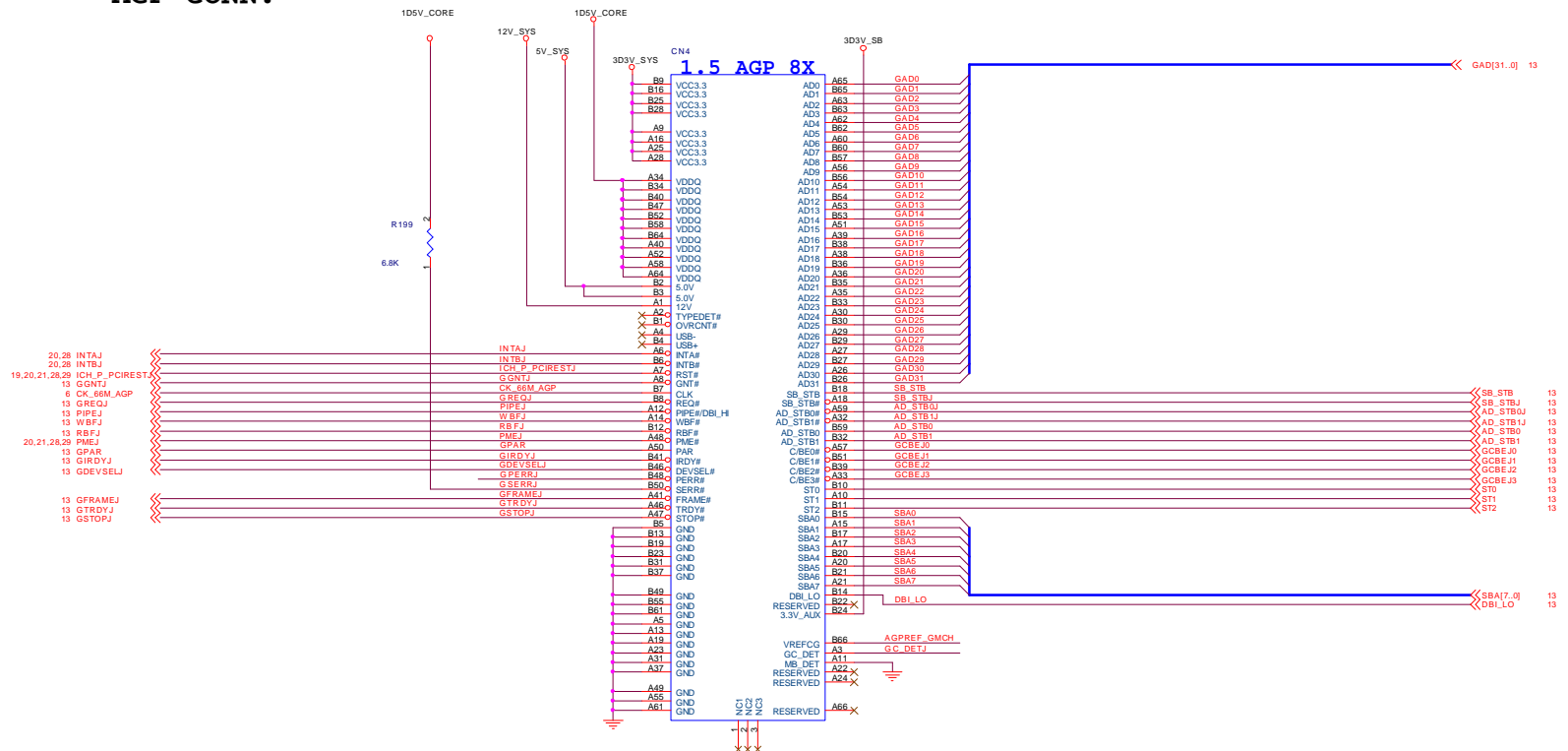


DDR Channel A Termination

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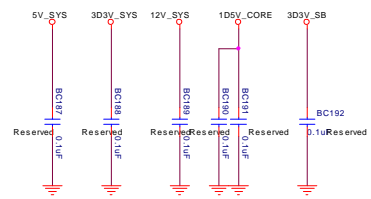
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AGP CONN.

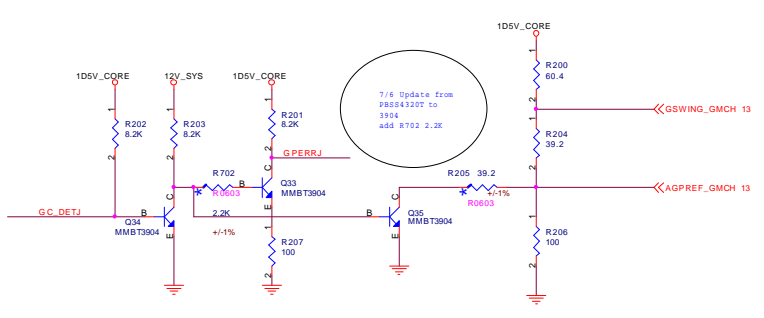


Reserved

DECUBLE CAP.



AGPREF & AGPSWING CIRCUIT



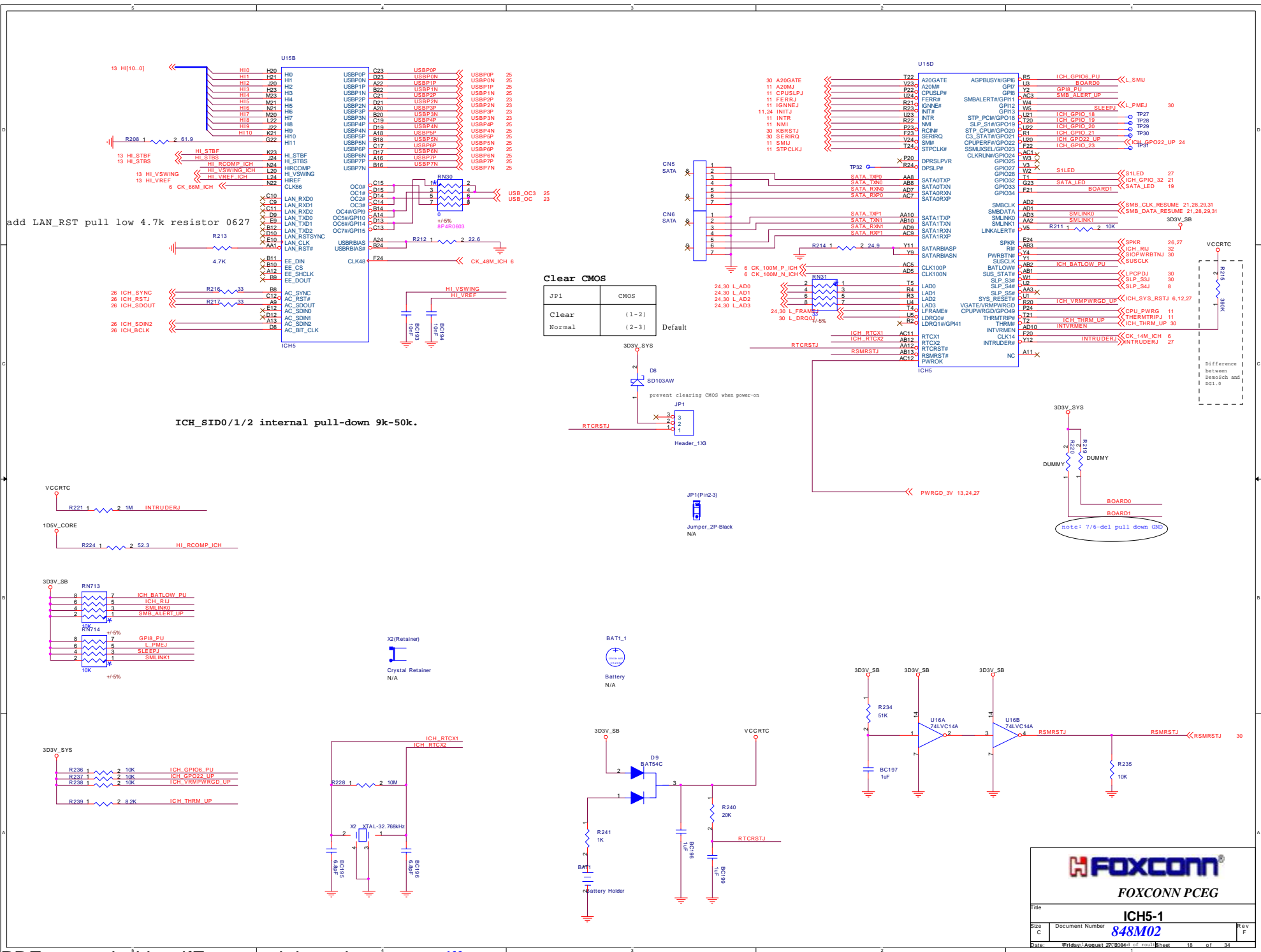
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AGP Connector

848M02

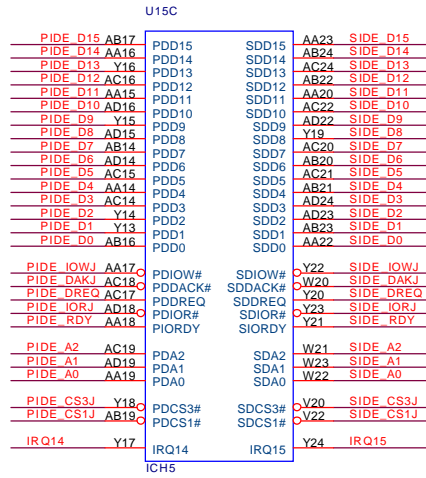
Rev F

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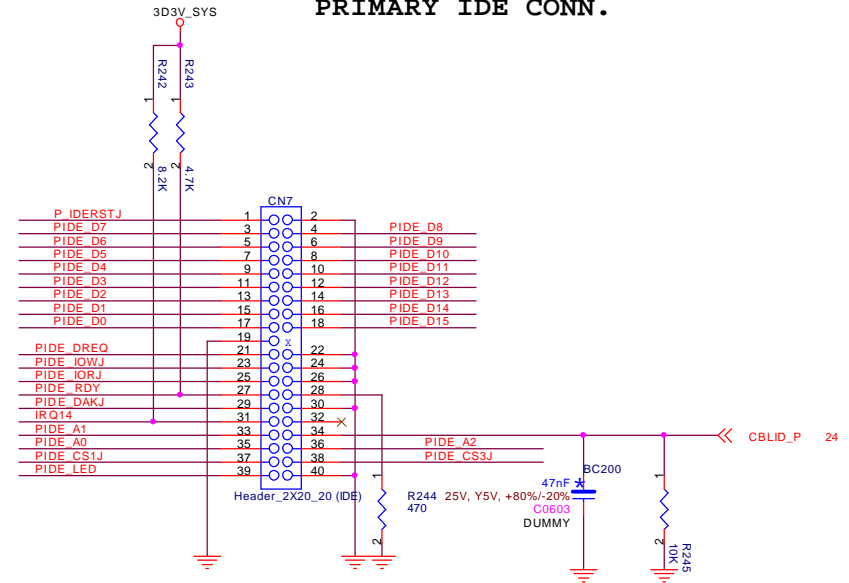


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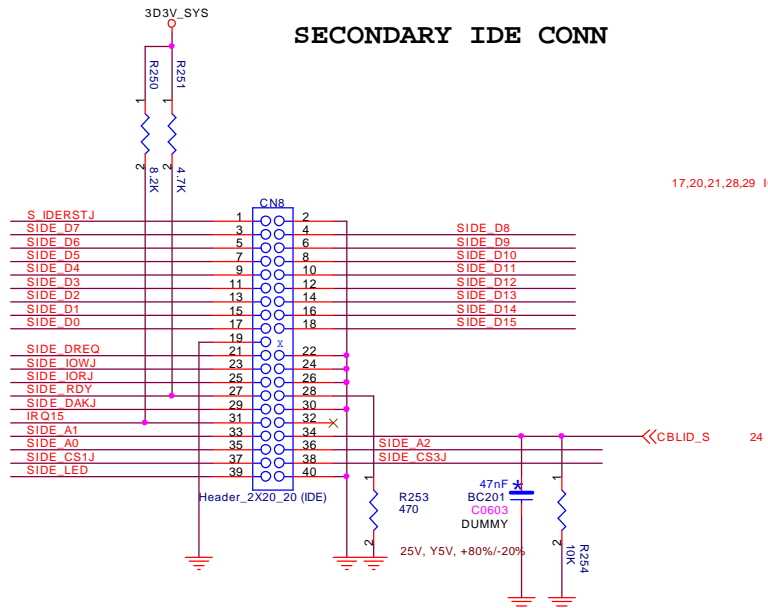
ICH5 IDE INTERFACE



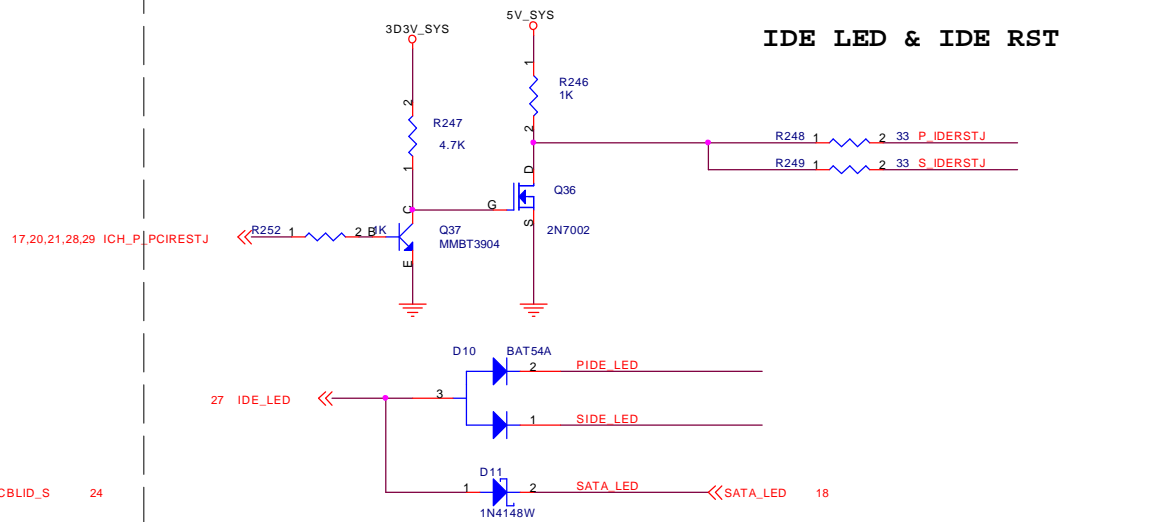
PRIMARY IDE CONN.



SECONDARY IDE CONN



IDE LED & IDE RST

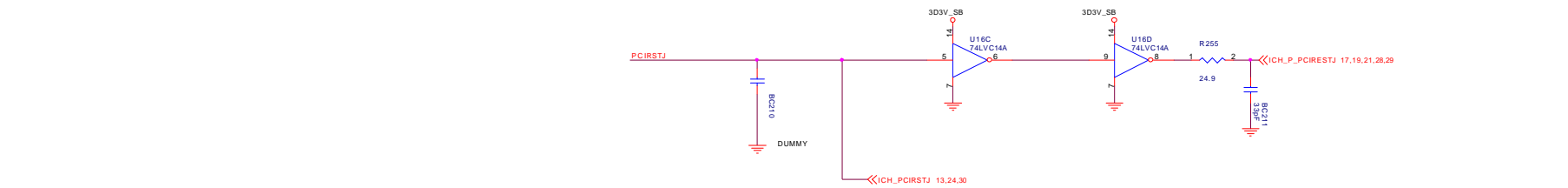
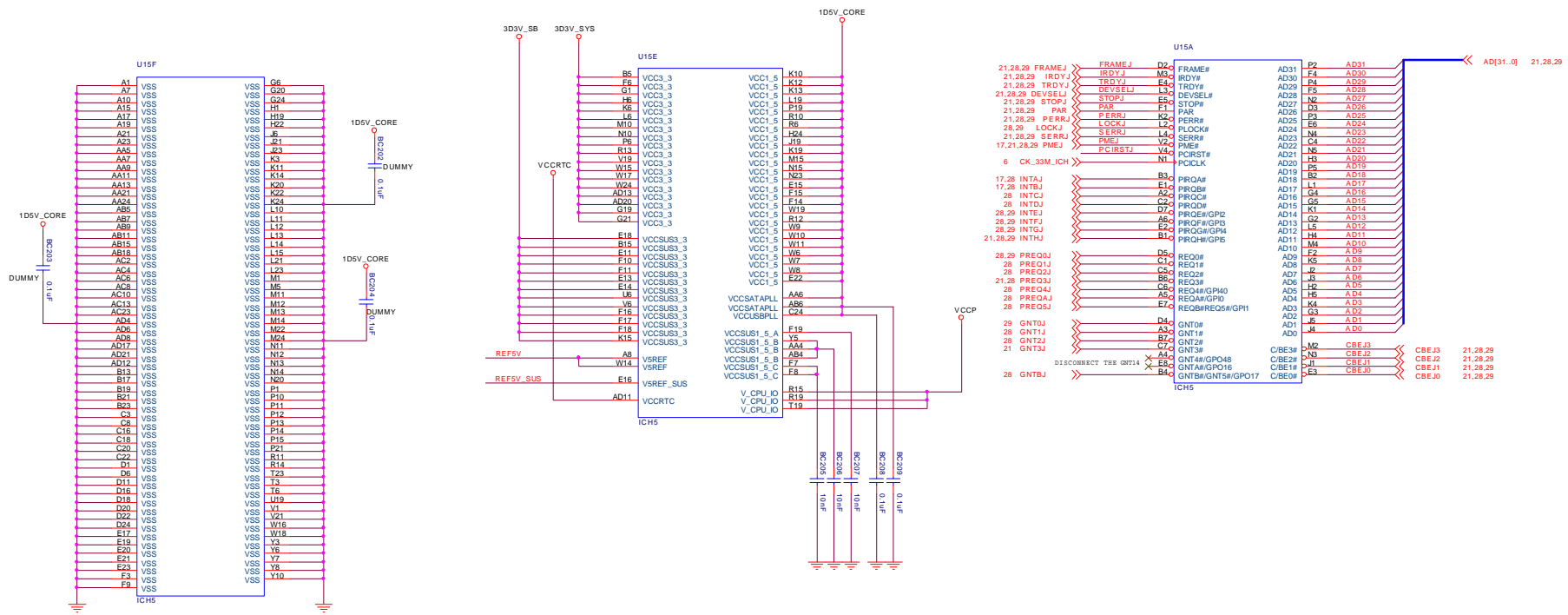


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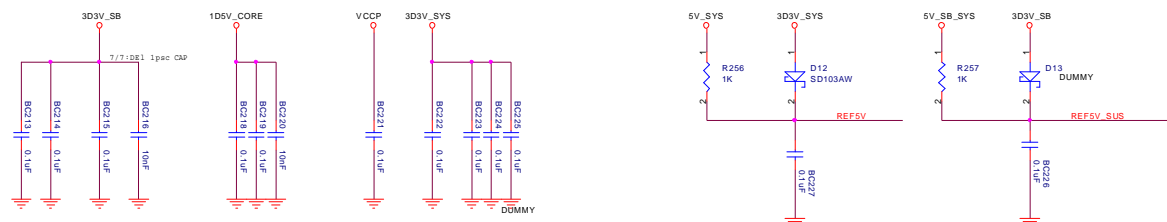
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ICH5-2 IDE Connectors

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There are component place on solid site

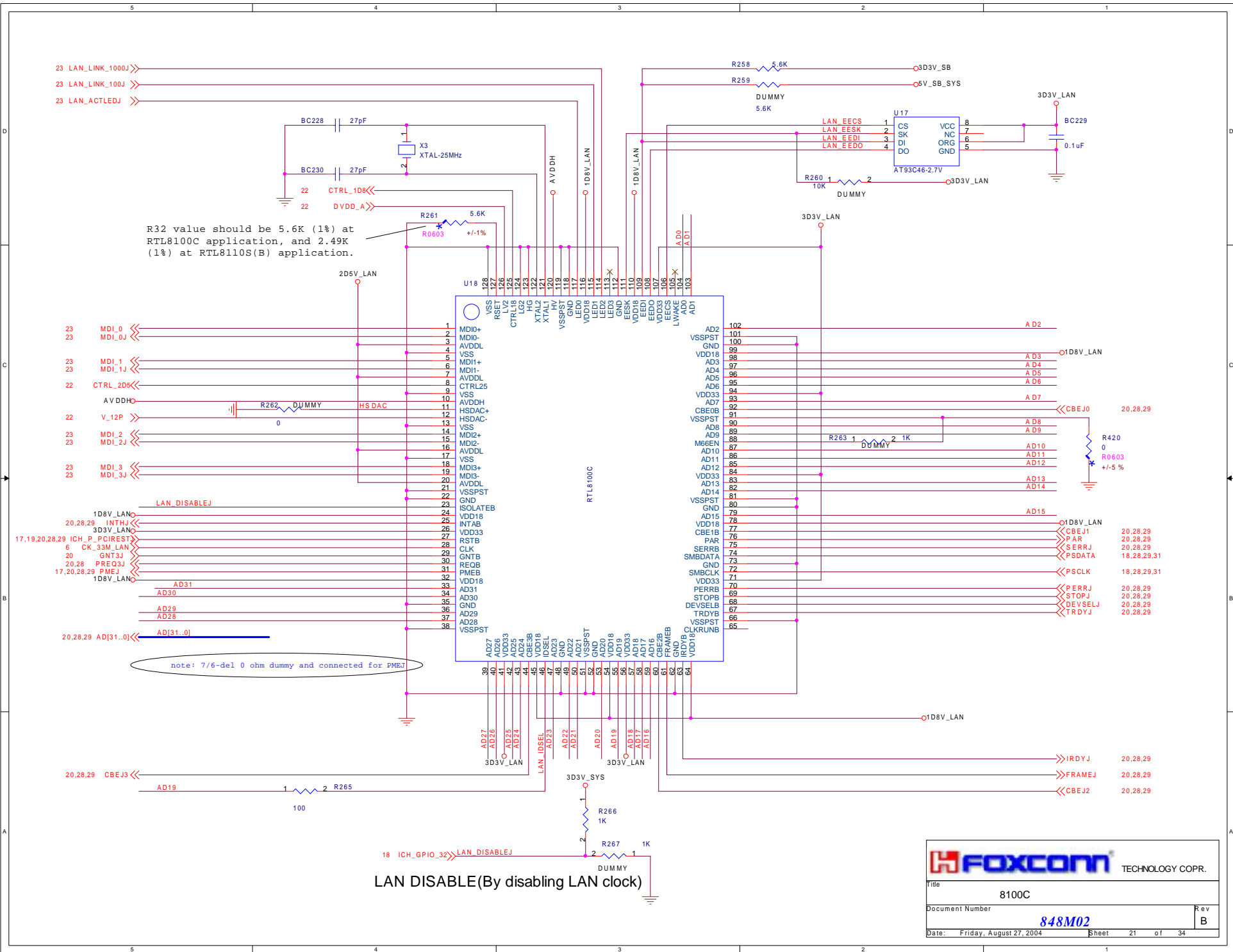


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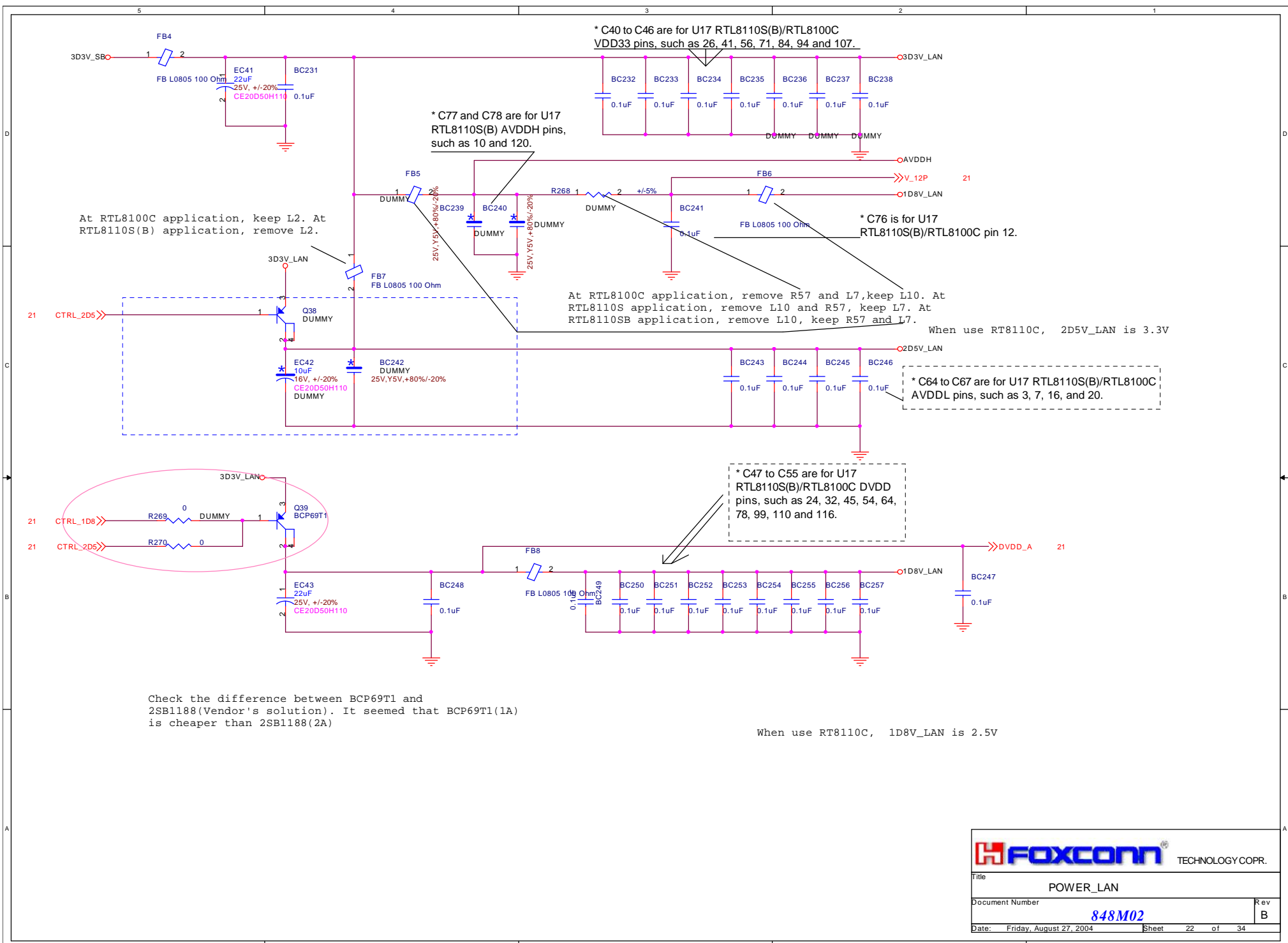
FOXCONN TECHNOLOGY COPR.

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Rev B



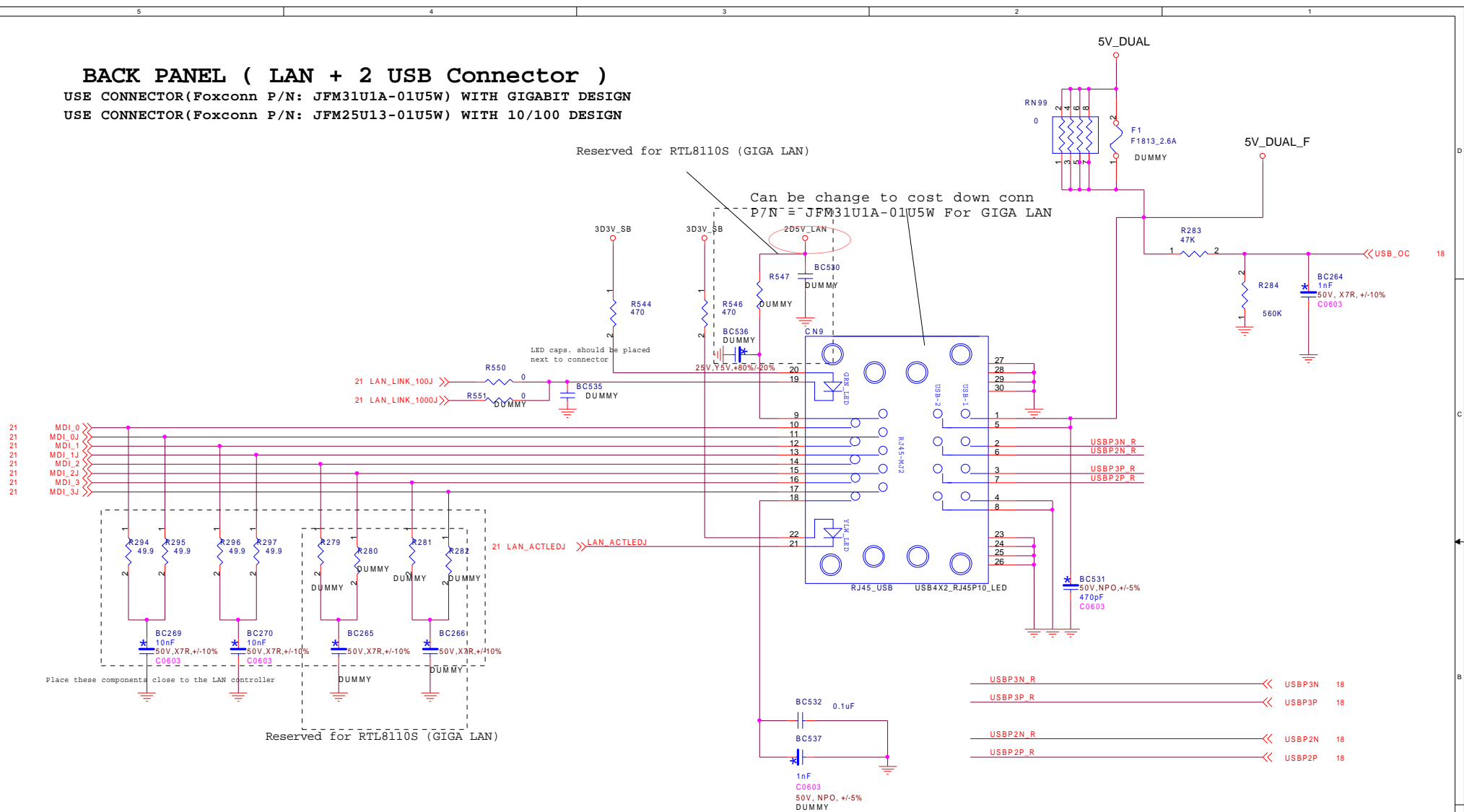
BACK PANEL (LAN + 2 USB Connector)


USE CONNECTOR (Foxconn P/N: JFM31U1A-01U5W) WITH GIGABIT DESIGN

USE CONNECTOR (Foxconn P/N: JFM25U13-01U5W) WITH 10/100 DESIGN

Reserved for RTL8110S (GIGA LAN)

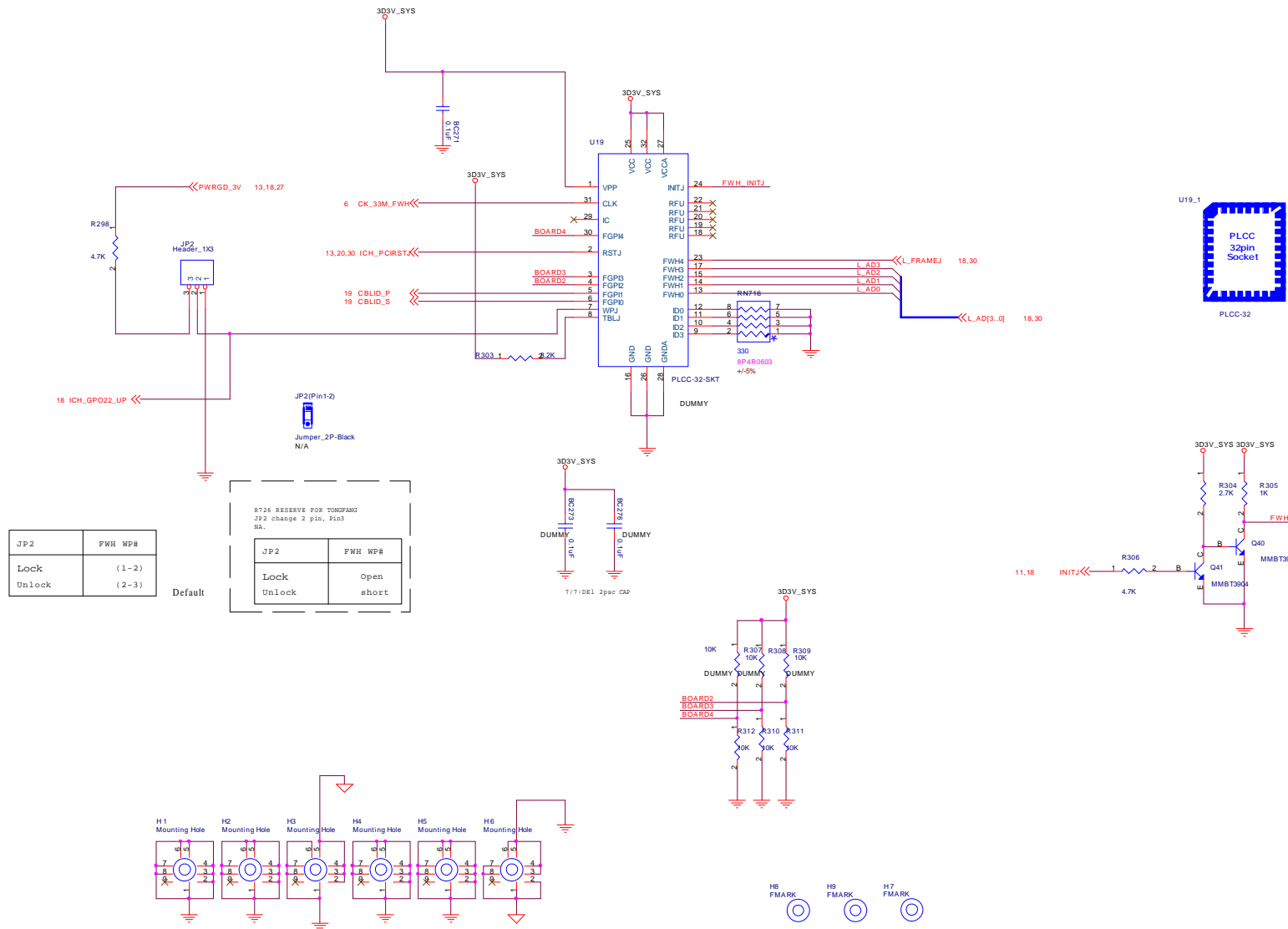
Can be change to cost down conn
P/N = JFM31U1A-01U5W For GIGA LAN



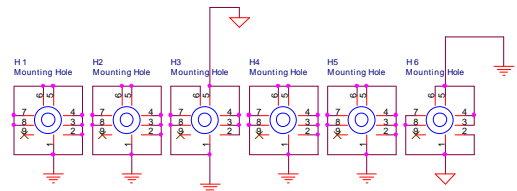
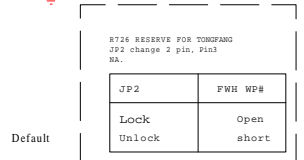


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Title		
LAN Connectors		
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JP2	FWH WP#
Lock	(1-2)
Unlock	(2-3)



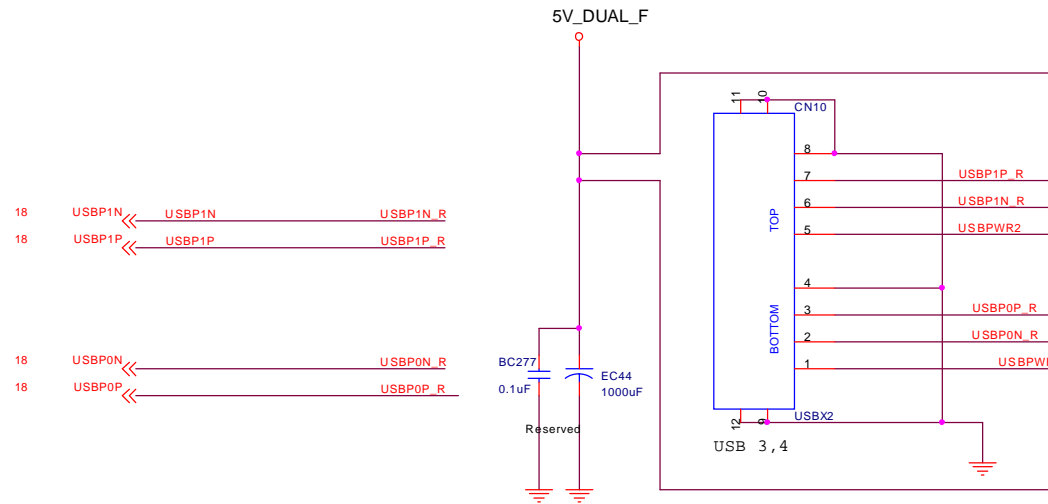
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Title: **FWH**

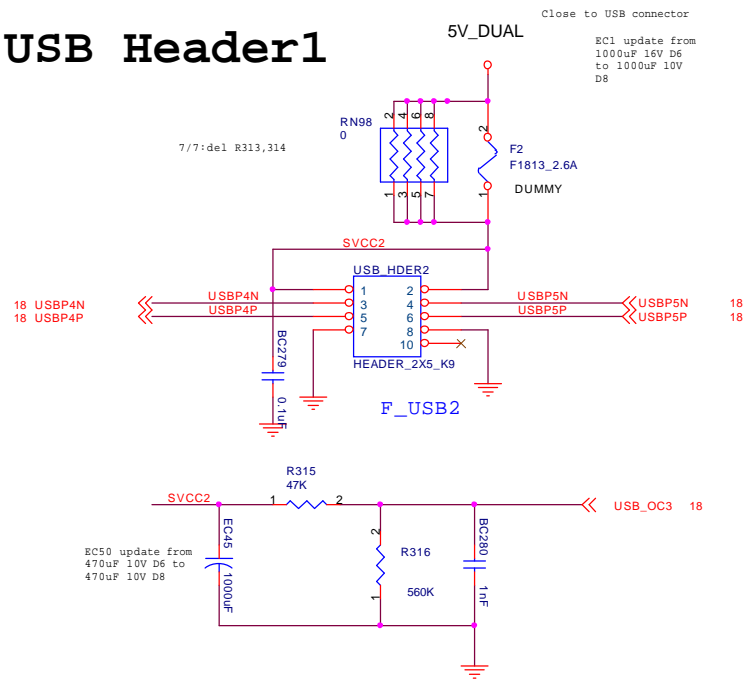
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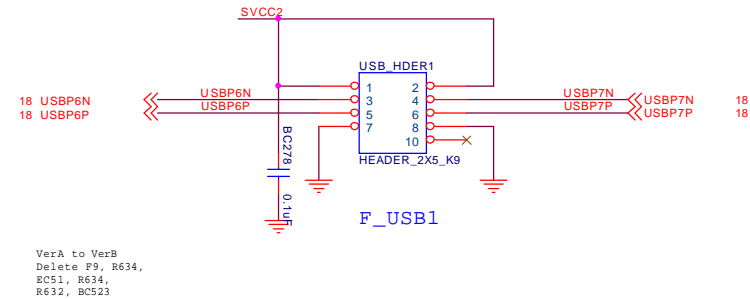
Rear Dual USB Connector



USB Header1

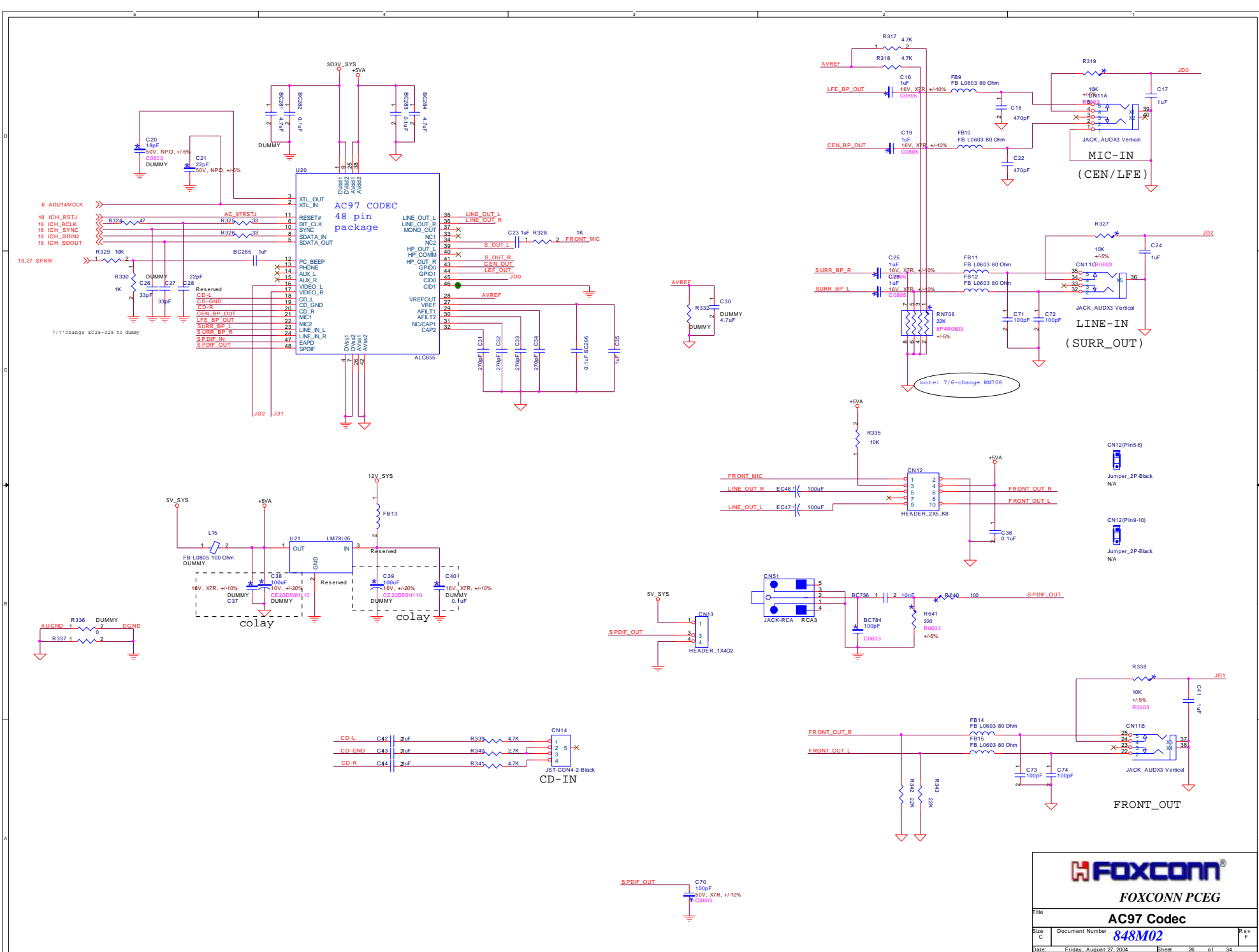


USB Header2



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USB Connector			
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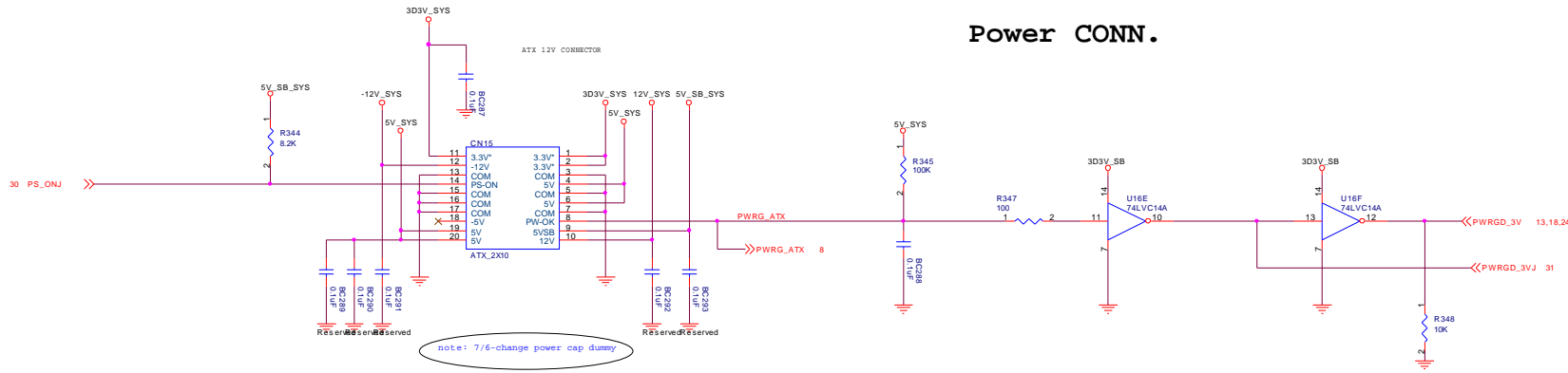
FOXCONN
FOXCONN PCEG

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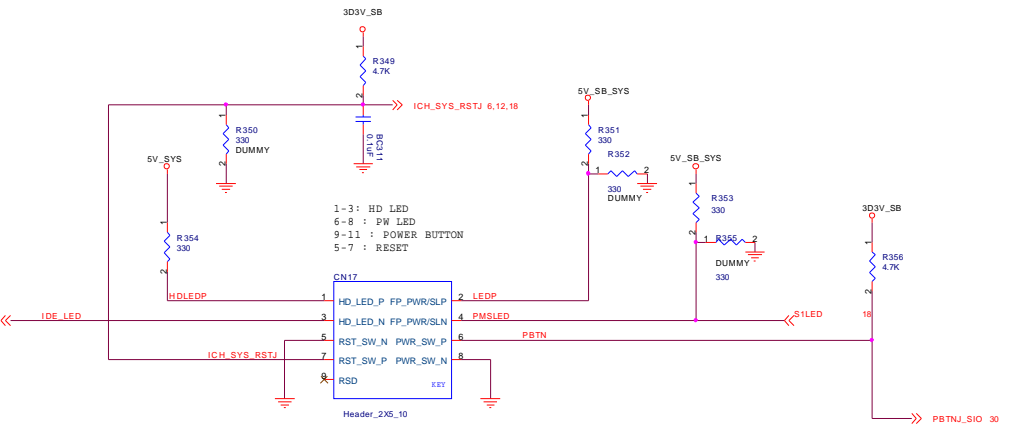
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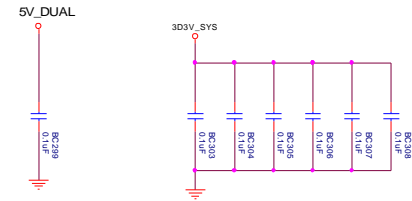
Power CONN.



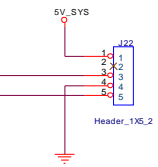
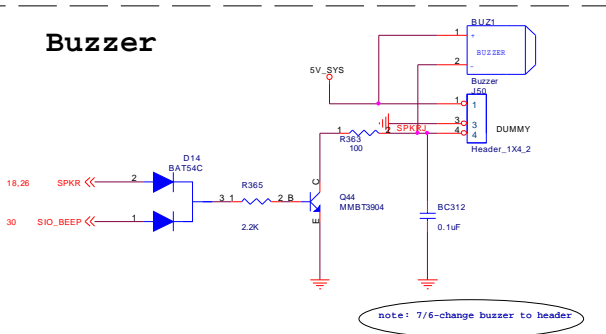
Front Panel



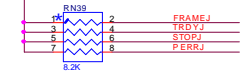
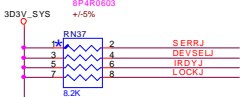
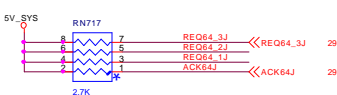
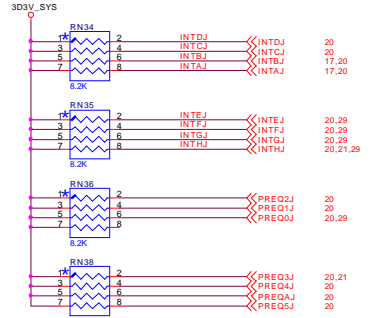
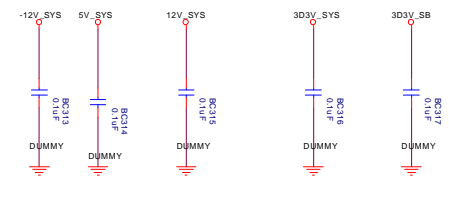
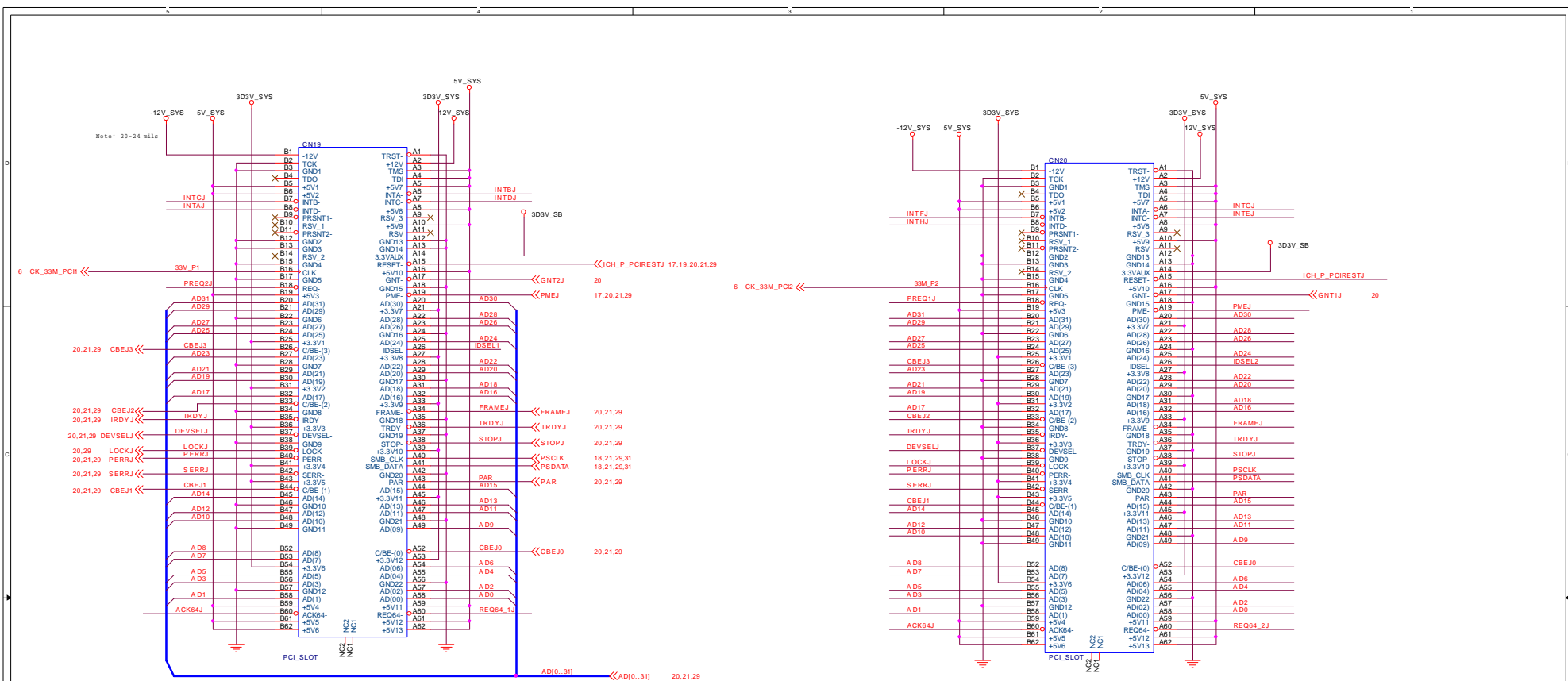
For EMI



Buzzer



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7/7:change BC313- BC321 to dummy
del BC48 -BC54

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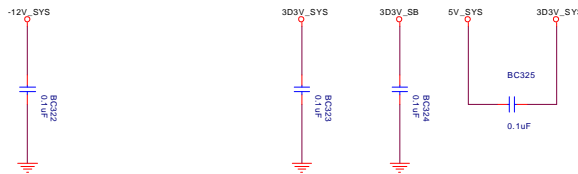
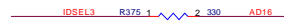
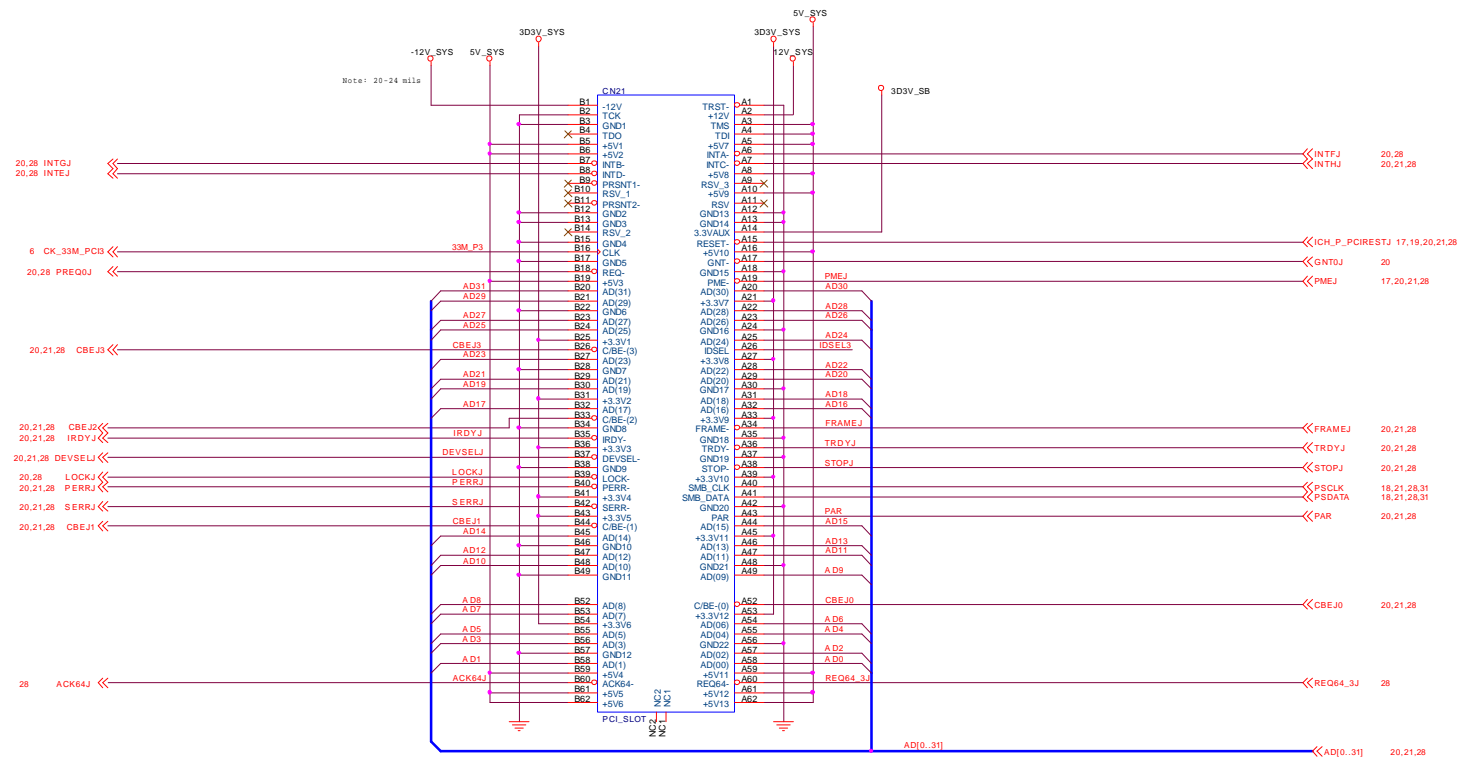
PCI Connectors 1,2

File: **848M02**

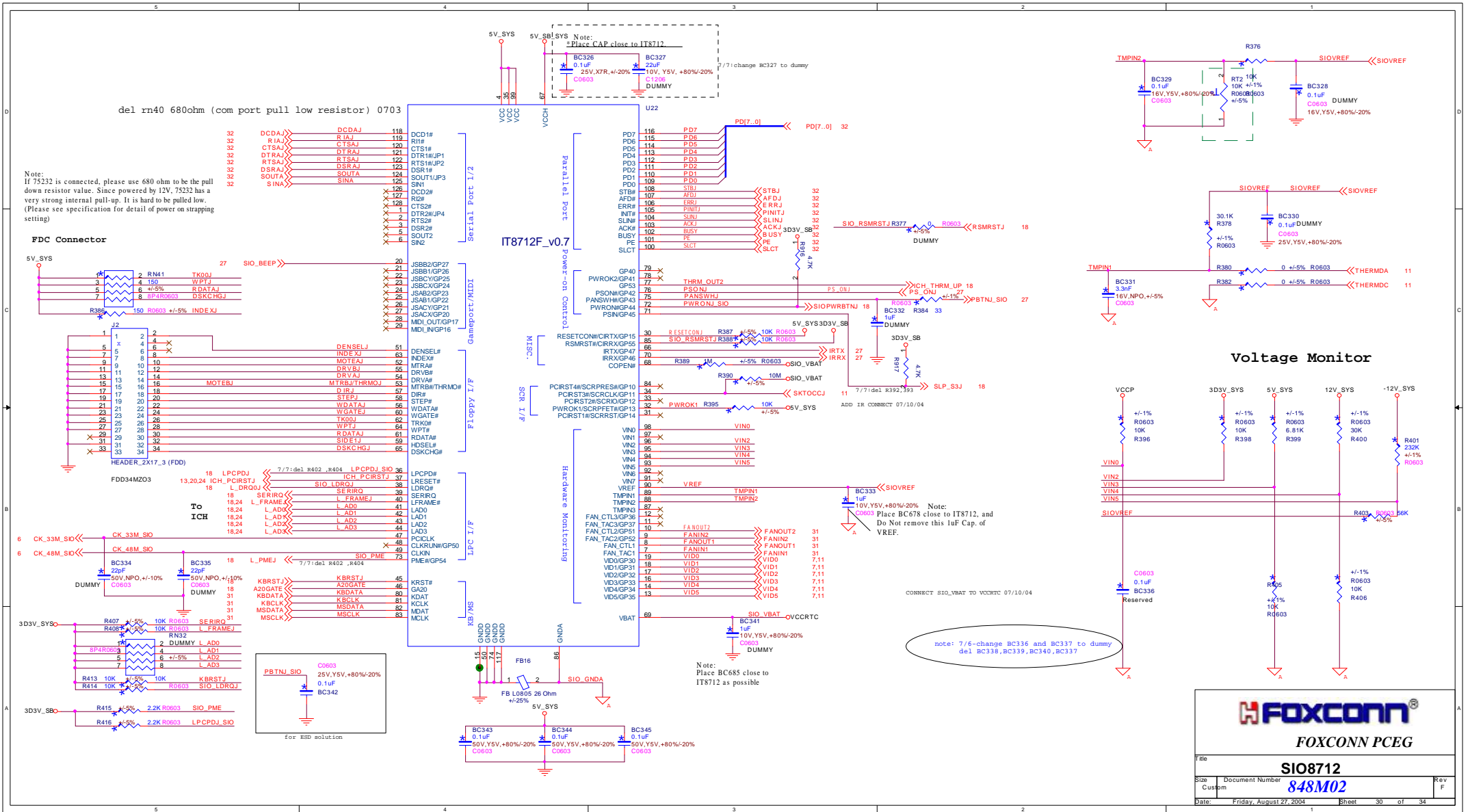
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PCI SLOT3

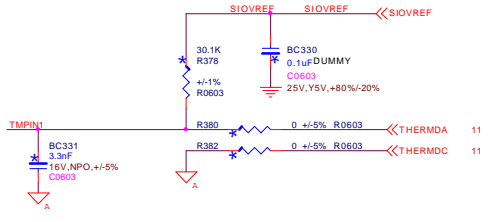
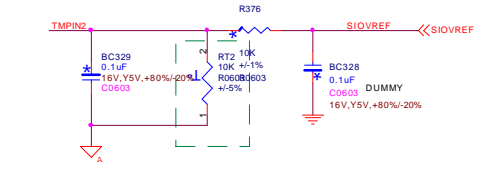
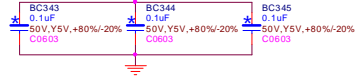
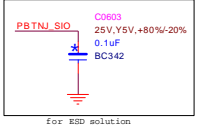
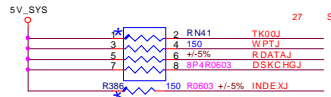


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FOXCONN PCEG	
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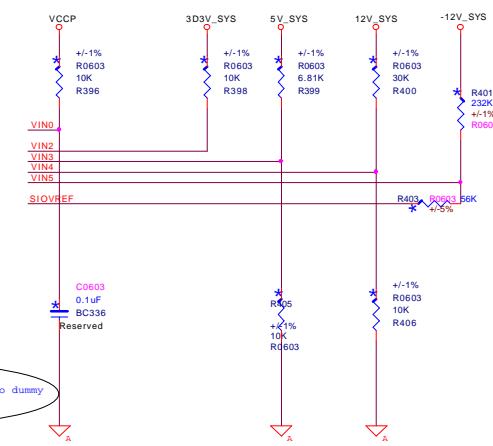


Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low.
(Please see specification for detail of power on strapping setting)

PFC Connector



Voltage Monitor

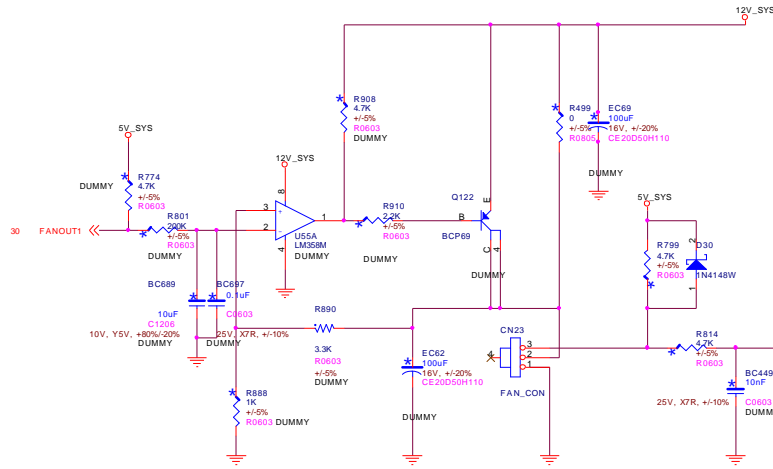


note: 7/6-change BC336 and BC337 to dummy
del BC338,BC339,BC340,BC337

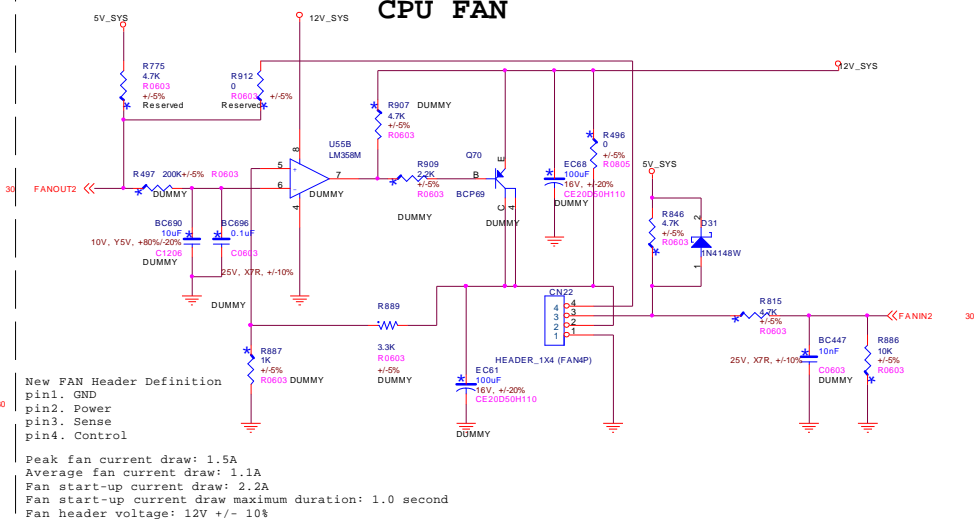


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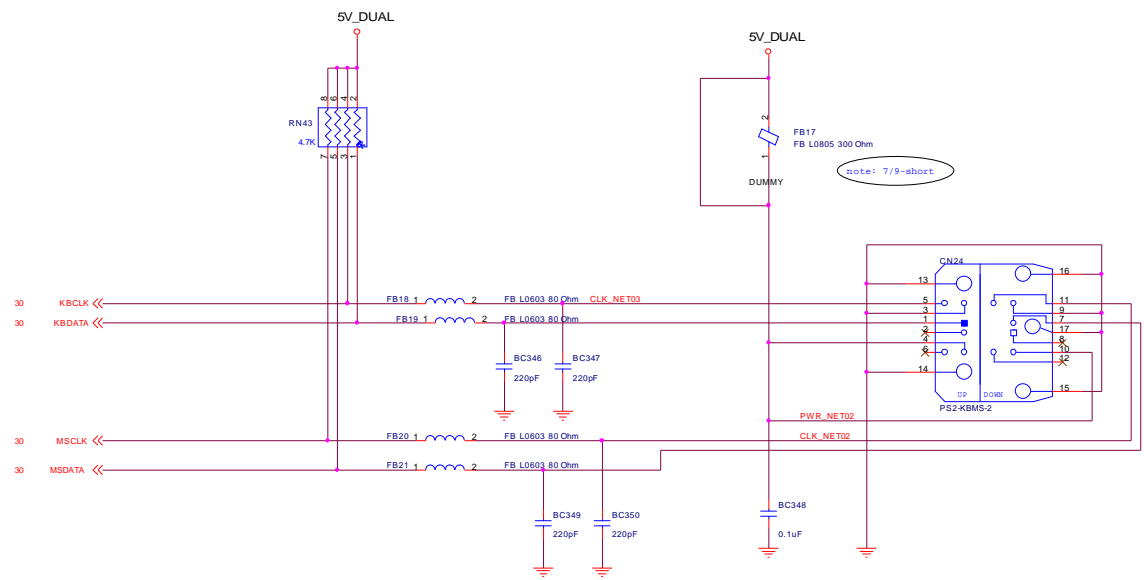
CHASSIS FAN



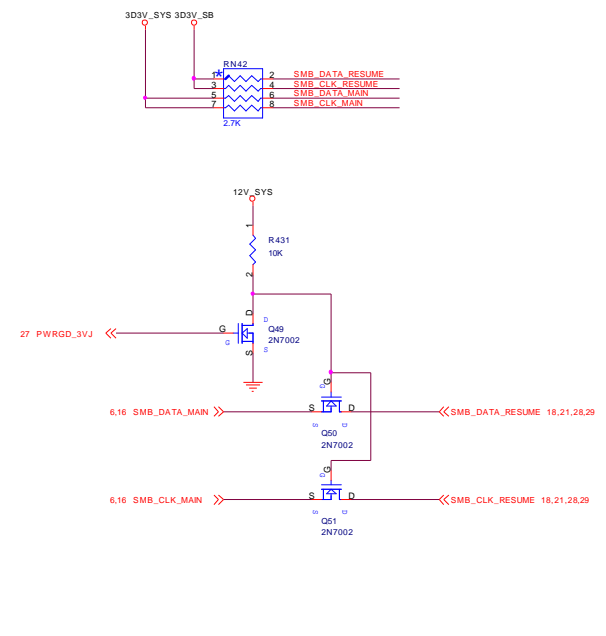
CPU FAN



PS2 MS & KB

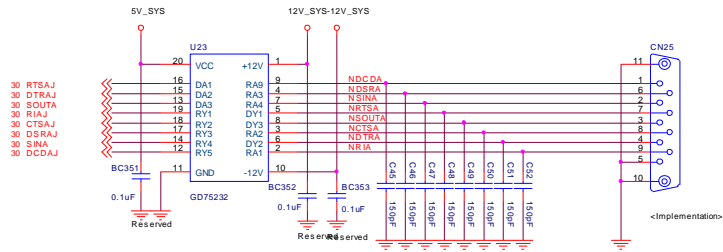


SM BUS



Title		Keyboard / Mouse / Fan	
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SERIAL PORT1

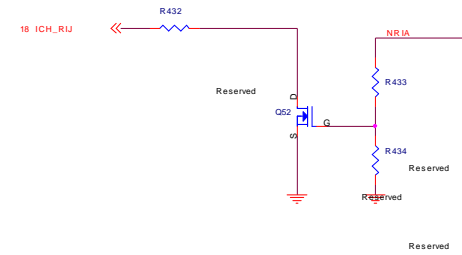
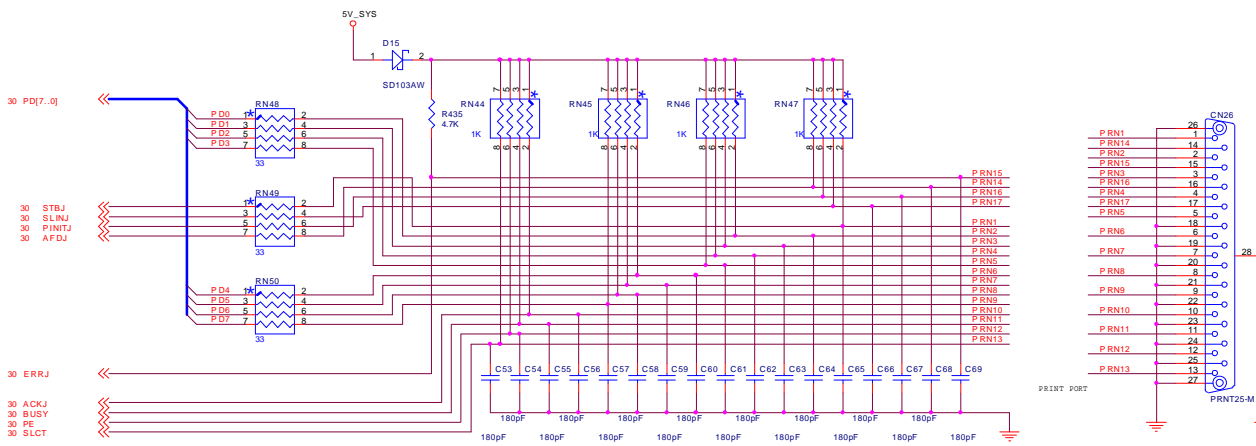


note: 7/6-change BC351,BC352,BC353 to dummy

SERIAL PORTII

Removed

PRINTER PORT1



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Title: Serial / Parallel / CNR

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ICH5 GPIO Summary

Name	Power Plane	Type	Description
GPIO0	Main	I	REQA#
GPIO1	Main	I	REQB# or REQ5#
GPIO2	Main	I	PIRQE#
GPIO3	Main	I	PIRQF#
GPIO4	Main	I	PIRQG#
GPIO5	Main	I	PIRQH#
GPIO6	Main	I	PLC SMI#
GPIO7	Main	I	
GPIO8	Resume	I	LAN PME#
GPIO9	Resume	I	OC4#
GPIO10	Resume	I	OC5#
GPIO11	Resume	I	Pull-up Resistor 10K(Non-use)
GPIO12	Resume	I	LPC PME#
GPIO13	Resume	I	Wake On LAN
GPIO14	Resume	I	OC6#
GPIO15	Resume	I	OC7#
GPIO16	Resume	O	GNTA#
GPIO17	Main	O	GNTB# or GNT5#
GPIO18	Main	O	
GPIO19	Main	O	
GPIO20	Main	O	
GPIO21	Main	O	
GPIO22	Main	OD	Pull-up Resistor 10K(Non-use)
GPIO23	Main	O	
GPIO24	Resume	I/O	
GPIO25	Resume	I/O	
GPIO26	Resume		S1_LED
GPIO27	Resume	I/O	S3_LED
GPIO28	Resume	I/O	
GPIO29			
GPIO30			
GPIO31			
GPIO32	Main	I/O	Board ID1
GPIO33	Main	I/O	SATE_LED
GPIO34	Main	I/O	Board ID0
GPIO35	N/A		
GPIO36	N/A		
GPIO37	N/A		
GPIO38	N/A		
GPIO39	N/A		
GPIO40	Main	I	REQ4#
GPIO41	Main	I	LDRQ1#
GPIO42	N/A		
GPIO43	N/A		
GPIO44	N/A		
GPIO45	N/A		
GPIO46	N/A		
GPIO47	N/A		
GPIO48	Main	O	GNT4#
GPIO49	Main	OD	CPUPWRGD

FWH GPIO Summary

Name	Power Plane	Type	Description
FGPIO0	Main	I	IDE1 Detect 33/66/100
FGPIO1	Main	I	IDE2 Detect 33/66/100
FGPIO2	Main	I	Unused
FGPIO3	Main	I	Unused

PCI Routing Summary

PCI Dev	Interrupt	Req/Gnt	ID Select
PCI1	BCDA	2	AD18
PCI2	GFHE	1	AD17
PCI3	FGHE	0	AD16
LAN	H	3	AD19



FOXCONN PCEG

Title: GPIO / IRQ / IDESEL Map

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To Rev 1.1
For FMB1.5:
Del R714.
Add BC597,BC598,BC599_2200pF/NA.
Change BC117,BC118,BC151,BC152,BC153,BC159,BC160,BC 161,BC185,BC187,BC188,BC189,BC190,BC191,BC192 From 1uF to 22uF X5R.
Change BC103~BC107,BC114~BC116,BC95~BC99 From 2.2uF to 22uF X5R.
Change TC2,TC3 footprint to CTD.
NA BC559,BC547.

For VRM10.1:
Change R600 from 1k to 2k,R738,R737 from 470 to 1k.
Add R784 2k/NA,R776_30 k,R777_20k 1%,BC590_5600pF,R778_0/NA,R779_0,R780_0/NA.
Del Q90,Q94,BC541,BC552,Q92,Q96,R695,R709.
Change Q91,Q95 from 06N03L to 80N02R,Q89,Q93 from 12N03L to 60N02R.
Add Q101_60N02R,Q102_80N02R,L20_500nH,U47_SC1211,D25_1N4148,R781_1,R782_100,
R783_1,BC591_1uF/C0805,BC592_4.7uF/C1206,BC593_1uF/X7R,BC595_4700pF/X7R,BC596_4.7uF/C1206.

For Fan Speed:
Attach R496,R499_0.

For 1.5V_CORE:
Del U35,EC54.
Add U46_LM358,BC586,BC588_0.01uF,BC587,BC589_0.1uF.
Change R237 value to 1.24k 1%,R235 to 0,R231 to 549 1%,R226 to 1.54k 1%.
NA Q83,R612.
Change Q38,Q39 to SDU3055L2.

For USB/1394:
NA TF1~TF8,F1,F2,F5~F8.
Add R742~R769_0.

For Audio:
Add L19_120 ohm@100M,R791,R792_22k,R785,R786,R787,R790.
Change R27,R20,R8,R17 value to 80ohm@100M Ferri Bead.
NA U1,FB1,BC1,C276.

For DDR_VTT:
Del EC56,EC57,Q87,R679,R680.
Add U43,R770,R771.

For 3D3VSB:
Del U18,R225,R219.
Add U45_AIC1086,R772,R773.

For GMCH_VTT:
NA GMCH_VTT Module,Add RN83.

07/12
Add Board ID2.

07/15
For case open:
Add J3,R318
For WOM:
Add CN32,R579,R578,Q75

07/16
Modify Board ID0~4

07/16
Final Sch is date 0716

08/21
Change VCCVID_GD pull-up voltage to 1.2v.
NA R699.

06/12/04
Change R672 to C281
Change BC449 to R9956

08/17/04
1. Add R5 at clock pin20 for reset issue



Title		
Modify List		
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