

Foxconn Precision Co. Inc.

915A01 Schematic

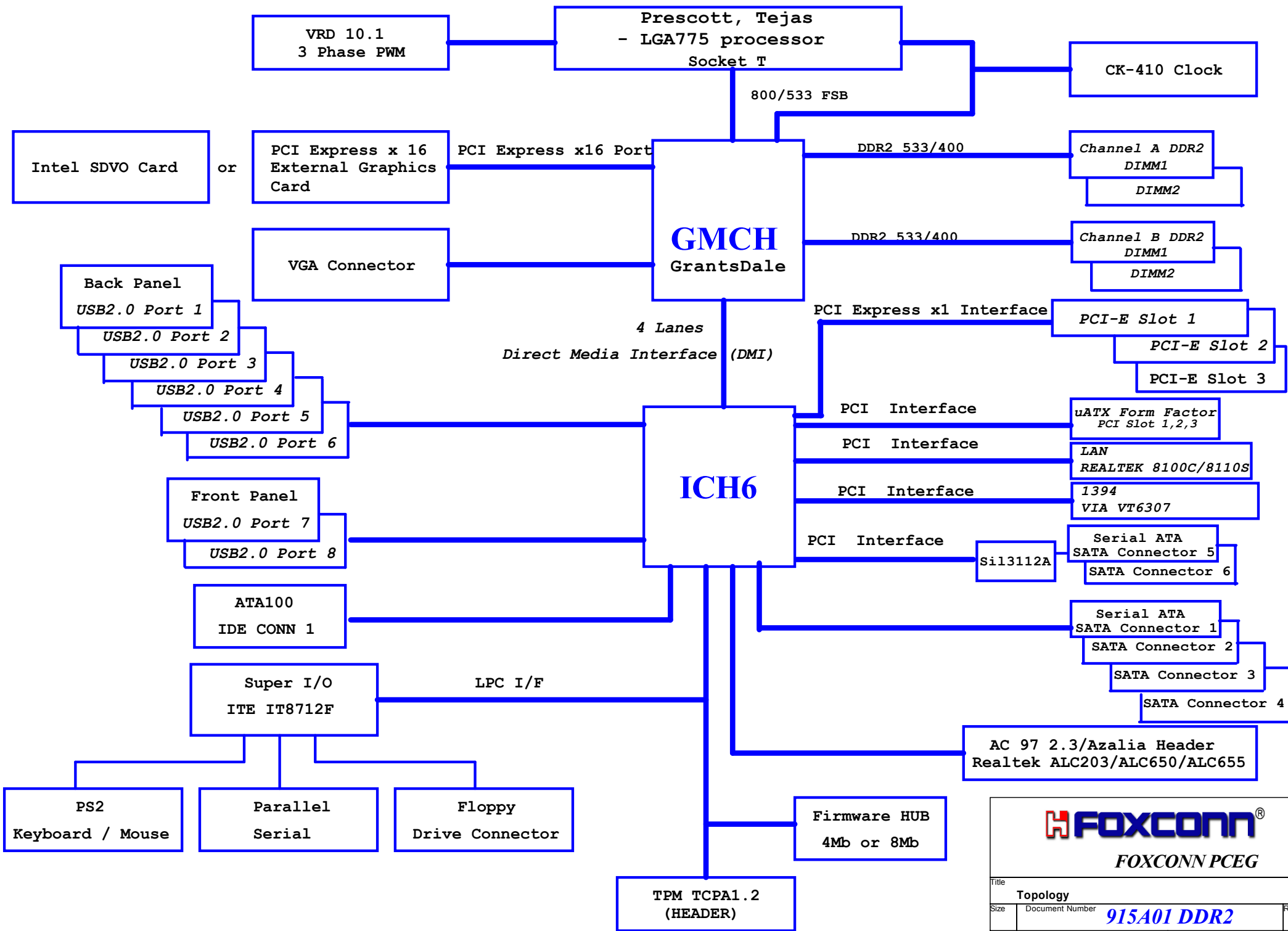
Fab.B Date: 2004/05/01

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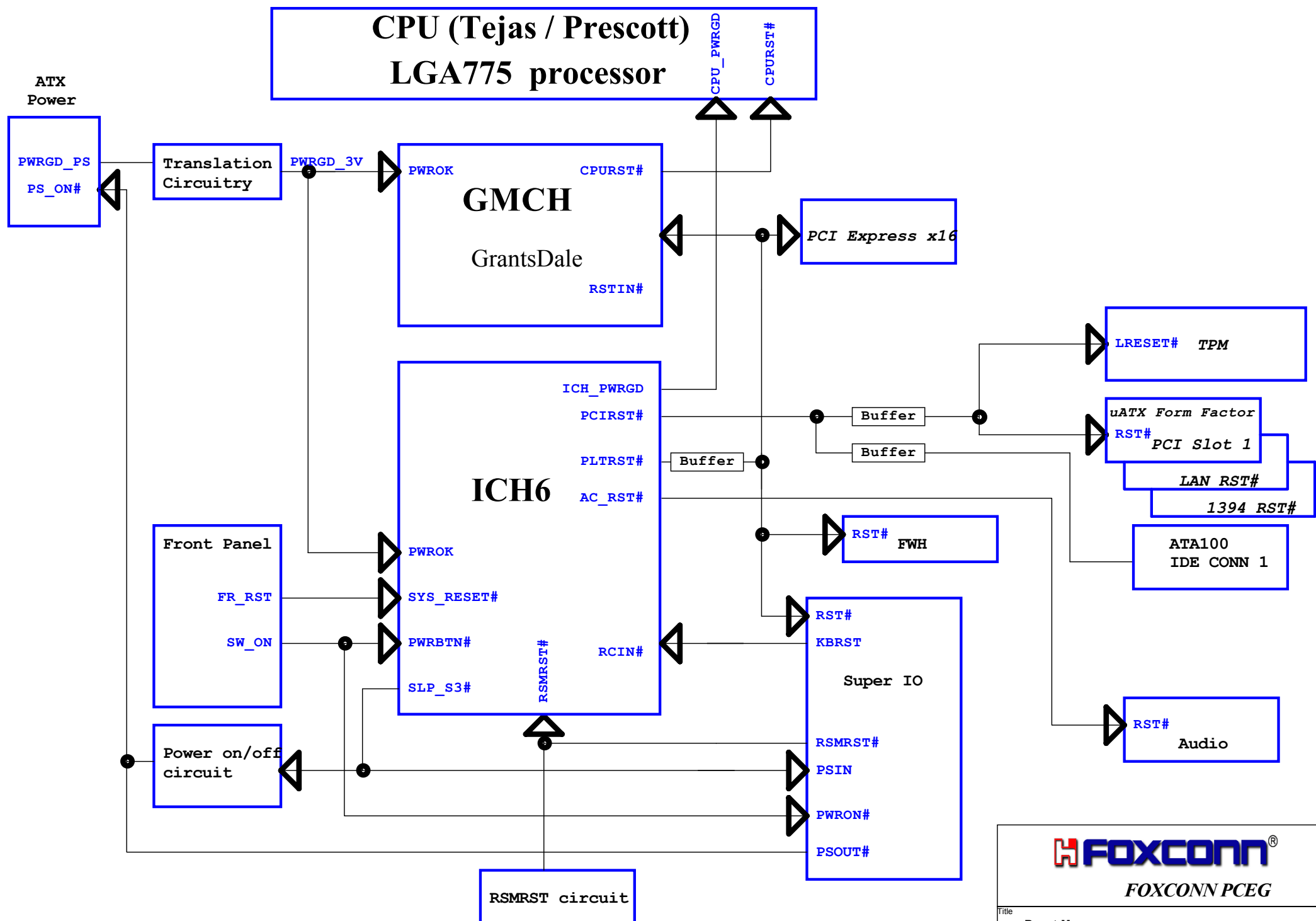


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Title Topology		
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14.318MHz

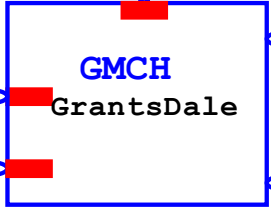


CPU 133/200 MHz Diff Pair

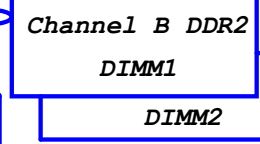
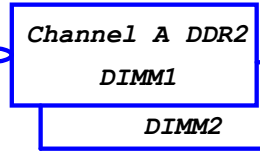
MCH 133/200 MHz Diff Pair

PCI Express 100 MHz Diff Pair

PCI Express x16 Gfx



DDR 4 Slots 12 Diff CLKs



DOT 96 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

USB/SIO 48 MHz

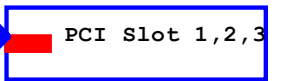
ICH 33 MHz

REF 14 MHz

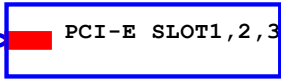
FWH 33 MHz



PCI 33 MHz



PCI Express 100 MHz Diff Pair



LAN 33 MHz



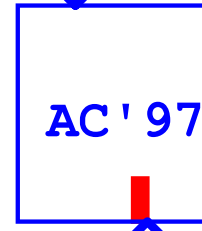
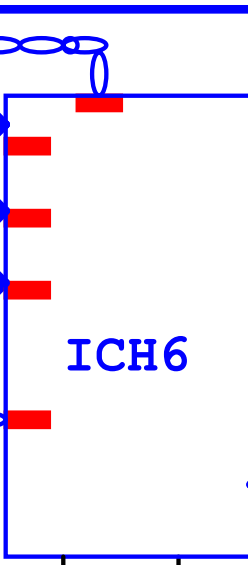
TPM 33 MHz



1394 33 MHz



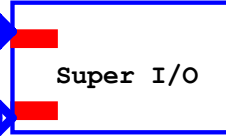
SIO 33 MHz



24.576MHz

AC97 Bit Clock

32.768KHz

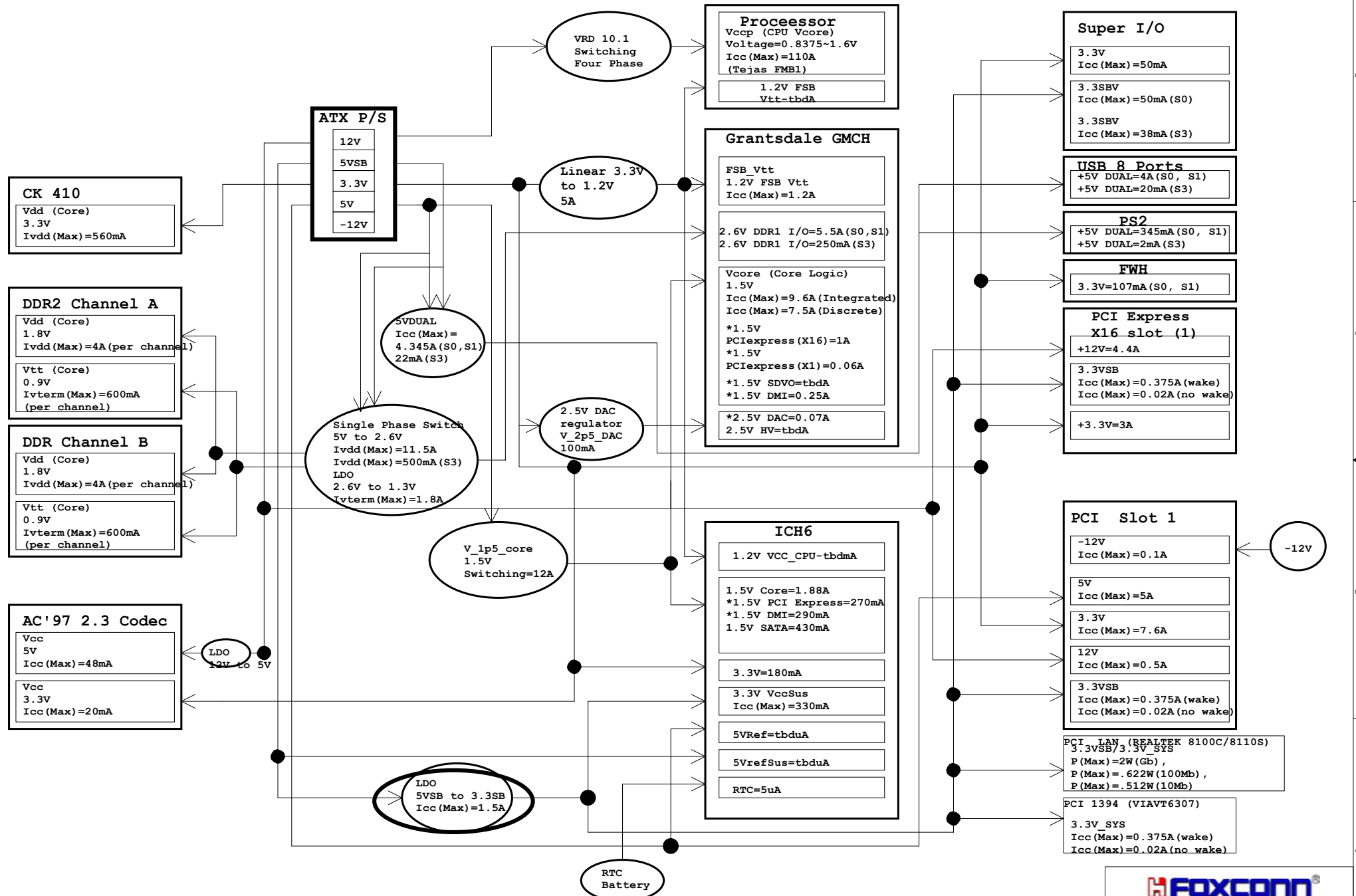


SATA 100 MHz Diff Pair

CK-410



Title CLOCK Distribution		
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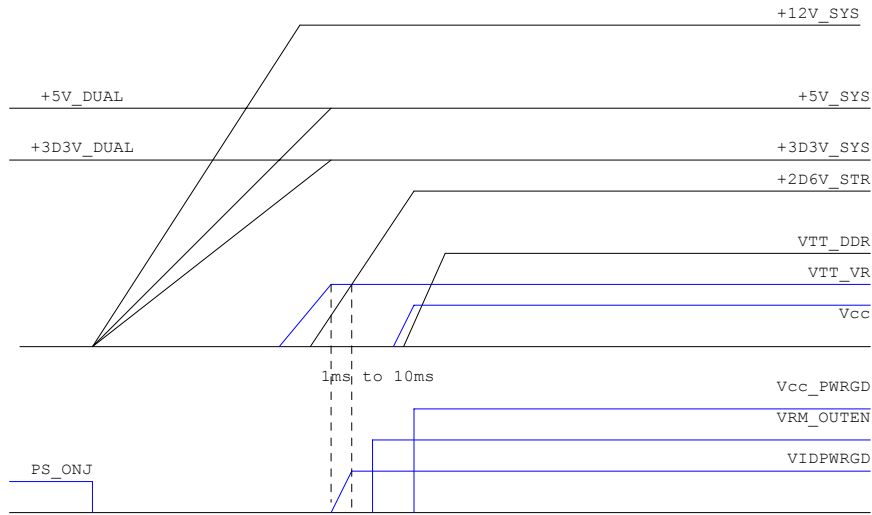
*Power derived through filter



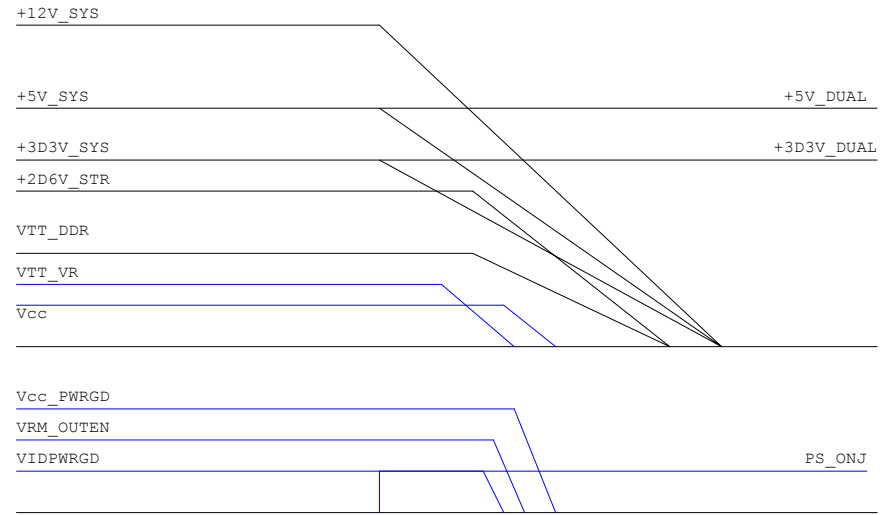
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Title		
Power Delivery Map		
Size	Document Number	Rev
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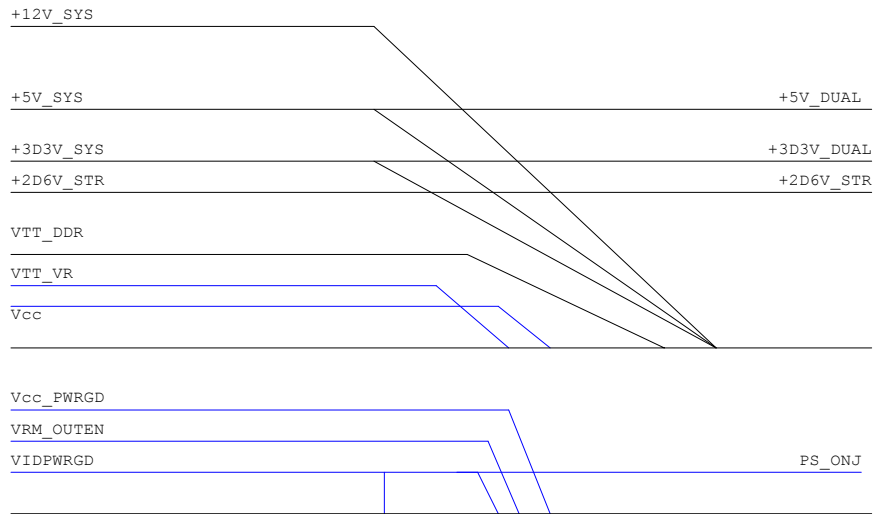
S5->S0



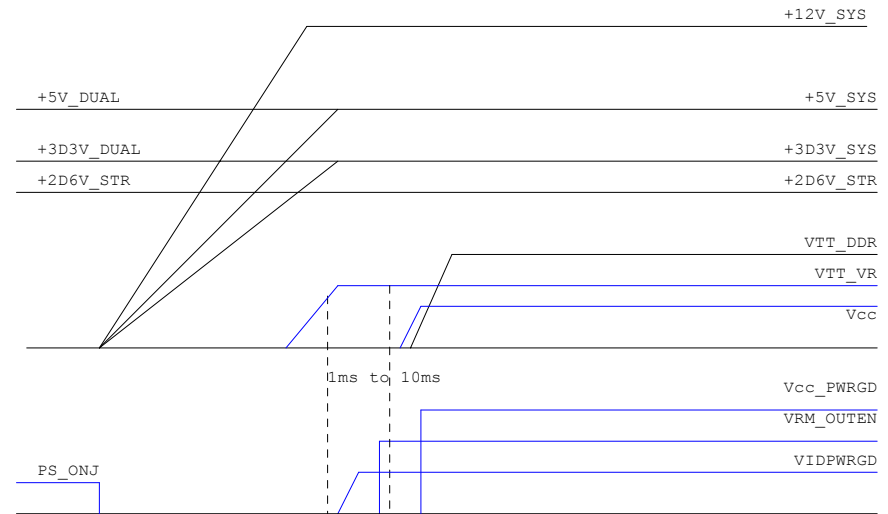
S0->S5



S0->S3

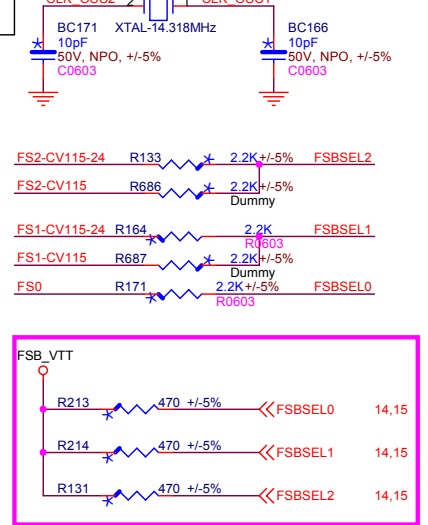
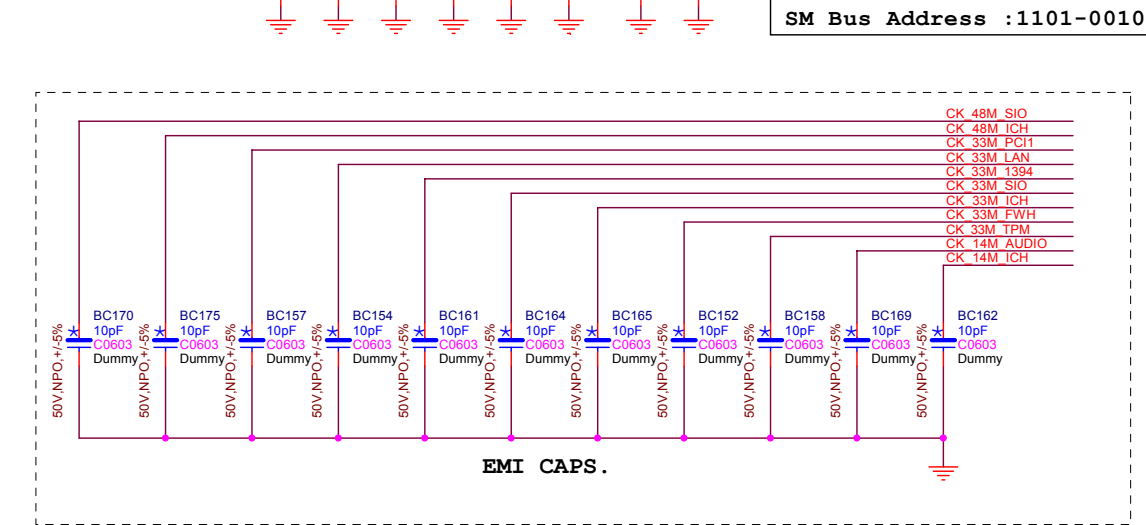
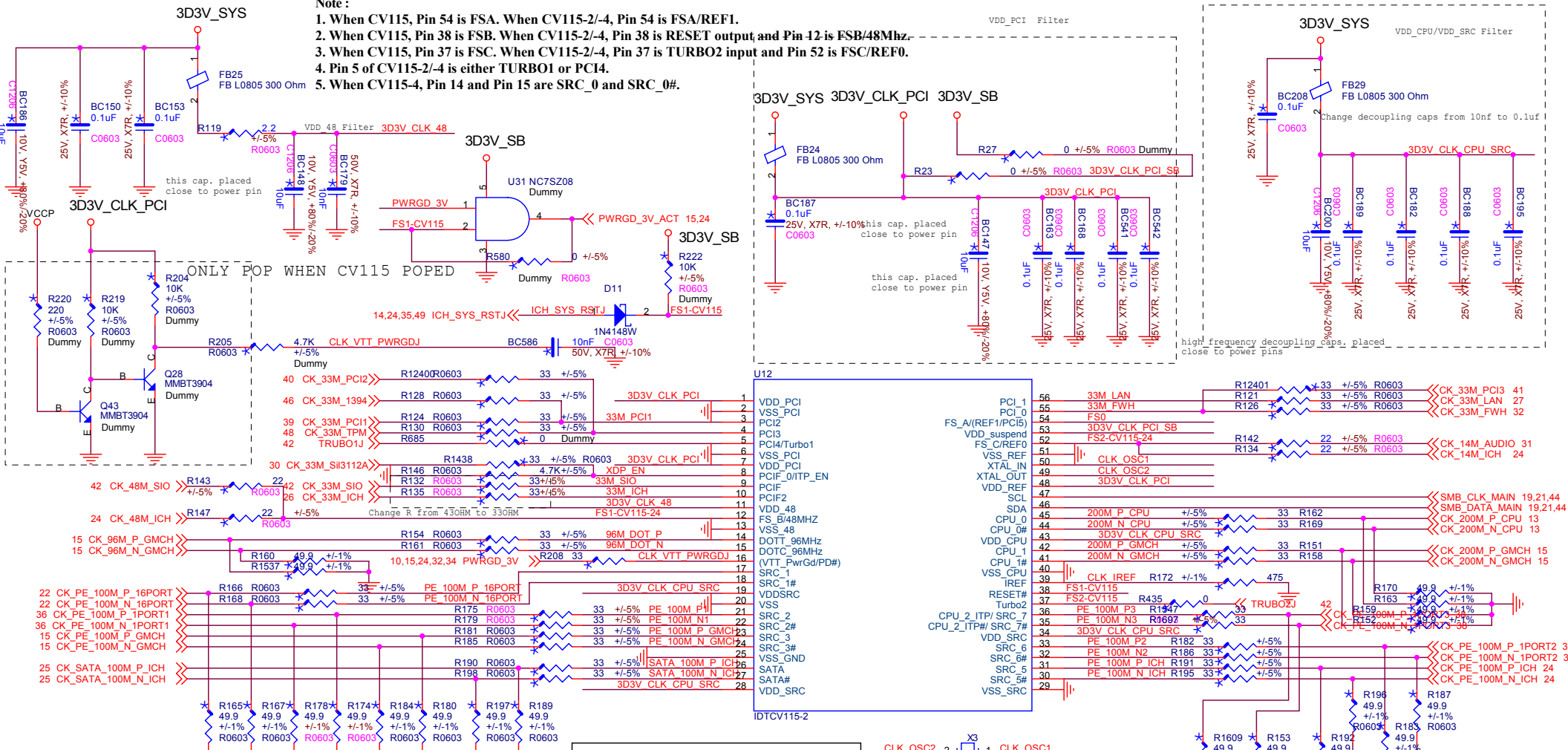


S3->S0



Title Power Sequence		
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- Note:
1. When CV115, Pin 54 is FSA. When CV115-2/-4, Pin 54 is FSA/REF1.
 2. When CV115, Pin 38 is FSB. When CV115-2/-4, Pin 38 is RESET output and Pin 12 is FSB/48Mhz.
 3. When CV115, Pin 37 is FSC. When CV115-2/-4, Pin 37 is TURBO2 input and Pin 52 is FSC/REF0.
 4. Pin 5 of CV115-2/-4 is either TURBO1 or PCIA4.
 5. When CV115-4, Pin 14 and Pin 15 are SRC_0 and SRC_0#.

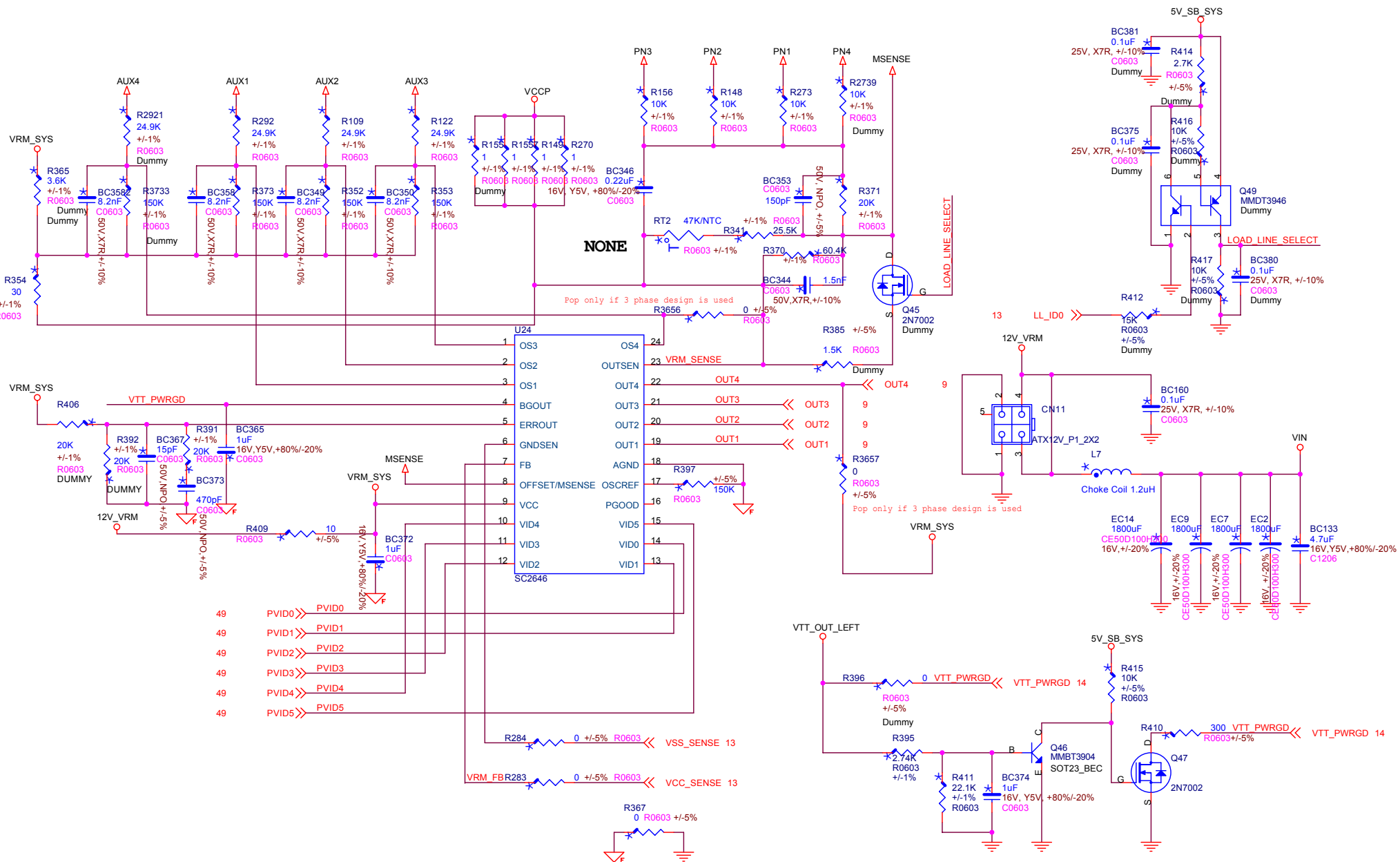


SM Bus Address : 1101-0010

BSEL TABLE

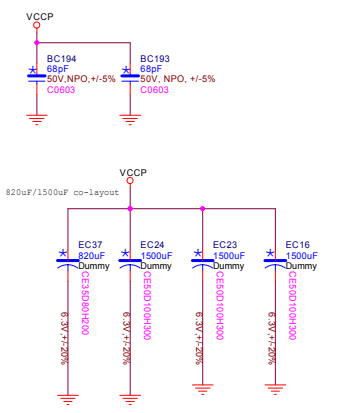
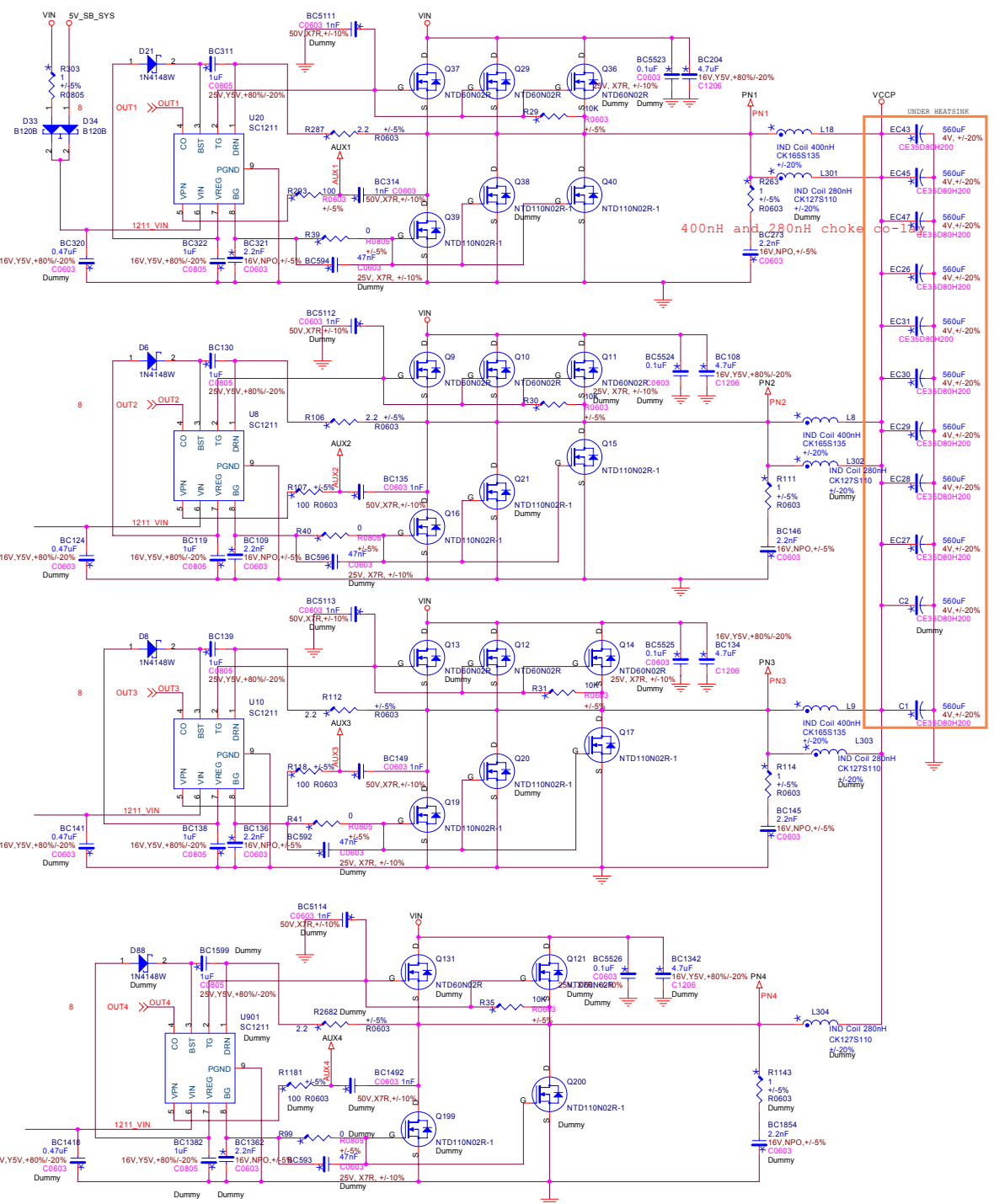
C	B	A	FSB Frequency
0	0	0	266MHz
0	0	1	133MHz (533)
0	1	0	200MHz (800)

- FS2-CV115-24 R133 2.2K +/-5% FSBSEL2
- FS2-CV115 R686 2.2K +/-5% Dummy
- FS1-CV115-24 R164 2.2K +/-5% FSBSEL1
- FS1-CV115 R687 2.2K +/-5% Dummy
- FS0 R171 2.2K +/-5% FSBSEL0



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Title Voltage Regulator Down 10.1		
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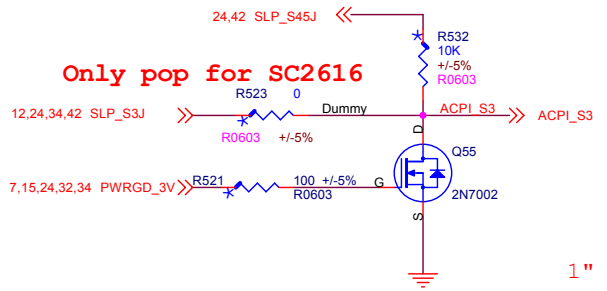


De-pop if 4 phase design is used.

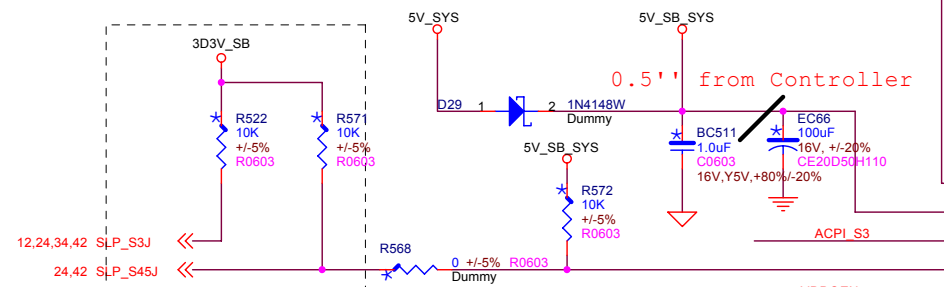
Q37, Q29, Q39, Q9, Q11, Q15, Q12, Q14, Q20, Q121



Only pop for SC2616



1" from controller

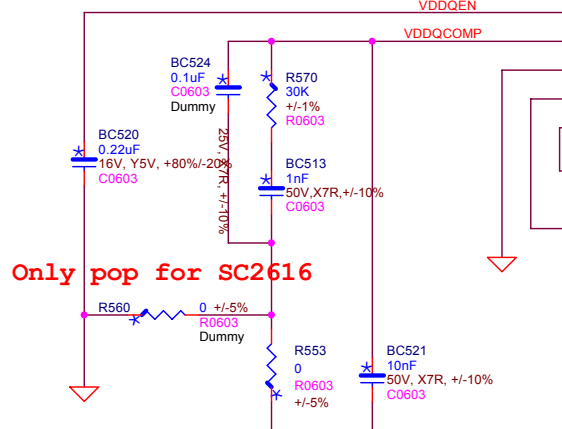


0.5" from Controller

Close to PIN9 of SC2616

These two resistors are necessary. S3# and S5# must be tied to 5Vsb to prevent them floating.

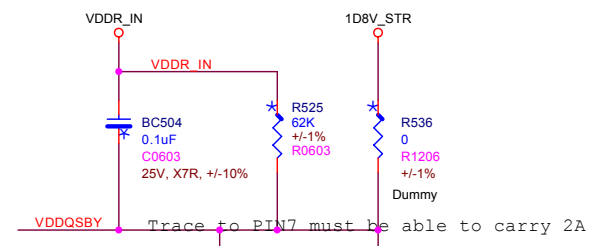
Only pop for SC2616



Only pop for NCP5201

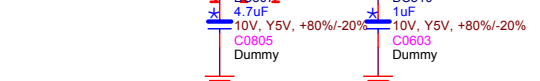
Place less than 0.25" from Controller

Only pop for NCP5201



Place close to PIN8 of SC2616

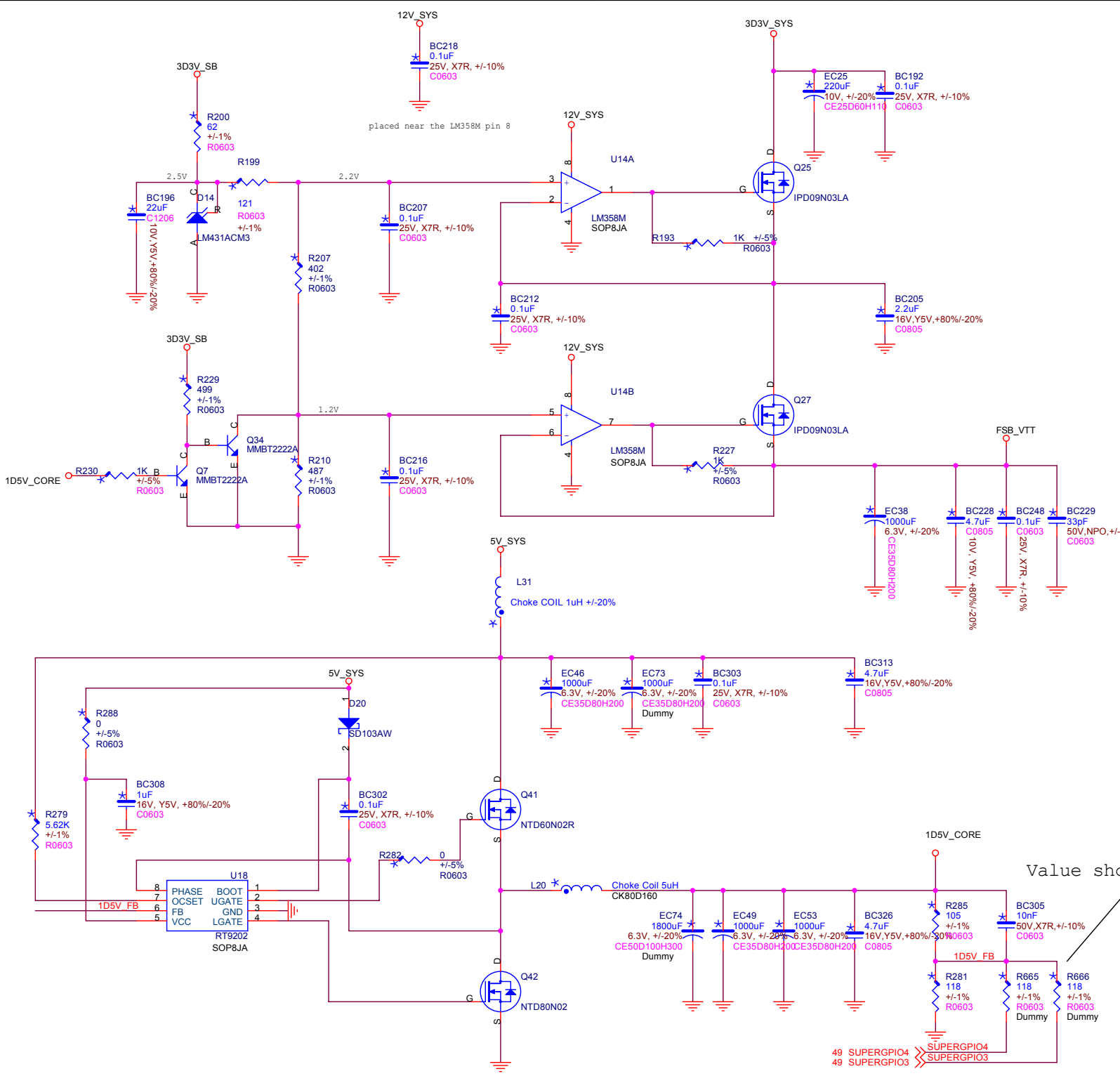
Only pop for SC2616




Value should be tuned

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Title	DDR1 2.6V/1.3V	
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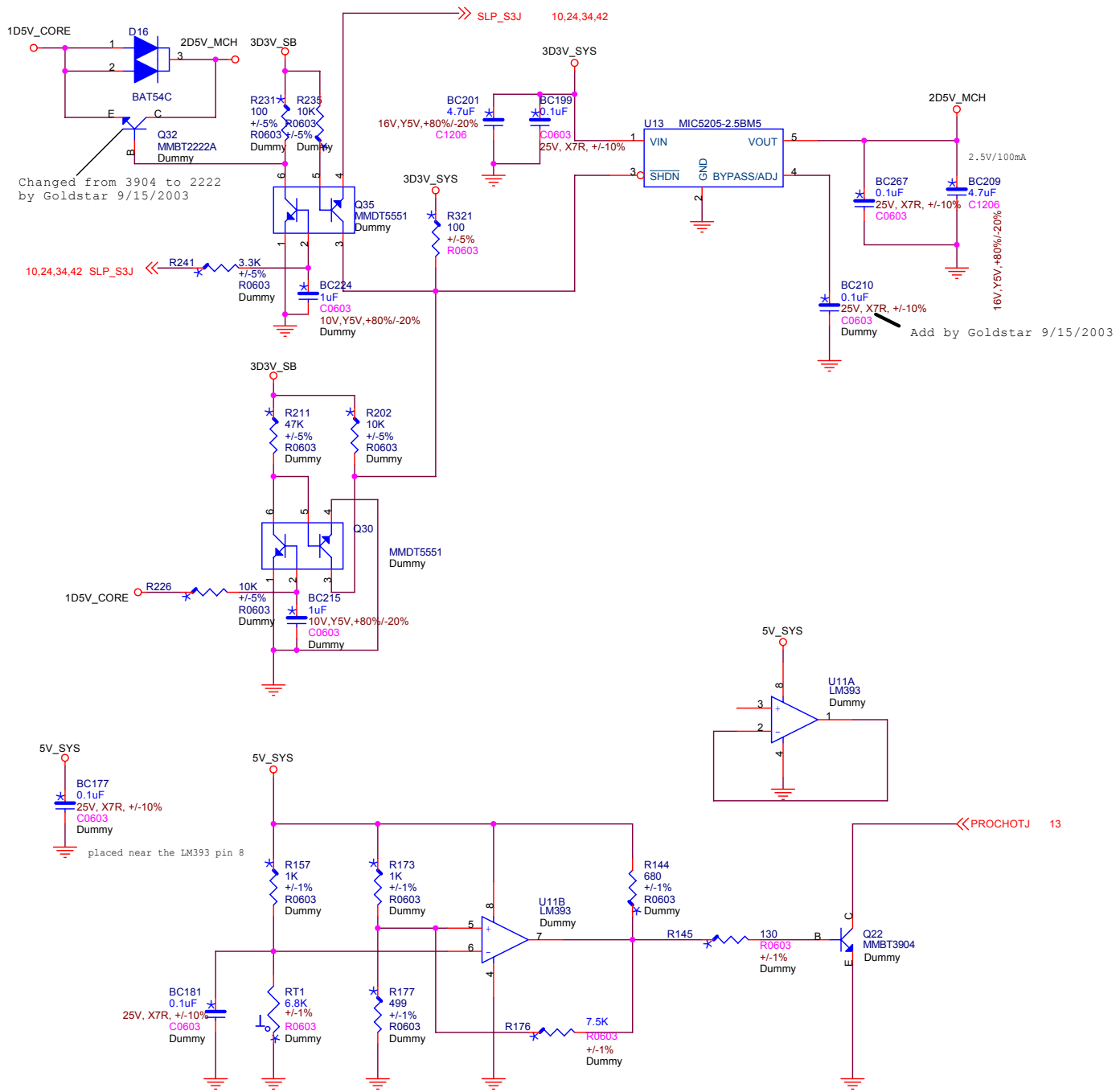


Value should be tuned



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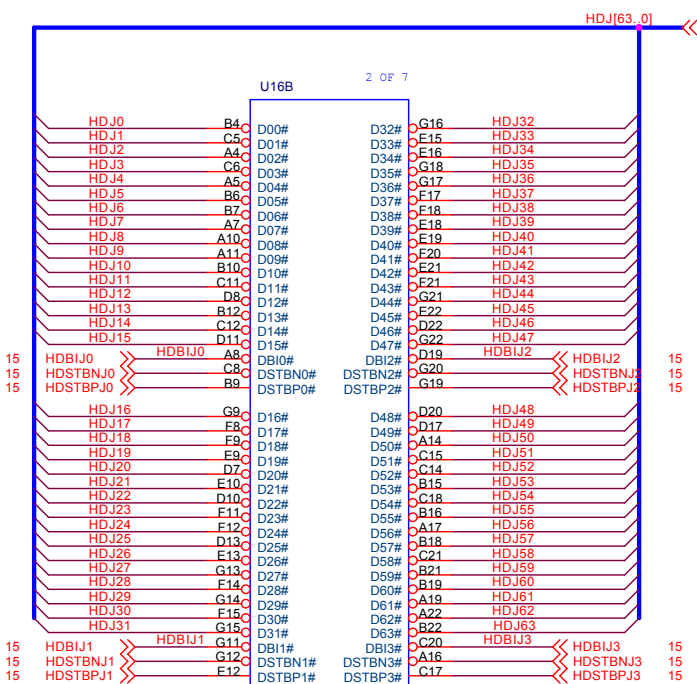
Title		Power 1.5V 1.2V	
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		Rev	B



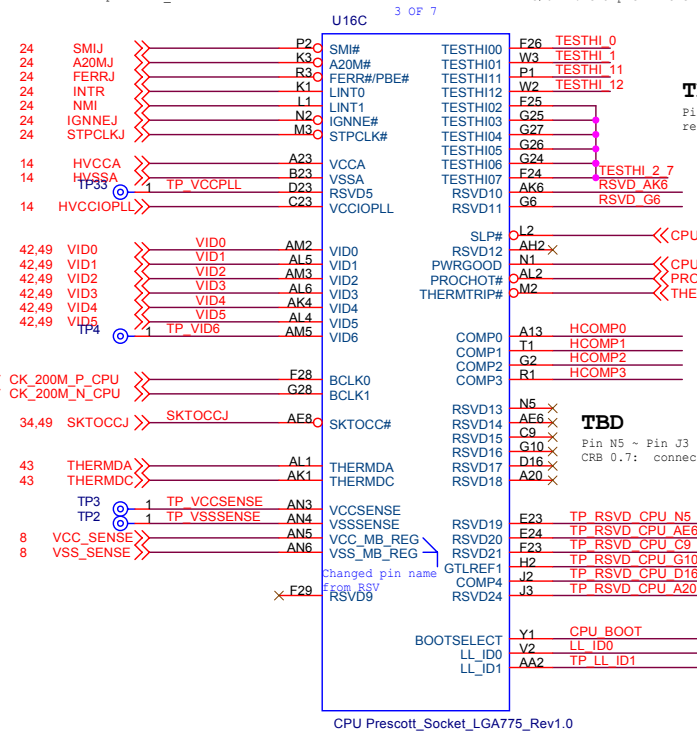
VR Thermal Monitor Circuit

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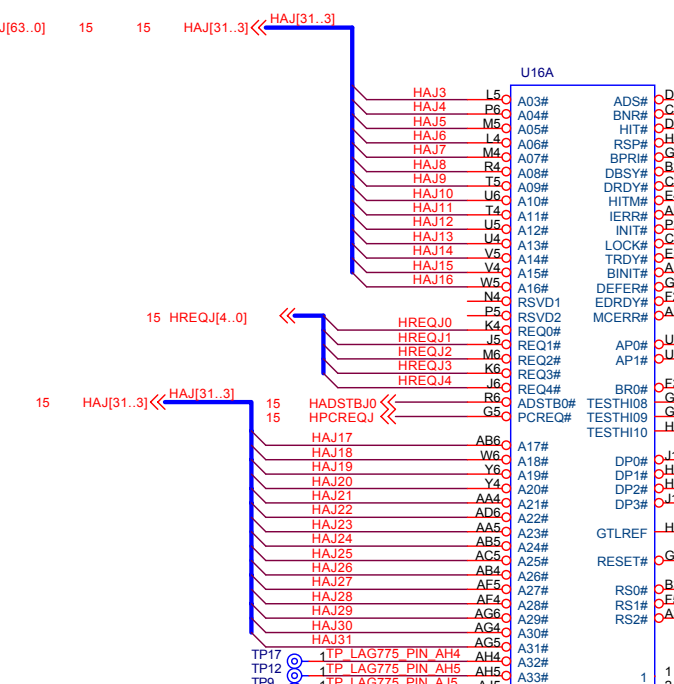
Title		2.5V_MCH	
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		1	B



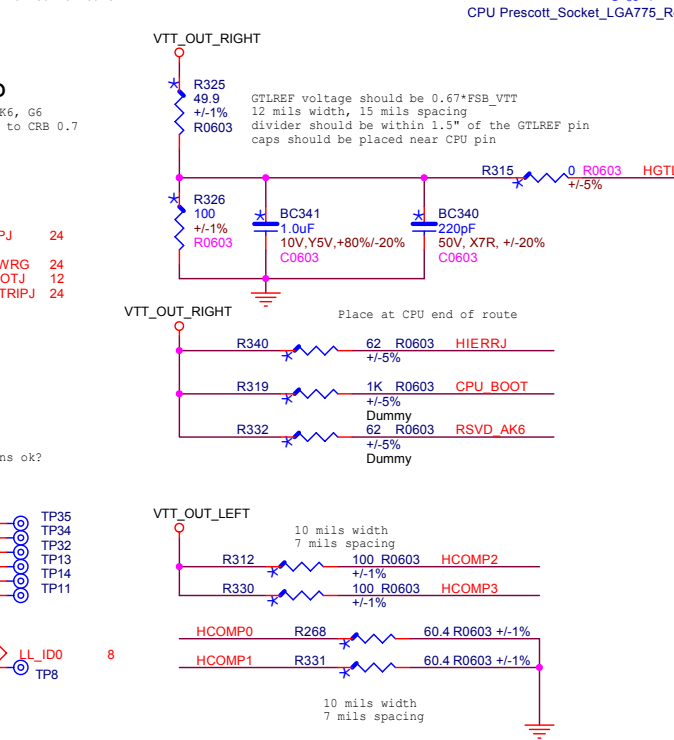
TBD
Pin D23
CRB 0.7: test point TP_VCCPLL
Pin AM5
CRB 0.7: test point TP_VID6



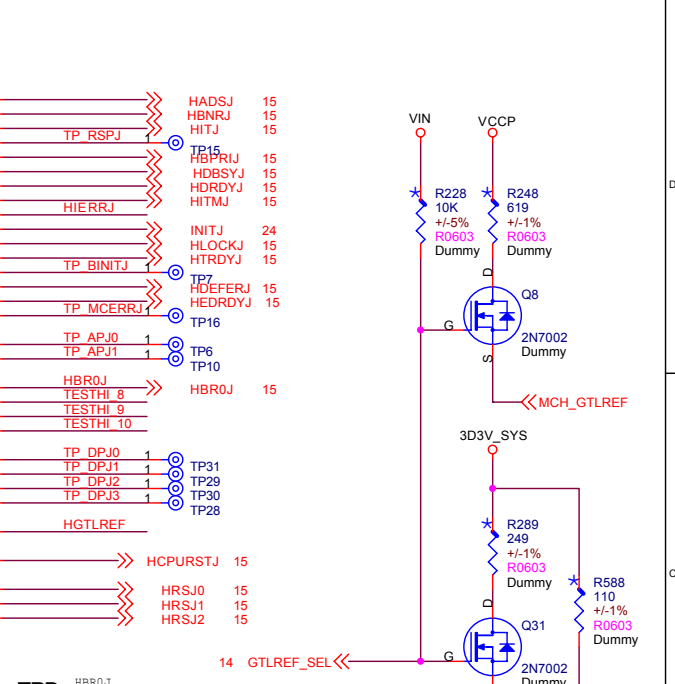
CPU Prescott_Socket_LGA775_Rev1.0



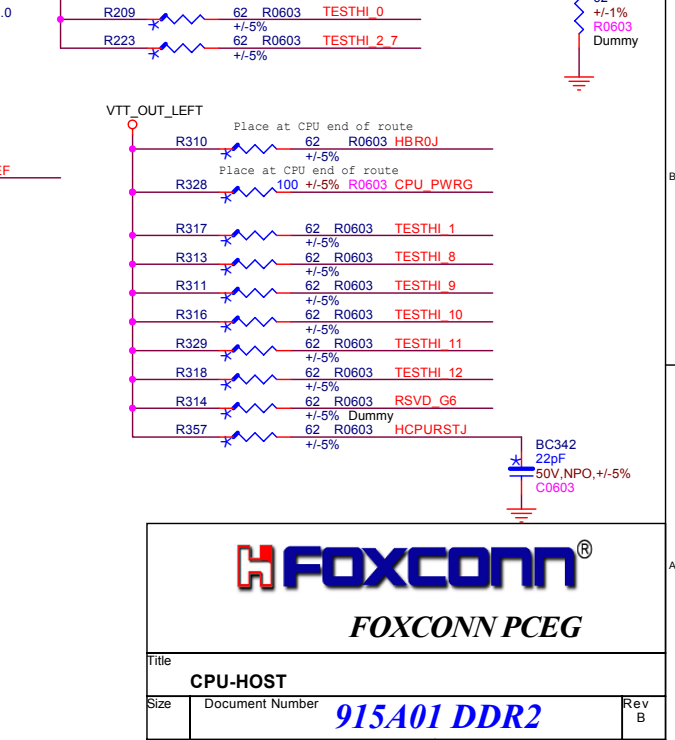
TBD
Pin AL2 PROCHOT#
CRB 0.7: pull up to VTT_OUT_RIGHT
DG/611A: example VR thermal monitor circuit



CPU Prescott_Socket_LGA775_Rev1.0



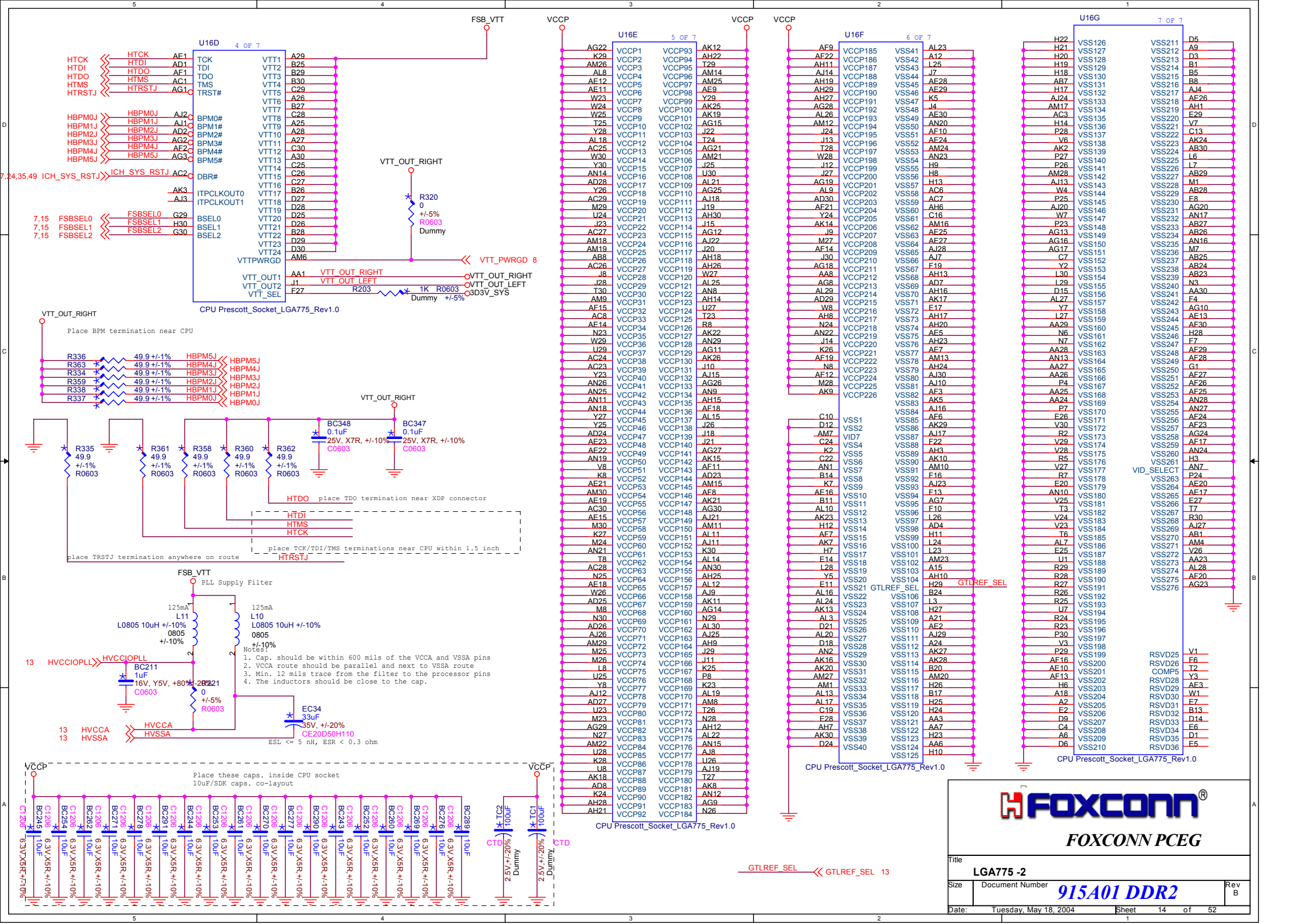
TBD
HBR0J
CRB 0.7: 220 ohm, 5%
DG 0.51: 62 ohm, 5%



CPU Prescott_Socket_LGA775_Rev1.0



Title		CPU-HOST	
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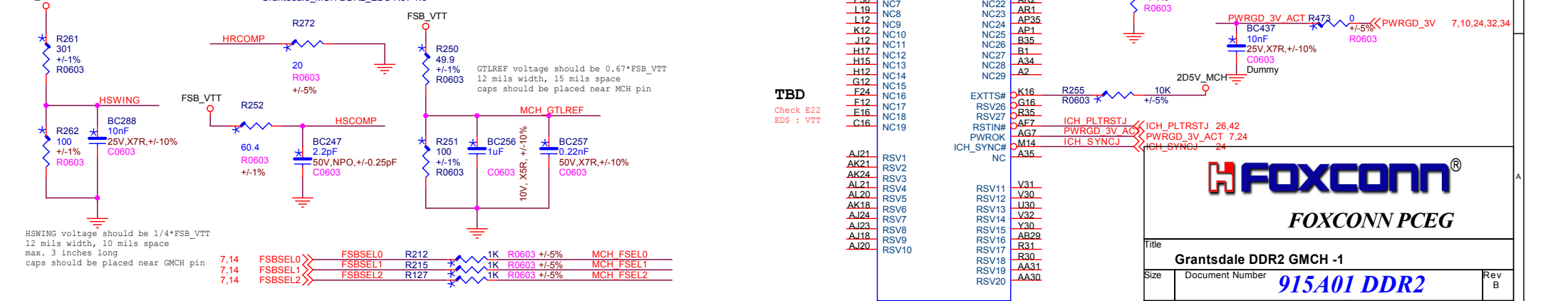
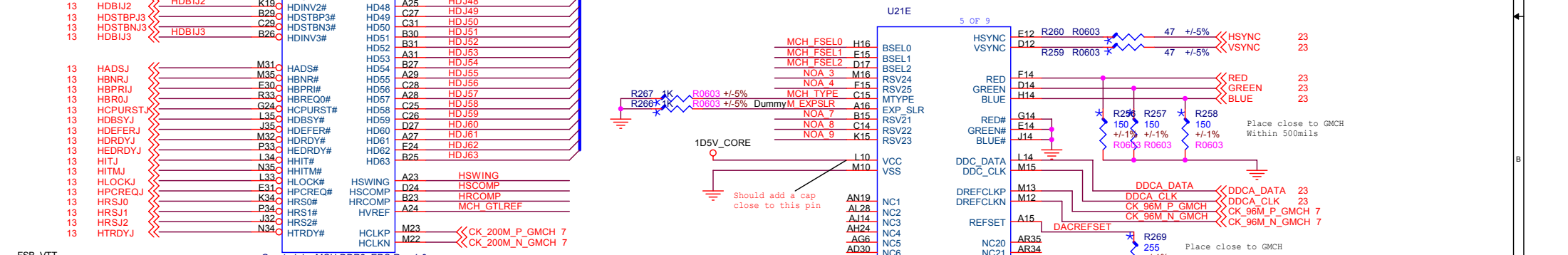
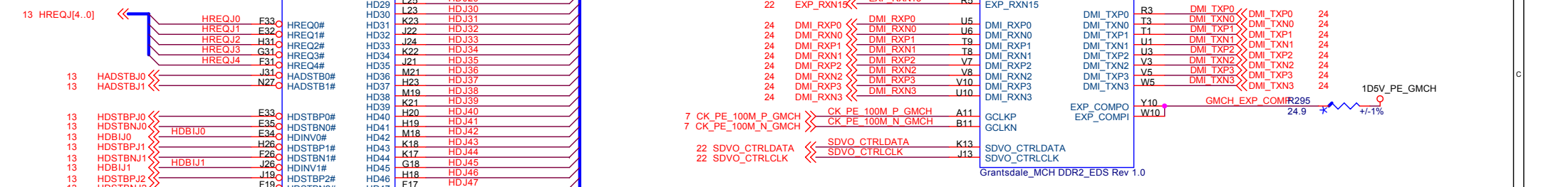
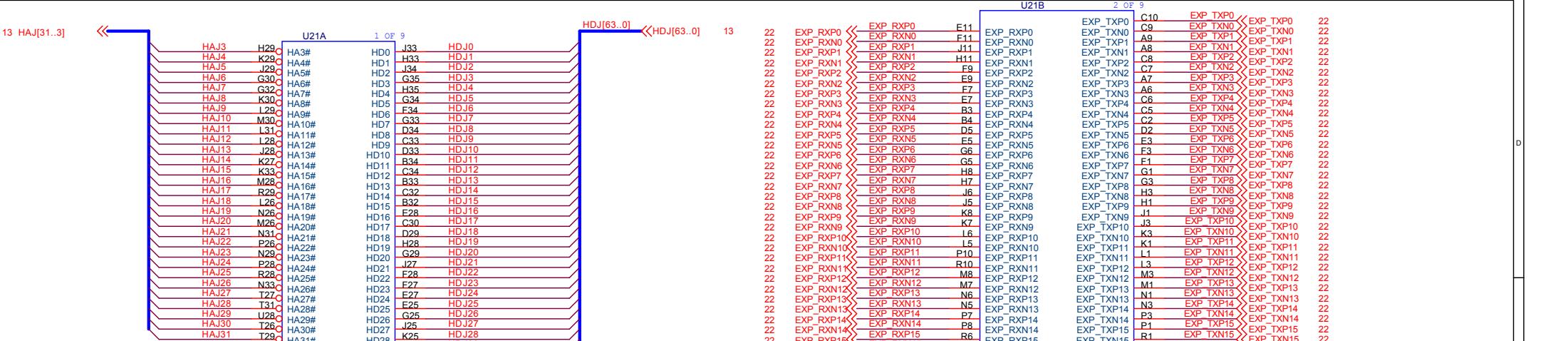


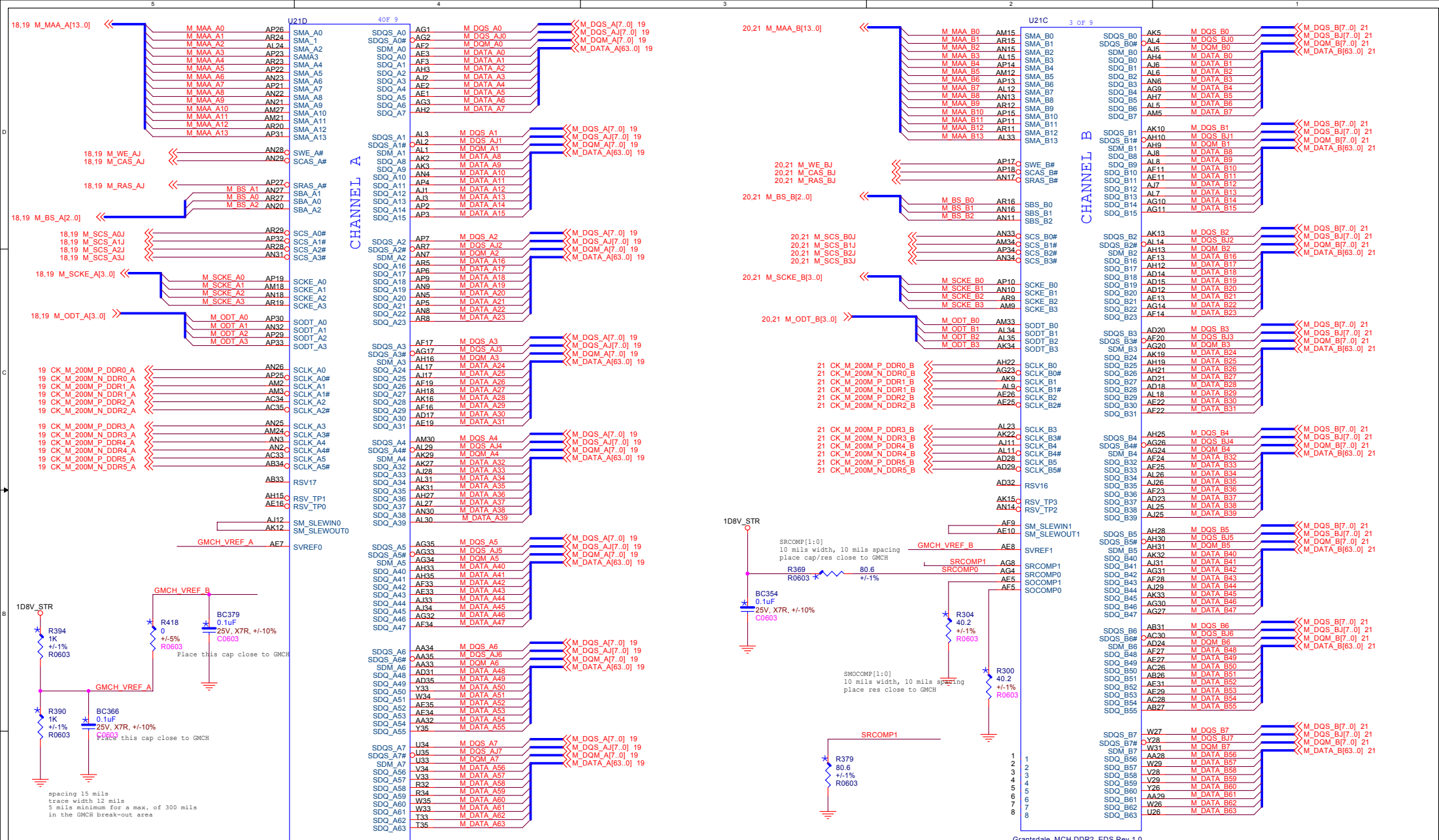
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Title: **LGA775 -2**

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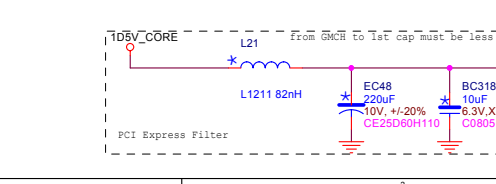
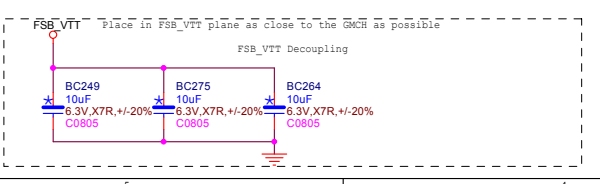
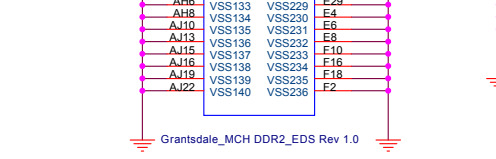
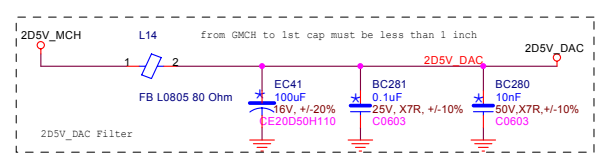
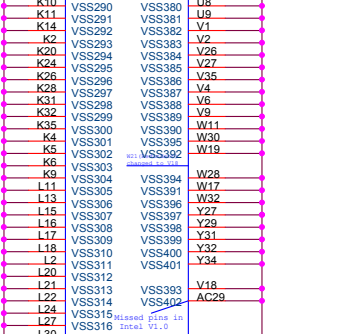
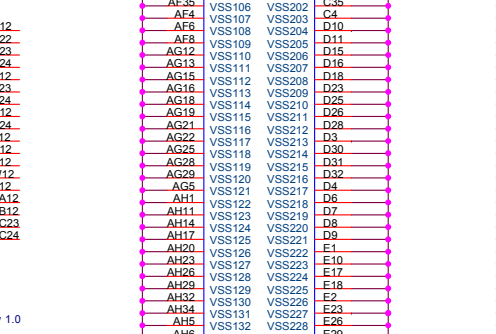
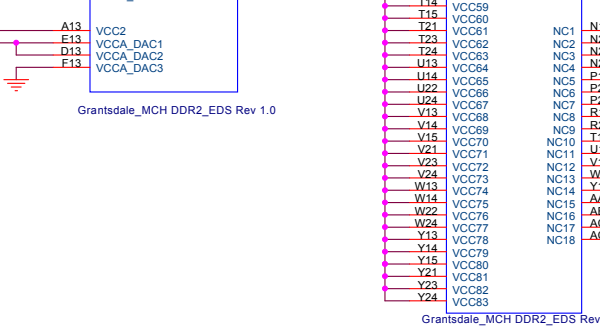
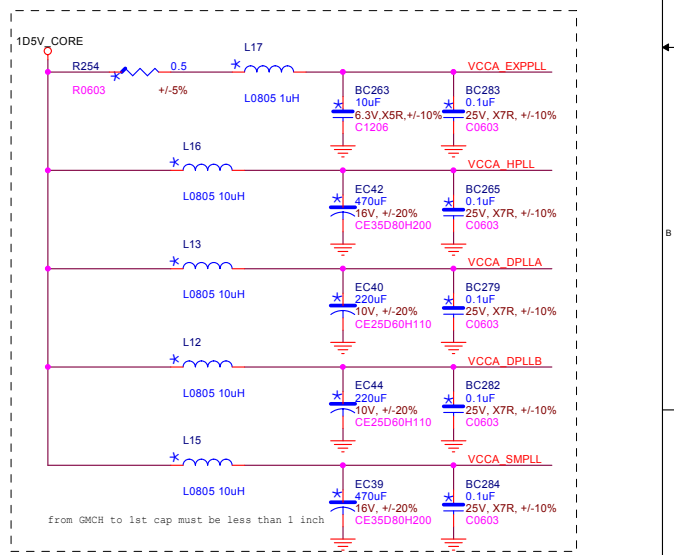
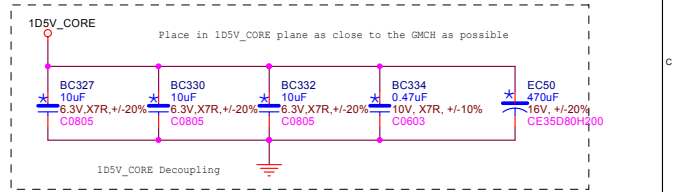
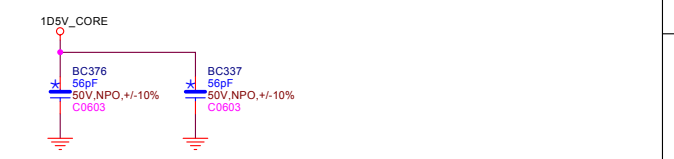
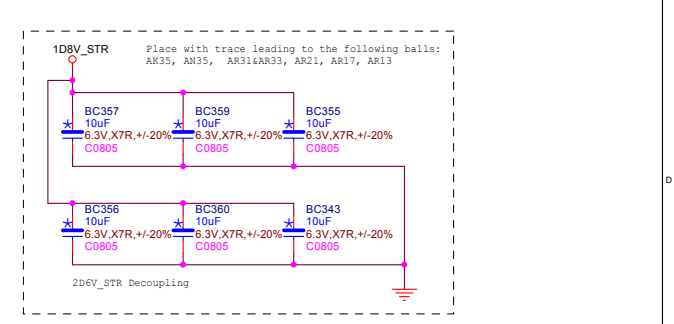
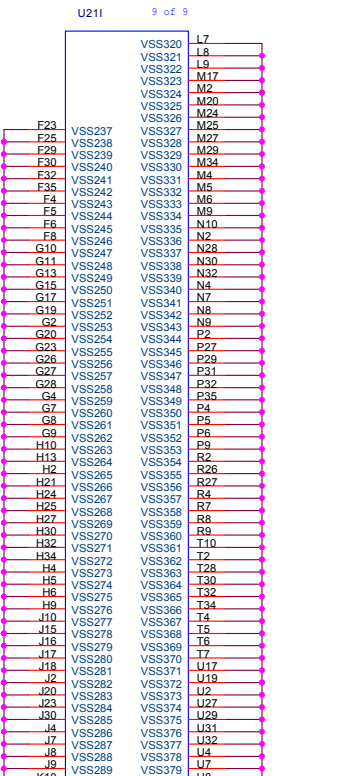
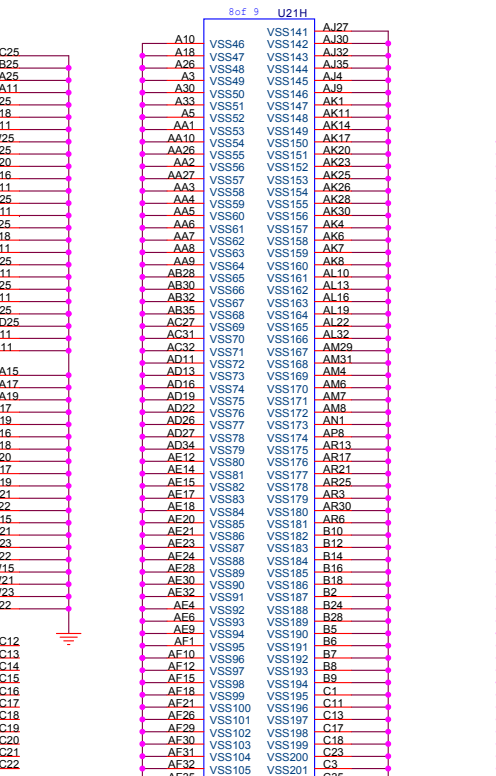
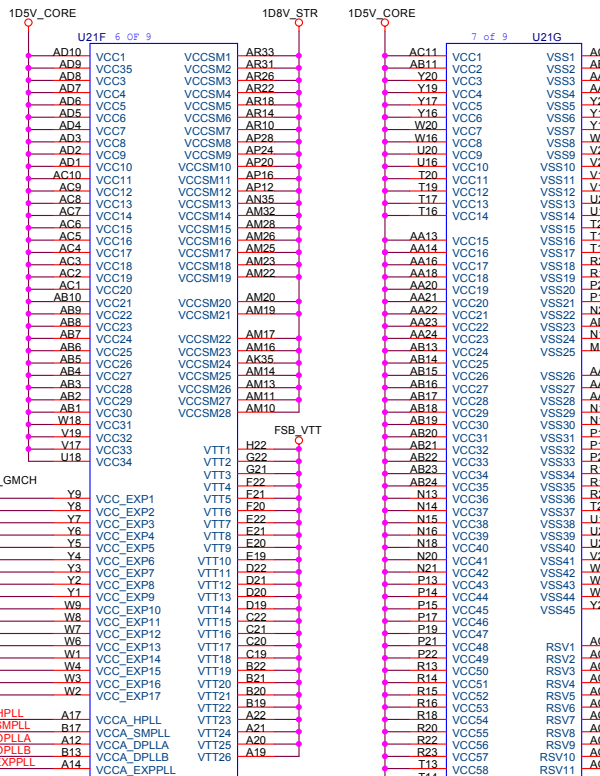


Grantsdale_MCH_DDR2_EDS Rev 1.0

Grantsdale_MCH_DDR2_EDS Rev 1.0



Title			Grantsdale DDR2 GMCH -2		
Size	Document Number	915A01 DDR2		Rev	B
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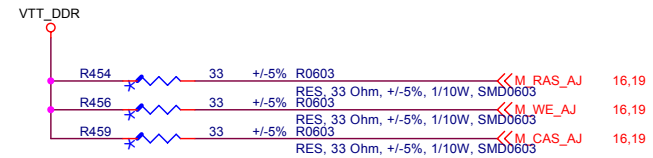
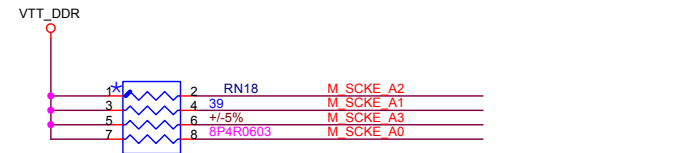
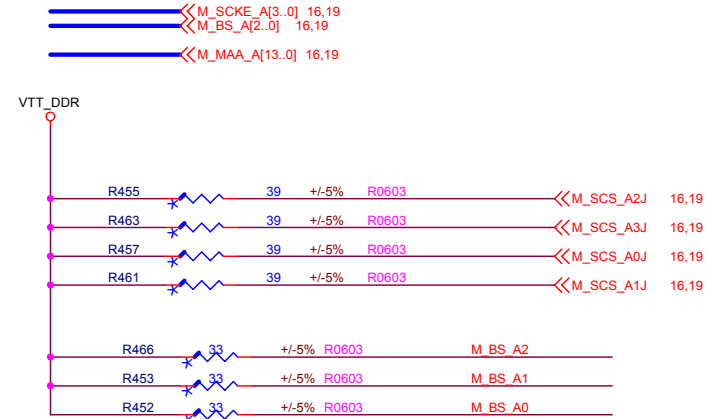
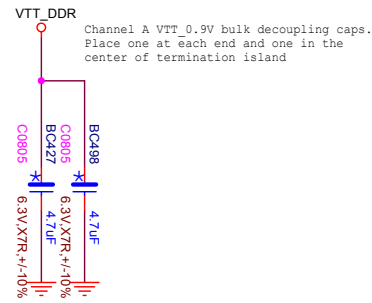
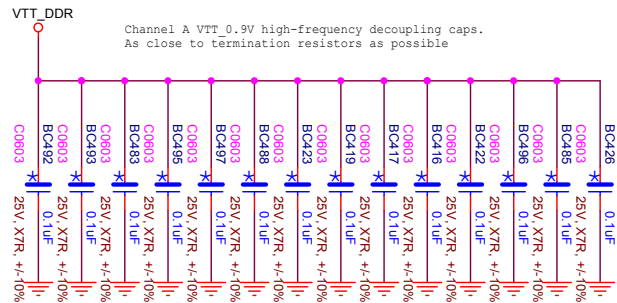
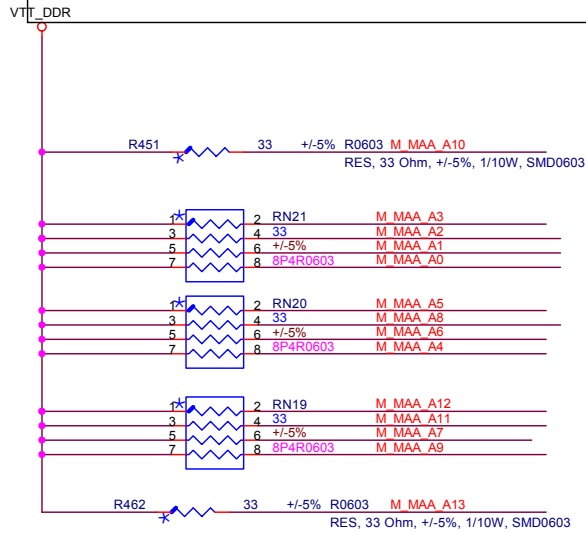
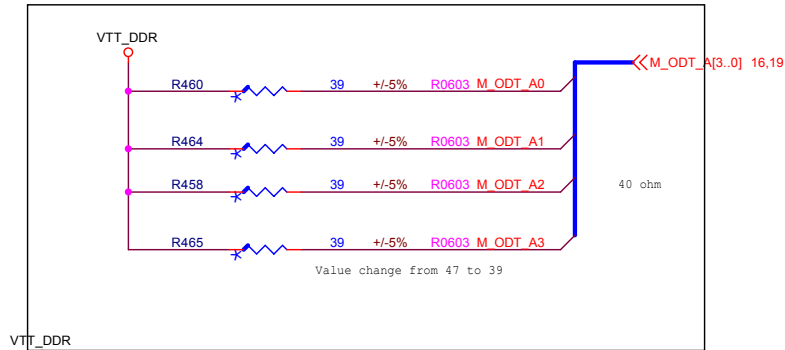


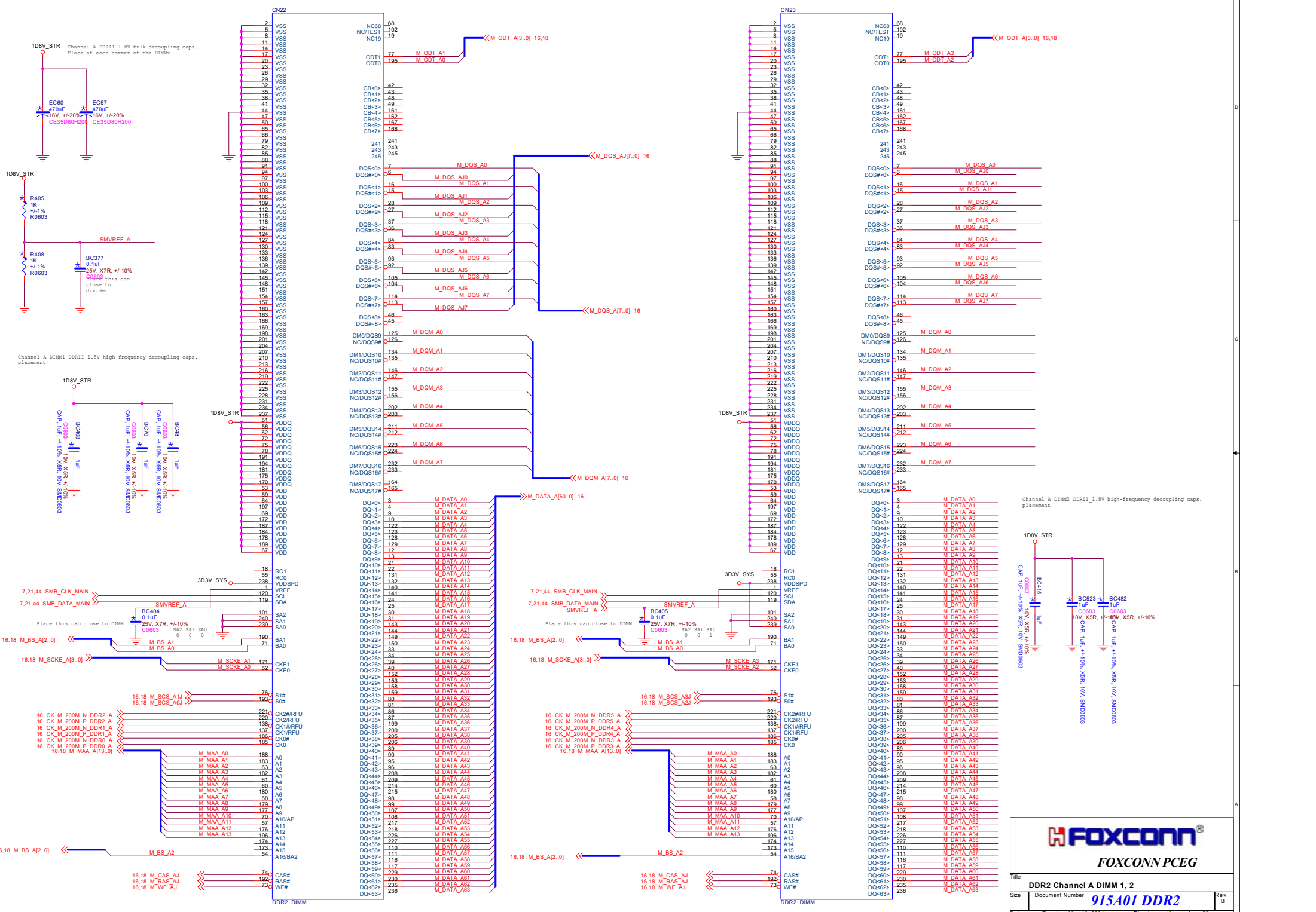
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Title: **Grantsdale DDR2 GMCH -3**

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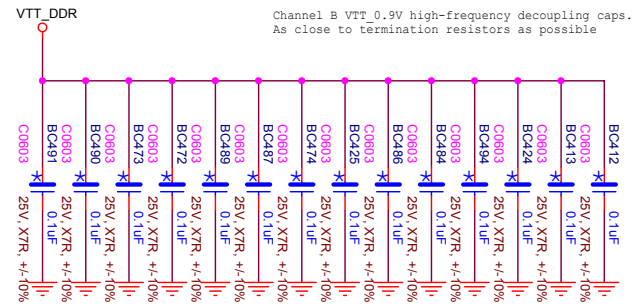
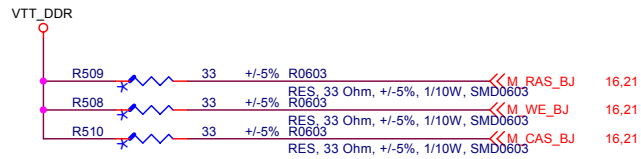
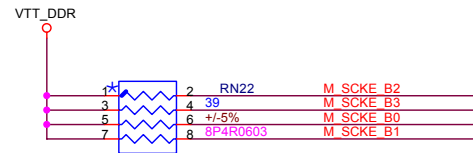
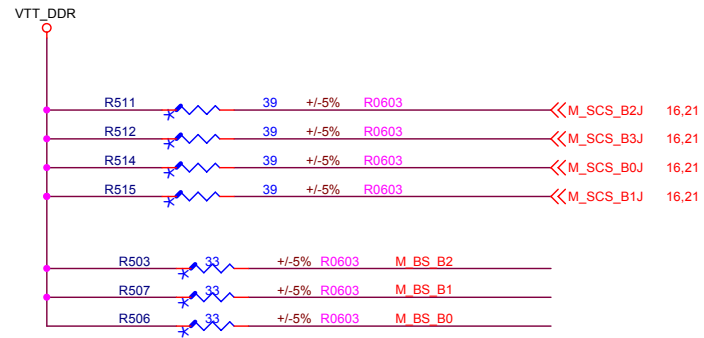
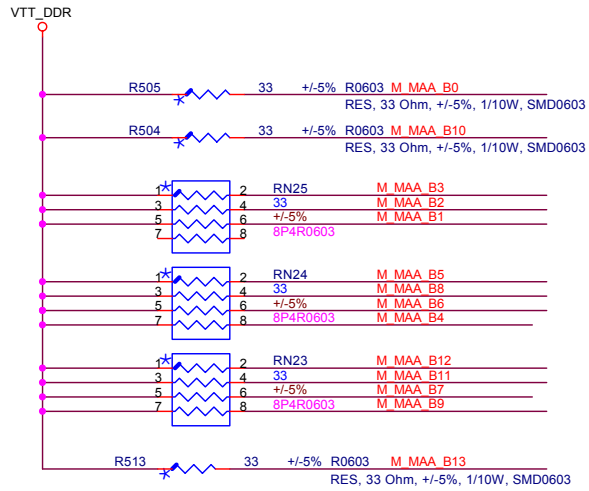
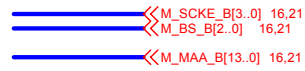
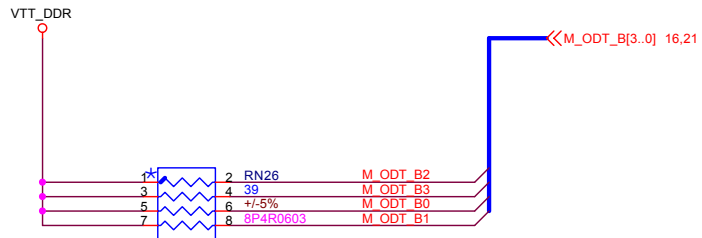
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File: **DDR2 Channel A DIMM 1, 2**

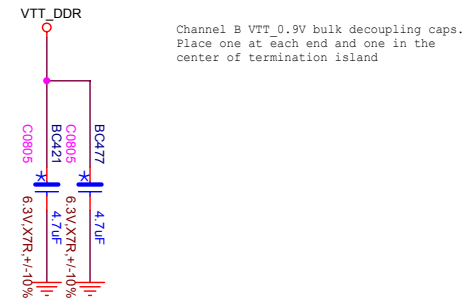
Size: Document Number **915A01 DDR2**

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Rev 8



Channel B VTT_0.9V high-frequency decoupling caps.
As close to termination resistors as possible

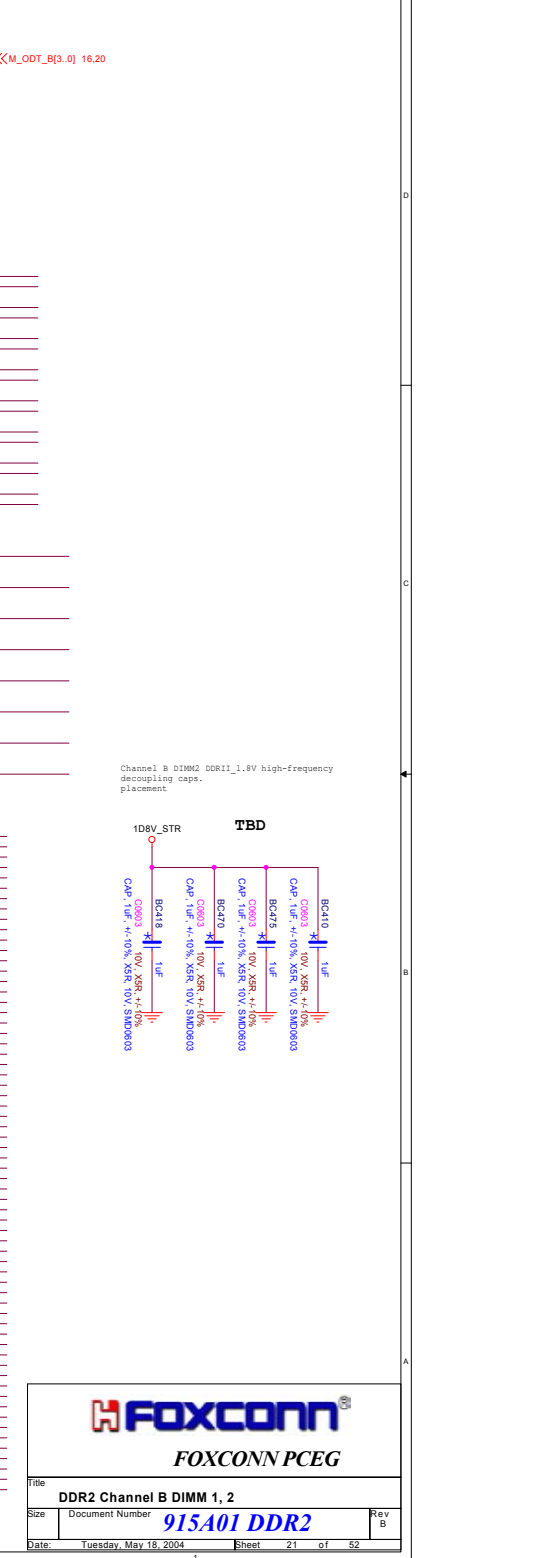
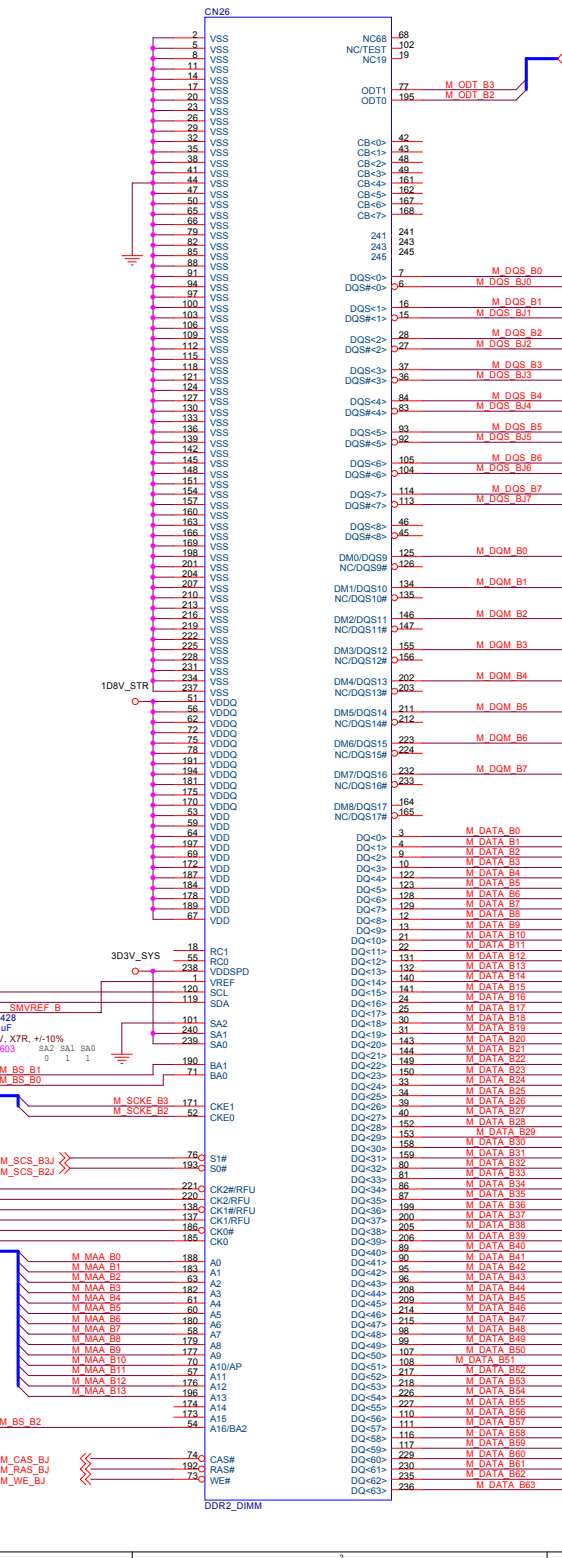
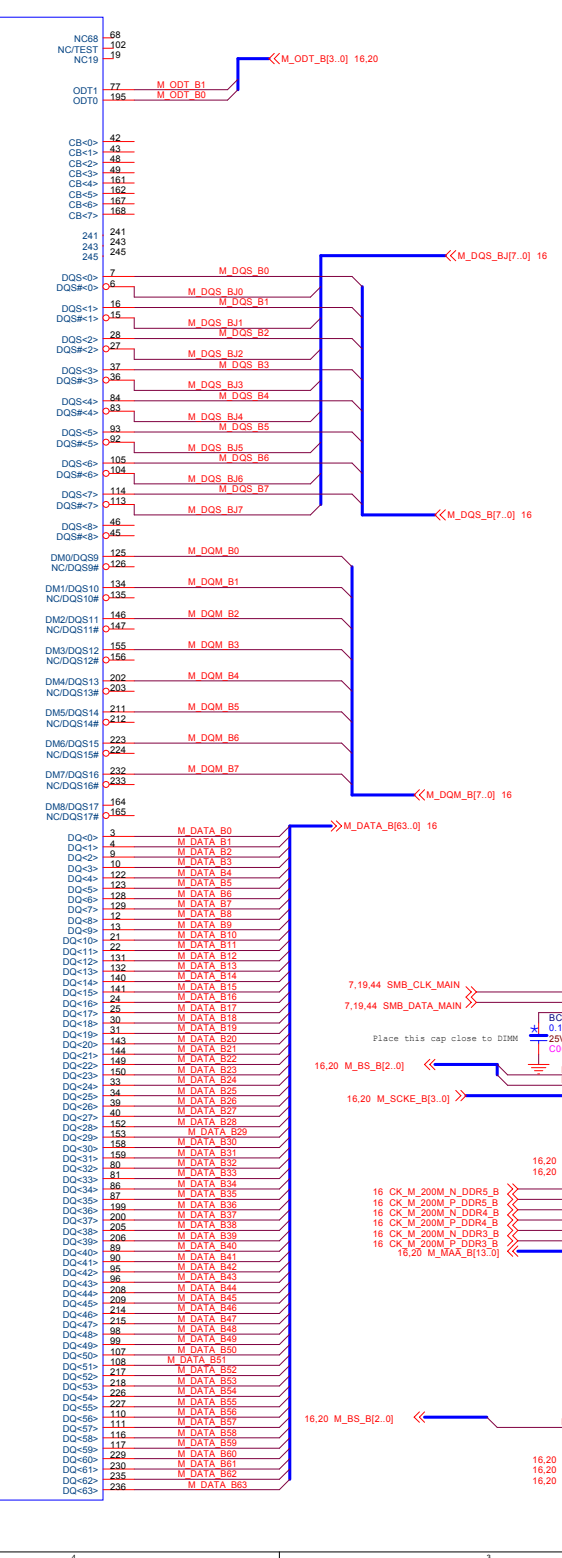
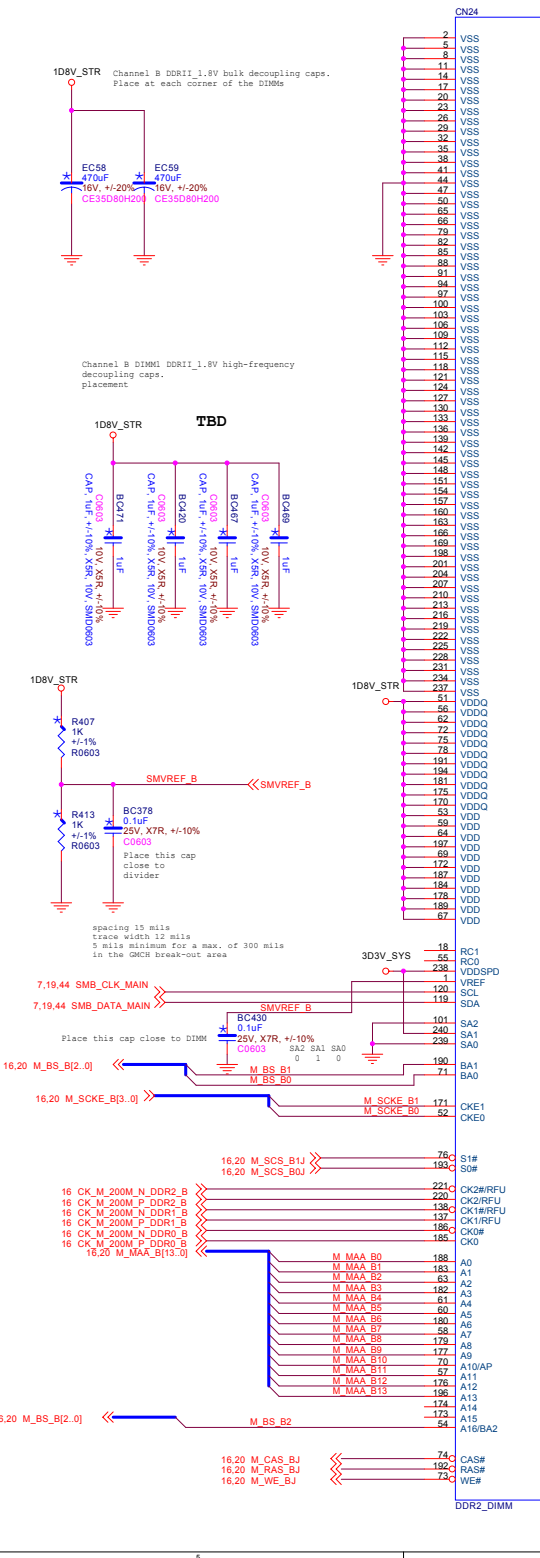


Channel B VTT_0.9V bulk decoupling caps.
Place one at each end and one in the center of termination island

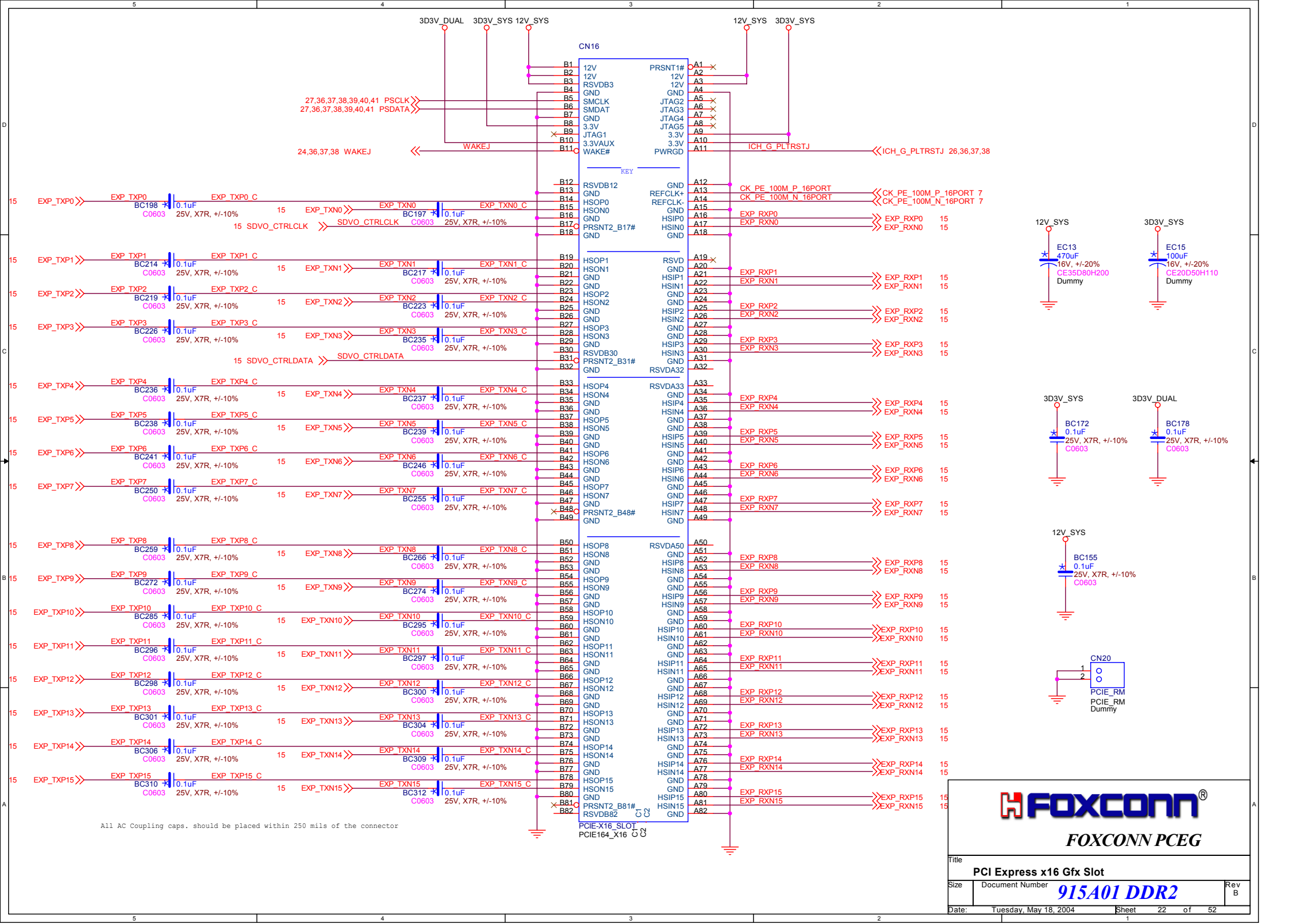


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Title DDR2 Channel B Termination		
Size	Document Number 915A01 DDR2	Rev B
Date:	Tuesday, May 18, 2004	Sheet 20 of 52

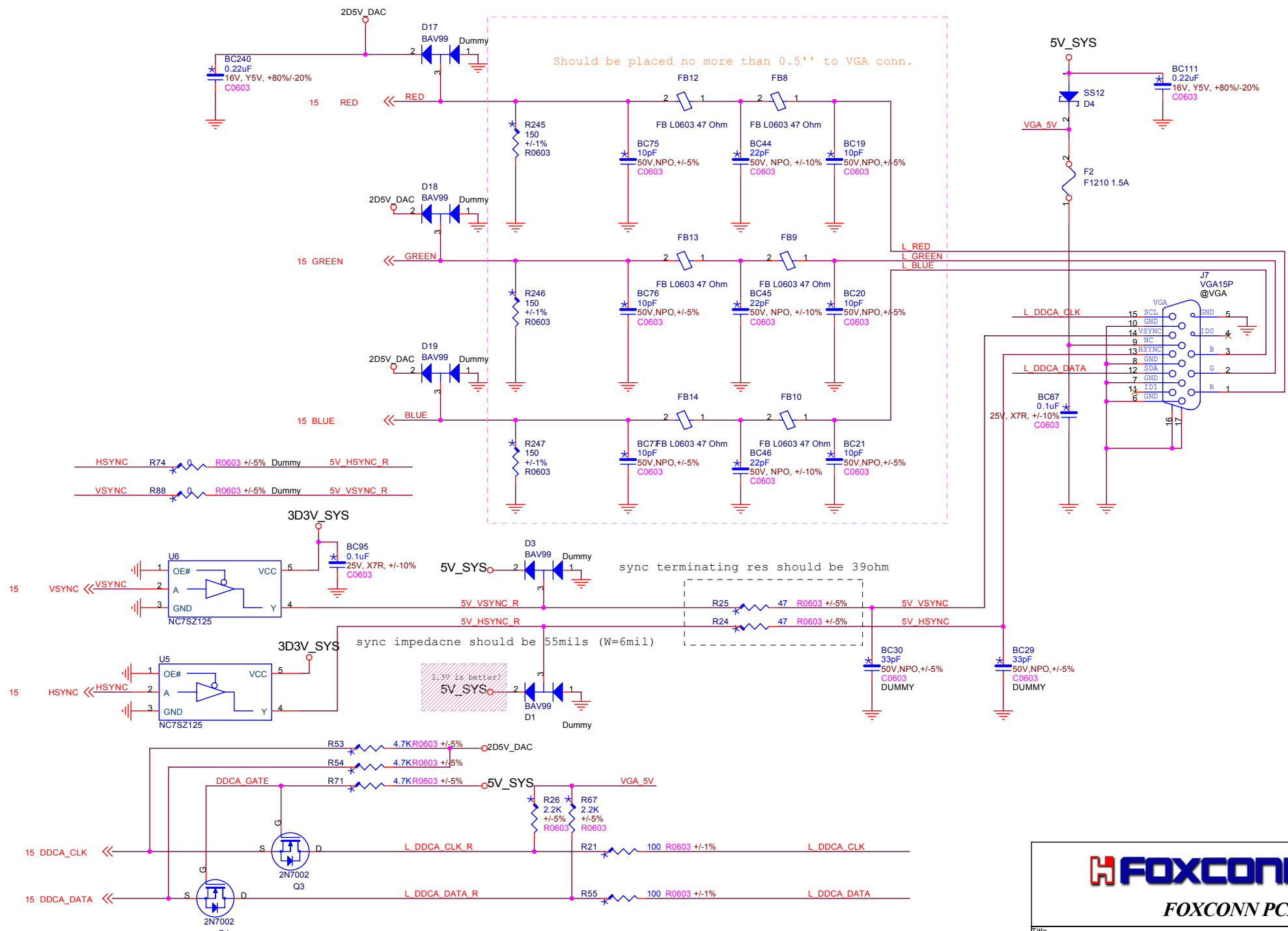


Title: DDR2 Channel B DIMM 1, 2
 Size: Document Number: 915A01 DDR2
 Date: Tuesday, May 18, 2004 Sheet 21 of 52



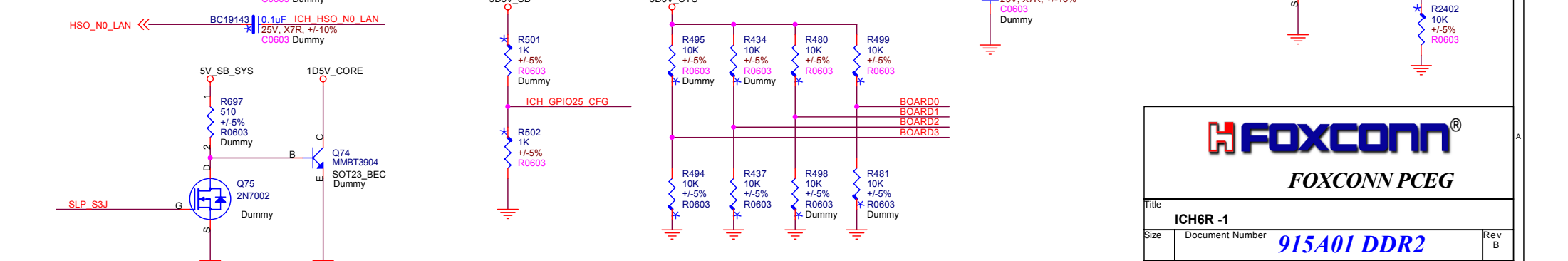
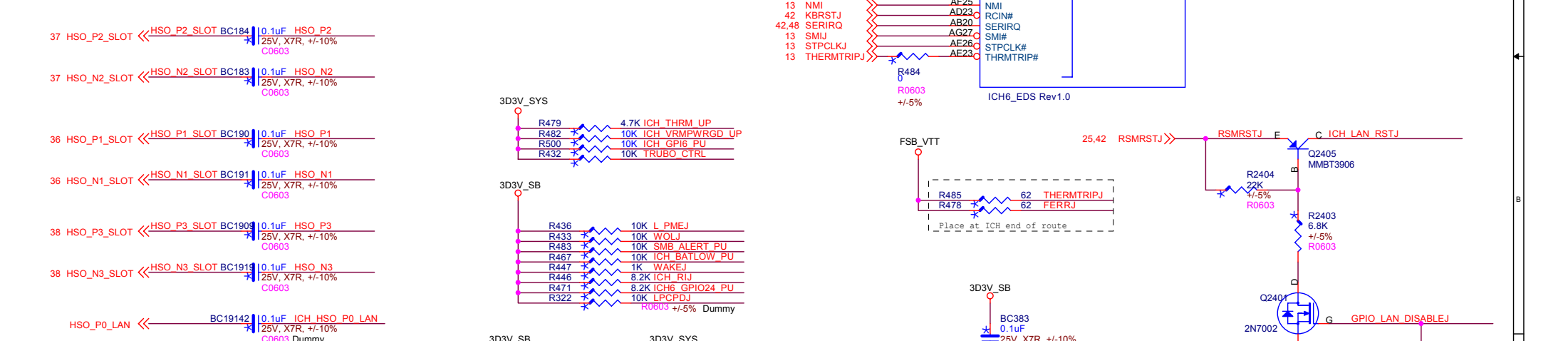
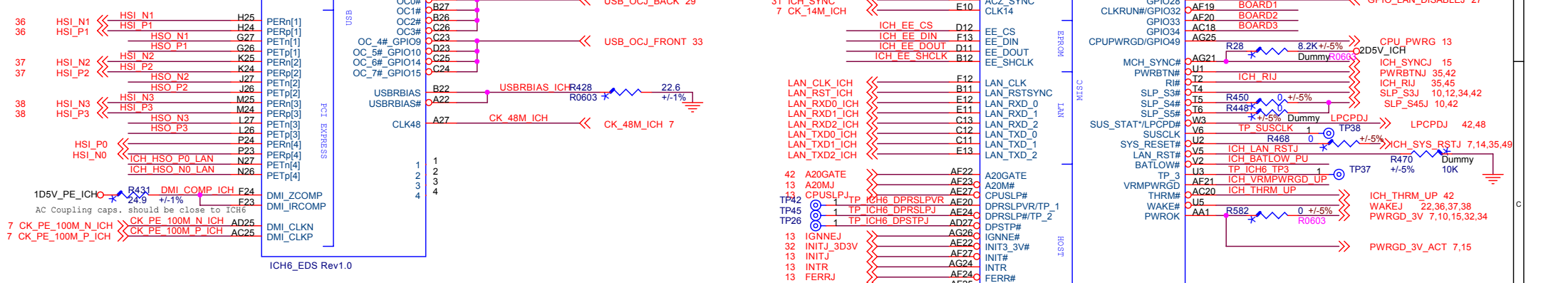
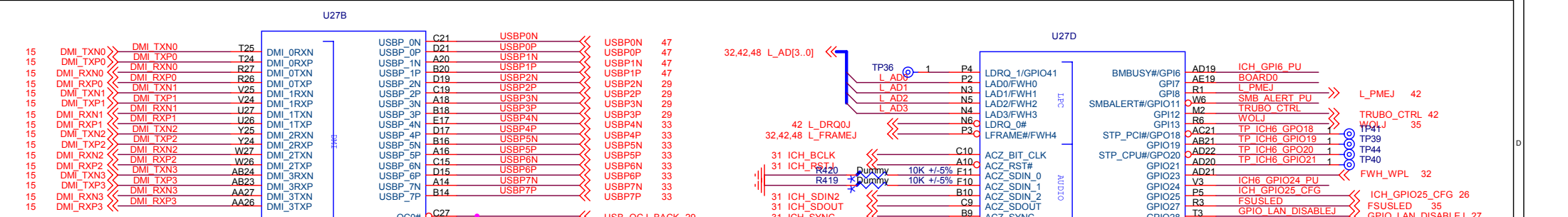
All AC Coupling caps. should be placed within 250 mils of the connector





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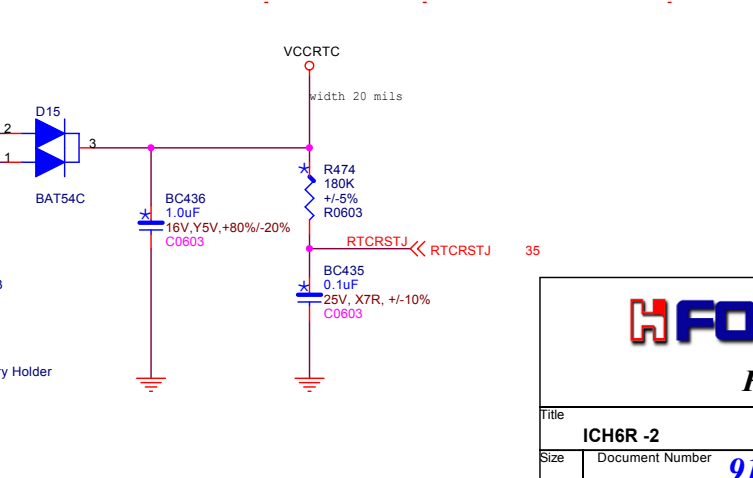
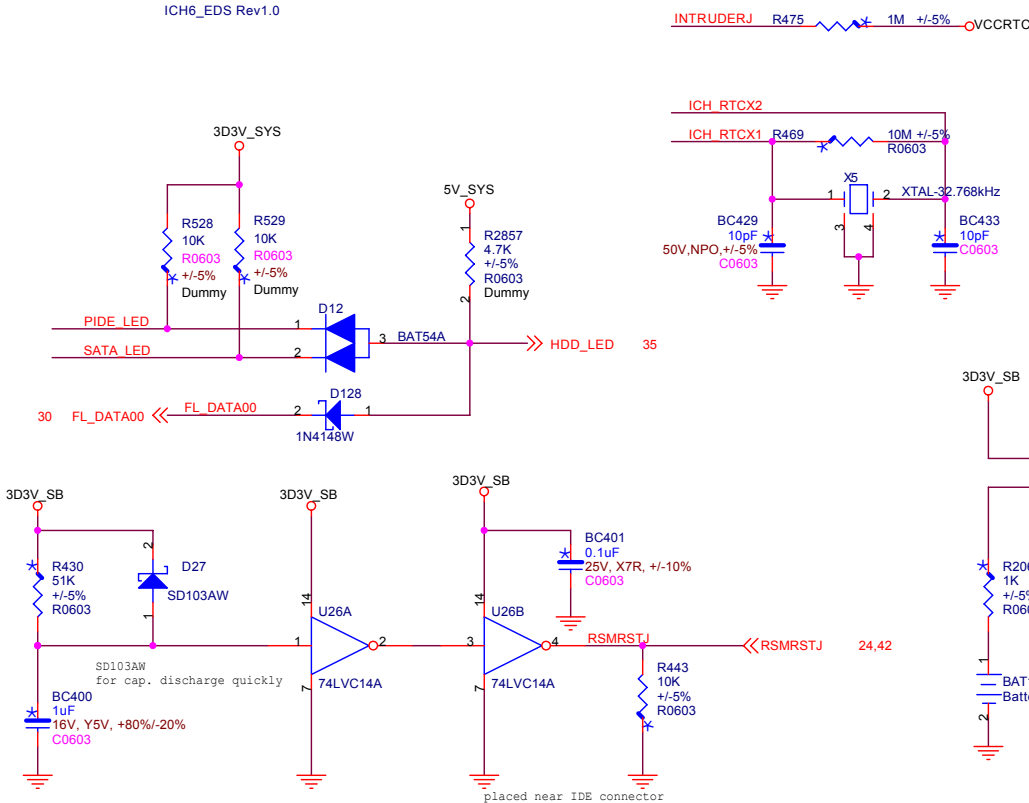
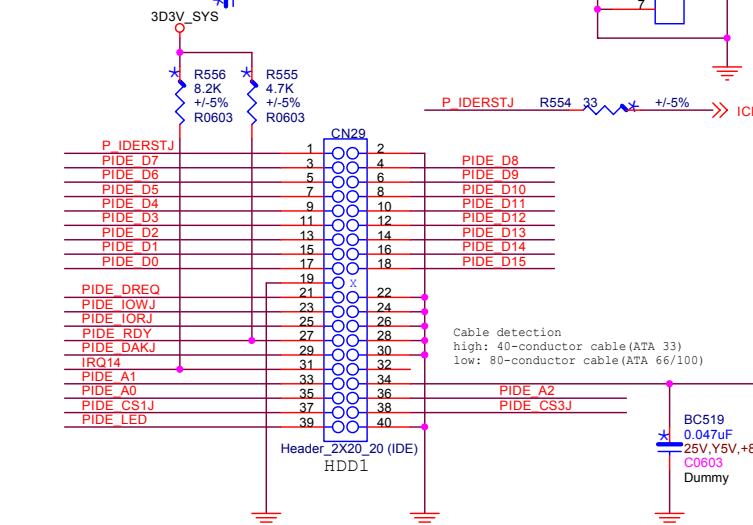
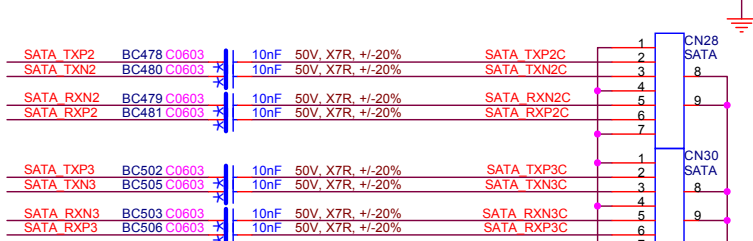
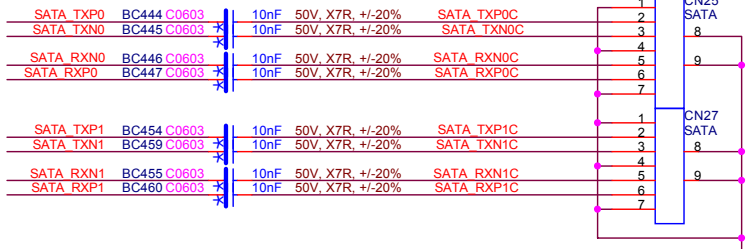
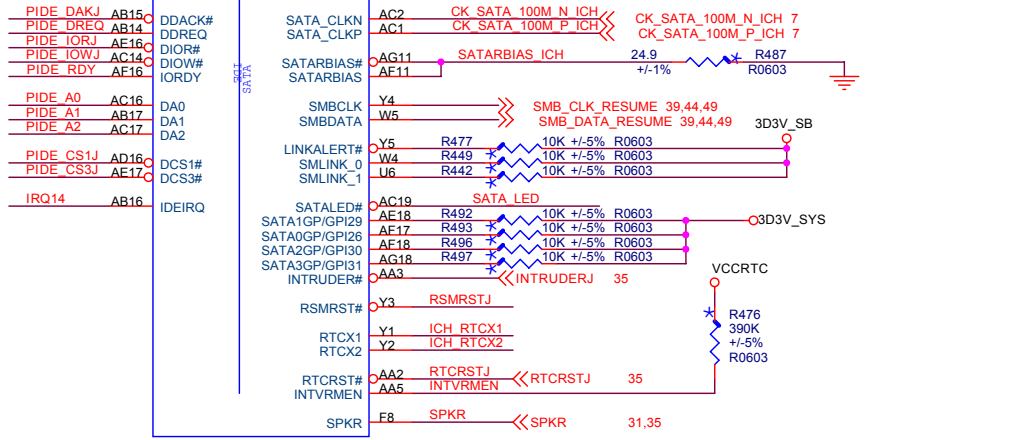
Title VGA Connector		
Size	Document Number 915A01 DDR2	Rev B
Date:	Tuesday, May 18, 2004	Sheet 23 of 52



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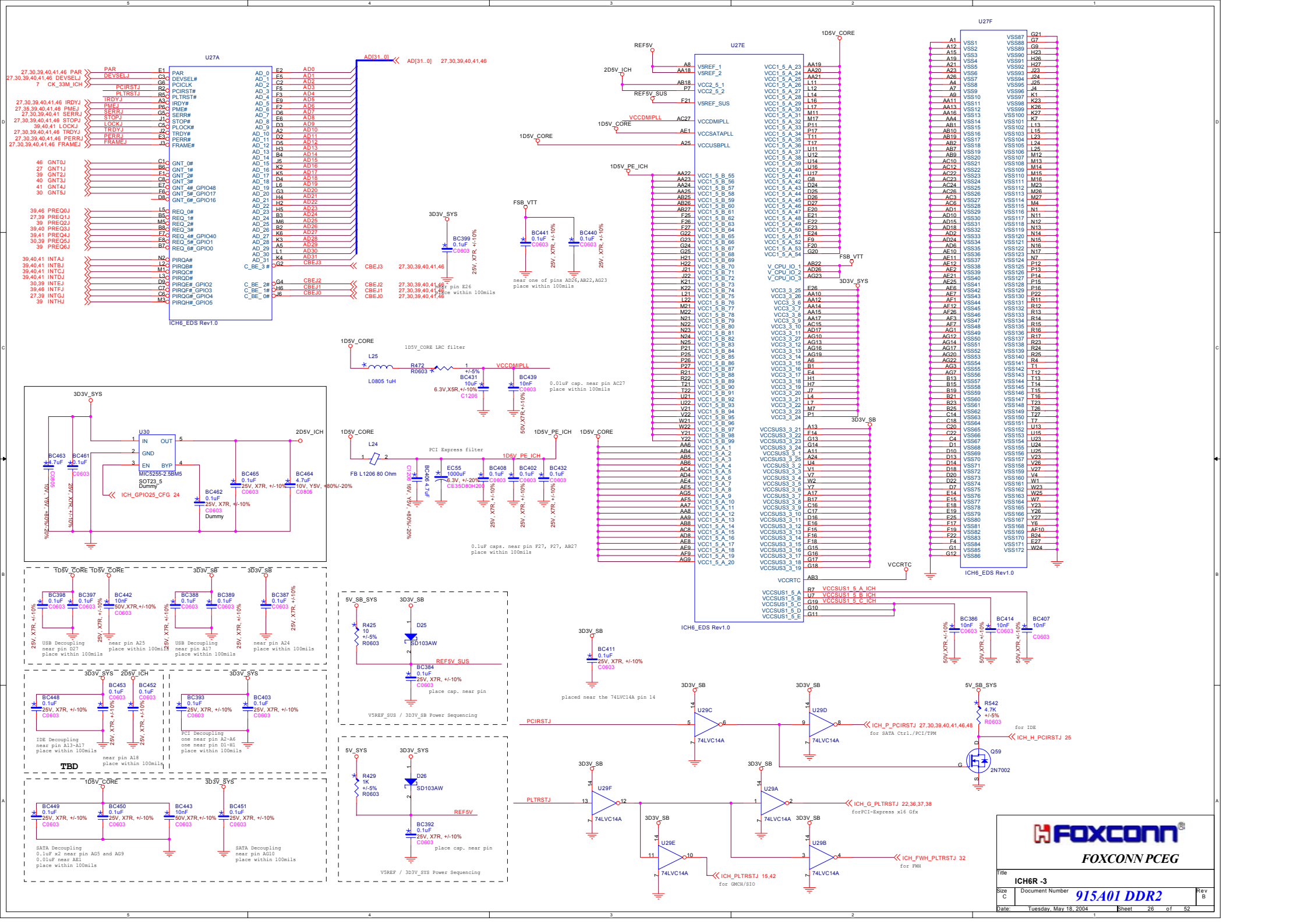
Title	ICH6R -1	
Size	Document Number	915A01 DDR2
Date:	Tuesday, May 18, 2004	Sheet 24 of 52
		Rev B

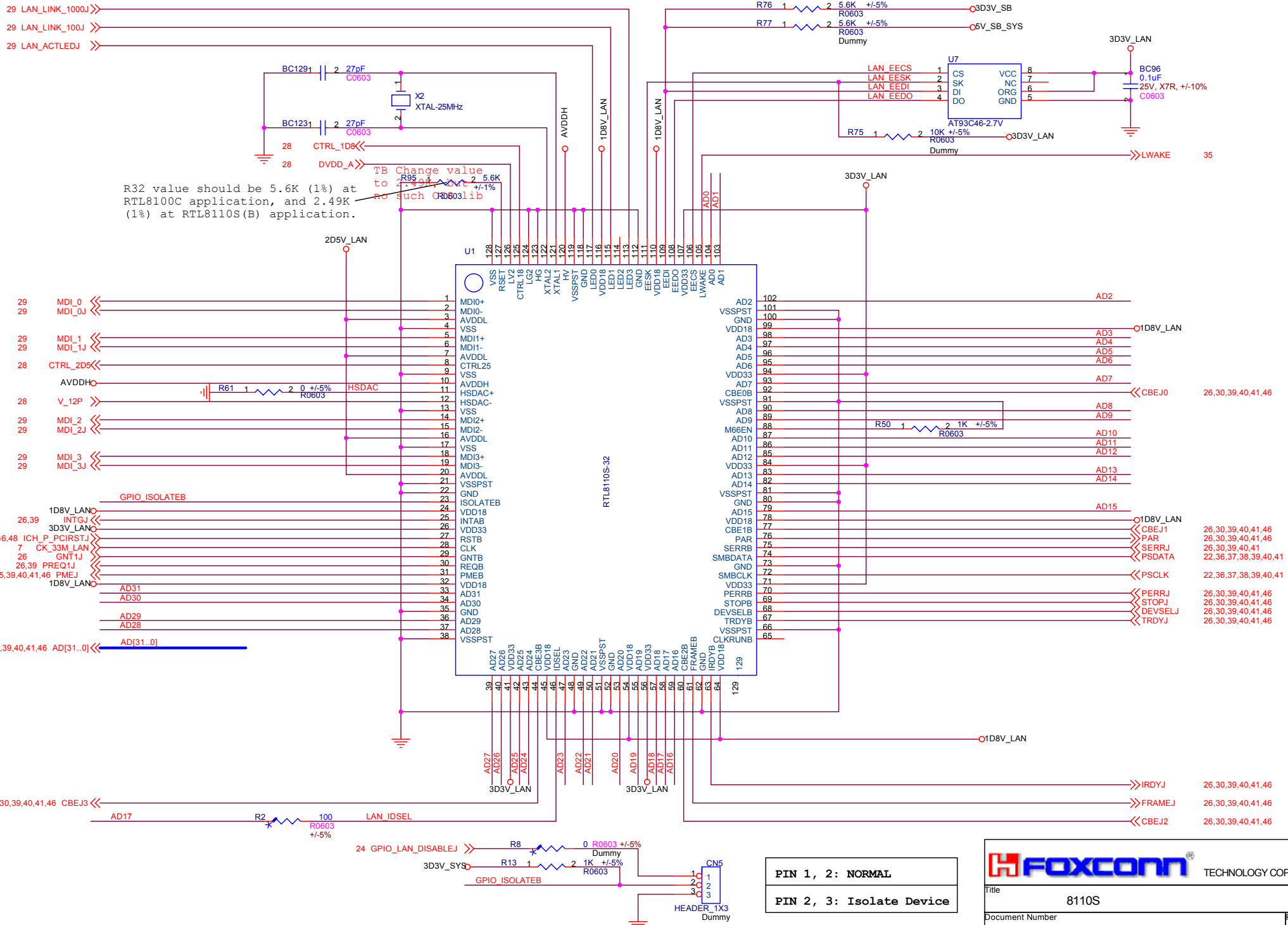
PIDE D15	AD13	DD_15	SATA0RXN	AE3	SATA_RXN0
PIDE D14	AG15	DD_14	SATA0RXP	AD3	SATA_RXP0
PIDE D13	AE15	DD_13	SATA0TXN	AG2	SATA_TXN0
PIDE D12	AC13	DD_12	SATA0TXP	AE2	SATA_TXP0
PIDE D11	AB13	DD_11	SATA1RXN	AC5	SATA_RXN1
PIDE D10	AB12	DD_10	SATA1RXP	AD5	SATA_RXP1
PIDE D9	AF13	DD_9	SATA1TXN	AE4	SATA_TXN1
PIDE D8	AE13	DD_8	SATA1TXP	AG4	SATA_TXP1
PIDE D7	AB11	DD_7	SATA2RXN	AD7	SATA_RXN2
PIDE D6	AD11	DD_6	SATA2RXP	AC7	SATA_RXP2
PIDE D5	AC11	DD_5	SATA2TXN	AE6	SATA_TXN2
PIDE D4	AE14	DD_4	SATA2TXP	AG6	SATA_TXP2
PIDE D3	AD12	DD_3	SATA3RXN	AD9	SATA_RXN3
PIDE D2	AF14	DD_2	SATA3RXP	AE8	SATA_RXP3
PIDE D1	AE15	DD_1	SATA3TXN	AG8	SATA_TXN3
PIDE D0	AD14	DD_0	SATA3TXP	AG8	SATA_TXP3



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Title		ICH6R -2	
Size	Document Number	915A01 DDR2	
Date:	Tuesday, May 18, 2004	Sheet	25 of 52





R32 value should be 5.6K (1%) at RTL8100C application, and 2.49K (1%) at RTL8110S(B) application.

TB Change value to 2.49K +/-1% no such component lib

PIN 1, 2: NORMAL
 PIN 2, 3: Isolate Device

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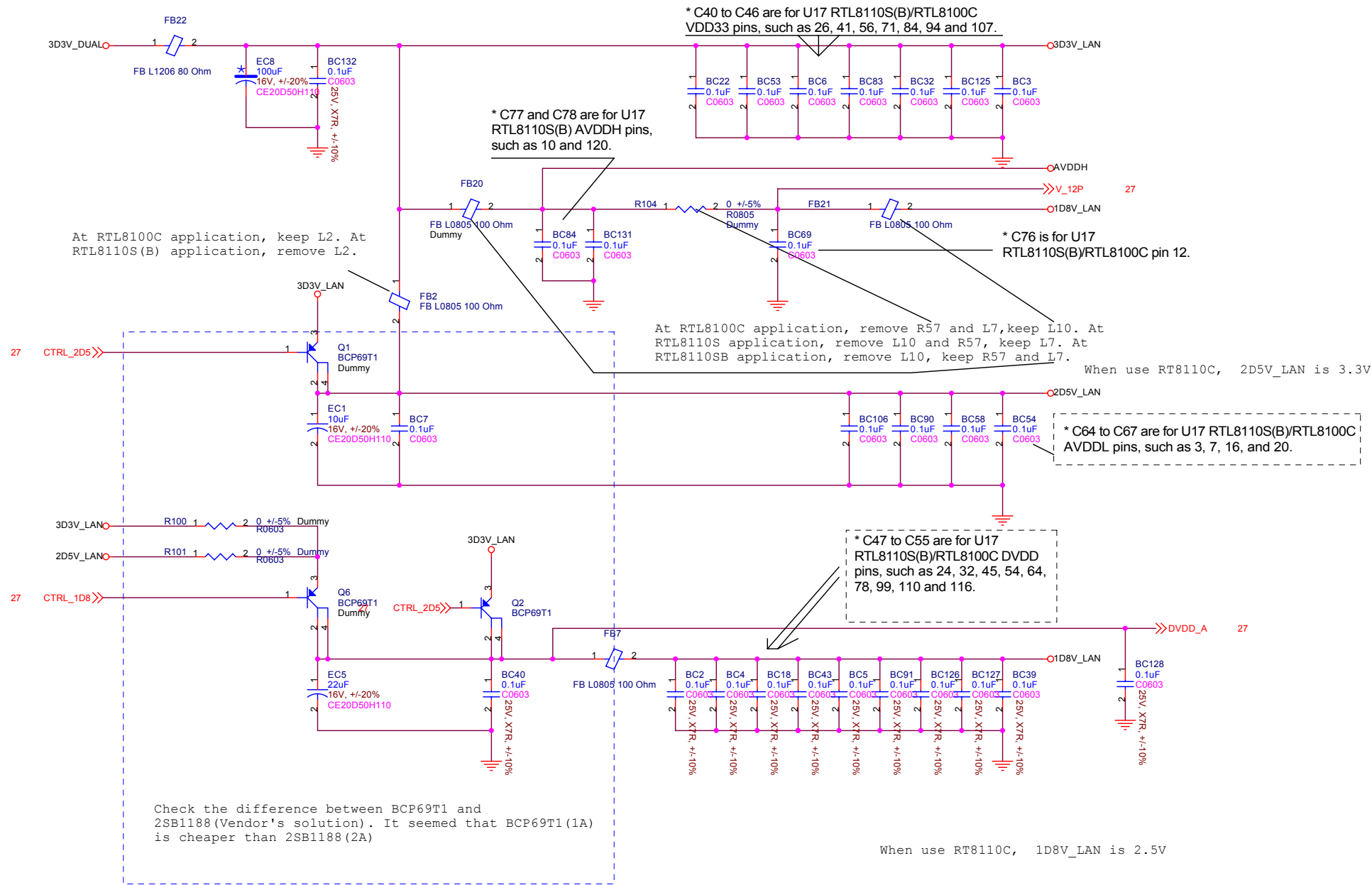
Title: 8110S

Document Number: 915A01 DDR2

Date: Tuesday, May 18, 2004

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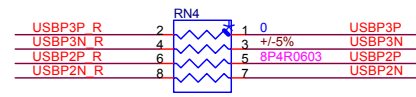
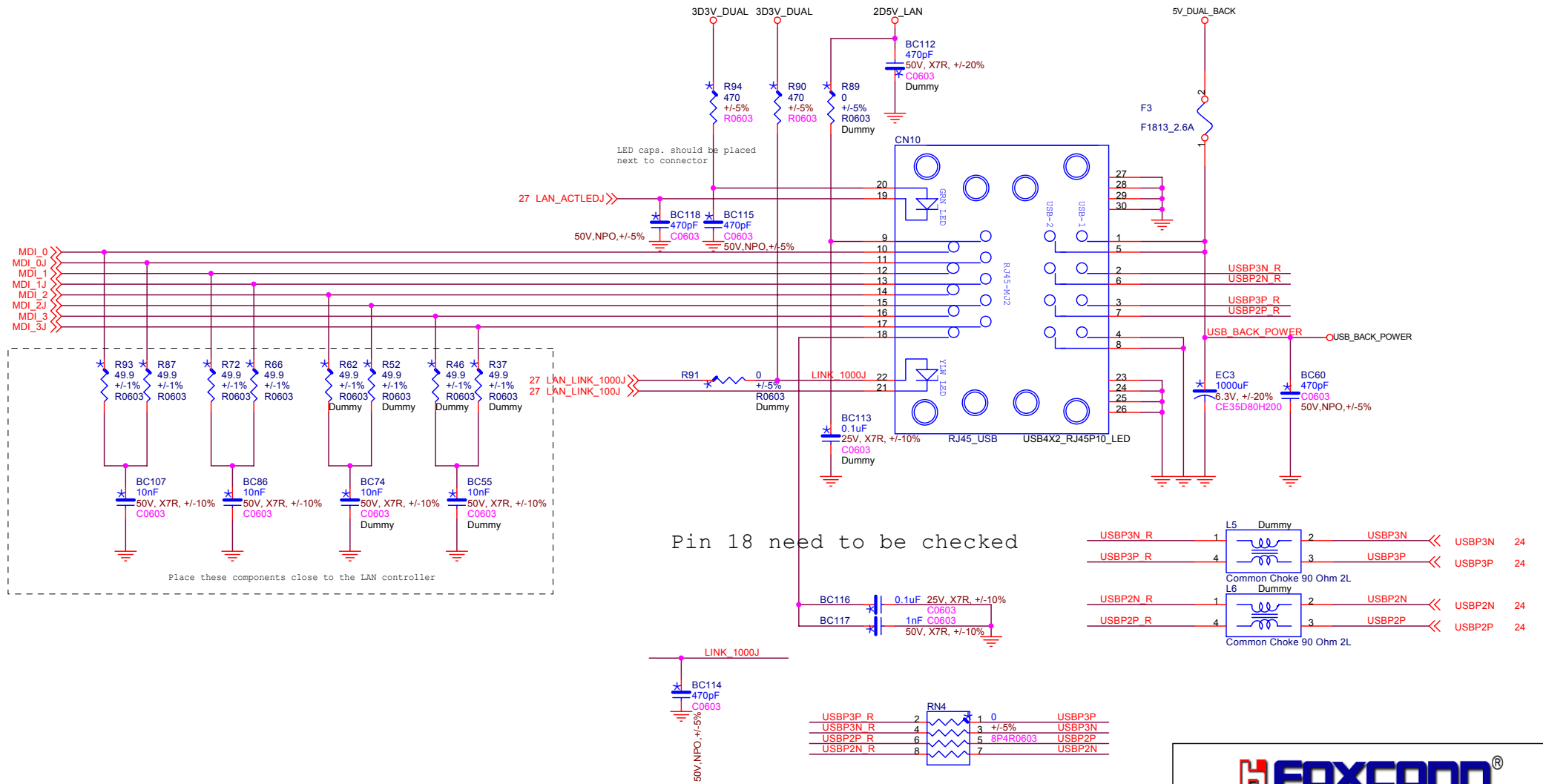
Rev B




BACK PANEL (LAN + 2 USB SLOT)

USE CONNECTOR A74314-001 WITH 10/100 DESIGNS (Foxconn P/N:UB11123-L71-001)

USE CONNECTOR A74307-002 WITH GIGABIT DESIGNS (Foxconn P/N:UB11123-L91X8-1)

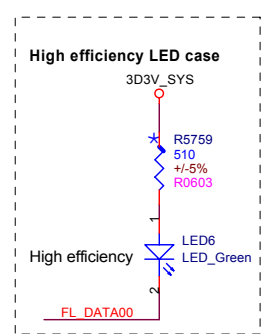
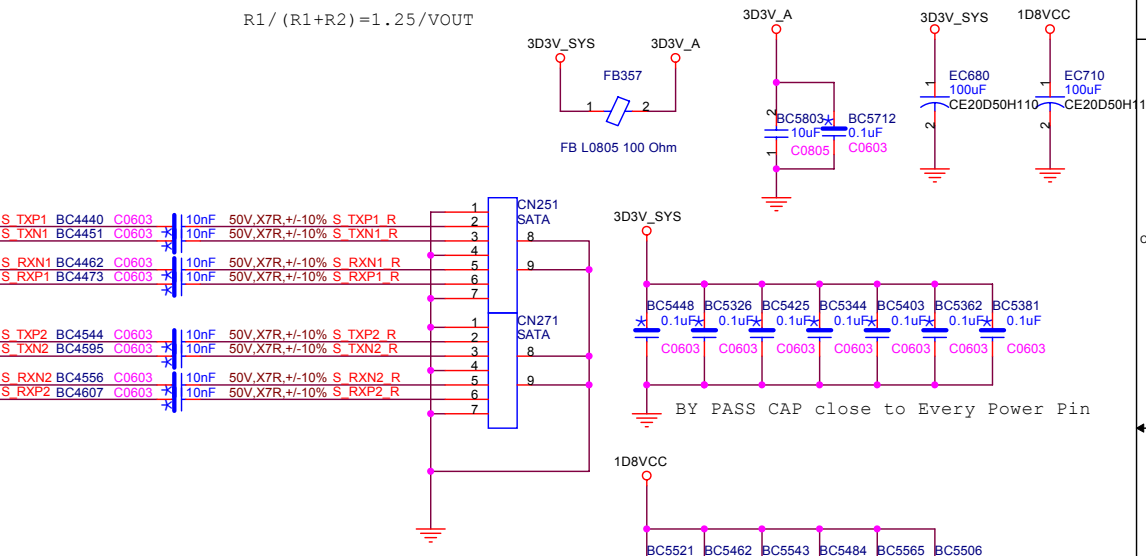
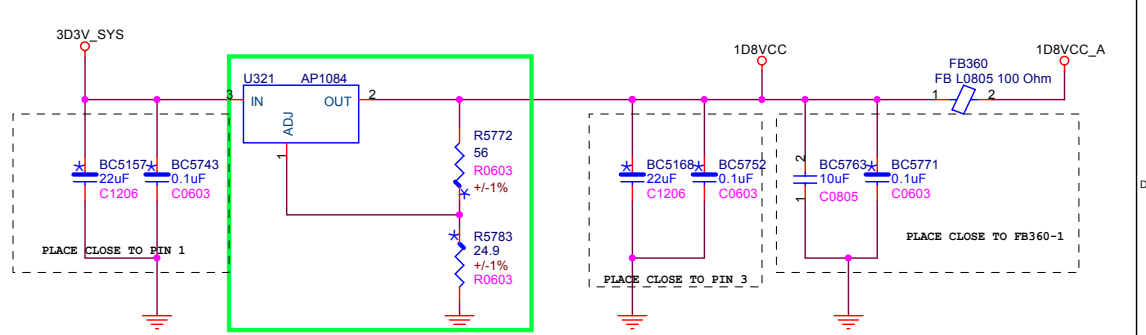
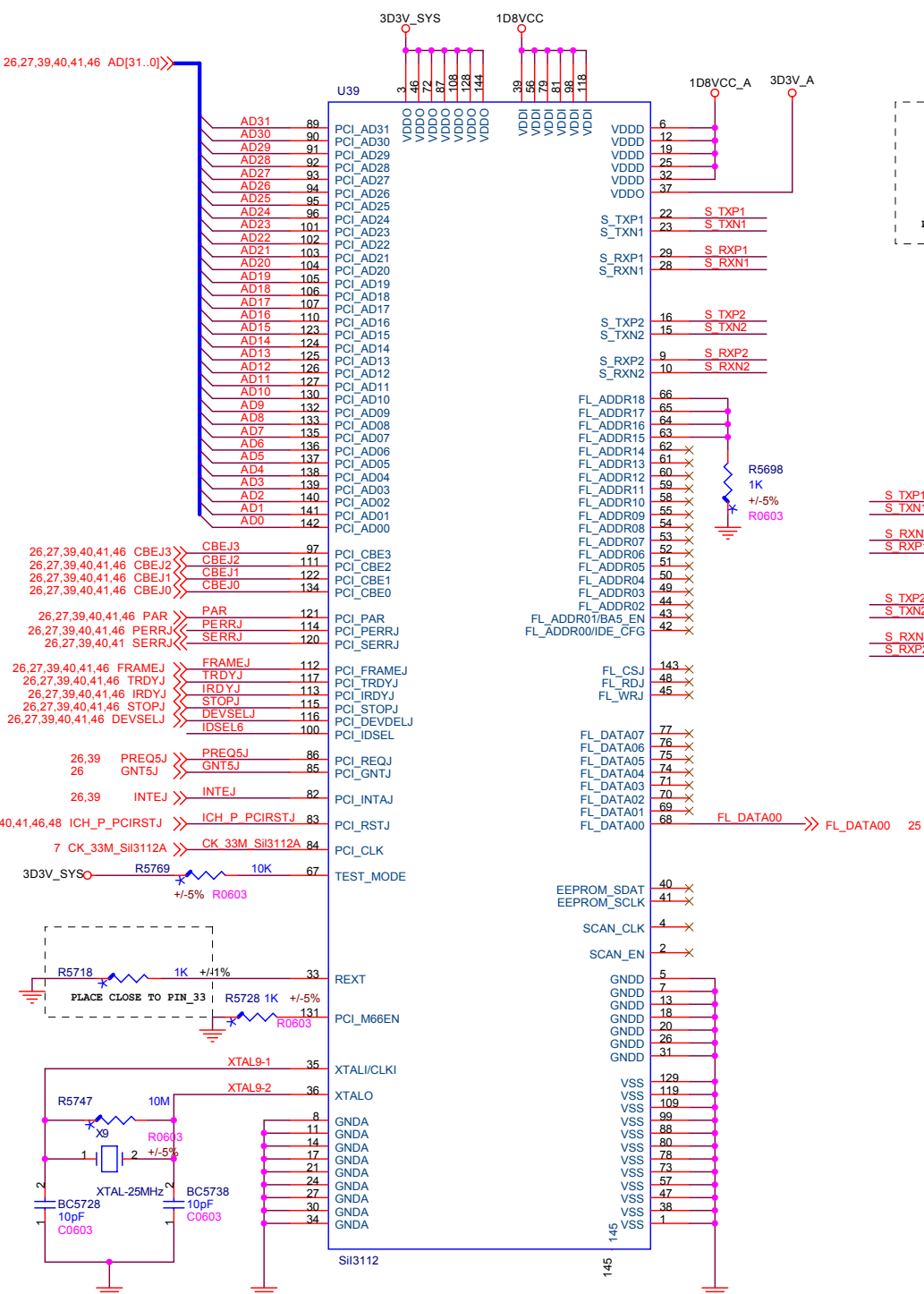


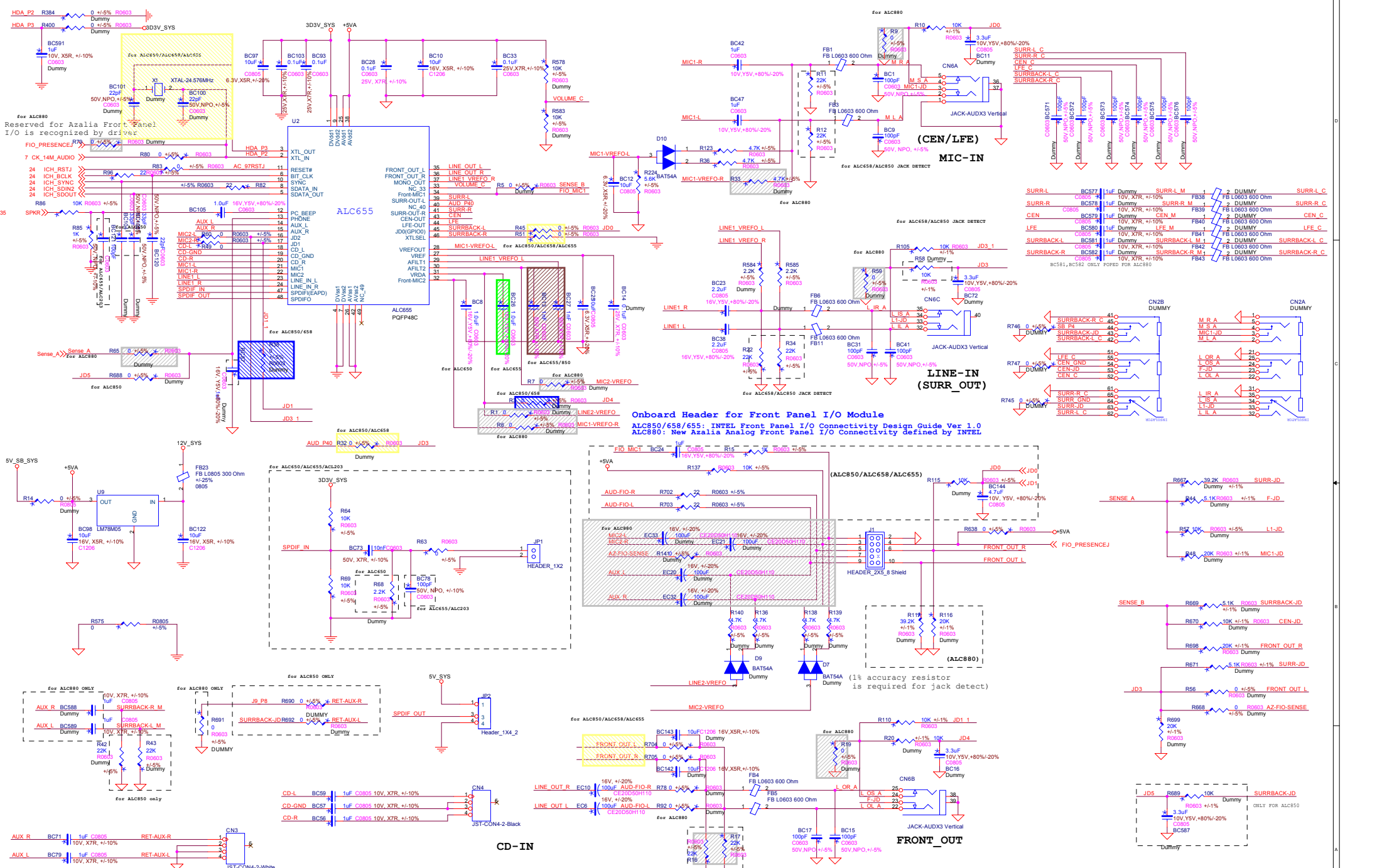
two common chokes and one RN co-layout



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Title		
LAN / XDP Connectors		
Size	Document Number	Rev
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Connector	Signal	Component	Value	Notes
SURR-L	SURR-L-M	BC571	1000pF	DUMMY
	SURR-L-C	BC572	1000pF	DUMMY
SURR-R	SURR-R-M	BC573	1000pF	DUMMY
	SURR-R-C	BC574	1000pF	DUMMY
CEN	CEN-M	BC575	1000pF	DUMMY
	CEN-C	BC576	1000pF	DUMMY
LFE	LFE-M	BC577	1000pF	DUMMY
	LFE-C	BC578	1000pF	DUMMY
SURRBACK-L	SURRBACK-L-M	BC579	1000pF	DUMMY
	SURRBACK-L-C	BC580	1000pF	DUMMY
SURRBACK-R	SURRBACK-R-M	BC581	1000pF	DUMMY
	SURRBACK-R-C	BC582	1000pF	DUMMY

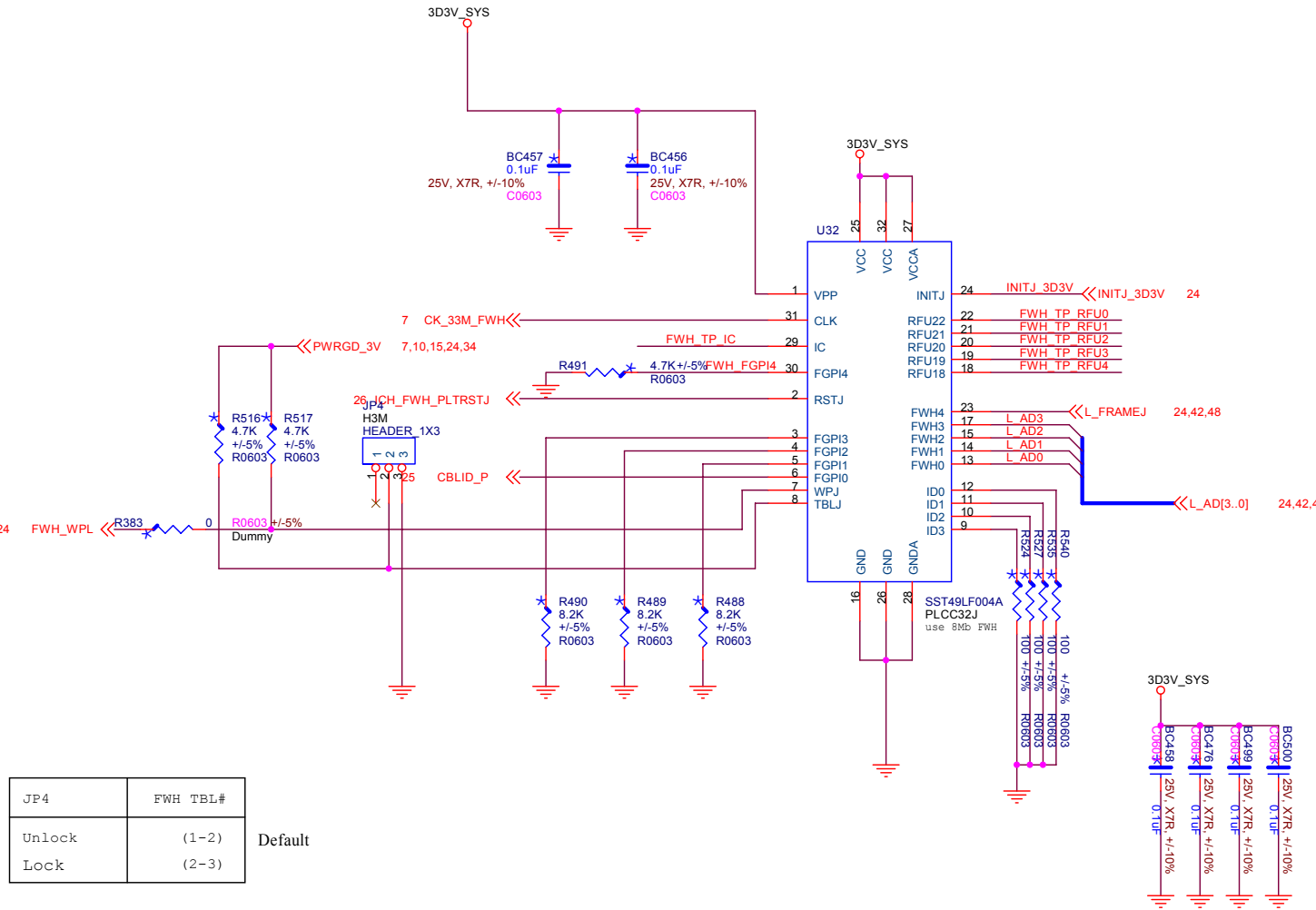
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Title: AC'97 2.3/Azalia Codec		Rev: B
Size: Custom	Document Number: 915A01 DDR2	Rev: B
Date: Tuesday, May 18, 2004	Sheet: 31 of 52	

JP2	MODE
NORMAL	(1-2)
Safe Speed	(2-3)
RECOVERY	OPEN

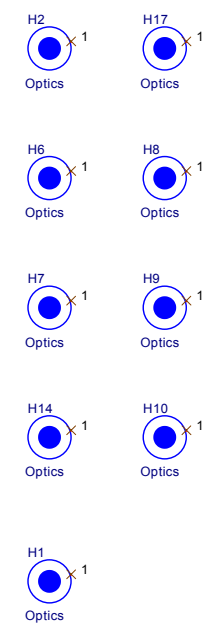
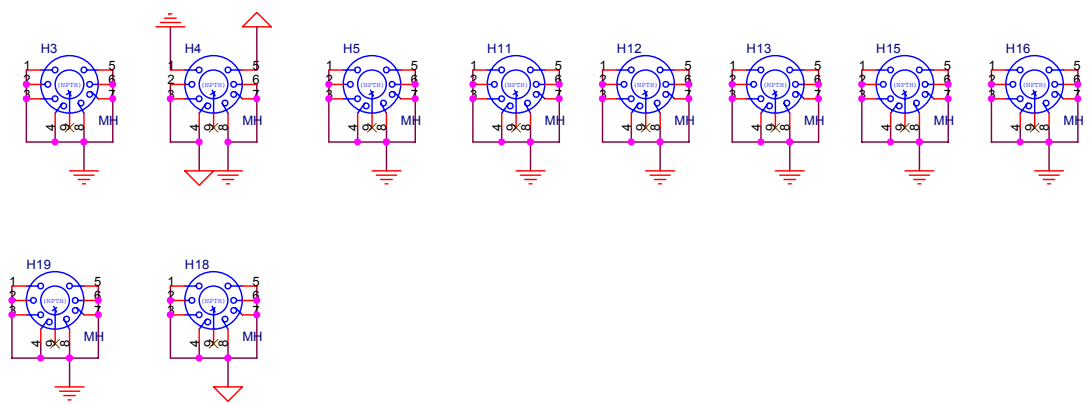
Default

TBD		
AC_SDOUT functional strap definitions	signal	usage
Platform	865	AC_SDOUT Safe mode
Grantsdale	AC2_SDOUT	XOR chain(TBD)



JP4	FWH TBL#
Unlock	(1-2)
Lock	(2-3)

Default

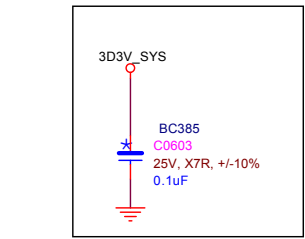
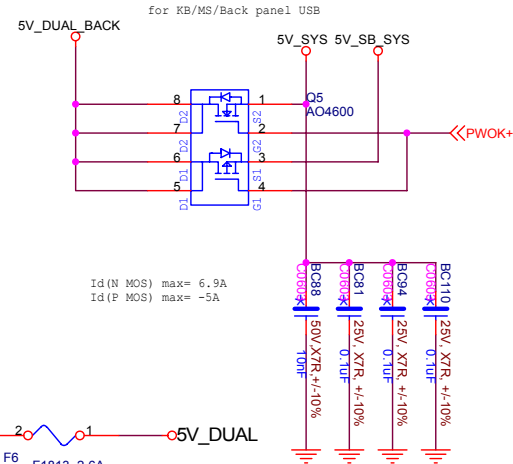
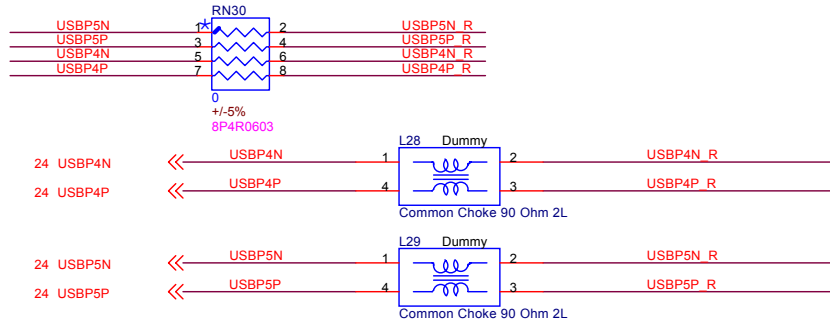


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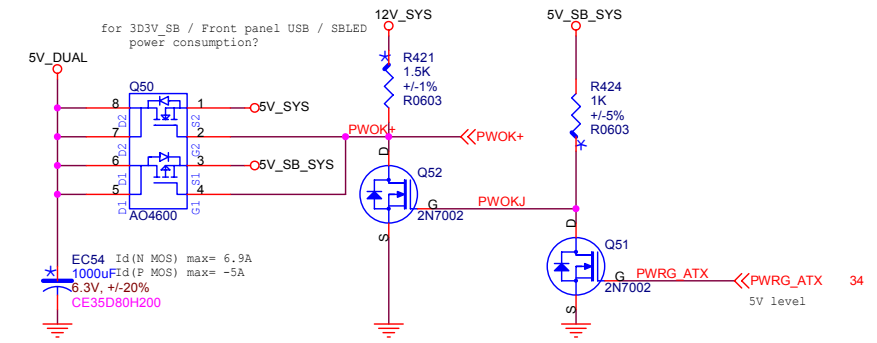
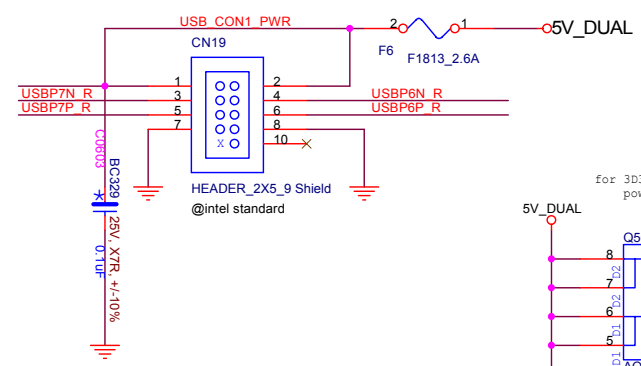
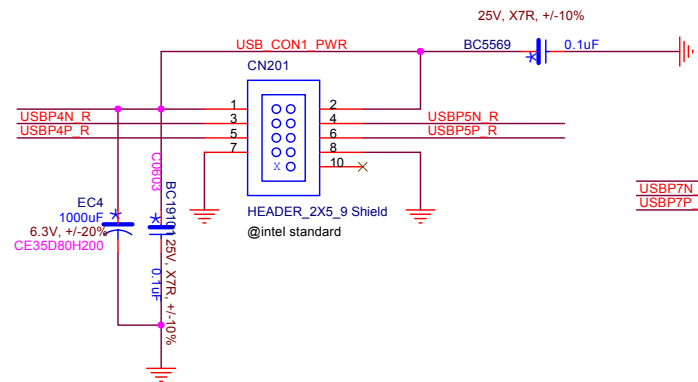
Title FWH		
Size	Document Number 915A01 DDR2	Rev B
Date:	Tuesday, May 18, 2004	Sheet 32 of 52

USB Connector: Back side 4 ports and Front side 4 ports.

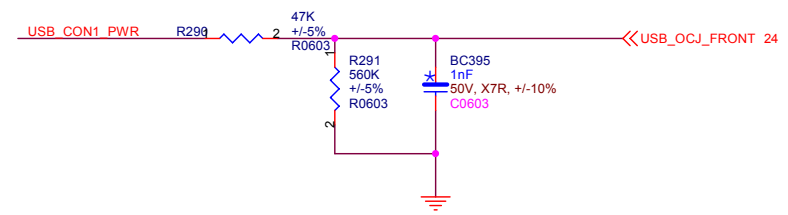
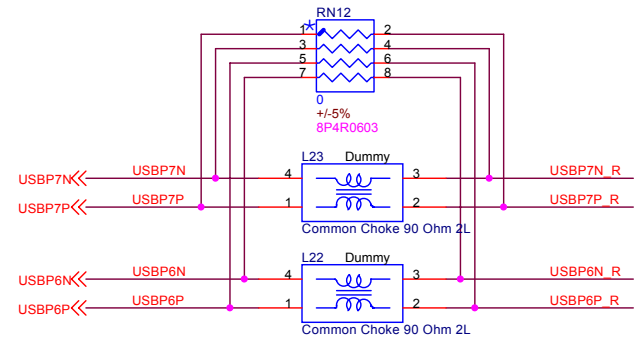
two common chokes and one RN co-layout



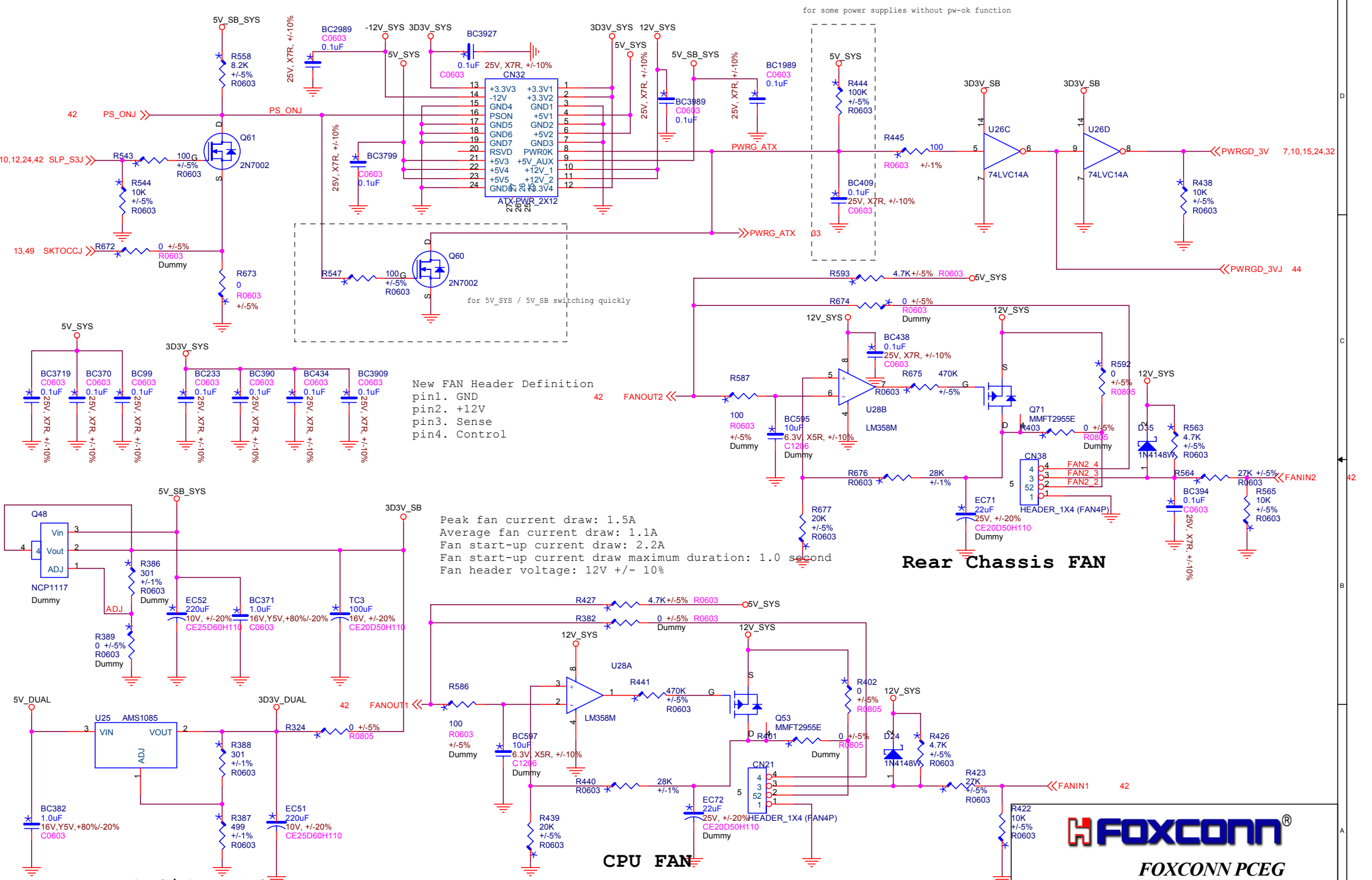
for USB differential trace change layer



two common chokes and one RN co-layout



Title		
USB Connectors		
Size	Document Number	Rev
	915A01 DDR2	B
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New FAN Header Definition
 pin1. GND
 pin2. +12V
 pin3. Sense
 pin4. Control

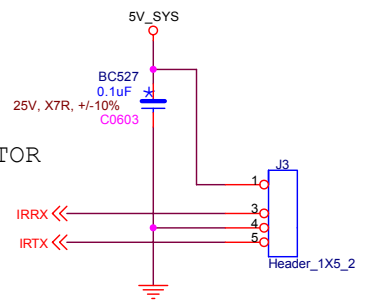
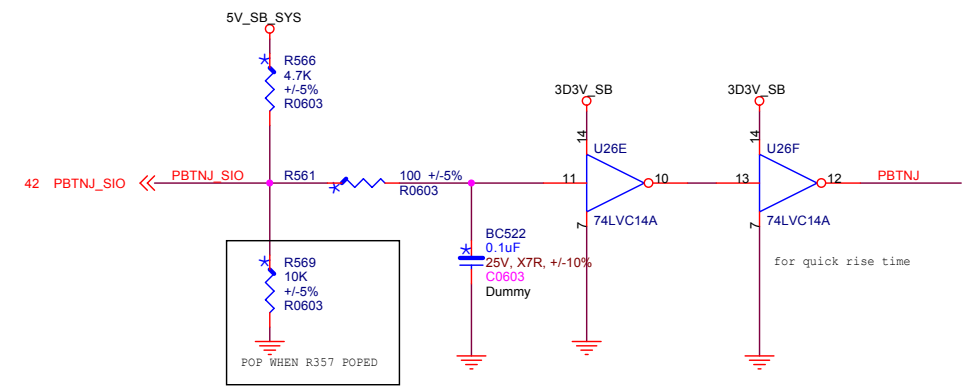
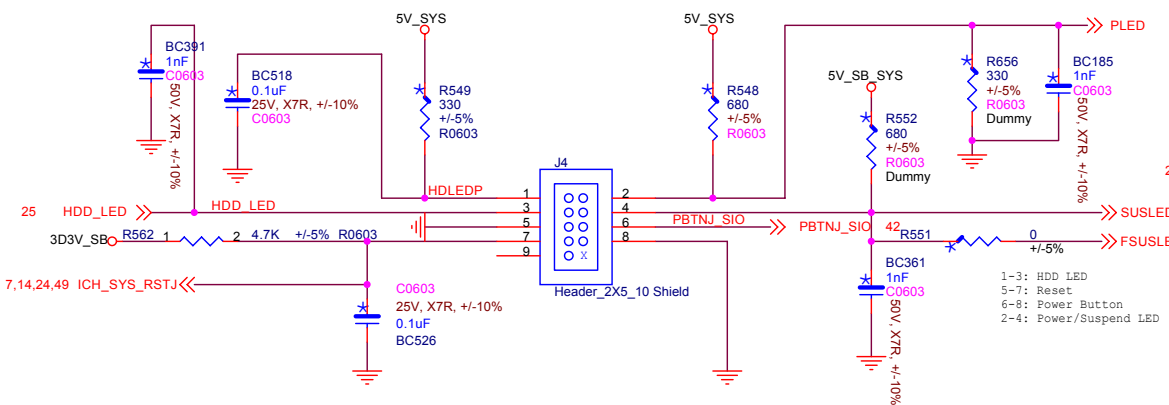
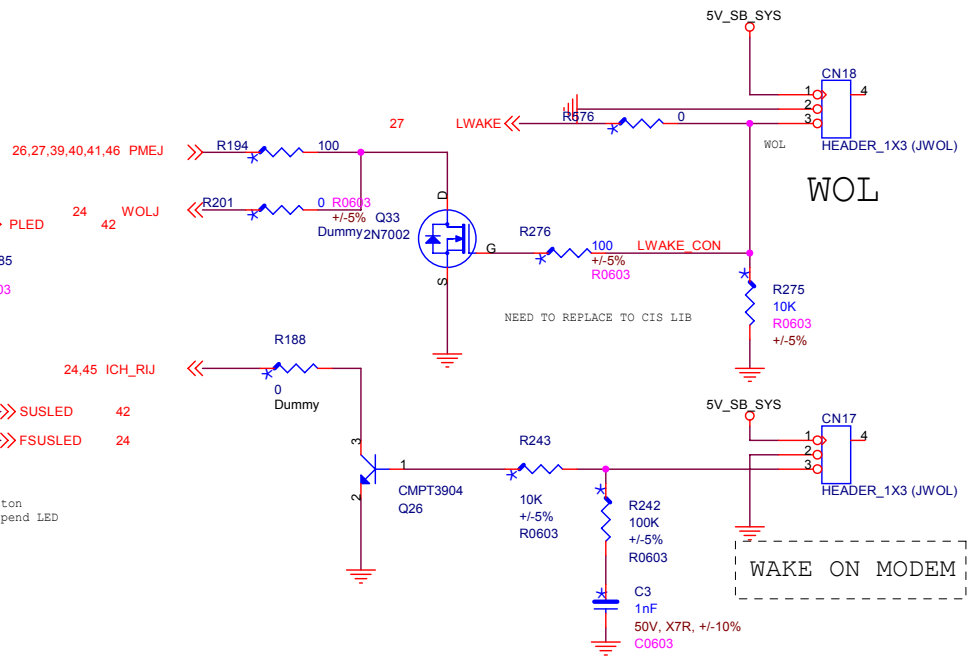
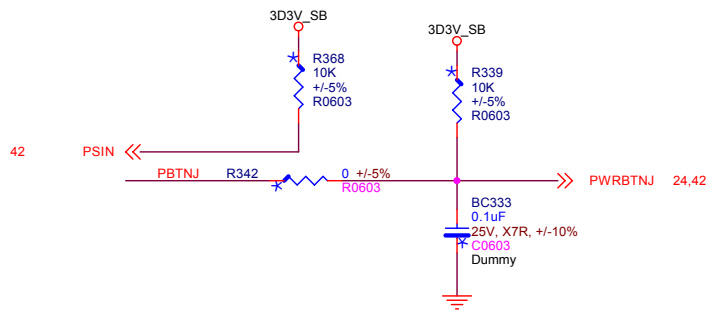
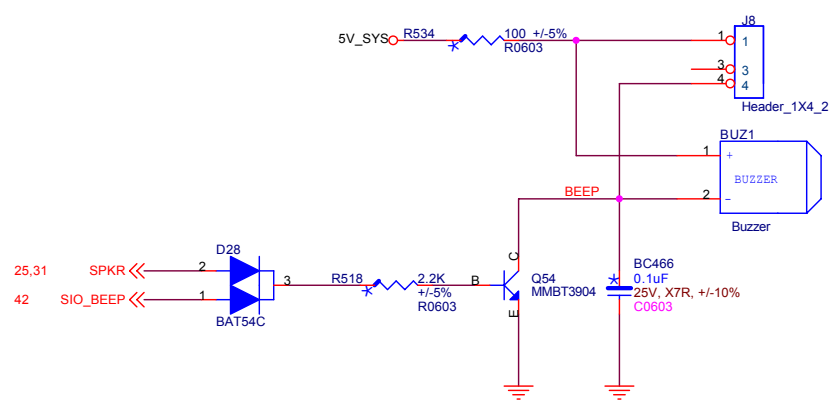
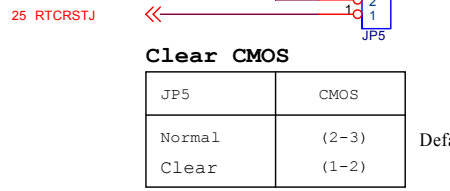
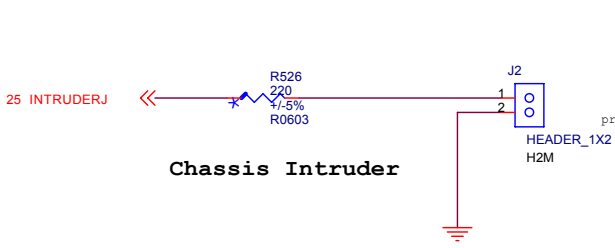
Peak fan current draw: 1.5A
 Average fan current draw: 1.1A
 Fan start-up current draw: 2.2A
 Fan start-up current draw maximum duration: 1.0 second
 Fan header voltage: 12V +/- 10%

$$V_{out} = V_{ref} (1 + R2/R1) + I_{adj} R2$$

R1 is Up Resistor.
 Iadj=50uA
 Vref=1.25V



Power Conn. / 3V_SB/FAN		915A01 DDR2	Rev B
Size	Document Number		
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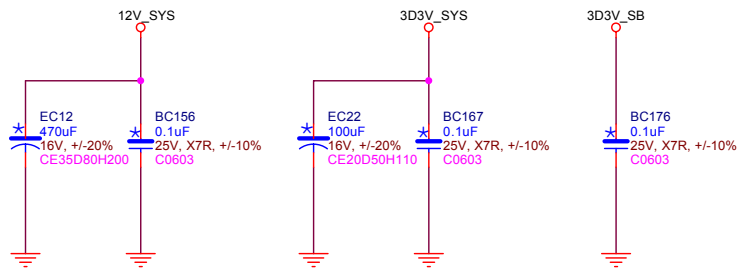
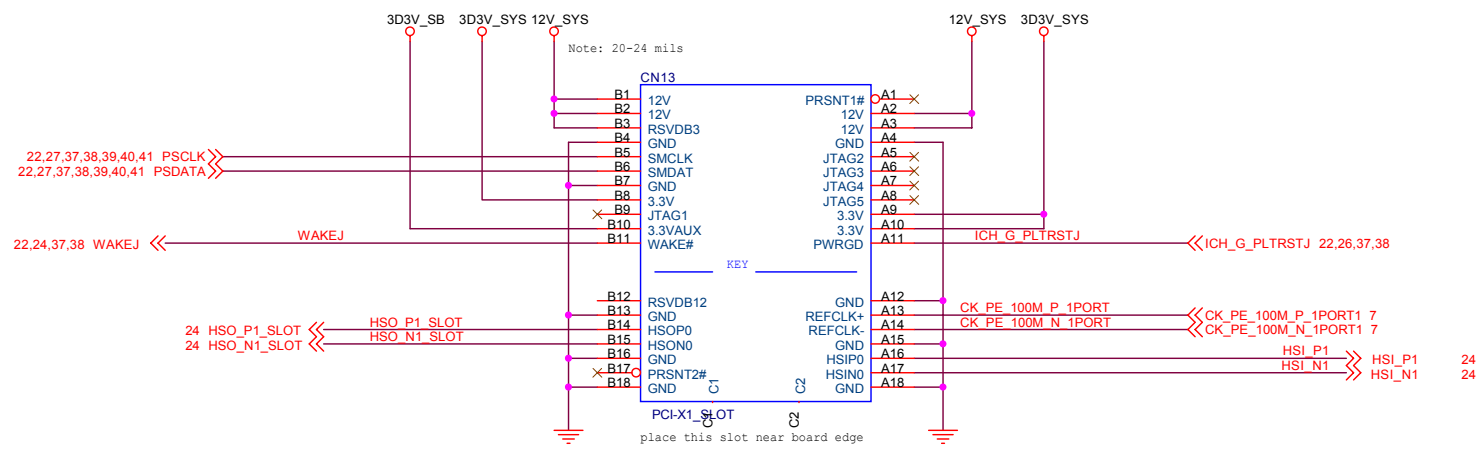
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Title: Front Panel / MISC Conn.

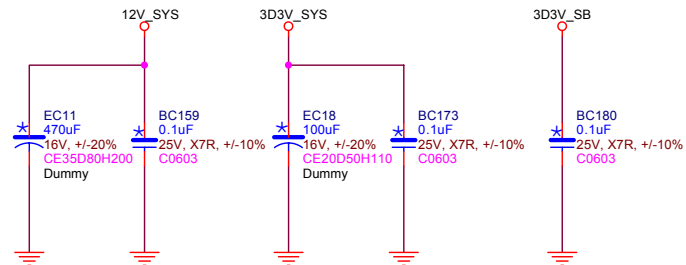
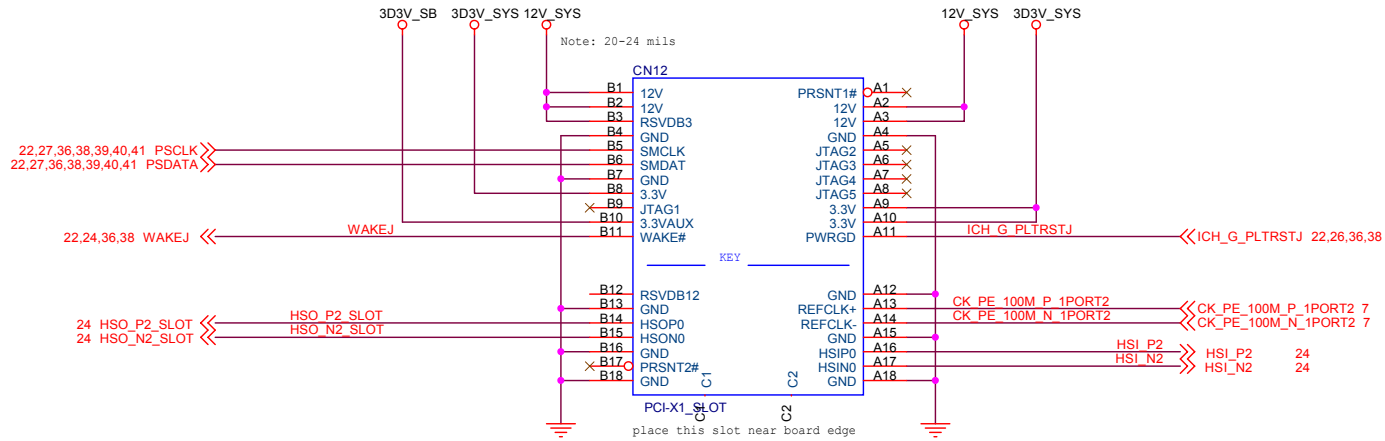
Size: Document Number **915A01 DDR2** Rev B

Date: Tuesday, May 18, 2004 Sheet 35 of 52

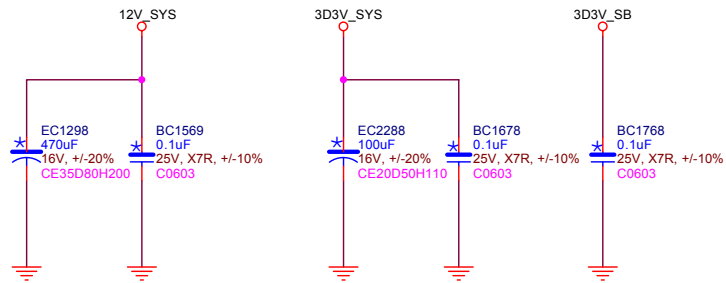
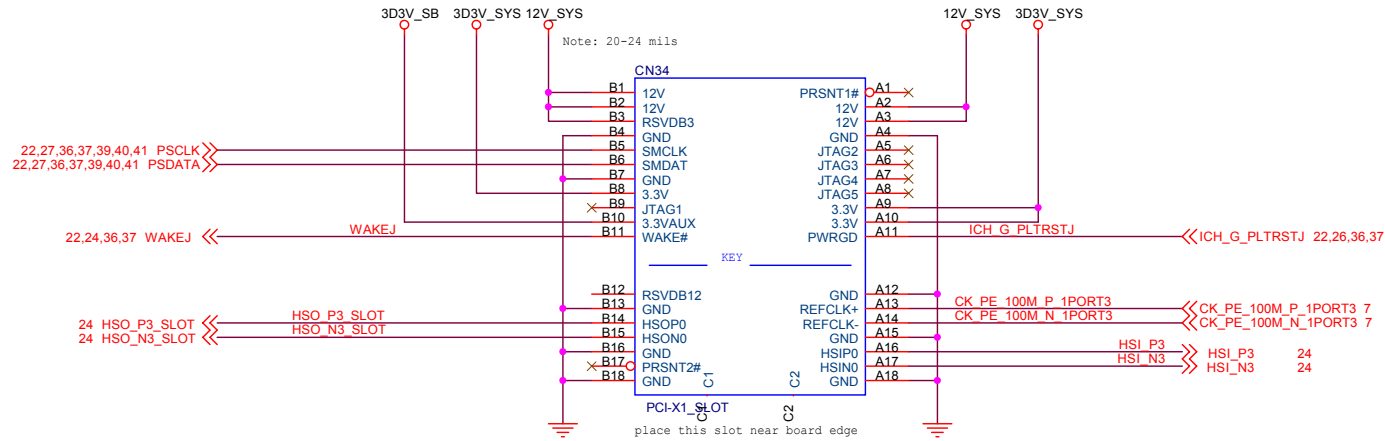


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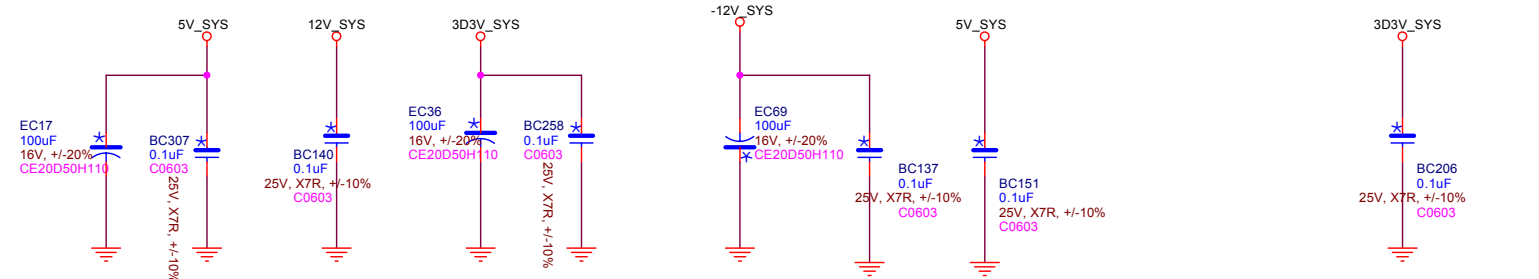
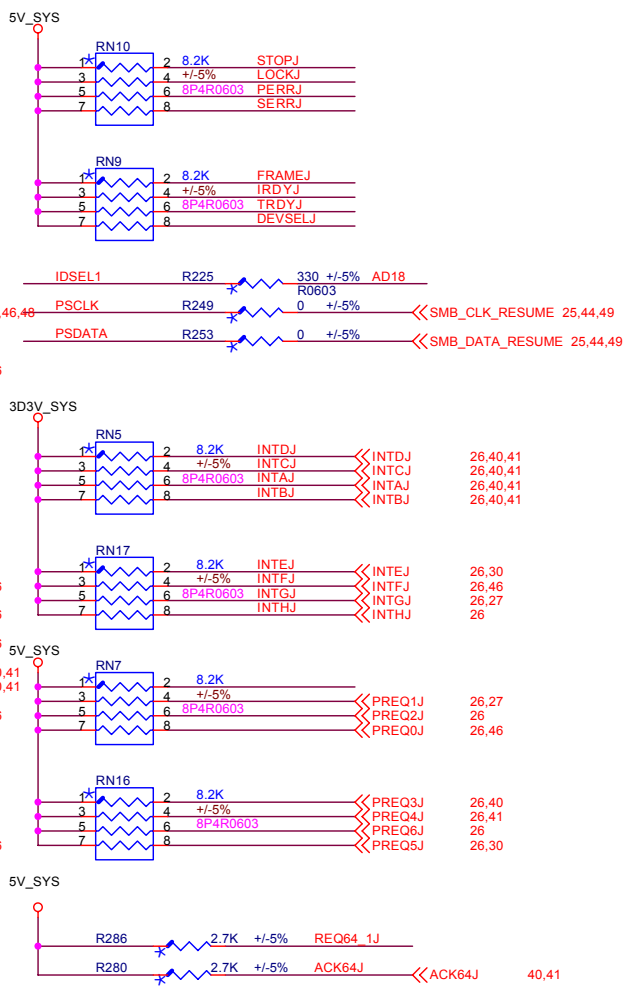
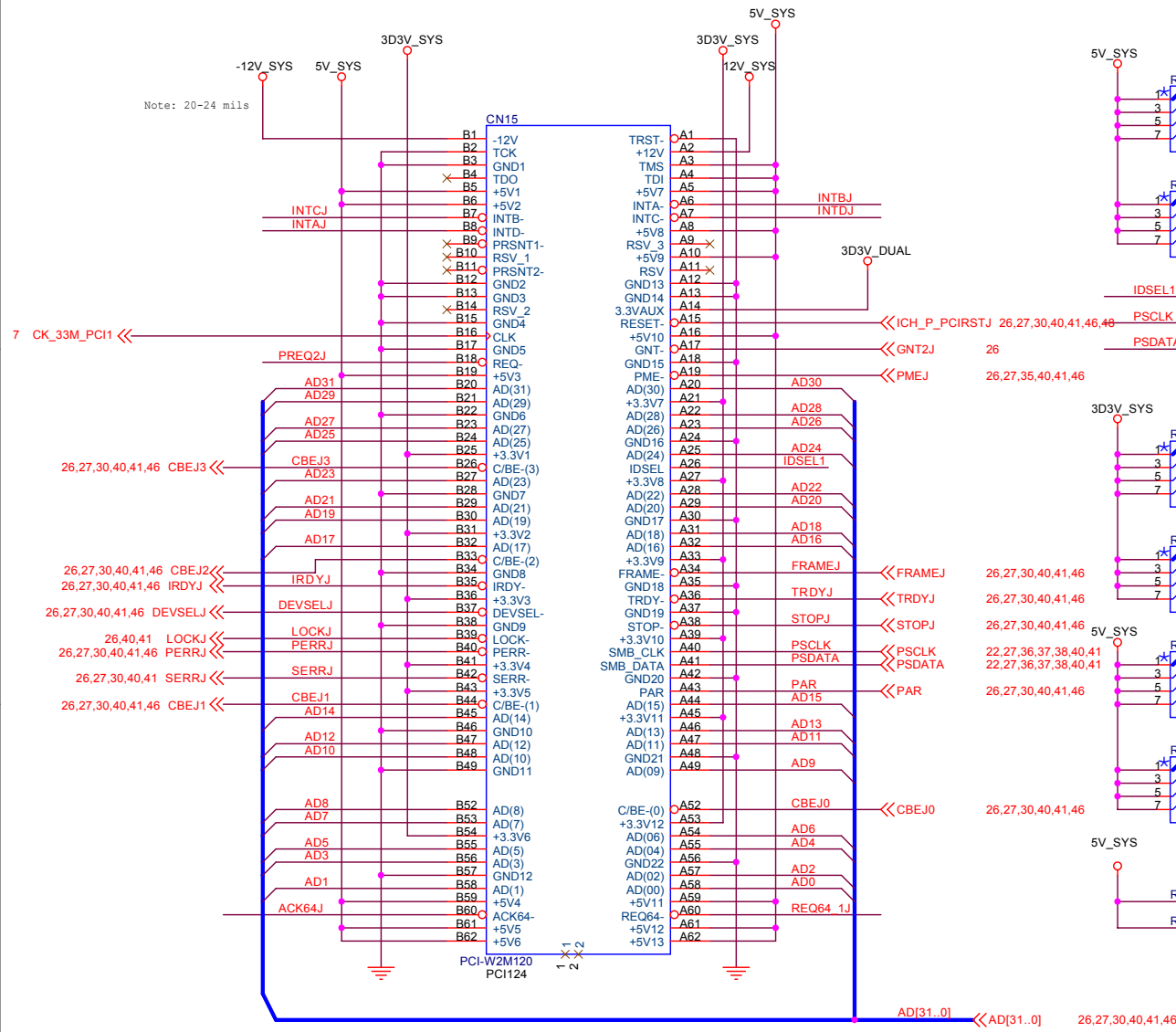
Title PCI Express x1 Slot 1		
Size	Document Number 915A01 DDR2	Rev B
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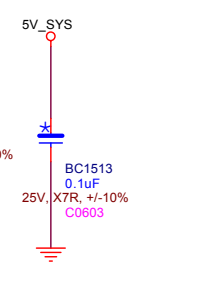
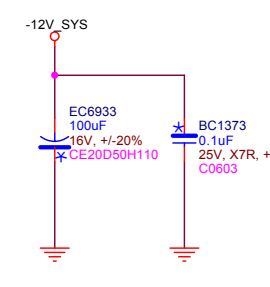
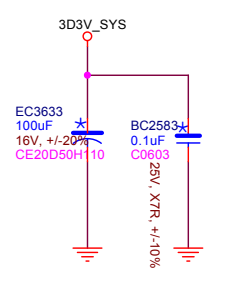
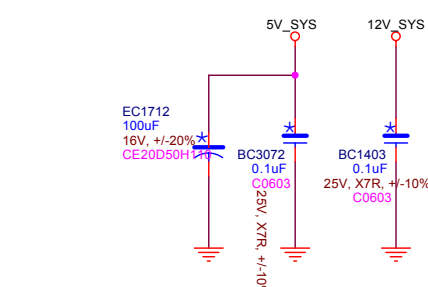
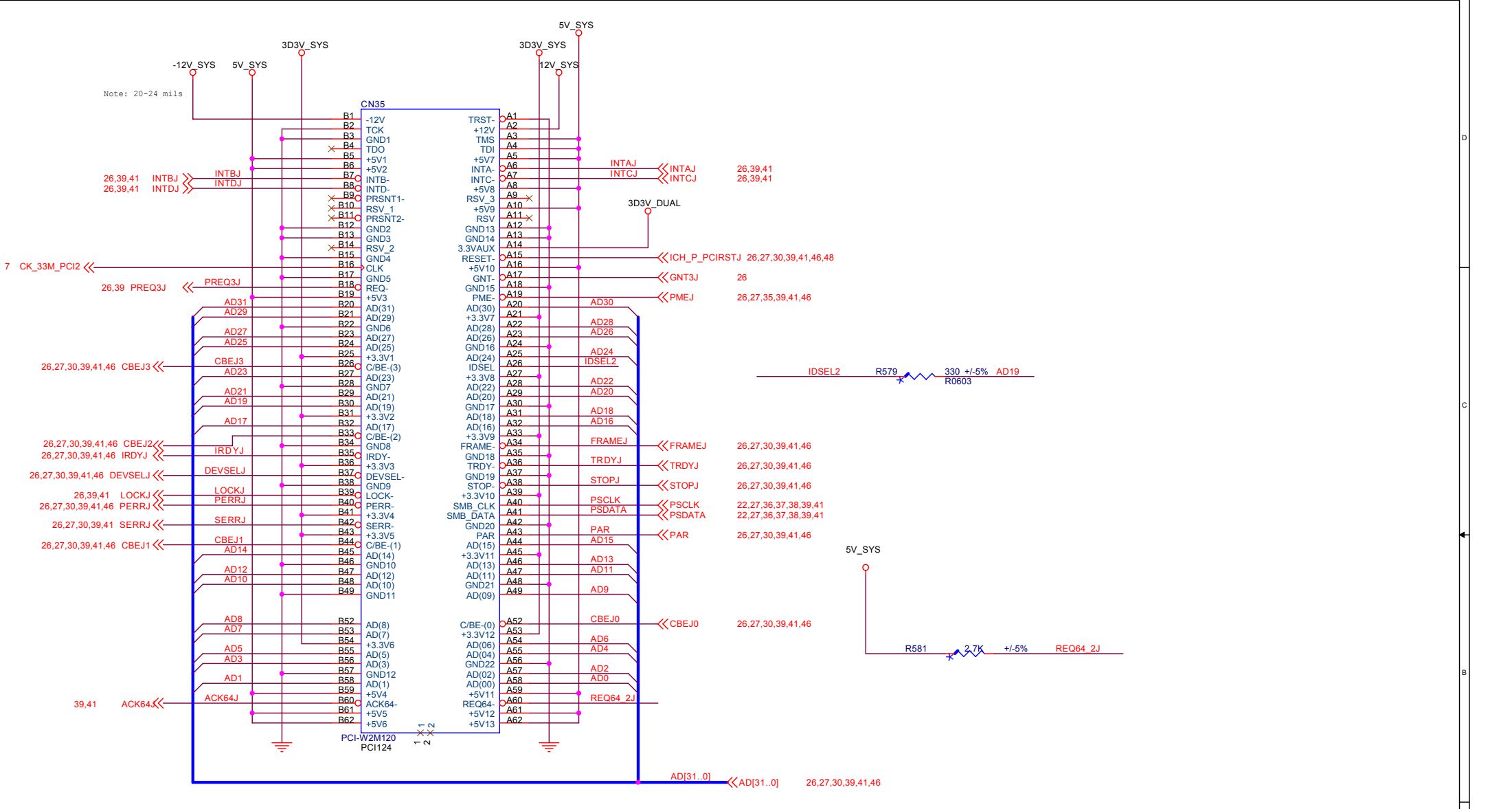


Title PCI Express x1 Slot 2		
Size	Document Number 915A01 DDR2	Rev B
Date:	Tuesday, May 18, 2004	Sheet 37 of 52



Title PCI Express x1 Slot3]		
Size	Document Number 915A01 DDR2	Rev B
Date:	Tuesday, May 18, 2004	Sheet 38 of 52



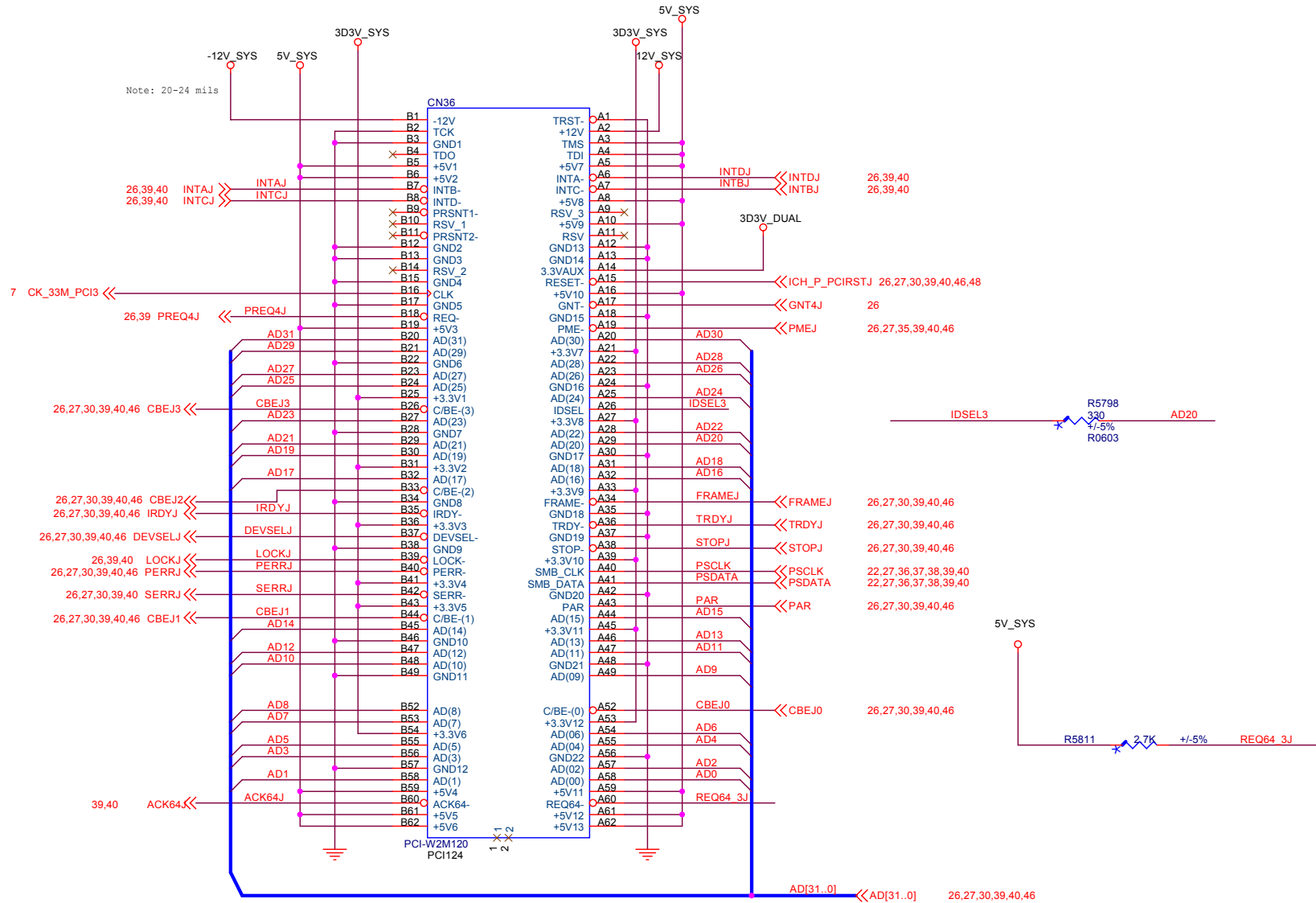


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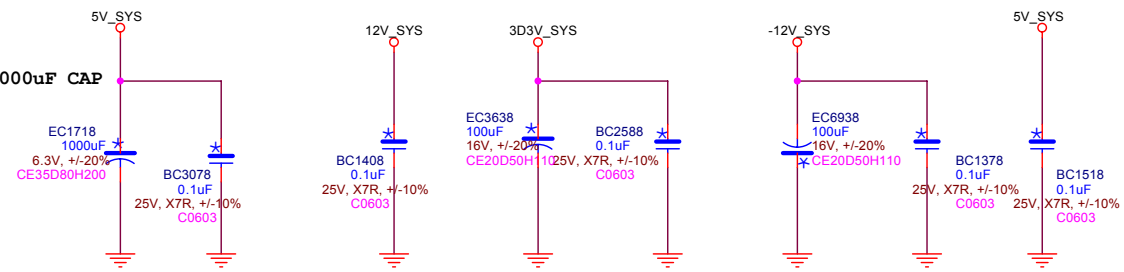
Title: **PCI Slot 2**

Size: Document Number **915A01 DDR2** Rev B

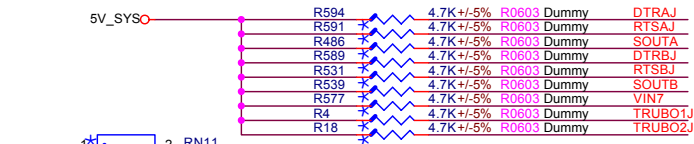
Date: Tuesday, May 18, 2004 Sheet 40 of 52



Replace by 1000uF CAP

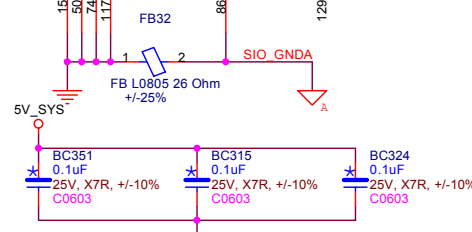
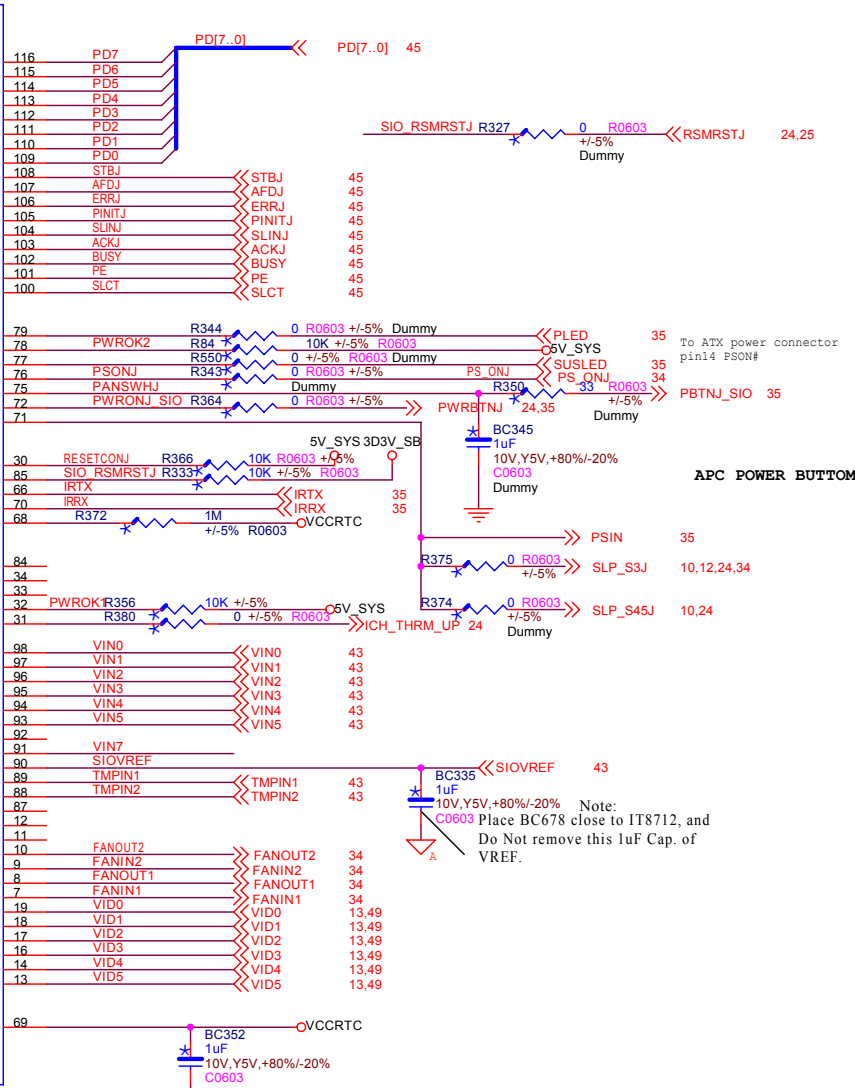
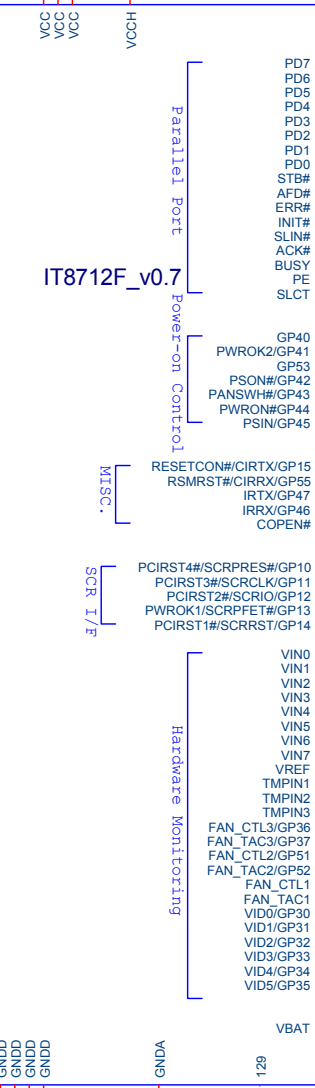
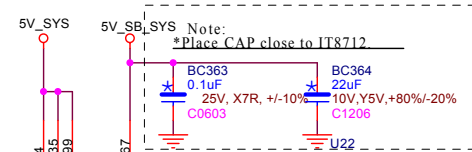
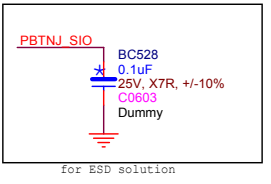
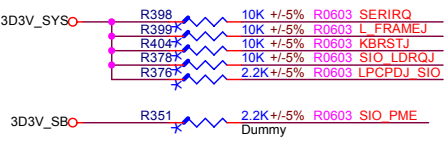
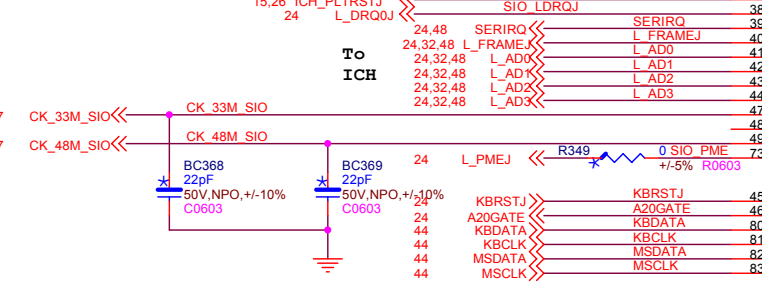
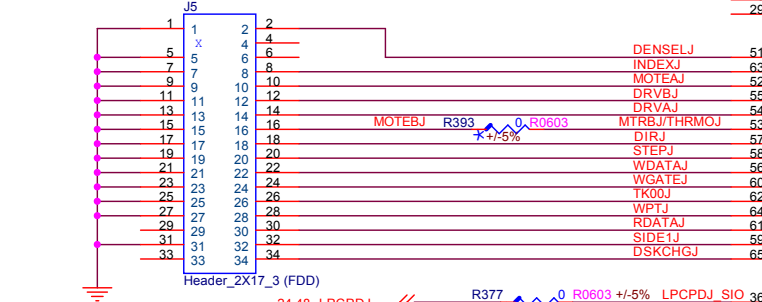
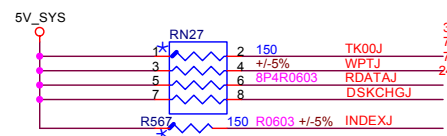


Title PCI Slot 3		
Size	Document Number 915A01 DDR2	Rev B
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Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low.
(Please see specification for detail of power on strapping setting)

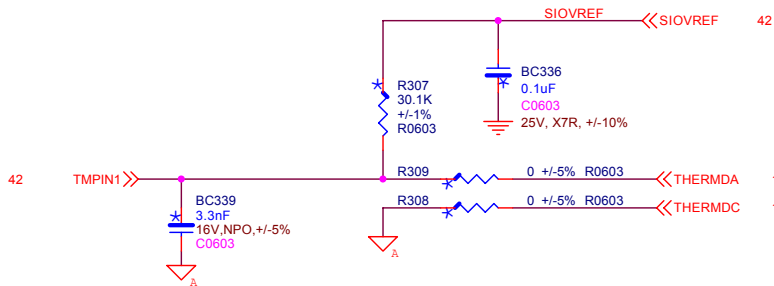
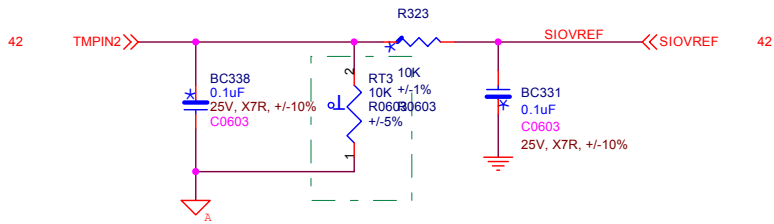
FDC Connector



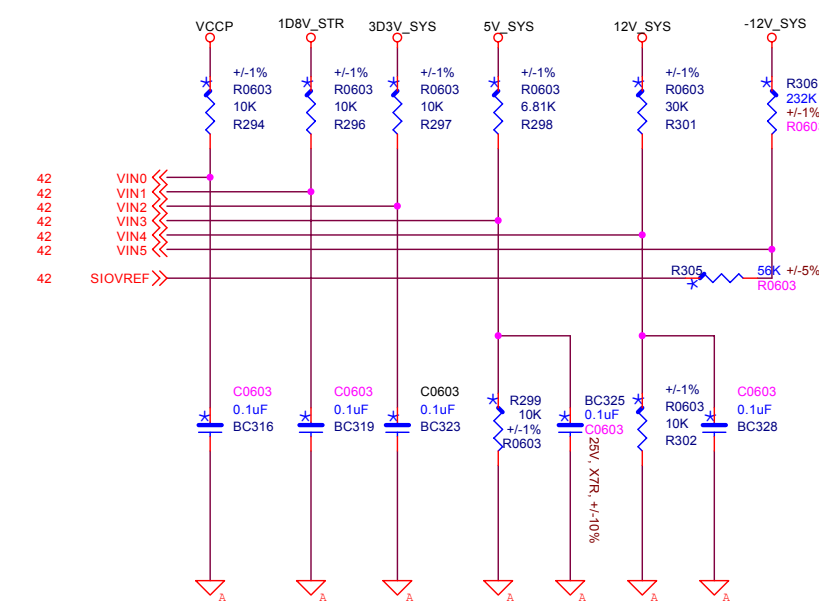
Note:
Place BC685 close to IT8712 as possible



Title		IT8712F/H	
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Rev	B		



Voltage Monitor



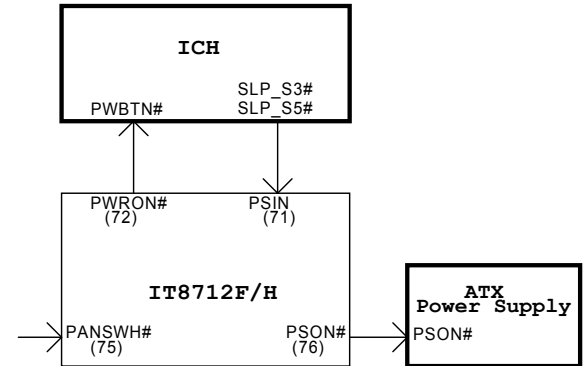
Power On Strapping Options

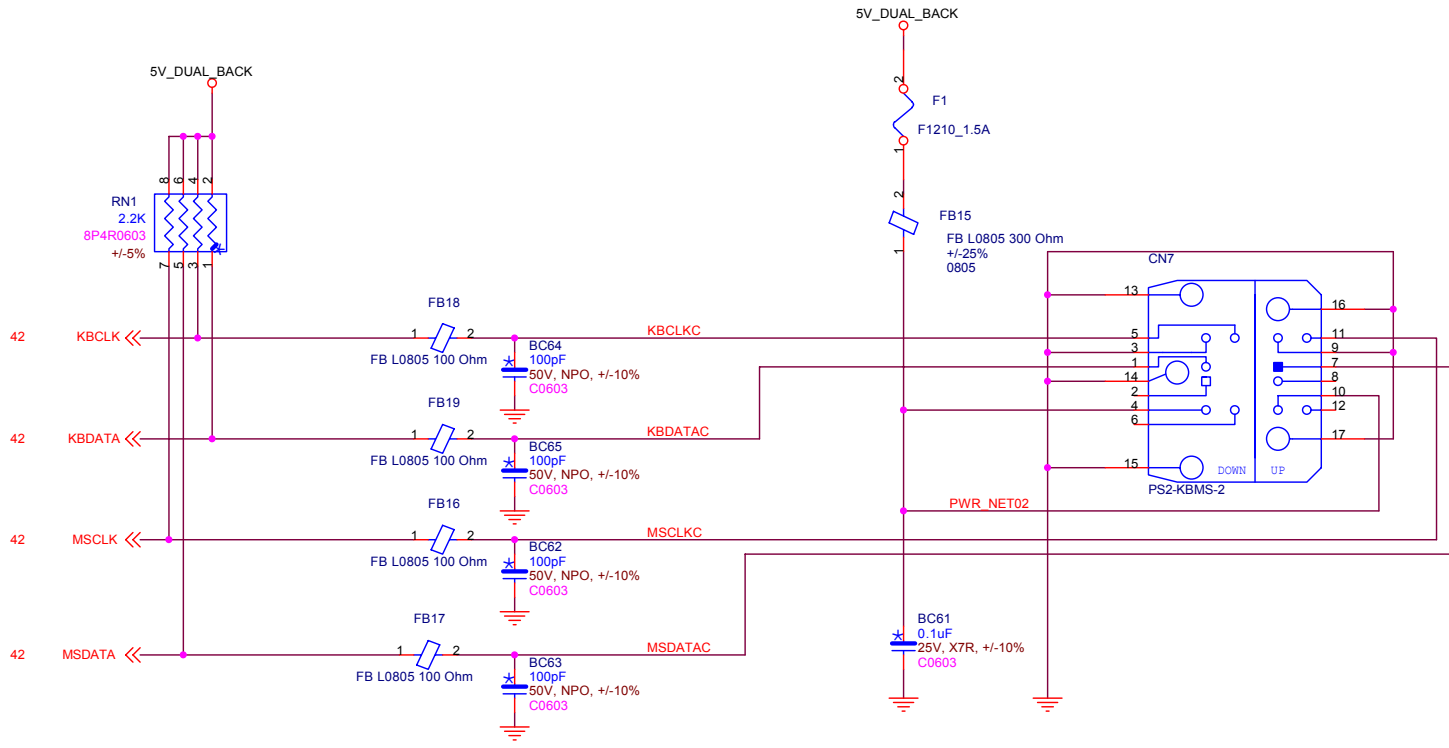
	Symbol	value	Description
DTR1#/JP1	KBCEN	1	KBC is enabled.
		0	KBC is disabled.
RTS1#/JP2	KBC_IROM	1	KBC's ROM is built in.
		0	KBC's ROM is external.
SOUT1#/JP3	CHIP_SEL	--	Chip selection in configuration.
DTR2#/JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, and PCIRST4# are enhanced open-drain. It will drive high about 10~20ns when the signal transit from low to high, and then Hi-Z.
		0	The output buffers are push-pull.

*Recommended net "VCCH" minimum trace width 12mils.

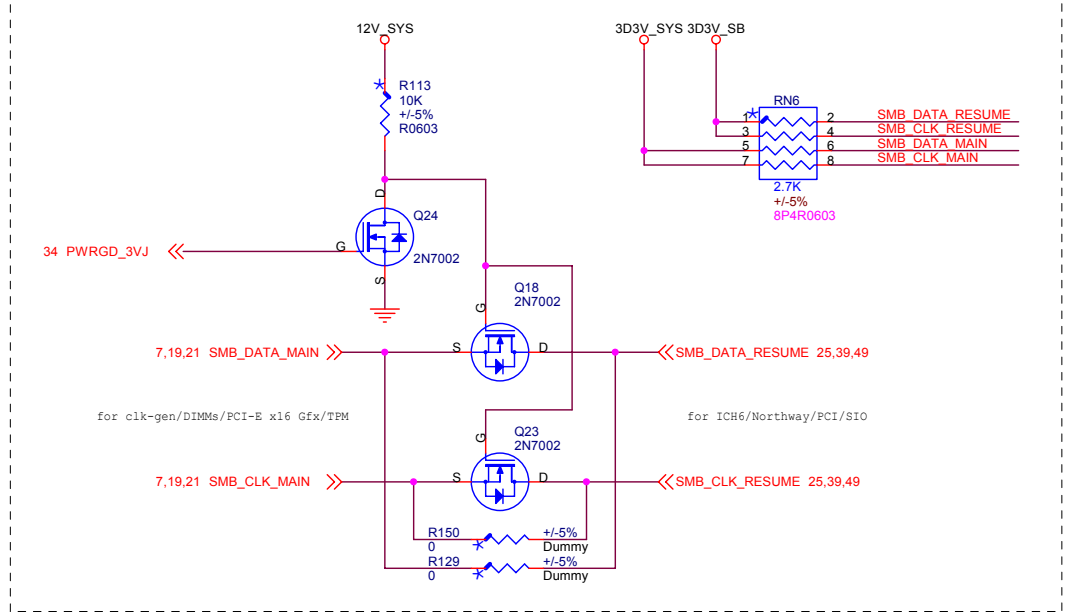
The different function pins between IT8712F/H and IT8712F/G			
Pin	IT8712F/HX	Pin	IT8712F/GX
13	VID5/GP35	13	WTI#/GP35
30	RESETCON#/CIRTX/GP15	30	CIRTX/GP15
31	PCIRST1#/SCRPRST/GP14	31	SCRPRST/GP14
32	PWROK1/SCRPFET#/GP13	32	SCRPFET#/GP13
33	PCIRST2#/SCRIO/GP12	33	SCRIO/ GP12
34	PCIRST3#/SCRCLK/GP11	34	SCRCLK/ GP11
77	GP53	77	RING#/GP53
78	PWROK2/GP41	78	GP41
84	PCIRST4#/SCRPRES#/GP10	84	SCRPRES#/GP10
85	RSMRST#/CIRRX/GP55	85	CIRRX/COPENO#/GP55

POWER ON SCHEME

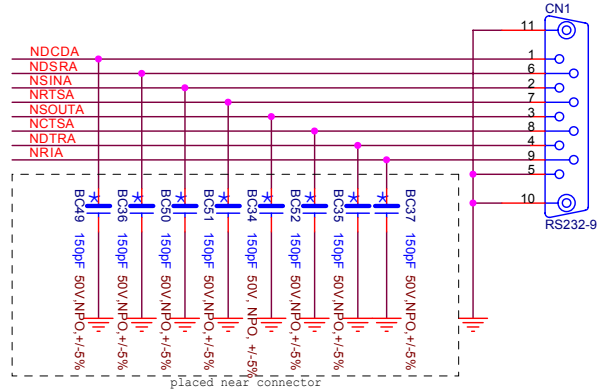
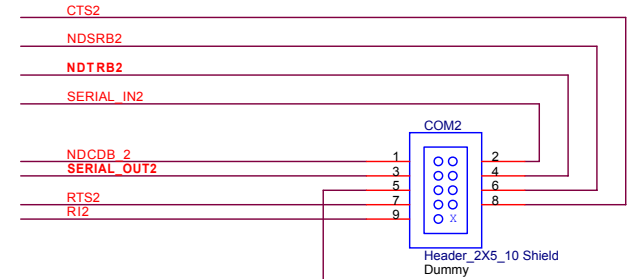
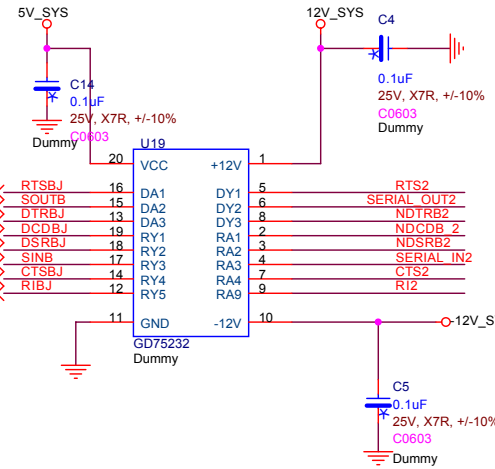
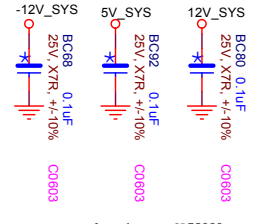
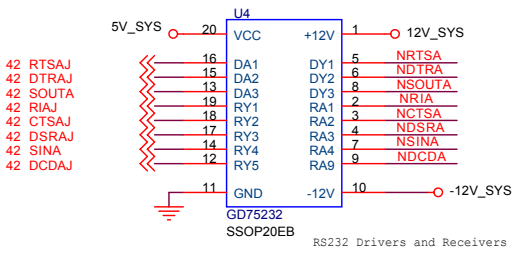




SM Bus Bridge



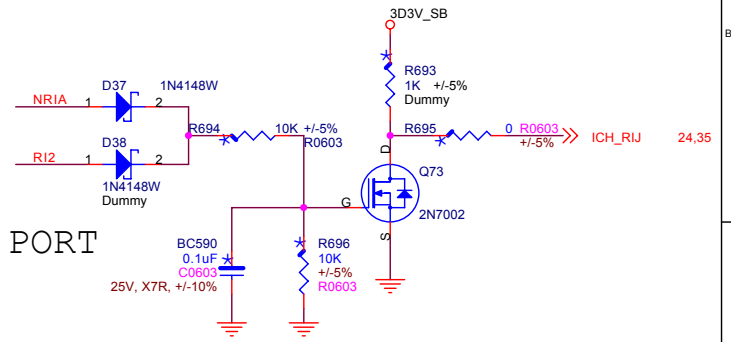
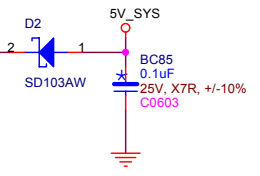
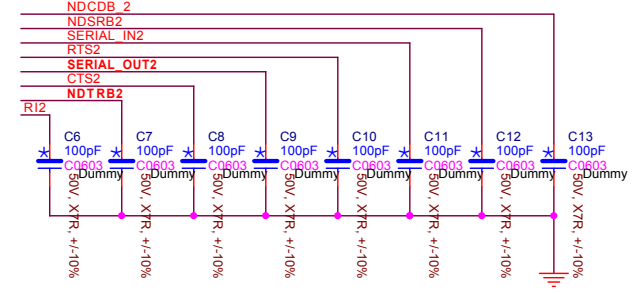
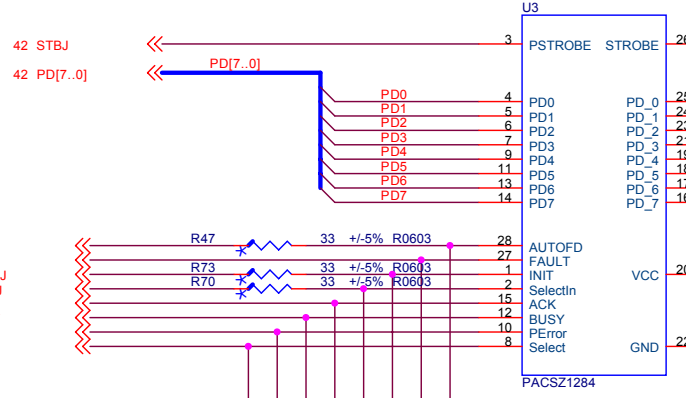
Title Keyboard / Mouse		
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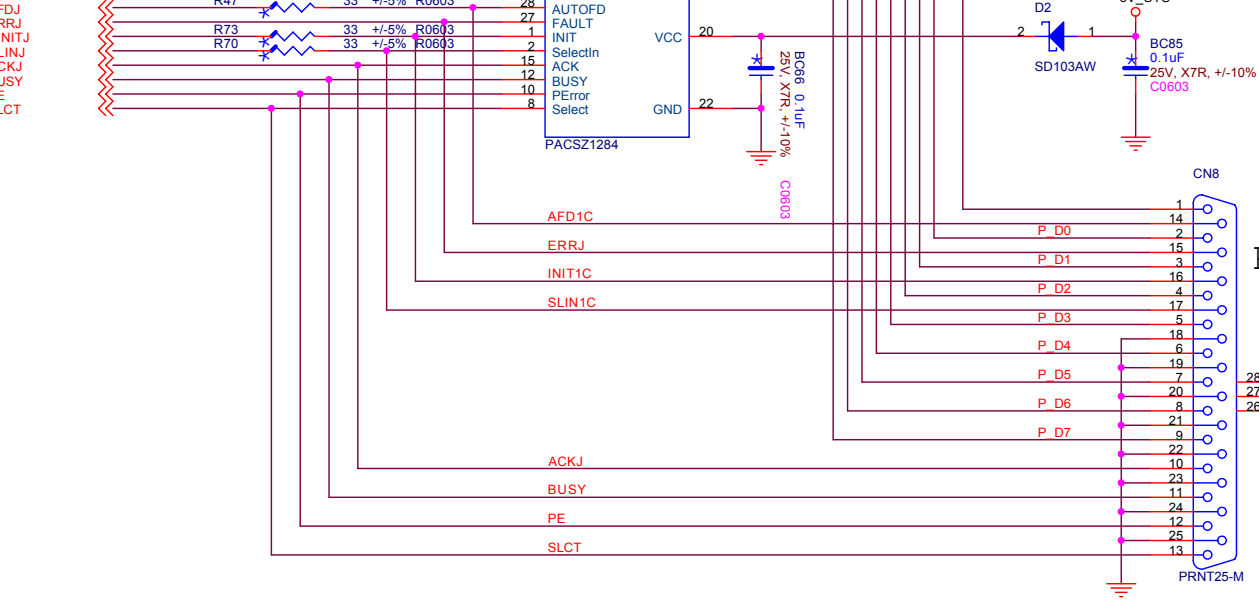
placed near GD75232

placed near connector

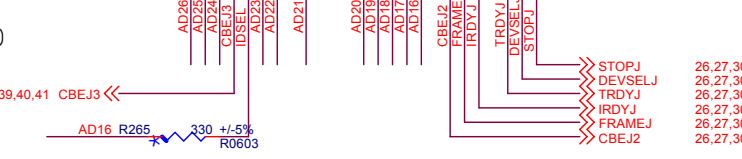
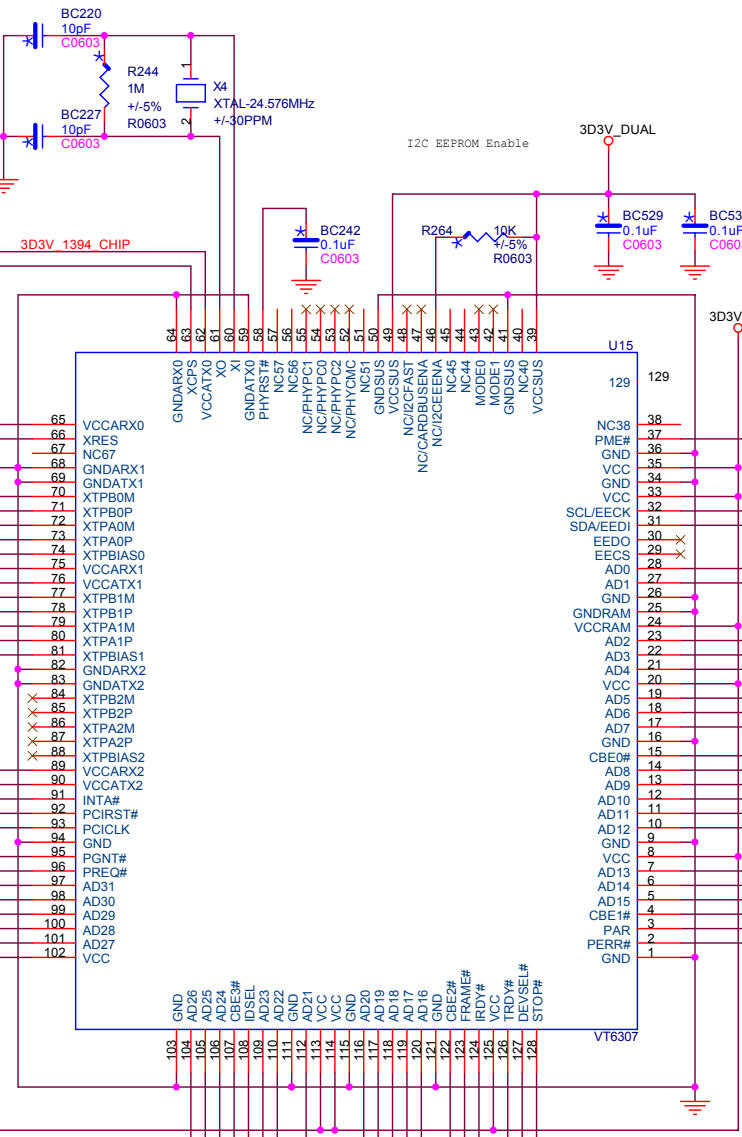
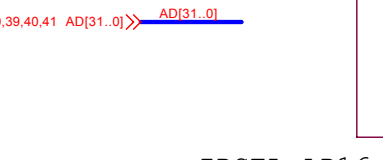
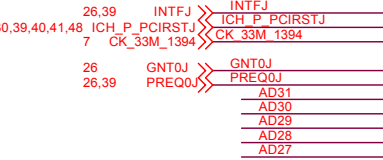
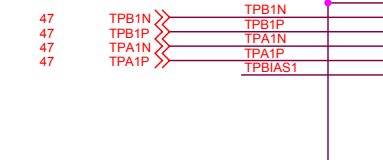
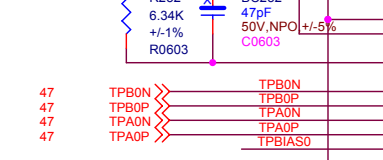
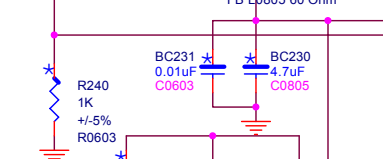
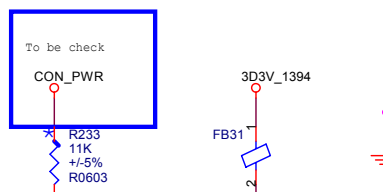
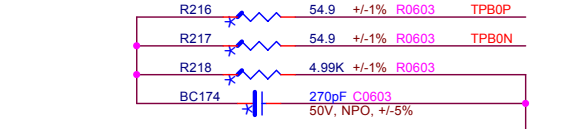
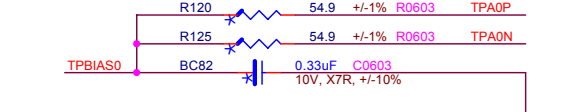
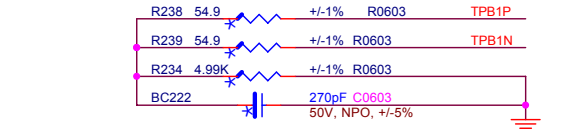
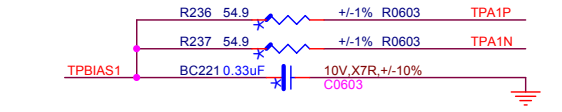
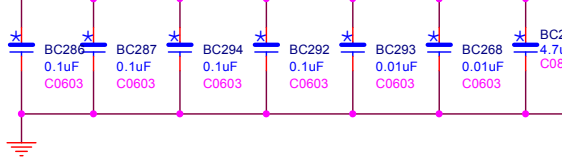
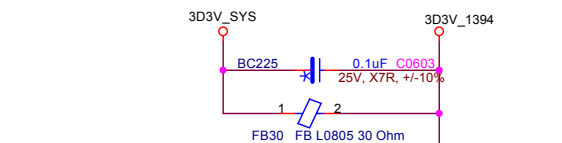
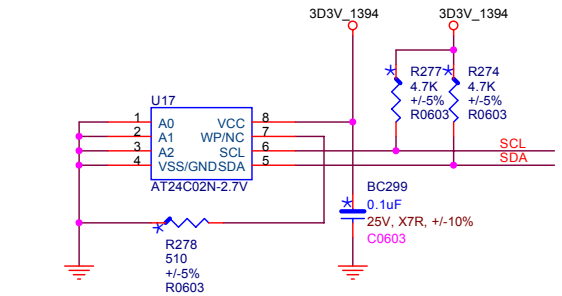
EMI/ESD/Termination Network



PRT PORT



Title		
Serial / Parallel		
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	915A01 DDR2	B
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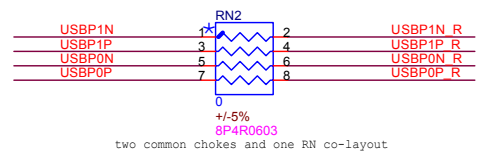
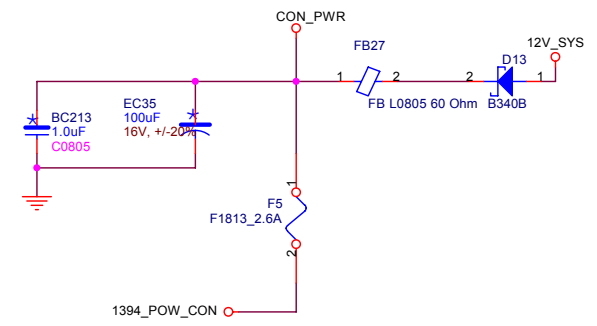
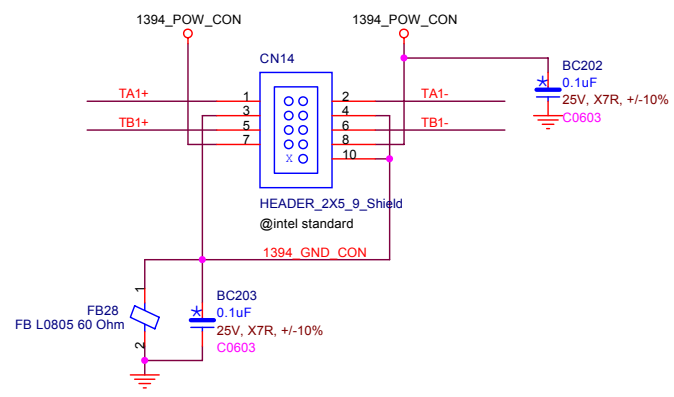
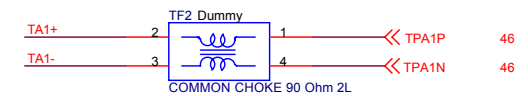
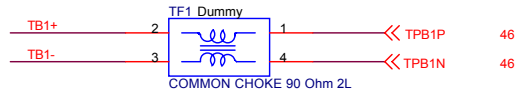
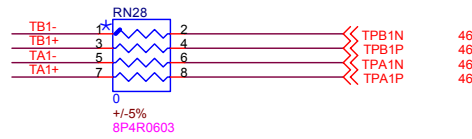


FOXCONN
FOXCONN PCEG

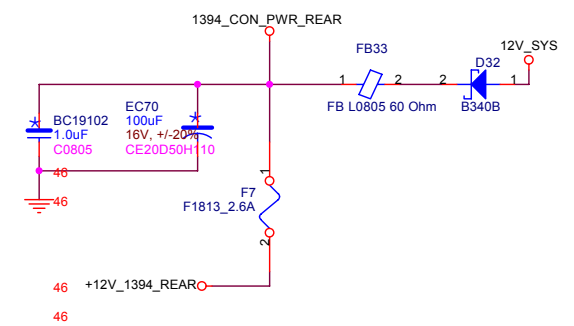
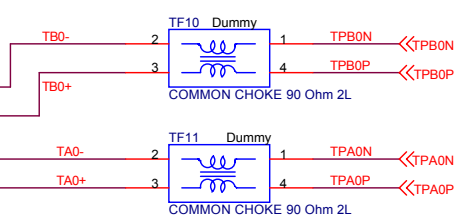
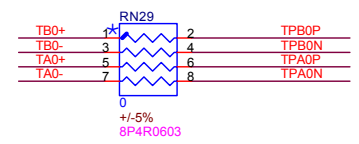
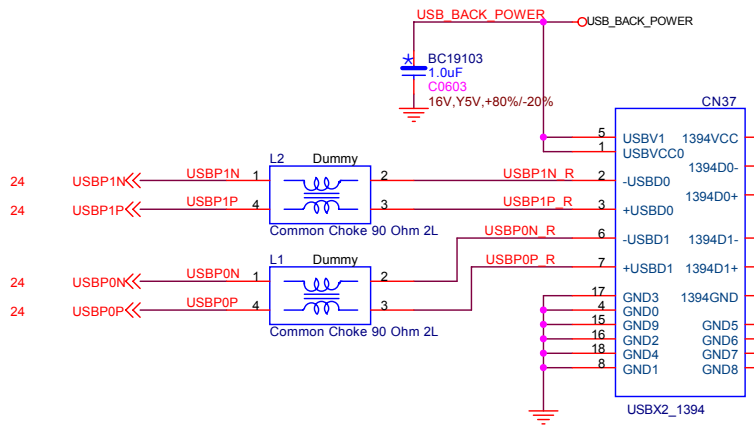
Title: **VT6307_1394**

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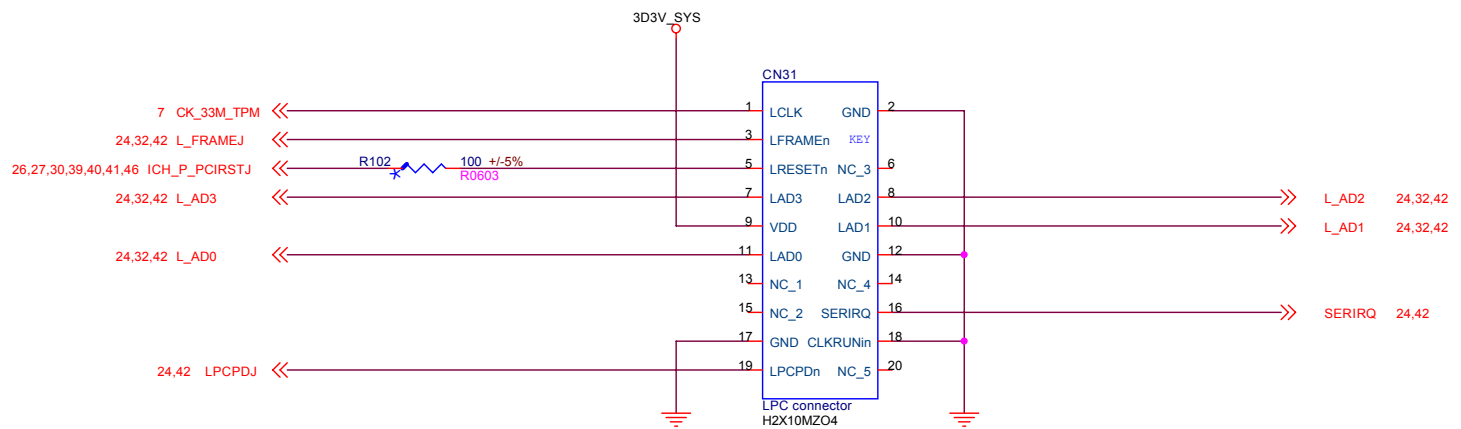
two common chokes and one RN co-layout



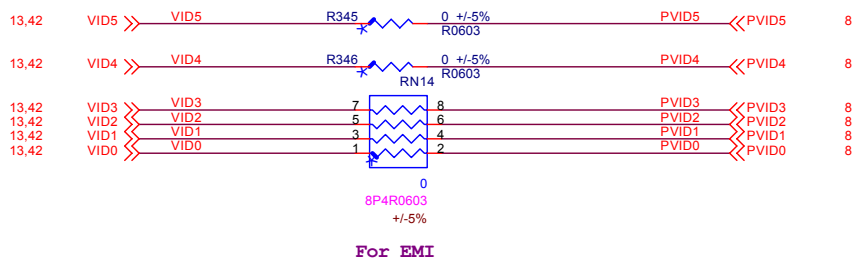
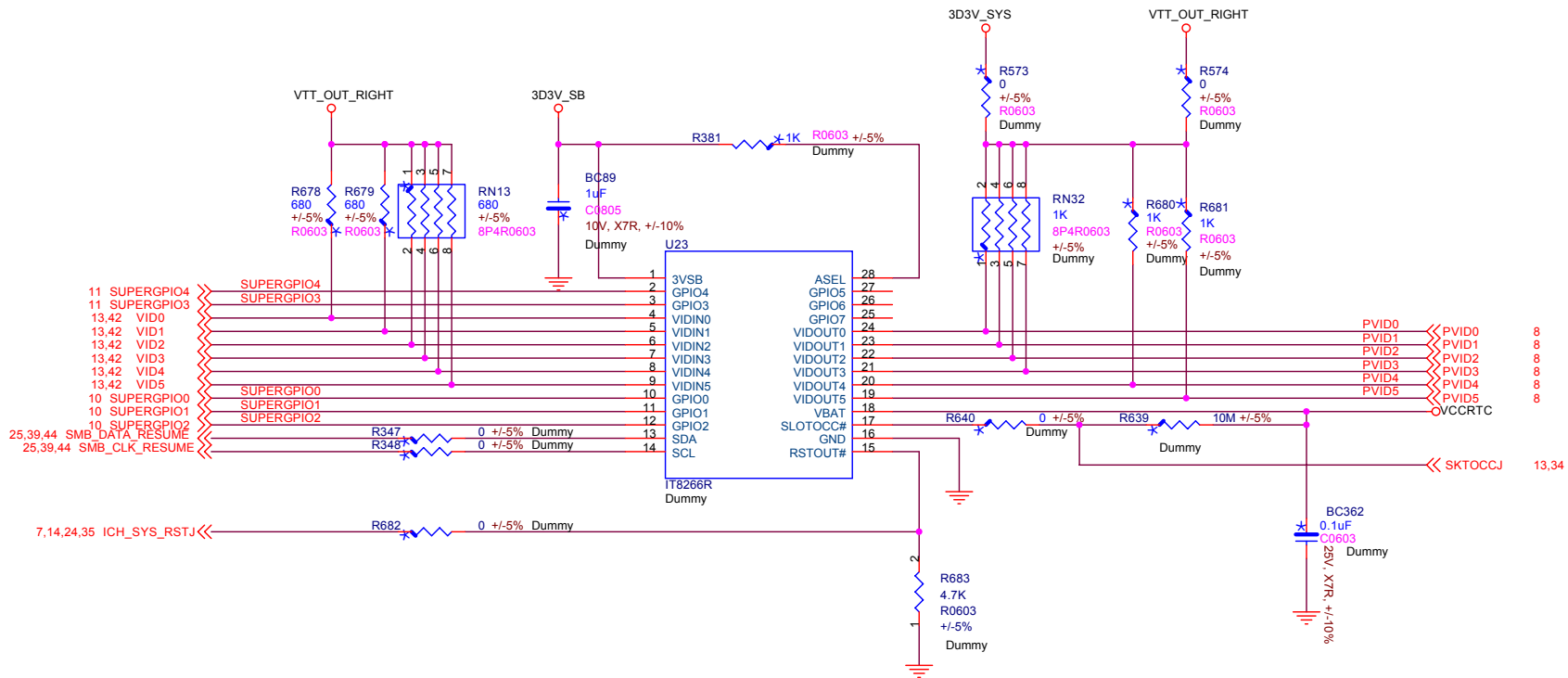
USB1 & 2 / 1394




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		1	Rev B



Title		
TPM		
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FOXCONN PCEG

Title		
VID Controller		
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ICH6 GPIO Summary

Name	Power Well	Type	Description
GPI0	V5REF	I	REQ_6#
GPI1	V5REF	I	REQ_5#
GPI2	V5REF	I	PIRQE#
GPI3	V5REF	I	PIRQF#
GPI4	V5REF	I	PIRQG#
GPI5	V5REF	I	PIRQH#
GPI6	Vcc3_3	I	Pull-up through 10K resistor (Unused)
GPI7	Vcc3_3	I	Board ID0
GPI8	VccSus3_3	I	LPC PME#
GPI9	VccSus3_3	I	USB OC4#
GPI10	VccSus3_3	I	USB OC5#
GPI11	VccSus3_3	I	Pull-up through 10K resistor (Unused)
GPI12	Vcc3_3	I	Pull-up through 10K resistor (Unused)
GPI13	VccSus3_3	I	Wake On LAN
GPI14	VccSus3_3	I	USB OC6#
GPI15	VccSus3_3	I	USB OC7#
GPO16	Vcc3_3	O	GNT_6#
GPO17	Vcc3_3	O	GNT_5#
GPO18	Vcc3_3	O	GP018 (Unused)
GPO19	Vcc3_3	O	GPO19 (Unused)
GPO20	Vcc3_3	O	GPO20 (Unused)
GPO21	Vcc3_3	O	GPO21 (Unused)
GPIO22	N/A	N/A	Not Implemented
GPO23	Vcc3_3	O	GPO23 (Unused)
GPIO24	VccSus3_3	I/O	GPIO24 (Unused)
GPIO25	VccSus3_3	I/O	GPIO25 Strap: 2.5 VRM Enable
GPIO26	Vcc3_3	I	SATA_0GP
GPIO27	VccSus3_3	I/O	Board ID2
GPIO28	VccSus3_3	I/O	GPIO LAN Disable
GPIO29	Vcc3_3	I	SATA_1GP
GPIO30	Vcc3_3	I	SATA_2GP
GPIO31	Vcc3_3	I	SATA_3GP
GPIO32	Vcc3_3	I/O	Board ID1
GPIO33	Vcc3_3	I/O	GPIO33 (Unused)
GPIO34	Vcc3_3	I/O	Board ID3
GPIO35	N/A	N/A	Not Implemented
GPIO36	N/A	N/A	Not Implemented
GPIO37	N/A	N/A	Not Implemented
GPIO38	N/A	N/A	Not Implemented
GPIO39	N/A	N/A	Not Implemented
GPI40	V5REF	I	REQ_4#
GPI41	Vcc3_3	I	TBD
GPIO42	N/A	N/A	Not Implemented
GPIO43	N/A	N/A	Not Implemented
GPIO44	N/A	N/A	Not Implemented
GPIO45	N/A	N/A	Not Implemented
GPIO46	N/A	N/A	Not Implemented
GPIO47	N/A	N/A	Not Implemented
GPO48	Vcc3_3	O	GNT_4#
GPO49	V_CPU_IO	OD	CPUPWRGD

Super I/O GPIO Summary

Name	Power Plane	Type	Description
GPIO10-17	Main	I/O	Not Implemented
GPIO20	Main	I/O	SIO-BEEP
GPIO30	Main	I/O	VID0
GPIO31	Main	I/O	VID1
GPIO32	Main	I/O	VID2
GPIO33	Main	I/O	VID3
GPIO34	Main	I/O	VID4
GPIO35	Main	I/O	VID5
GPIO40	Main	I/O	POWER LED
GPIO41	Main	I/O	SUSPEND LED
GPIO42	Main	I/O	PS-ON TO ATX POWER CONN.
GPIO43	Main	I/O	POWER BUTTON-IN
GPIO44	Main	I/O	POWER BUTTON TO ICH6
GPIO45	Main	I/O	PS-IN
GPIO46	Main	I/O	IRRX
GPIO47	Main	I/O	IRTX
GPIO50	Main	I/O	Not Implemented
GPIO43	Main	I/O	POWER BUTTON-IN
GPIO44	Main	I/O	POWER BUTTON TO ICH6
GPIO45	Main	I/O	PS-IN
GPIO46	Main	I/O	IRRX
GPIO47	Main	I/O	IRTX
GPIO51	Main	I/O	FAN_CTRL2
GPIO52	Main	I/O	FAN_TAC2
GPIO53	Main	I/O	THERM-UP TO ICH6
GPIO54	Main	I/O	PME
GPIO55	5V_SB	I/O	RSMRST

FWH GPIO Summary

Name	Power Plane	Type	Description
FGPIO0	Main	I	IDEL Cable Detection(33 or 66/100)
FGPI1	Main	I	Unused
FGPI2	Main	I	Unused
FGPI3	Main	I	Unused

PCI Routing Summary

	PCI1	LAN	1394
INTA#	B		
INTB#	C		
INTC#	D		
INTD#	A		
INTE#			
INTF#			A
INTG#		A	
INTH#			
REG#/GNT#	2	1	0
IDSEL	18	17	16



FOXCONN PCEG

Title GPIO / IRQ / IDSEL Map		
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Jumper Setting Summary

JP5	Clear CMOS 1-2 : Normal (Default) 2-3 : Clear CMOS
JP1	FWH TBL# 1-2 : Unlock 2-3 : Lock

TBD

GrantsDale Family Option Table

82570EI and 82562EX Option Table

ALC655, ALC650 and ALC203 Option Table



FOXCONN PCEG

Title Jumper Setting / Option Table		
Size C	Document Number 915A01 DDR2	Rev B
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Item\Quantity\Reference\Value\Description\Foxconn Part Number\Mfg Part Number\PCB Footprint\Remark
(Item)\(Quantity)\(Reference)\(Value)\(Description)\(Foxconn Part Number)\(Mfg)\(Mfg Part Number)\(PCB Footprint)\(Remark)

- 1.Remove R685.Modified 1394/PCI3 clock connection.(P07)
- 2.Modified ICH-SYNCJ Net connection.(P24)
- 3.Add R13.Fixed Lan Wake up Fail.(P27)
- 4.Add R364.Fixed PS/2 Wake up Fail.(P42)
- 5.Add R380,R355.Fixed Over thermal Shut down Fail.(P42)
- 6.Modified FWH write protection silk screen and connection.(P32)
- 7.Modified Silicon Image SATA connector direction.(P30)
- 8.Modified Lan 2.5V power plan.(Layout)
- 9.Modified ICH6R 1.5V core plan.(Layout)
- 10.Changed audio power capacitors (BC122,BC98,BC10) size to 1206 from 1210.(P31)
- 11.Cancel VGA and COM2 co-layout.
- 12.Changed USB power fuse (F6,F3) and EC1718,FB22 size.
- 13.Add R23.Fixed over clock Fail.(P07)
- 14.Del CN5,R365;Q13,Q20,Q21,Q11,Q36,Q38.(09)
- 15.Del Q45,R385,Q49,BC381,R414,R416,BC375,R417,BC380,R412.
- 16.Add R29,R30,R31,R35 (10K).(P09);R321 (100) (P12);J8 (P35).
- 17.Change L7,L26,L31,FB22,R520,EC46,EC49 Foot print.
- 18.Changed EC8,EC5 Value to 100uF from 10uF.
- 19.Add Q7 (MMBT2222).Change Q34 to MMBT2222.Chang R230 Value 19.1K to 1K.(P11)
- 20.Changed EC65,EC59 Location.
- 21.Add R321 (100), Del Q32,R231,R235,Q35,R241,BC224,R211,R202,Q30,R226,BC215.(P12).
- 22.Add R418,R402,R460,R427;Del R427,R582
- 23.Del R81



Title			
Modify List			
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