
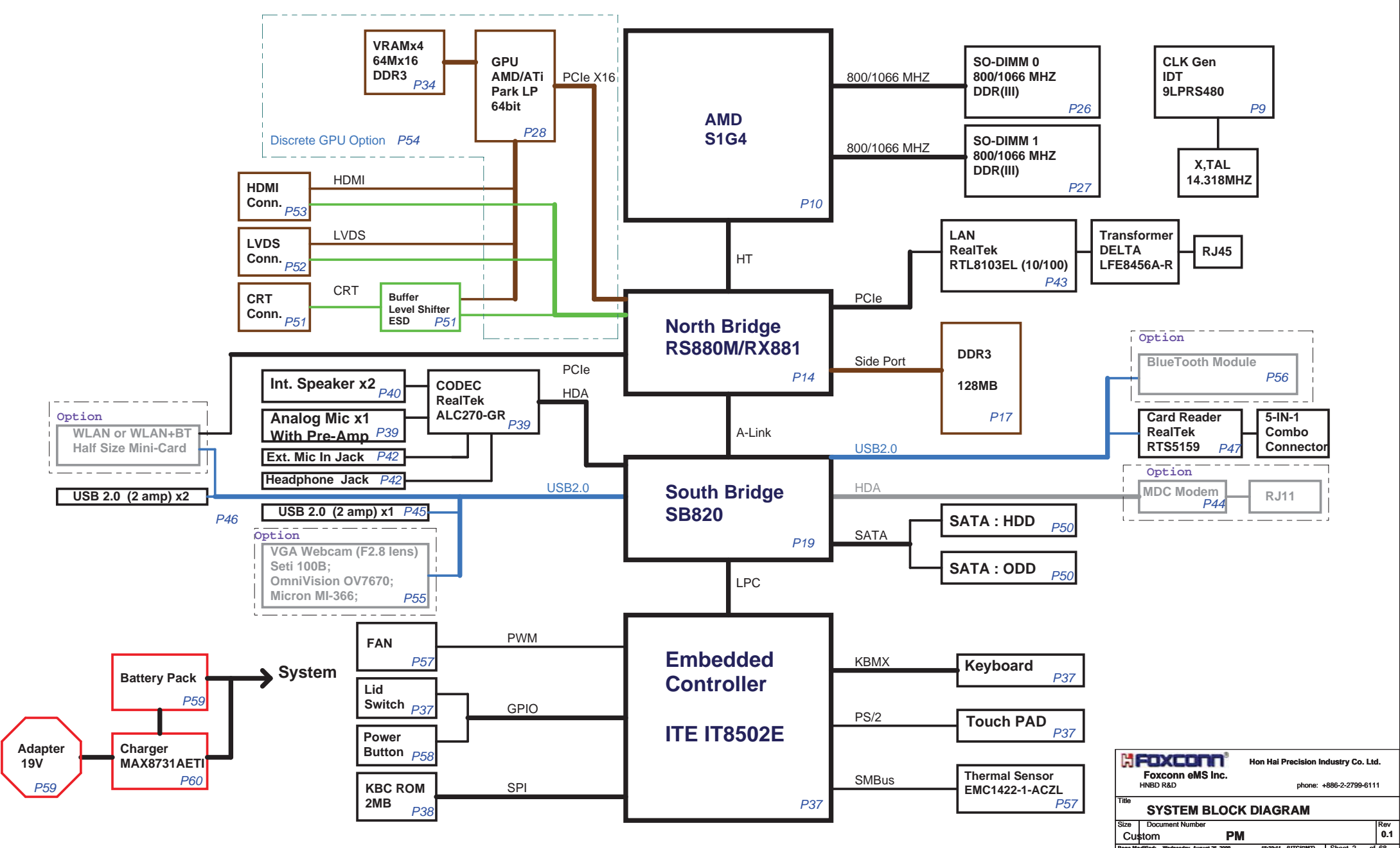


# TABLE OF CONTENTS

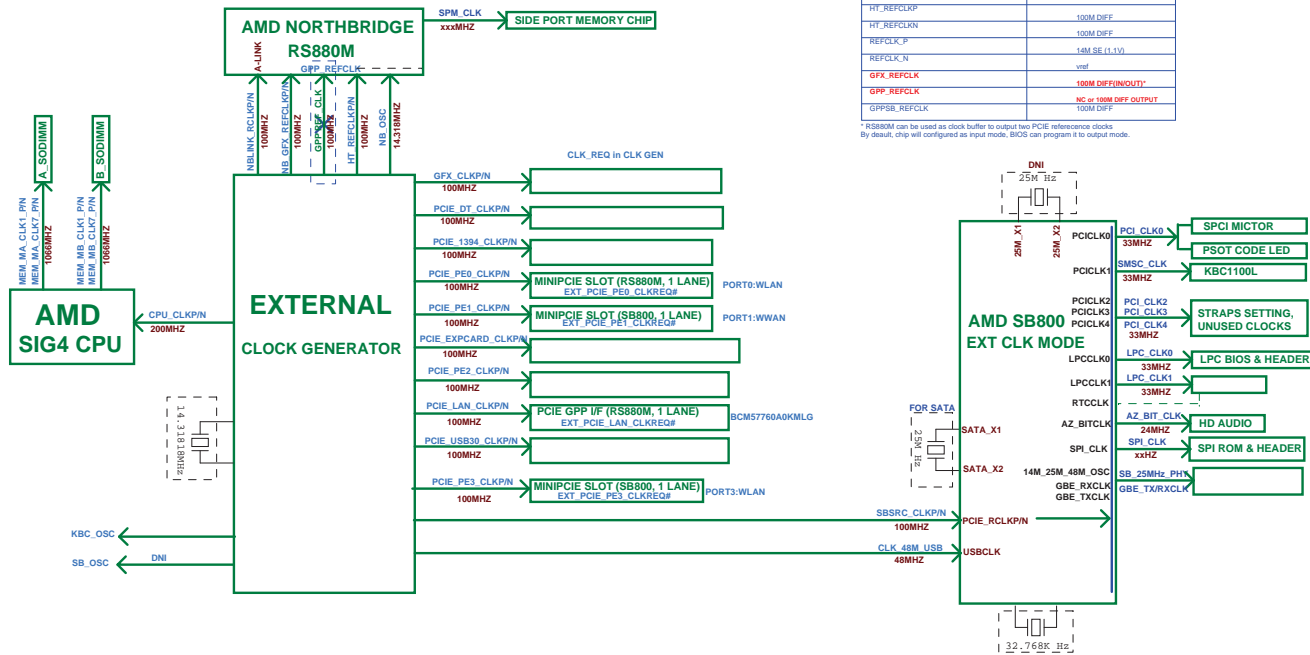
P02 : SYSTEM BLOCK DIAGRAM	P36 : EC Flash ROM/SPI
P03 : CLOCK MAP	P37 : Audio (CODEC_ALC270)
P04 : POWER DELIVERY CHART	P38 : Audio (SPK+AMP)
P05 : POWER SEQUENCY DIAGRAM	P39 : Audio (MUTE)
P06 : POWER SEQUENCE CHART	P40 : Audio (JACK+AMP)
P07 : SMBUS&I2C MAP	P41 : LAN(RTL8103EL)
P08 : RESET SIGNAL MAP	P42 : RJ11
P09 : EXTERNAL CLOCK GENERATOR	P43 : USBx2
P10 : S1G4 HT I/F	P44 : USB DB
P11 : S1G4 CTRL & DEBUG	P45 : Card Reader
P12 : S1G4 DDRIII MEMORY I/F	P46 : Mini-PCie(WLAN)
P13 : S1G4 PWR & GND	P47 : MOUNTING HOLE
P14 : RS880M-HT LINK I/F	P48 : SATA HDD/ODD
P15 : RS880M-PCIE I/F	P49 : CRT
P16 : RS880M-SYSTEM I/F	P50 : LVDS
P17 : RS880M-SPMEM/STRAPS	P51 : HDMI
P18 : RS880M-POWER	P52 : Discrete GPU Option
P19 : SB820-PCIE/PCI/CPU/LPC	P53 : Camera
P20 : SB820-GPIO/USB/AZ/RGMII	P54 : BlueTooth
P21 : SB820-SATA/IDE/HWM/SPI	P55 : FAN/Thermal Sensor
P22 : SB820-POWER & DECOUPLING	P56 : Power Button Board/LED
P23 : SB820-STRAPS	P57 : PWR_DCIN & Battery
P24 : DDR3(SO-DIMM_0) 1/2_M	P58 : PWR_Charger MAX8731AETI
P25 : DDR3(SO-DIMM_1) 2/2_M	P59 : 5V/3.3V MAX17020
P26 : VGA_S3 (PCI-E) 1/6	P60 : Vcore MAX17480
P27 : VGA_S3 (STRAP) 2/6	P61 : +V1.1A TPS51117
P28 : VGA_S3 (IO) 3/6	P62 : +V1.8S NB634
P29 : VGA_S3 (DDR3) 4/6	P63 : 1.5VDDR3 +0_75V TPS51116
P30 : VGA_S3 (DP) 5/6	P64 : VPCIE +VDDA_CPU
P31 : VGA_S3 (POWER) 6/6	P65 : PWR_Others power plane
P32 : VRAM (DDR3) 1/3	P66 : +VDDR_NB / VLDT/ NB634
P33 : VRAM (DDR3) 2/3	P67 : ATVDD TPS51217
P34 : VRAM (BYPASS) 3/3	P68 : +VCCNB TPS51117
P35 : EC+KBC (IT8502E)	

P. Leader	Check by	Design by
 <b>Foxconn eMS Inc.</b> HNBD R&D		
Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111		
Title		
<b>TABLE OF CONTENTS</b>		
Size	Document Number	Rev
C	<b>PM_AMD</b>	0.1
Page Modified: Wednesday, August 28, 2008 10:38:11 (UTC+0800) Sheet 1 of 68		



<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +886-2-2790-6111	
Title			
<b>SYSTEM BLOCK DIAGRAM</b>			
Size	Document Number	Rev	
Custom	<b>PM</b>	<b>0.1</b>	
Page Modified: Wednesday, August 26, 2009		18:38:11 (UTC+GMT)	Sheet 2 of 68

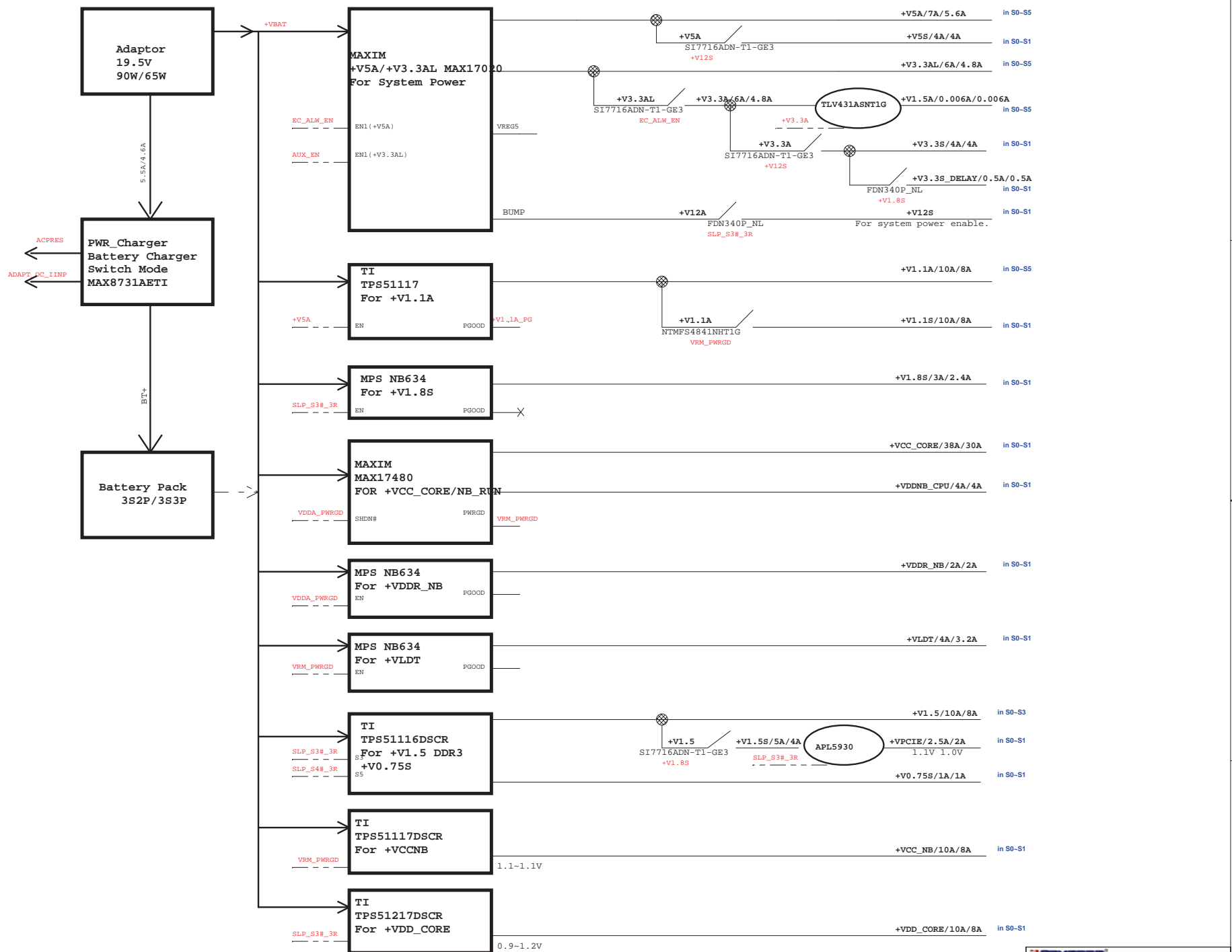
# EXTERNAL CLOCK MODE



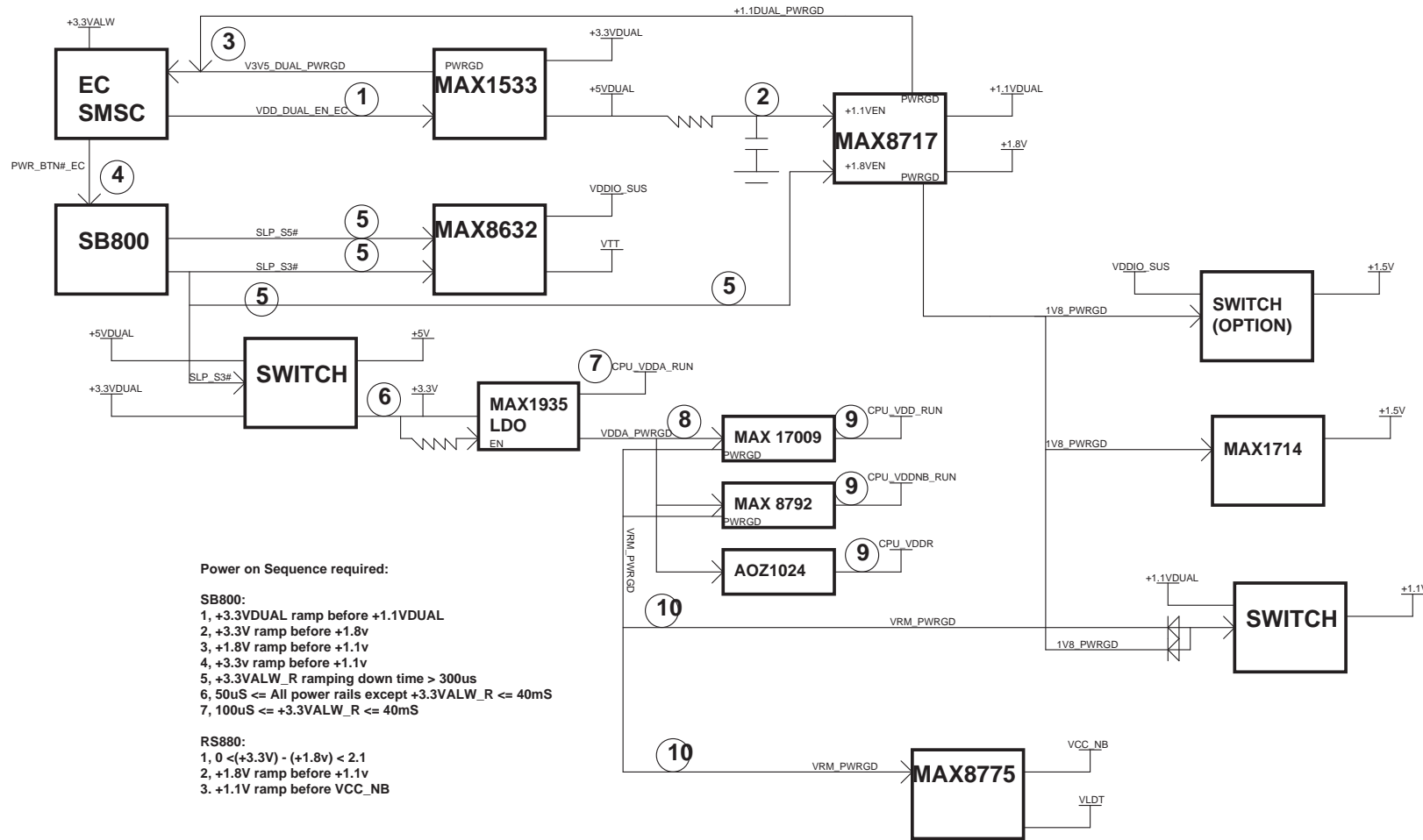
NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

\*RS880M can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode. BIOS can program it to output mode.



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		phone: +886-2-2799-6111	
<b>Title</b> POWER DELIVERY CHART			
<b>Size</b> Custom		<b>Doc Number</b> PM_AMD	
Prep: 11/2011		Rev: 0.1	
Industry: August 26, 2011		16211 (REV.02)   Sheet 4 of 88	



**Power on Sequence required:**

**SB800:**

- 1, +3.3VDUAL ramp before +1.1VDUAL
- 2, +3.3V ramp before +1.8v
- 3, +1.8V ramp before +1.1v
- 4, +3.3v ramp before +1.1v
- 5, +3.3VALW\_R ramping down time > 300us
- 6, 50uS <= All power rails except +3.3VALW\_R <= 40mS
- 7, 100uS <= +3.3VALW\_R <= 40mS

**RS880:**

- 1, 0 < (+3.3V) - (+1.8v) < 2.1
- 2, +1.8V ramp before +1.1v
- 3, +1.1V ramp before VCC\_NB

		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D	
		phone: +886-2-2799-6111	
<b>Title</b>			
<b>POWER SEQUENCY DIAGRAM</b>			
Size	Document Number	Rev	
Custom	PM	0.1	
Page Modified: Wednesday, August 26, 2009 18:39:11 (UTC+GMT)   Sheet 5 of 68			

Power on Sequence required:

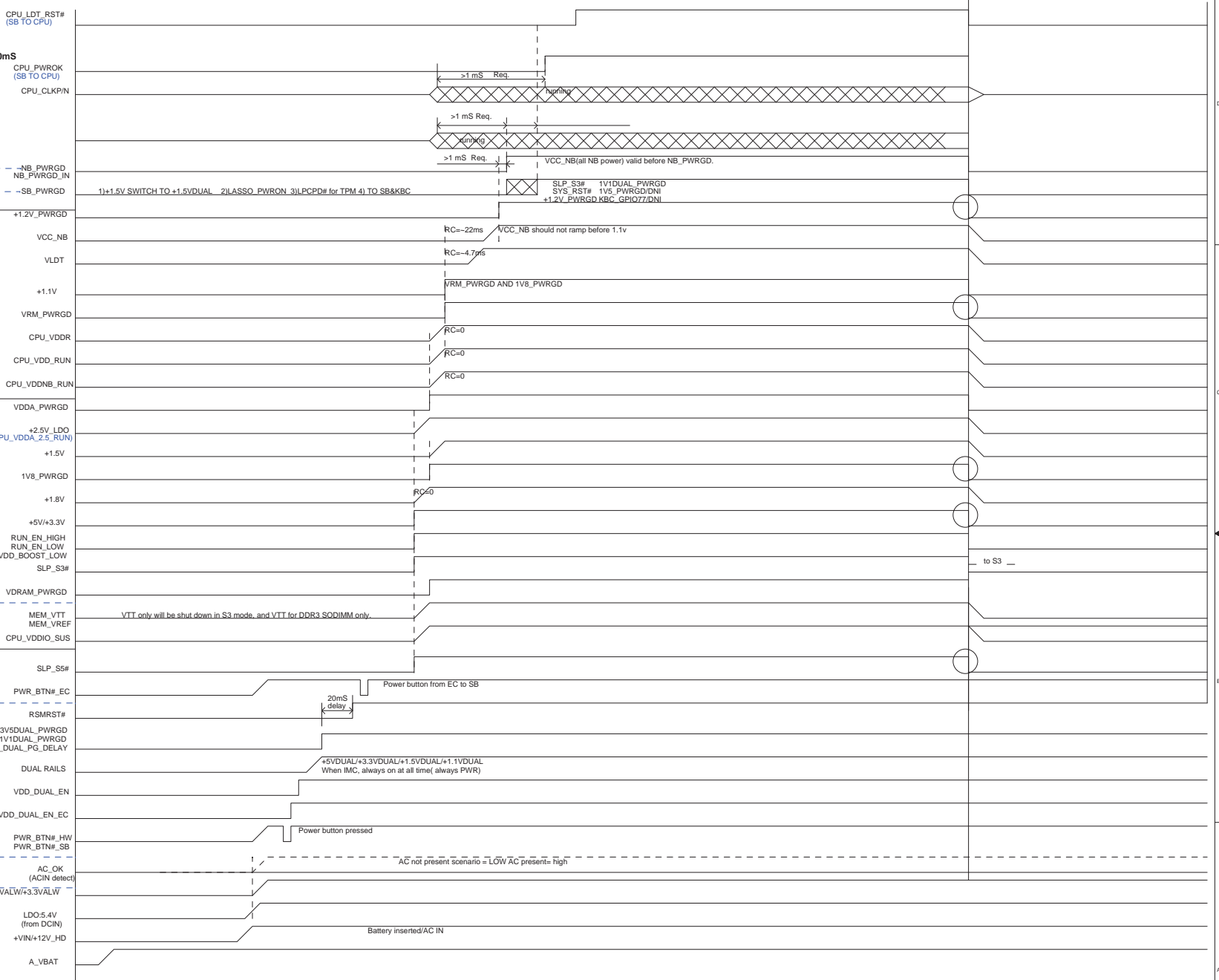
- SB800:**
- +3.3VDUAL ramp before +1.1VDUAL
  - +3.3V ramp before +1.8v
  - +1.8v ramp before +1.1v
  - +3.3v ramp before +1.1v
  - +3.3VALW\_R ramping down time > 300us
  - 50uS <= All power rails except +3.3VALW\_R <= 40mS
  - 100uS <= +3.3VALW\_R <= 40mS

- RS880:**
- 0 < (+3.3V) - (+1.8v) < 2.1
  - +1.8v ramp before +1.1v
  - +1.1V ramp before VCC\_NB

SB OUTPUT --- -NB\_PWRGD  
 NB\_PWRGD\_IN  
 SB INPUT --- -SB\_PWRGD

GROUP B

GROUP A



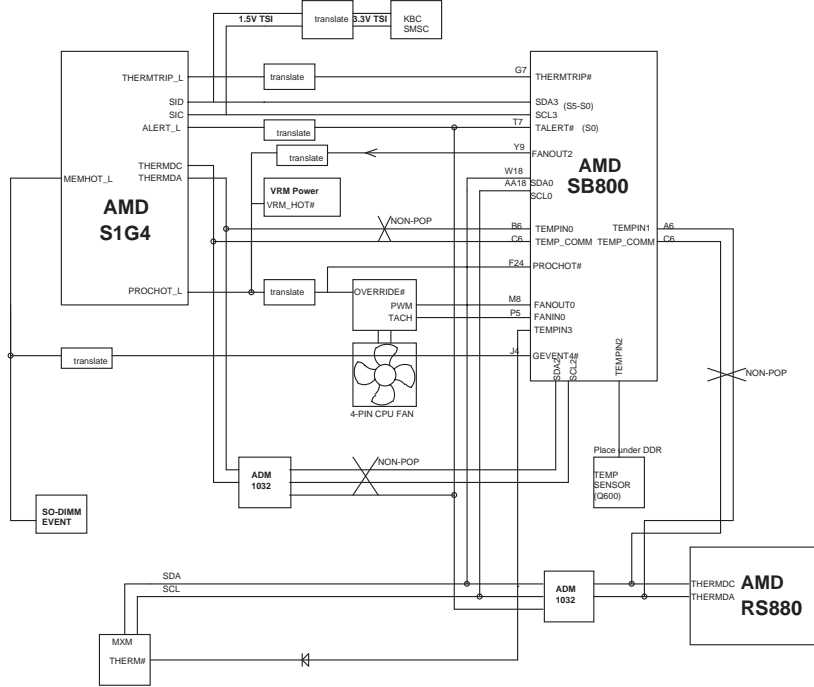
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc.  
 HINSD R&D phone: +886-2-2799-6111

Title: **POWER SEQUENCY TIMING**

Size	Document Number	Rev
Custom	PM	0.1

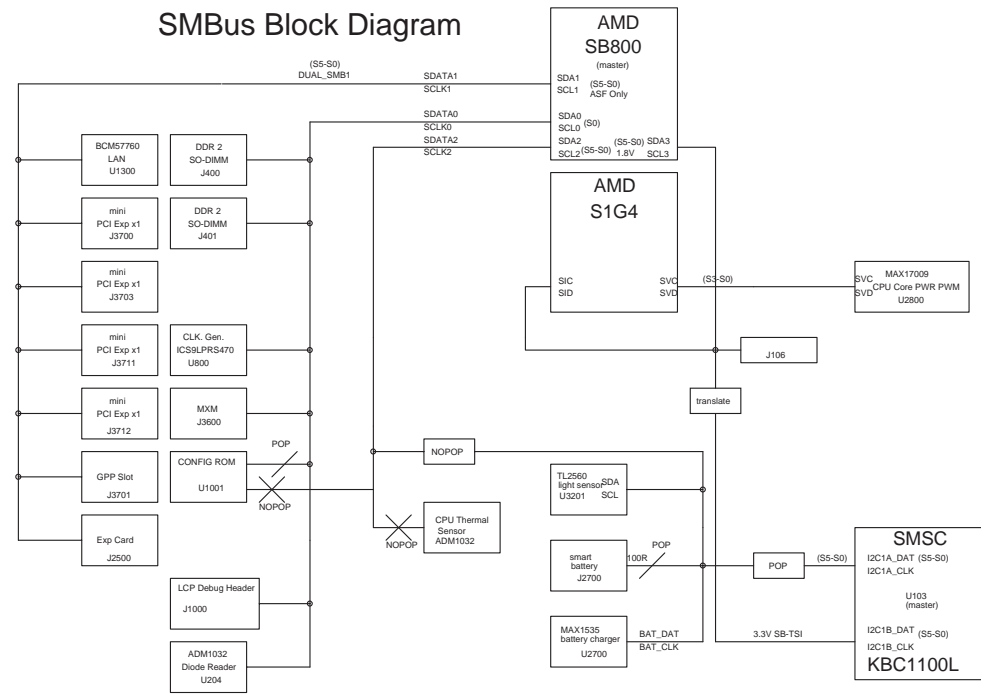
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## Thermal Systems (Emergency Shutdown, Throttling, Fan Control)



Thermal disaster prevention is implemented by PROCHOT\_L and THERMTRIP\_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

## SMBus Block Diagram



## Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description	RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running	ON	ON	ON	ON	ON
G0	S0	C0	Running	P-state transitions under OS control	ON	ON	ON	ON
G0	S0	C1	Halt		ON	ON	ON	ON
G0	S0	C2	Stop grant, caches snooperable		ON	ON	ON	ON
G0	S0	C3	TBD		ON	ON	ON	ON
G0	S0	C4	TBD		ON	ON	ON	ON
G1	S1	OFF	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off	ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN	ON	ON	ON	OFF	OFF
G3	OFF	OFF	Mechanical off	ON	OFF	OFF	OFF	OFF

## Group Name Description

INT: Stuff when use internal clock generator  
 EXT: Stuff when use external clock generator  
 DNI: DO NOT INSTALL  
 KBC: Stuff when use external KBC  
 IMC: Stuff when use internal EC  
 A11: Resistors marked with "A11" is only for SB800A11 ONLY.

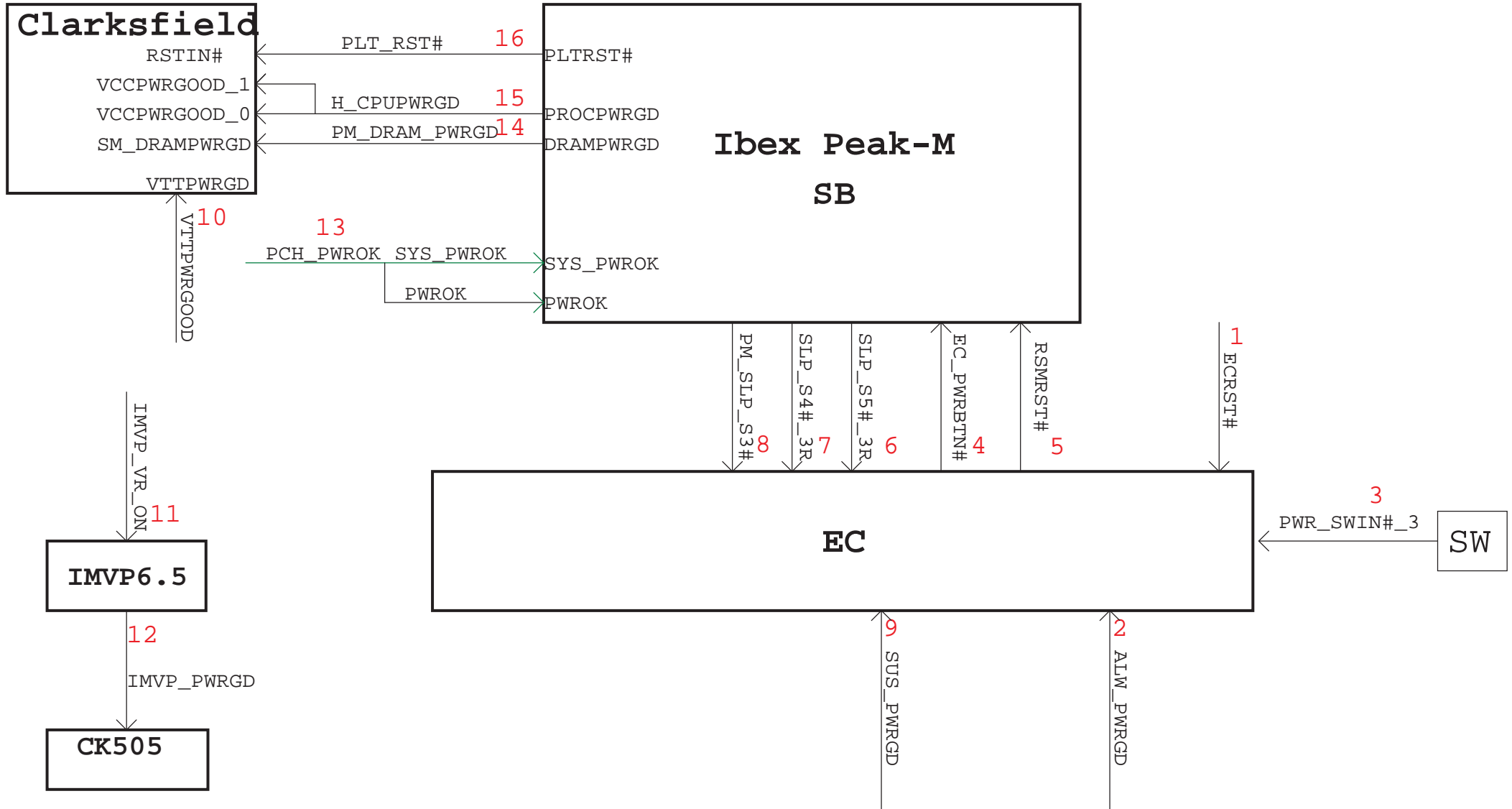
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc.  
 HNBD R&D phone: +886-2-2799-6111

Title: **SMBUS&I2C MAP**

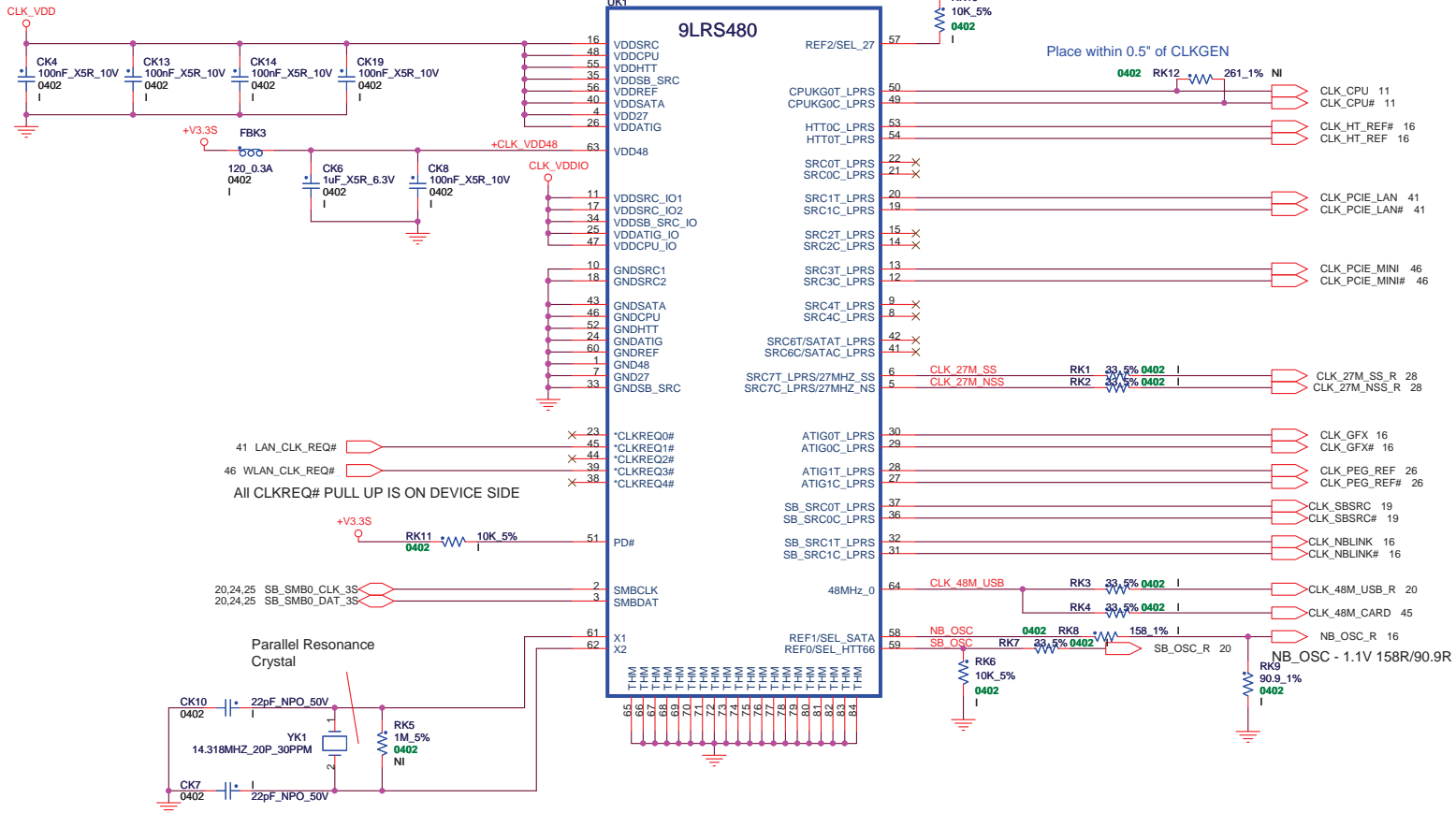
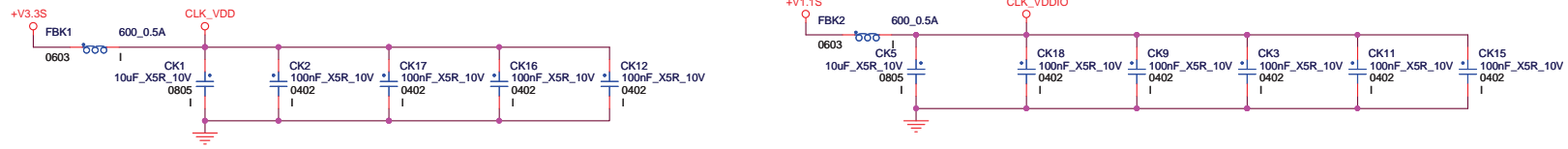
Size	Document Number	Rev
Custom	PM	0.1

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# RESET SIGNAL MAP







All CLKREQ# PULL UP IS ON DEVICE SIDE

### NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPSPB_REFCLK	100M DIFF

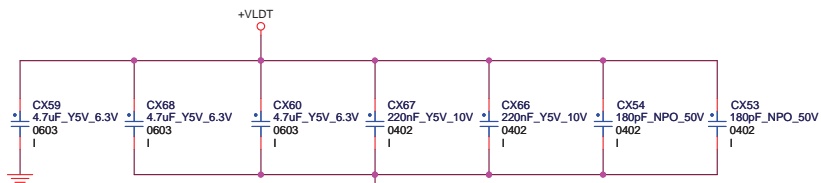
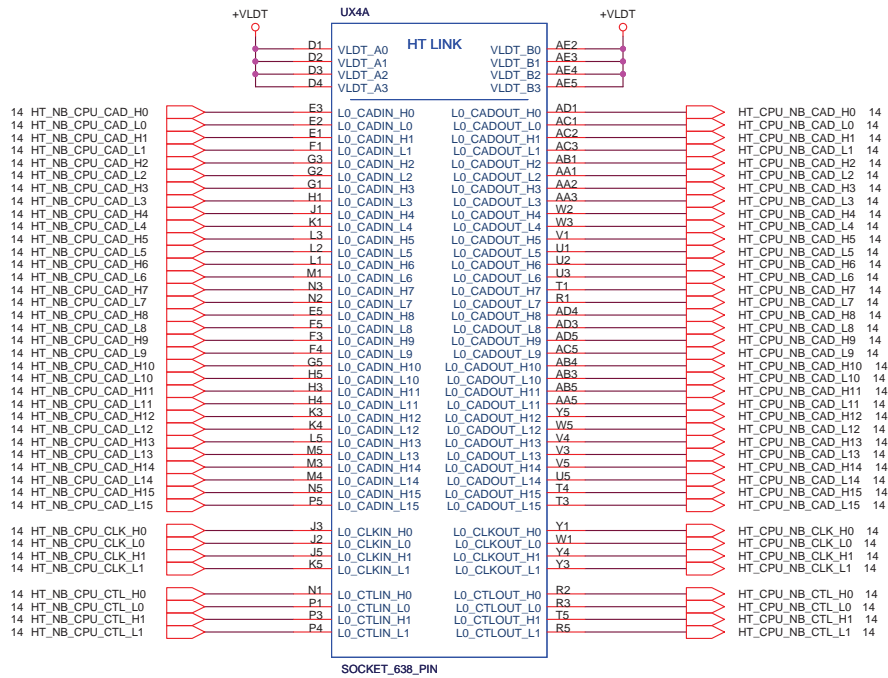
\* RS880M can be used as clock buffer to output two PCIe reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.

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Title: **EXTERNAL CLOCK GENERATOR**

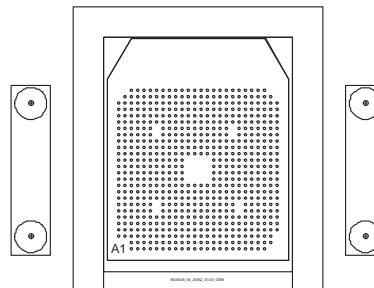
Size: Custom Document Number **PM** Rev: **0.1**


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Place close to socket

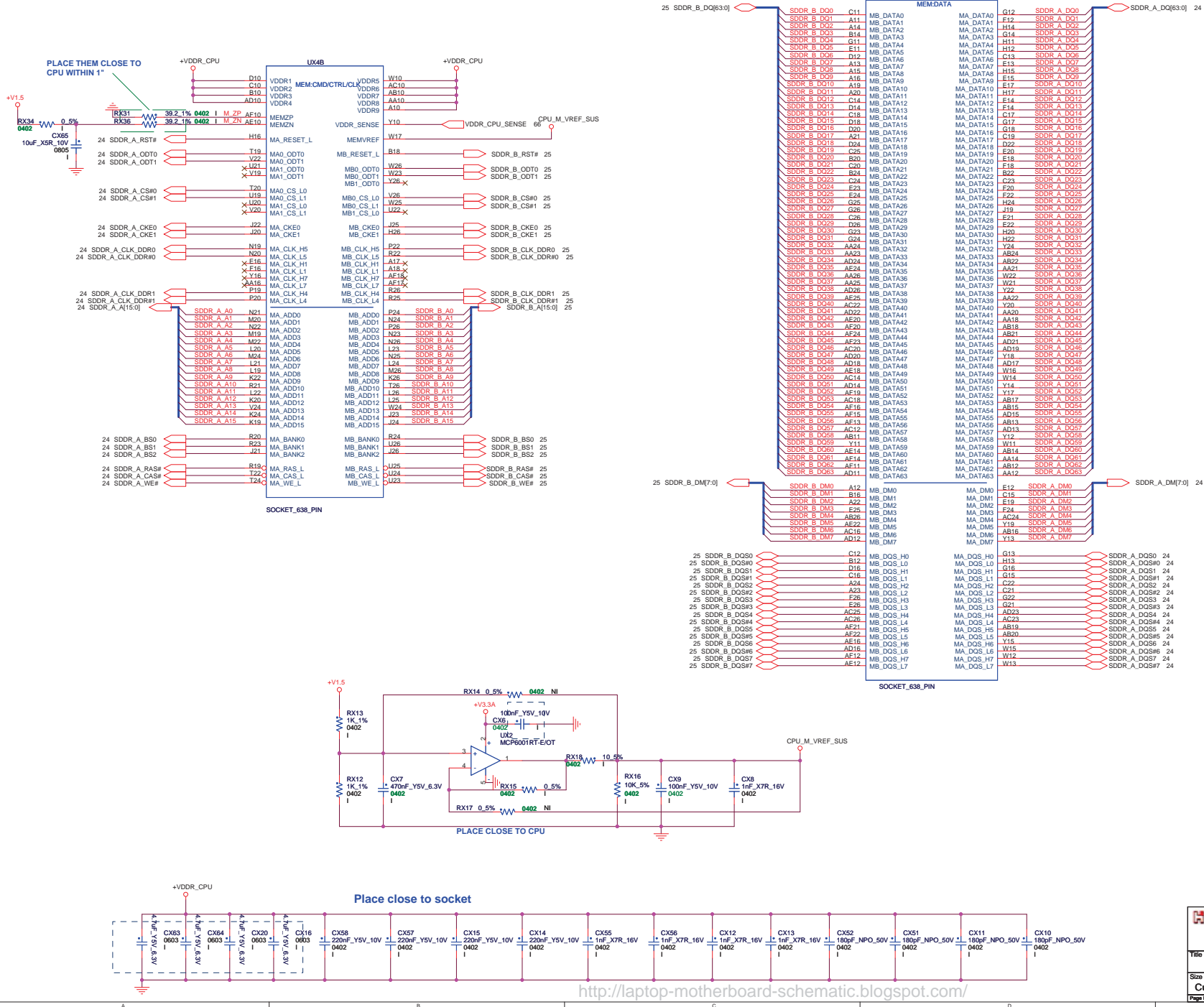
 \* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



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<b>Title</b>			
<b>S1G4 HT I/F</b>			
Size	Document Number		Rev
Custom	PM		0.1
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# Processor Memory Interface



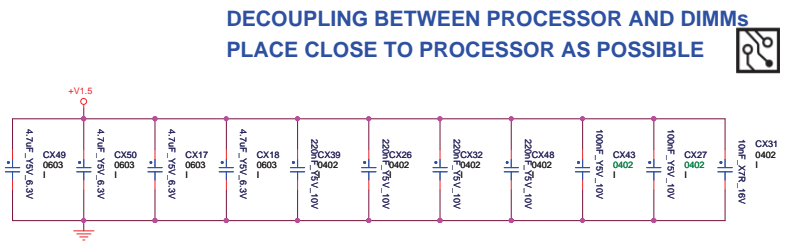
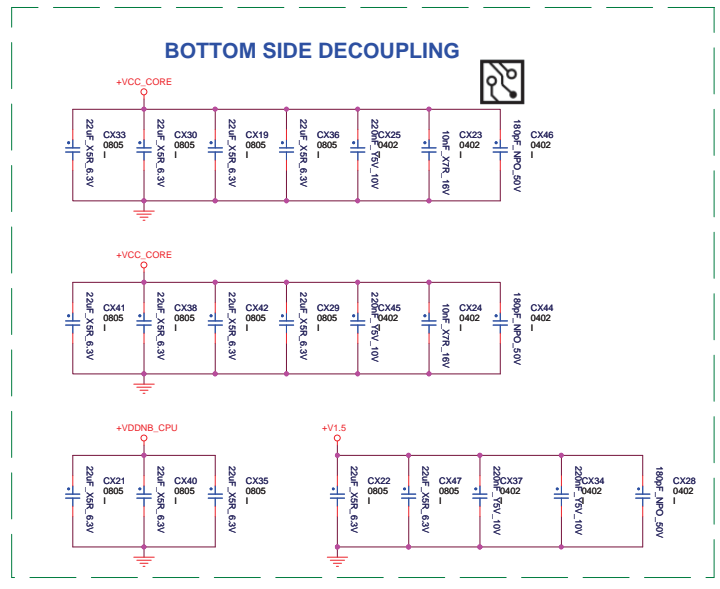
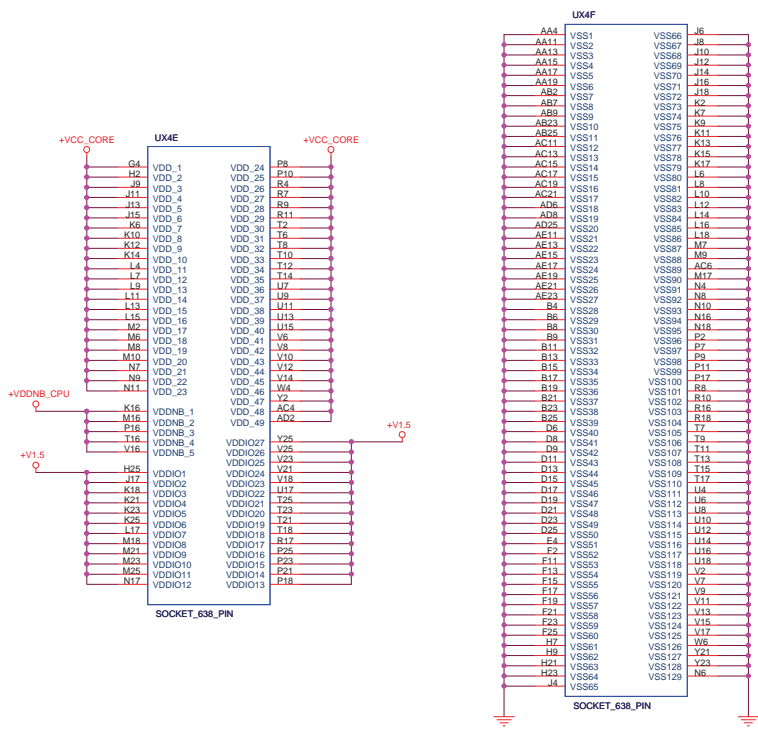
<http://laptop-motherboard-schematic.blogspot.com/>

**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
**Foxconn eMS Inc.**  
 HNEID R&D phone: +886-2-2799-6111

Title: **S1G4 DDRIII MEMORY W/F**

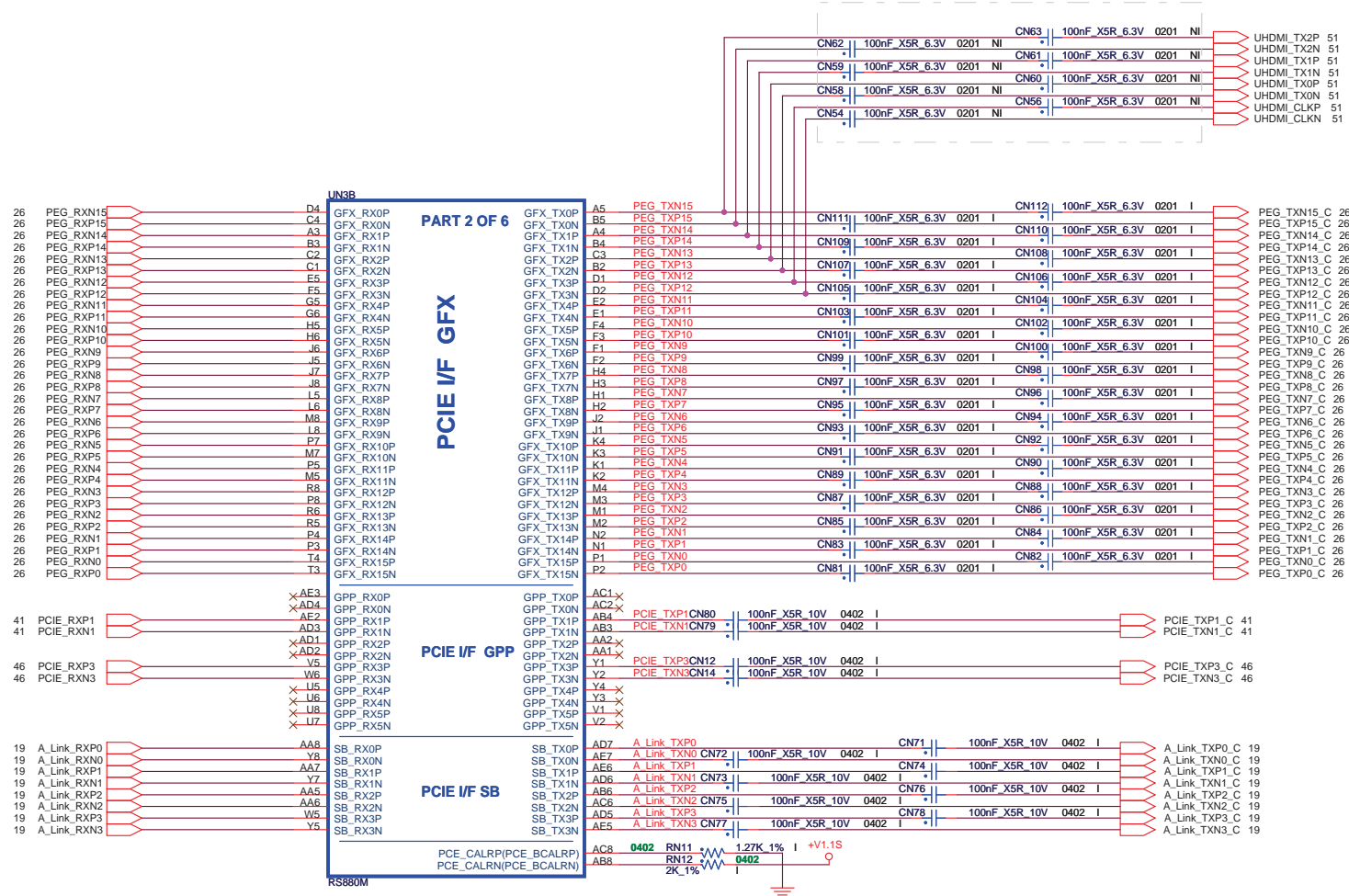
Size: Document Number  
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Discrete GPU: Not Install  
UMA: Install



Keep the impedance of PCIE lane to 85ohm +/-15%  
Including the A-link



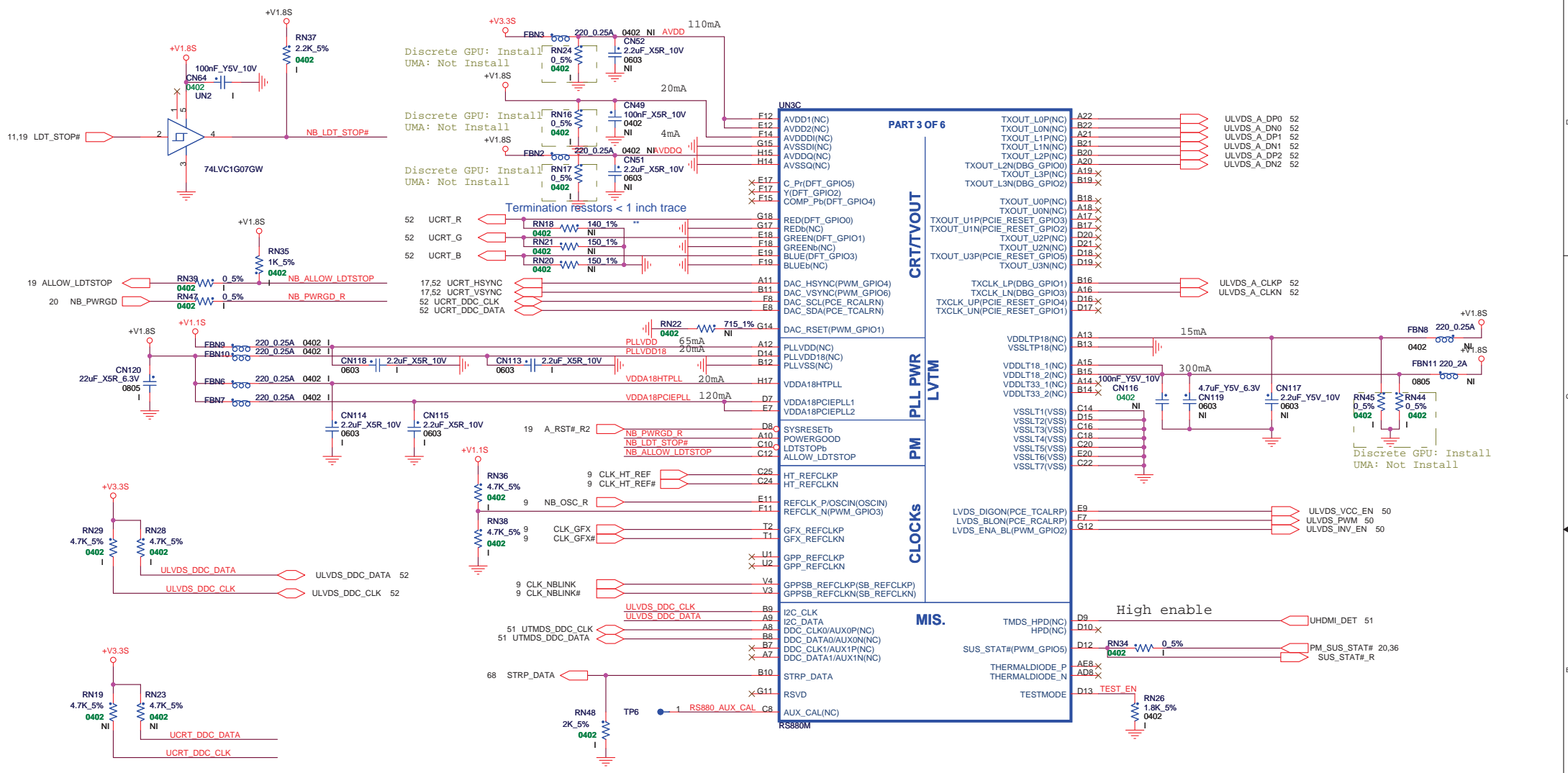
All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices  
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso cable for Guam.  
Customer need to follow the MBDD.

**Foxconn** Hon Hai Precision Industry Co. Ltd.  
Foxconn eMS Inc.  
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Title: **RS880M-PCIE I/F**

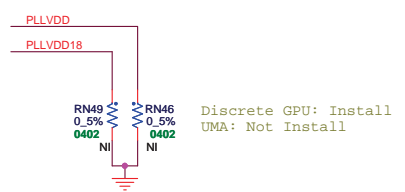
Size	Document Number	Rev
Custom	PM	0.1

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### RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMSD_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL



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Title: **RS880M-SYSTEM I/F**

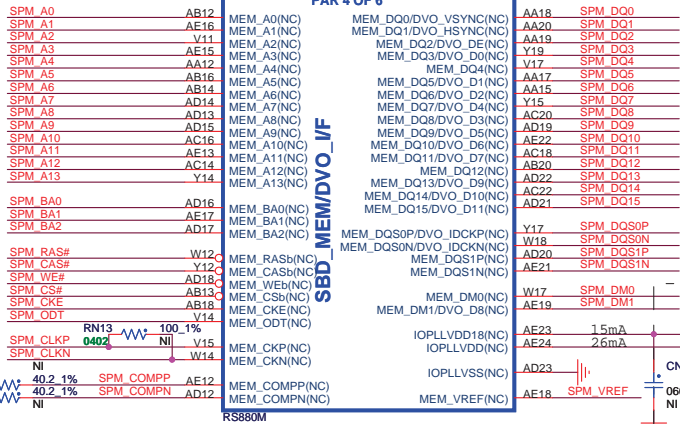
Size	Document Number	Rev
Custom	PM	0.1

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UN3D

PAR 4 OF 6



+V1.5S

DIS DNI

+V1.8S

+V1.5S

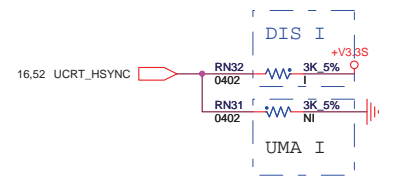
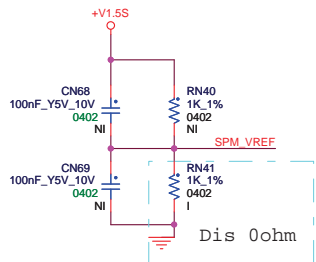
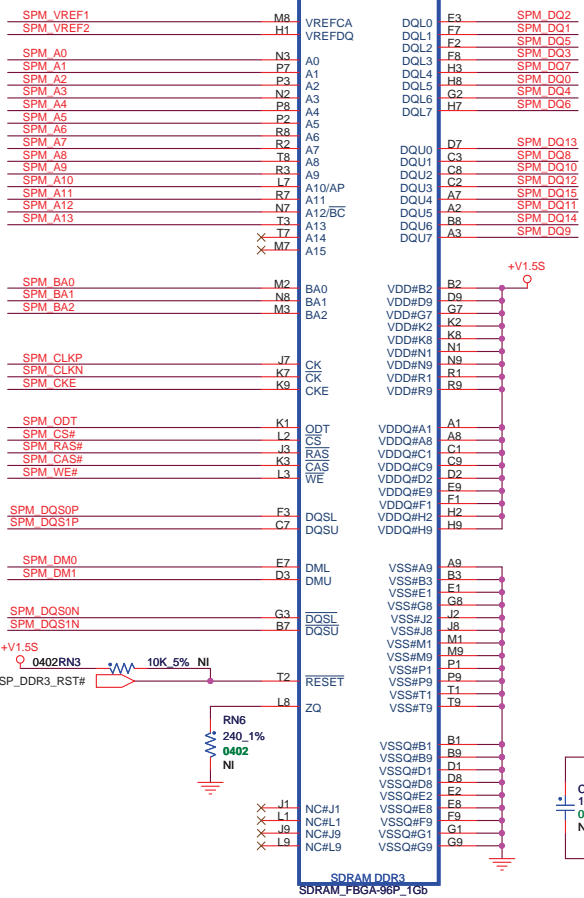
+V3.3S

**STRAP\_DEBUG\_BUS\_GPIO\_ENABLED**

Enables the Test Debug Bus using GPIO.

RS880M	
1	Disable
0	Enable

UN1



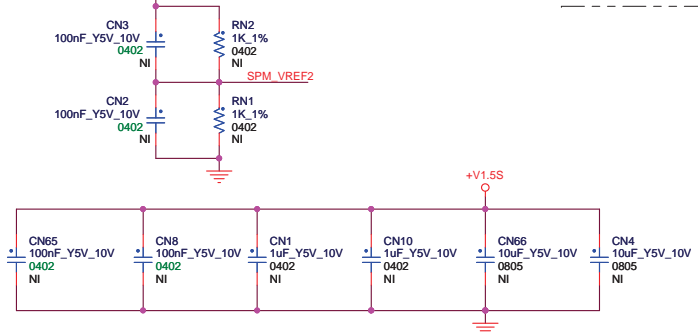
**RS880M: Enables Side port memory**

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not

- 1 = Memory Side port Not available
- 0 = Memory Side port available

Register Readback of strap: NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]

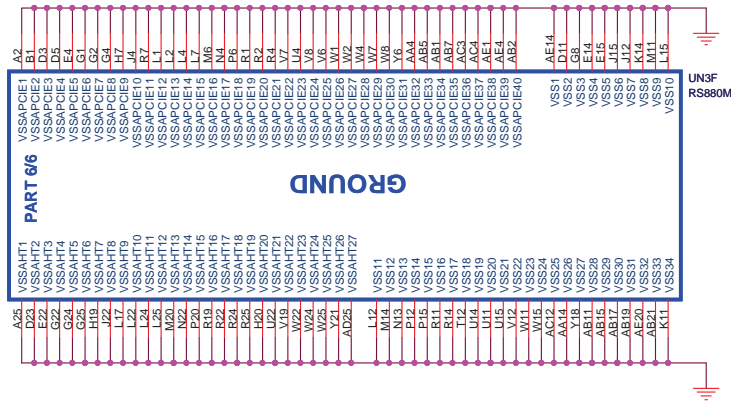


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Title: **RS880M-SPMEM/STRAPS**

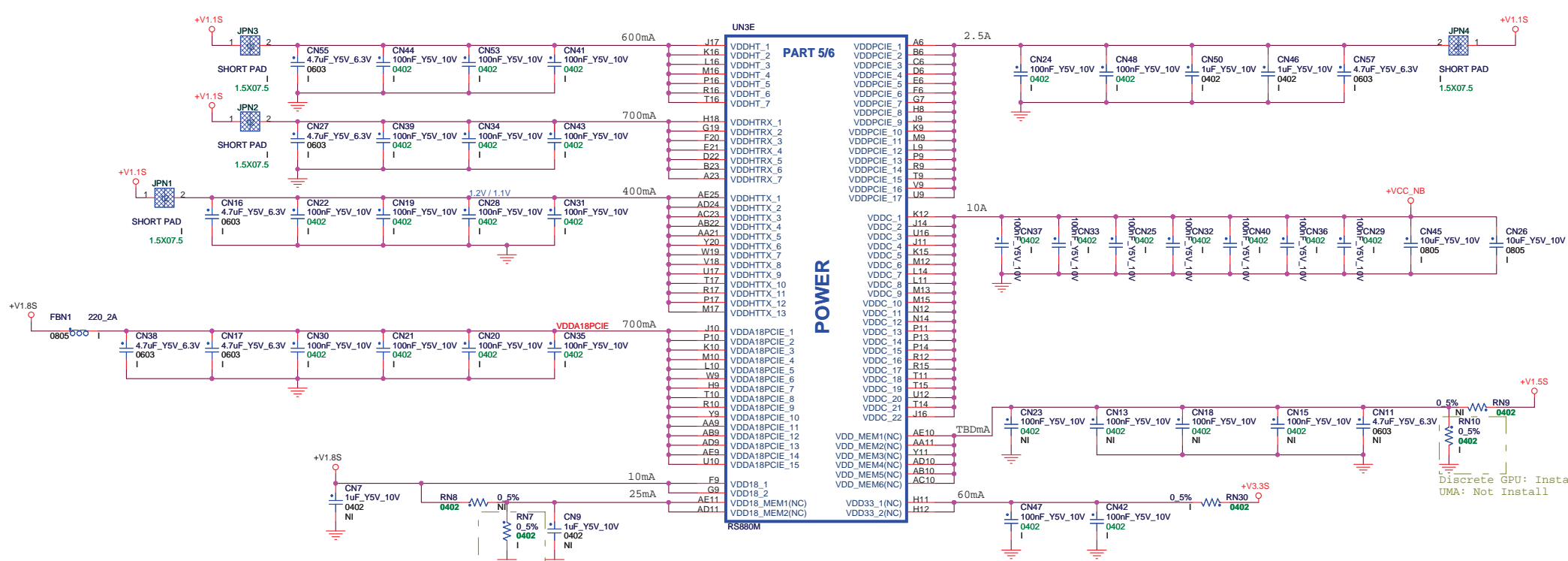
Size	Document Number	Rev
Custom	PM	0.1

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**RS880M POWER TABLE**

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVDD18	+1.8V	VDDL23	NC



Discrete GPU: Install  
UMA: Not Install

Discrete GPU: Install  
UMA: Not Install

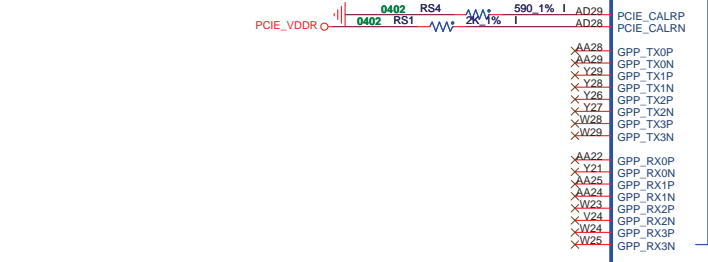
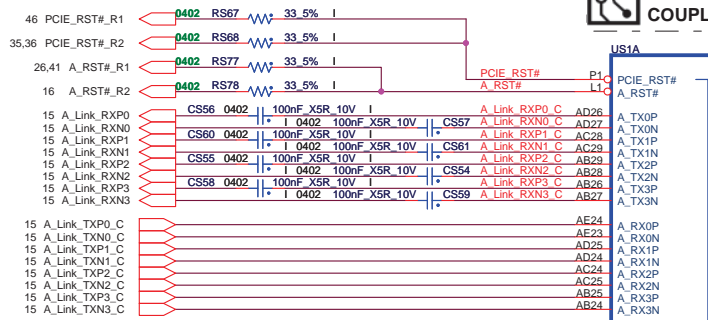
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
Foxconn eMS Inc.  
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Title: **RS880M-POWER**

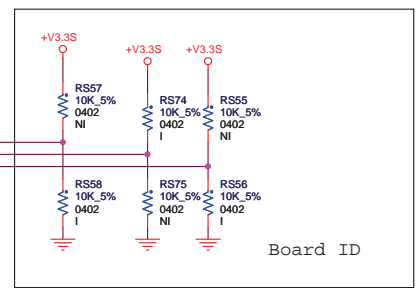
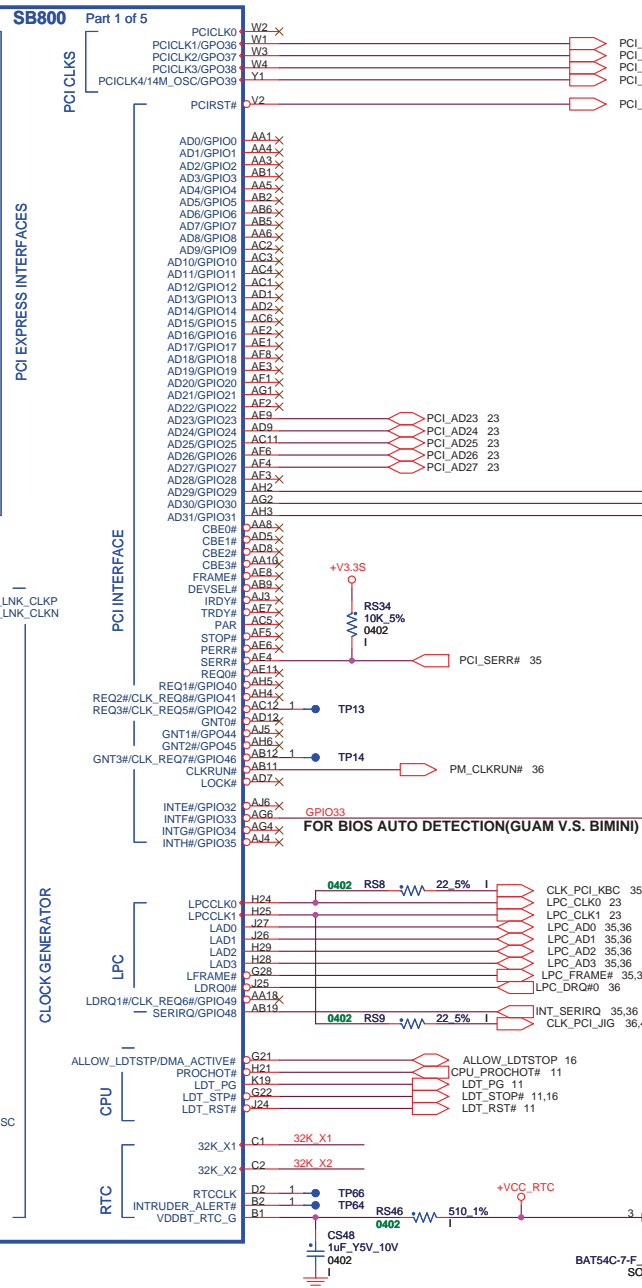
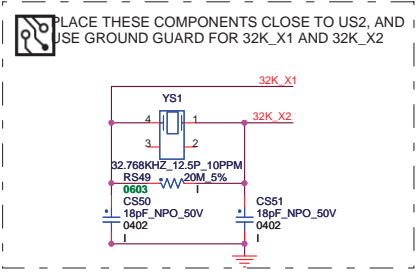
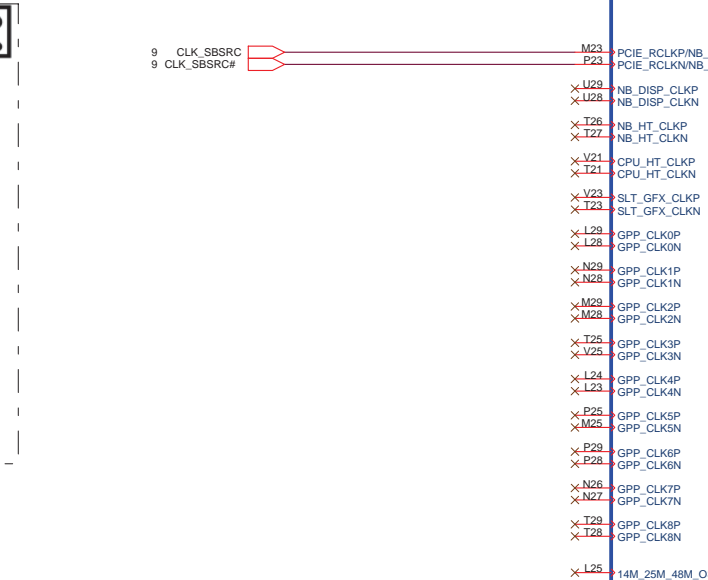
Size	Document Number	Rev
Custom	PM	0.1

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**PLACE THESE PCIE AC COUPLING CAPS CLOSE TO US2**



**NOTE:** The OR serial resistor on SB\_CLK pair must share Pad with the serial resistor close to U800



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Title: **SB820-PCIE/PCI/CPU/LPC/CLK**

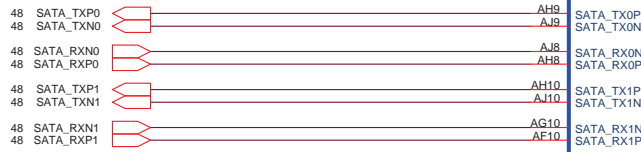
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Custom **PM** Rev: 0.1

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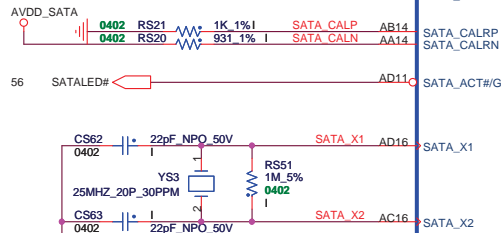
SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only



SATA PORTS DISTRIBUTION:  
0, - 2.5 INCH DISK DRIVER  
1, SATA ODD  
2 & 3 & 4 & 5, NOT USED

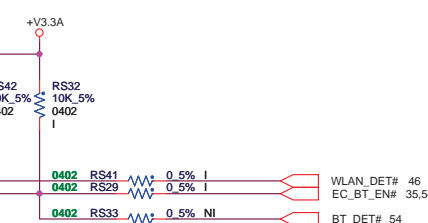
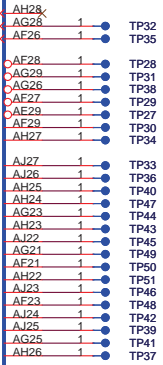
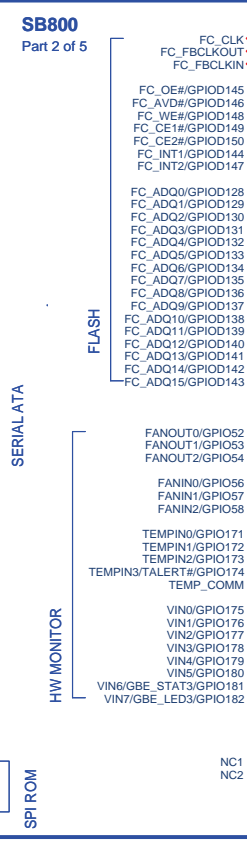


PLACE SATA\_CAL RES VERY CLOSE TO BALL OF U600



US1B

**SB800**  
Part 2 of 5



SB800 A11

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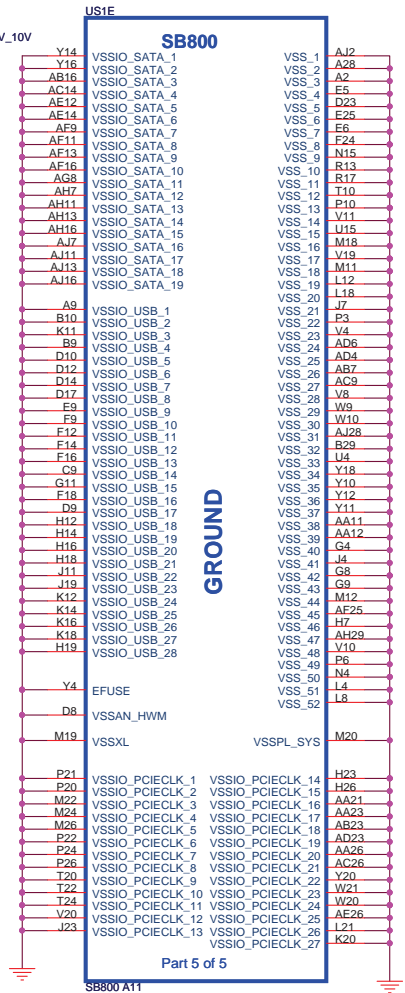
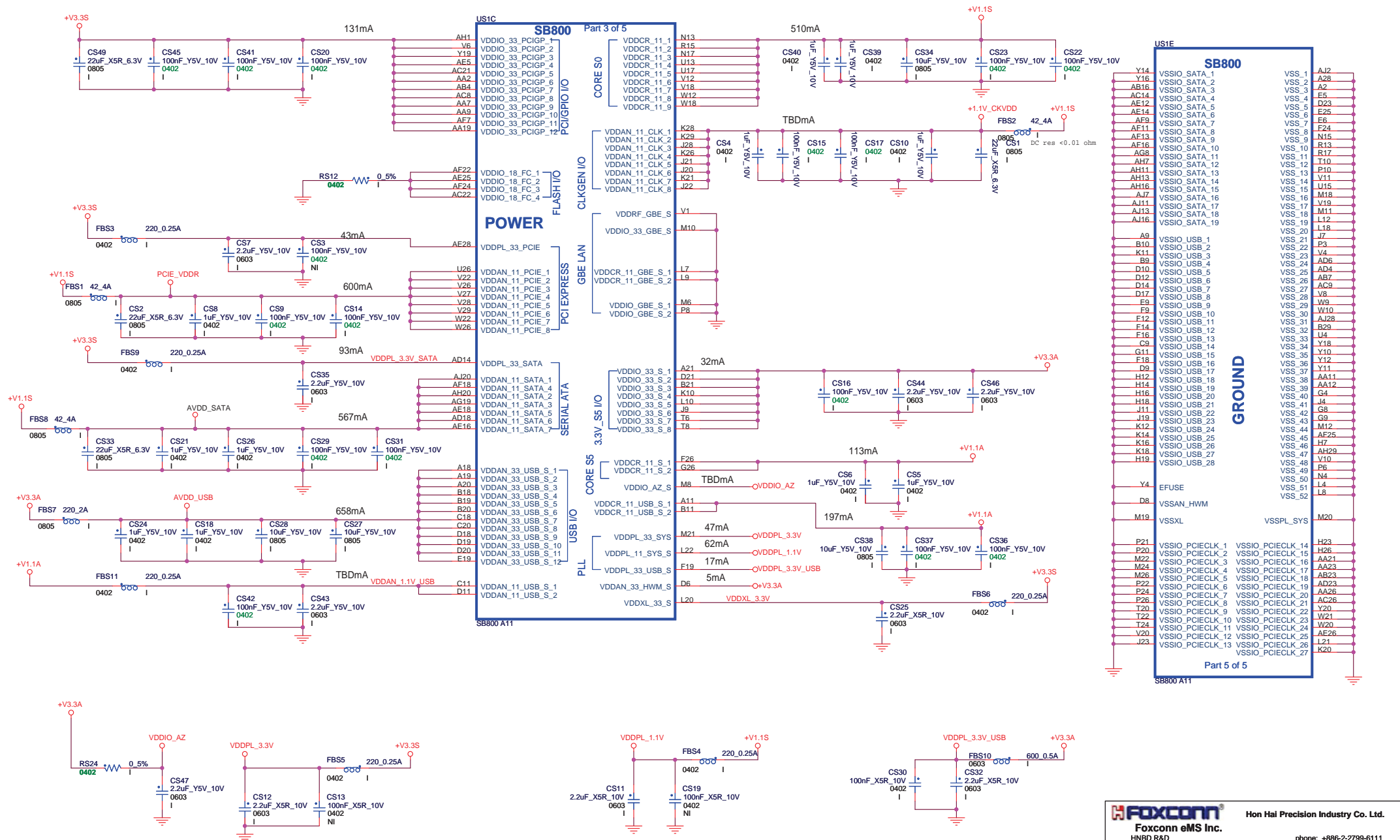
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Size	Document Number	Rev
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



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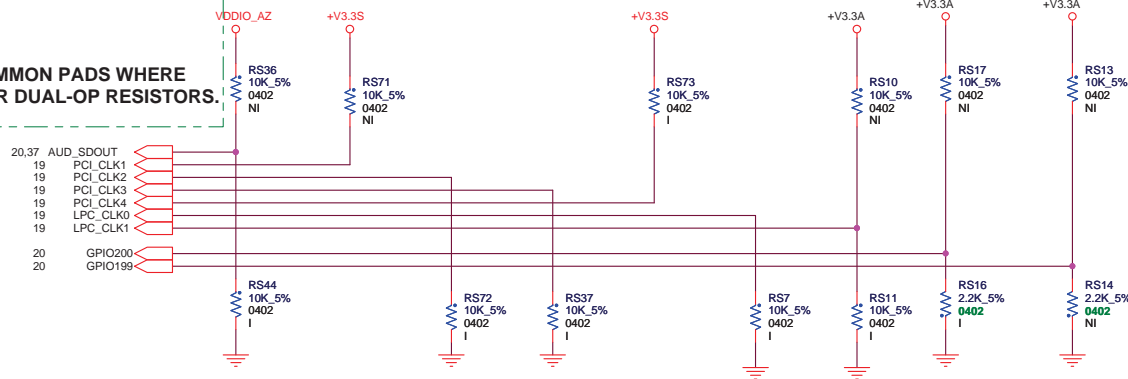
Title: **SB820-POWER & DECOUPLING**

Size	Document Number	Rev
Custom	PM	0.1

Page Modified: Wednesday, August 26, 2009 18:39:11 (UTC/GMT) Sheet 22 of 68



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

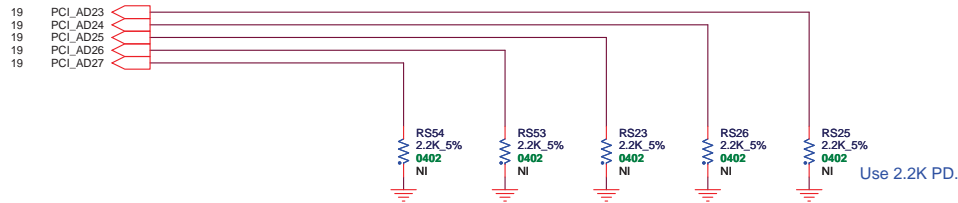


REQUIRED STRAPS

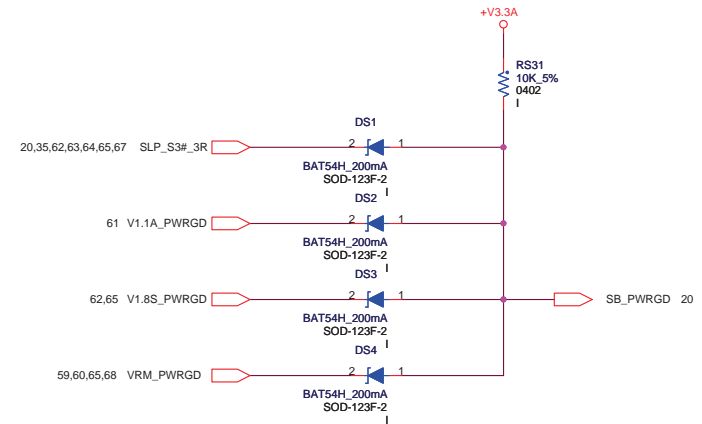
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



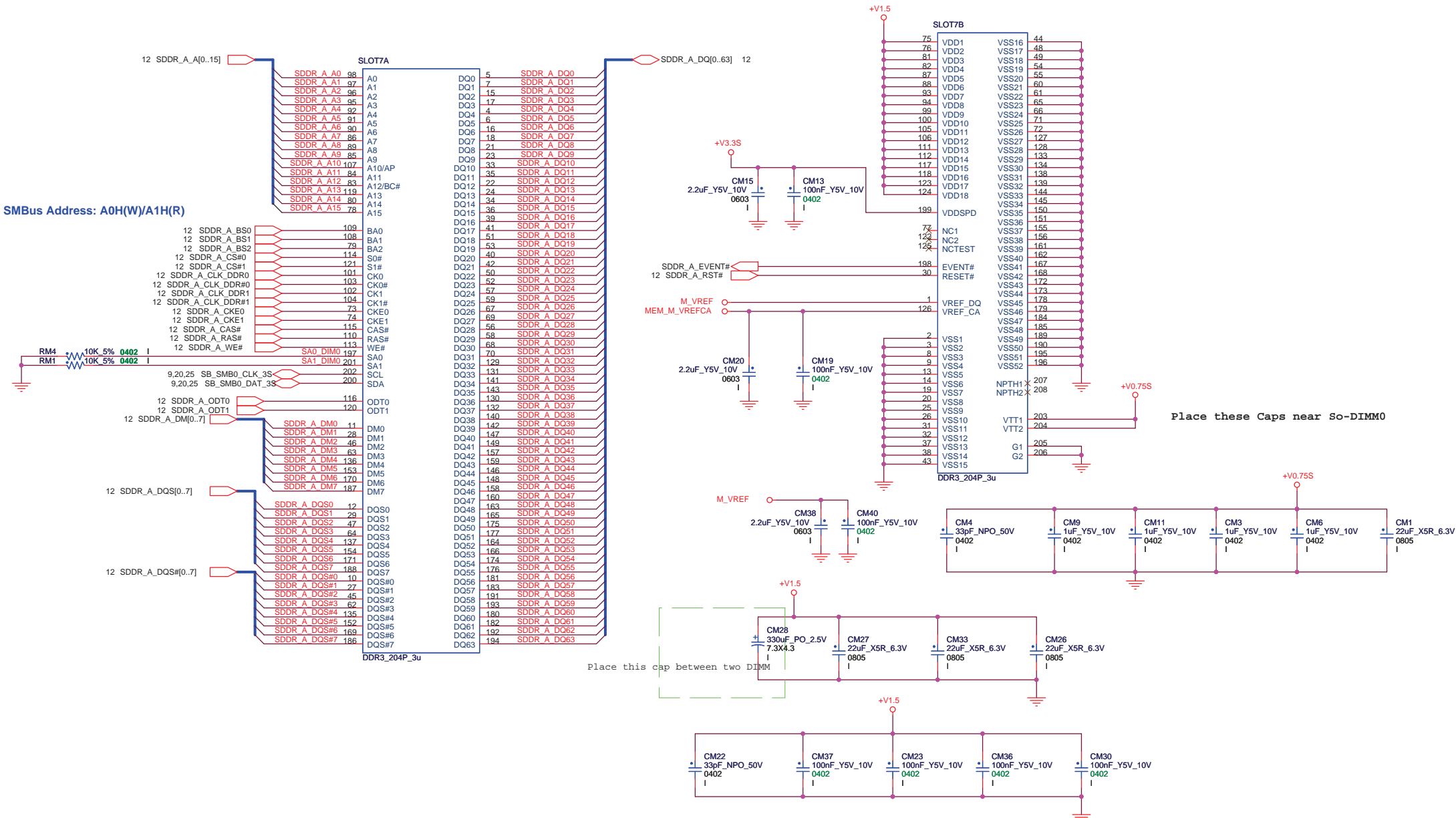
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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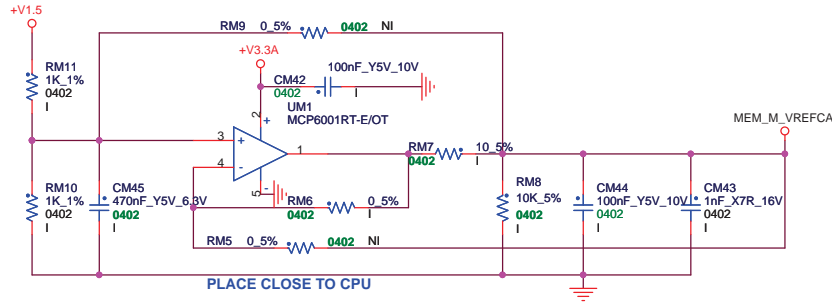
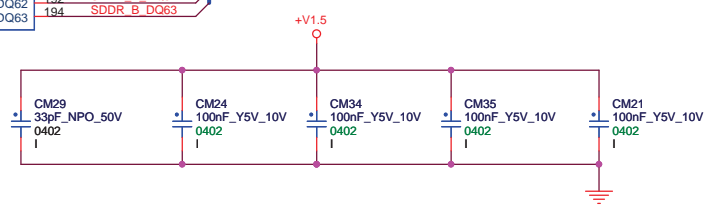
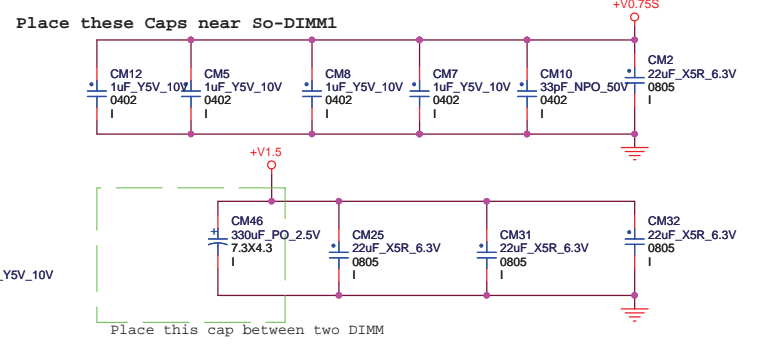
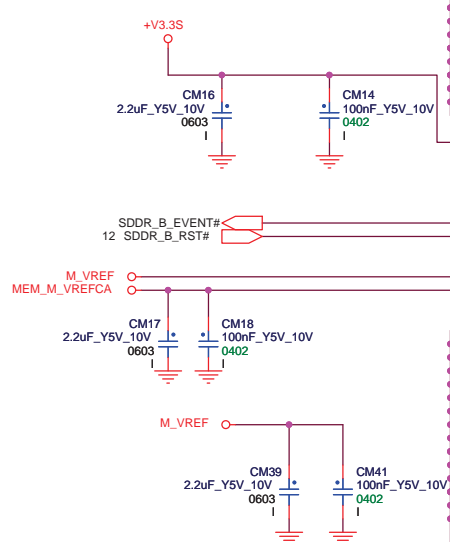
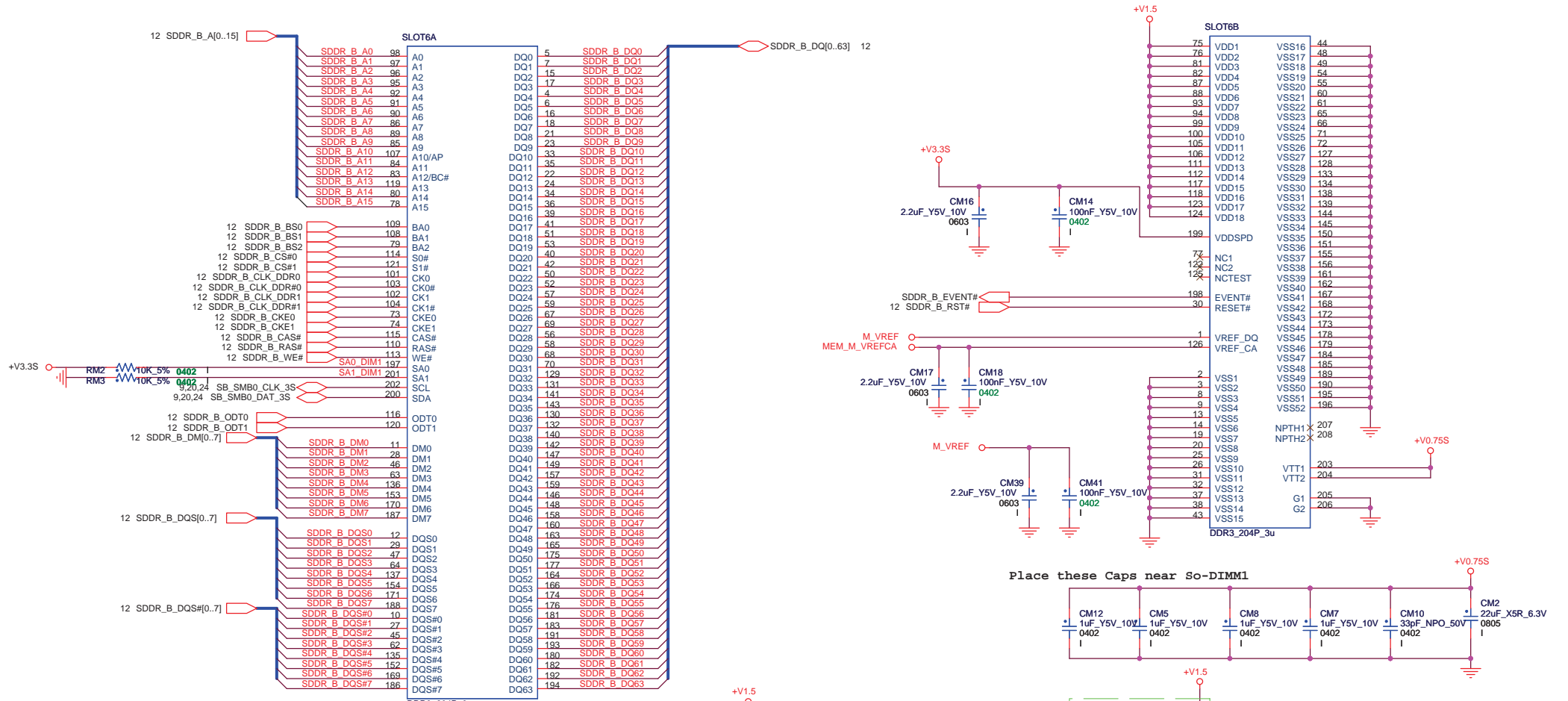
Title: **SB820-STRAPS**  
 Size: Custom Document Number: PM Rev: 0.1  
 Page Modified: Wednesday, August 26, 2009 18:39:11 (UTC/GMT) Sheet 23 of 68

SMBus Address: A0H(W)/A1H(R)



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HINBD R&D			
<b>Title</b> <b>DDR3 SO-DIMM_0</b>			
<b>Size</b> Custom	<b>Document Number</b> PM	<b>Rev</b> 0.1	
Page Modified: Wednesday, August 26, 2009 18:38:11 (UTC/GMT) Sheet 24 of 68			





Place these Caps near So-DIMM1

Place this cap between two DIMM

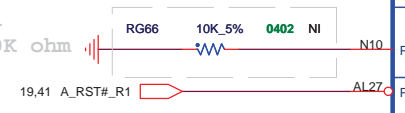
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
**Foxconn eMS Inc.**  
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Title: **DDR3 SO-DIMM\_2**

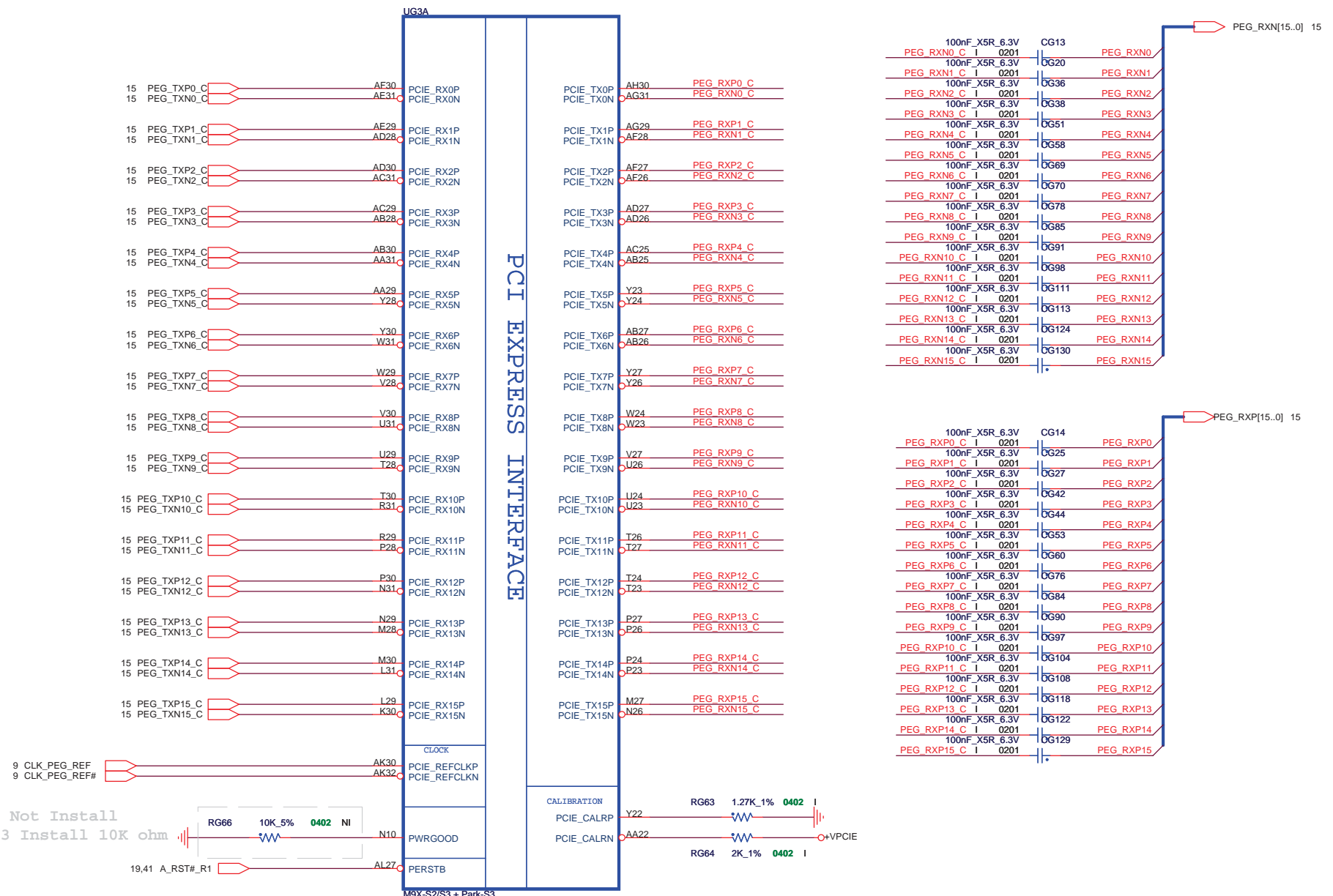
Size	Document Number	Rev
Custom	PM	0.1

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M93-S3 Not Install  
 PARK-S3 Install 10K ohm



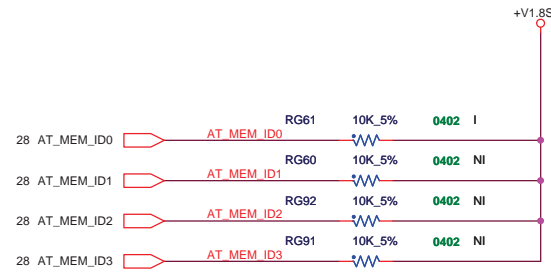
PCI EXPRESS INTERFACE



<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
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Title <b>VGA (PCI-E) 1/6</b>			
Size	Document Number	Rev	
Custom	PM	0.2	
Page Modified: Wednesday, August 26, 2009		18:38:11 (UTC/GMT)	Sheet 26 of 68

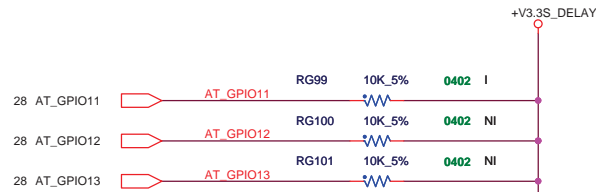
**Strap for DDR3  
MEM\_ID (0:1:2:3)**

0000 64Mx16 Samsung (K4W1G1646E-HC12) 512MB  
 0001 64Mx16 Hynix (H5TQ1G63BFR-12C) 512MB  
 1000 64Mx16 Qimonda 512MB



If no ROM attached, GPIO[13:12:11] ;  
 CONFIG{2:0}  
 controls the memory aperture size.

Reserved 011  
 512MB 001



**HSYNC , VSYNC  
AUD[1] , AUD[0]**

0,0 No audio function  
 0,1 Audio for DisplayPort and HDMI if dongle is detected  
 1,0 Audio for DisplayPort only  
 1,1 Audio for both DisplayPort and HDMI

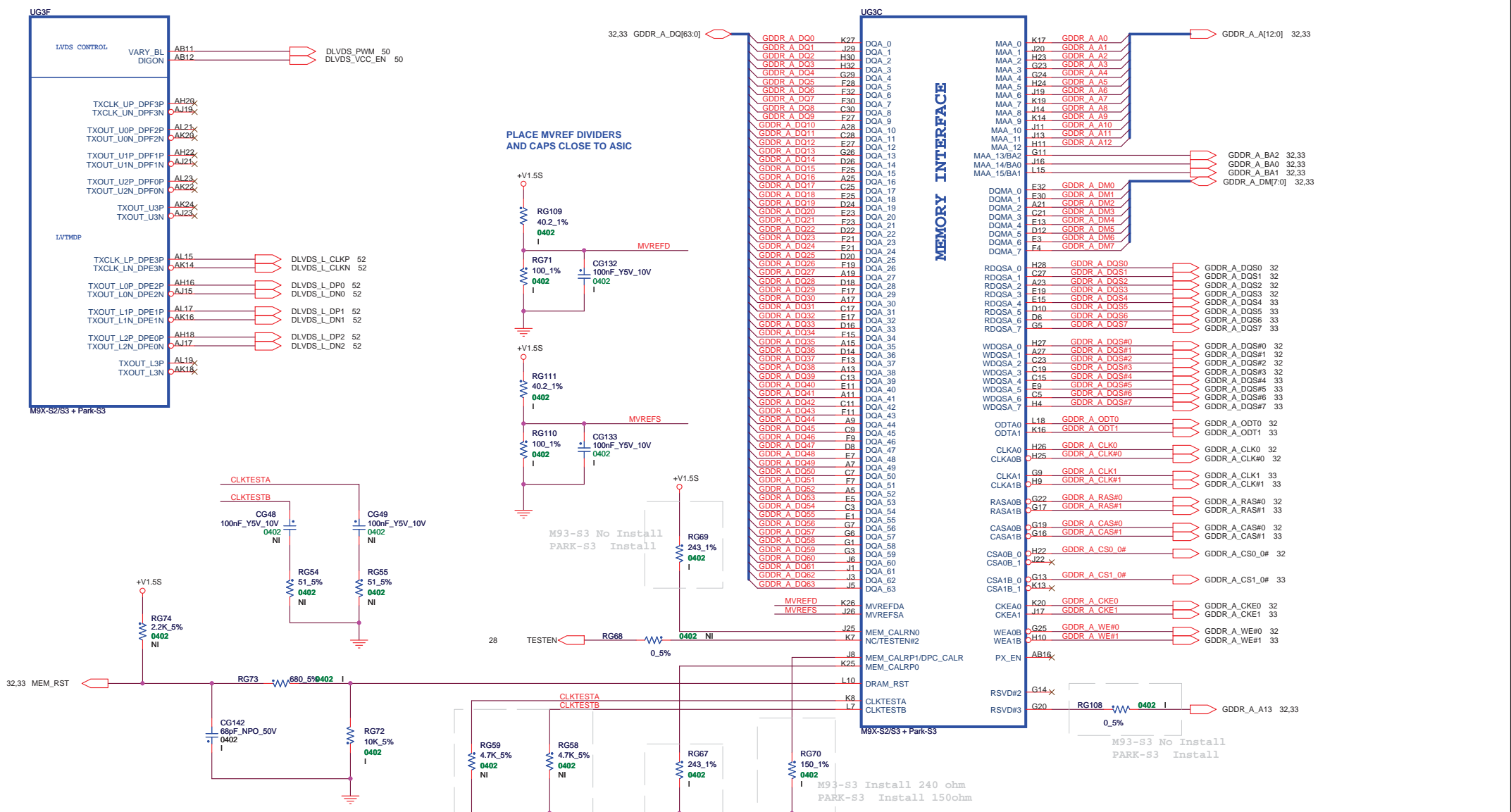


GPIO 0 : PCIE FULL TX OUTPUT SWING  
 GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED  
 GPIO 2 : PCIE GEN2 ENABLED



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Title <b>VGA (STRAP) 2/6</b>			
Size	Document Number	Rev	
Custom	PM	0.1	
Page Modified: Wednesday, August 26, 2009 18:38:11 (UTC/GMT)		Sheet 27 of 68	





	M93-S3	PARK-S3
RG141	DNI	10K
RG142	0R	680R
RG145	2.2K	DNI
CG781	2.2nF	68pF

M93-S3 Install  
PARK-S3 Not Install

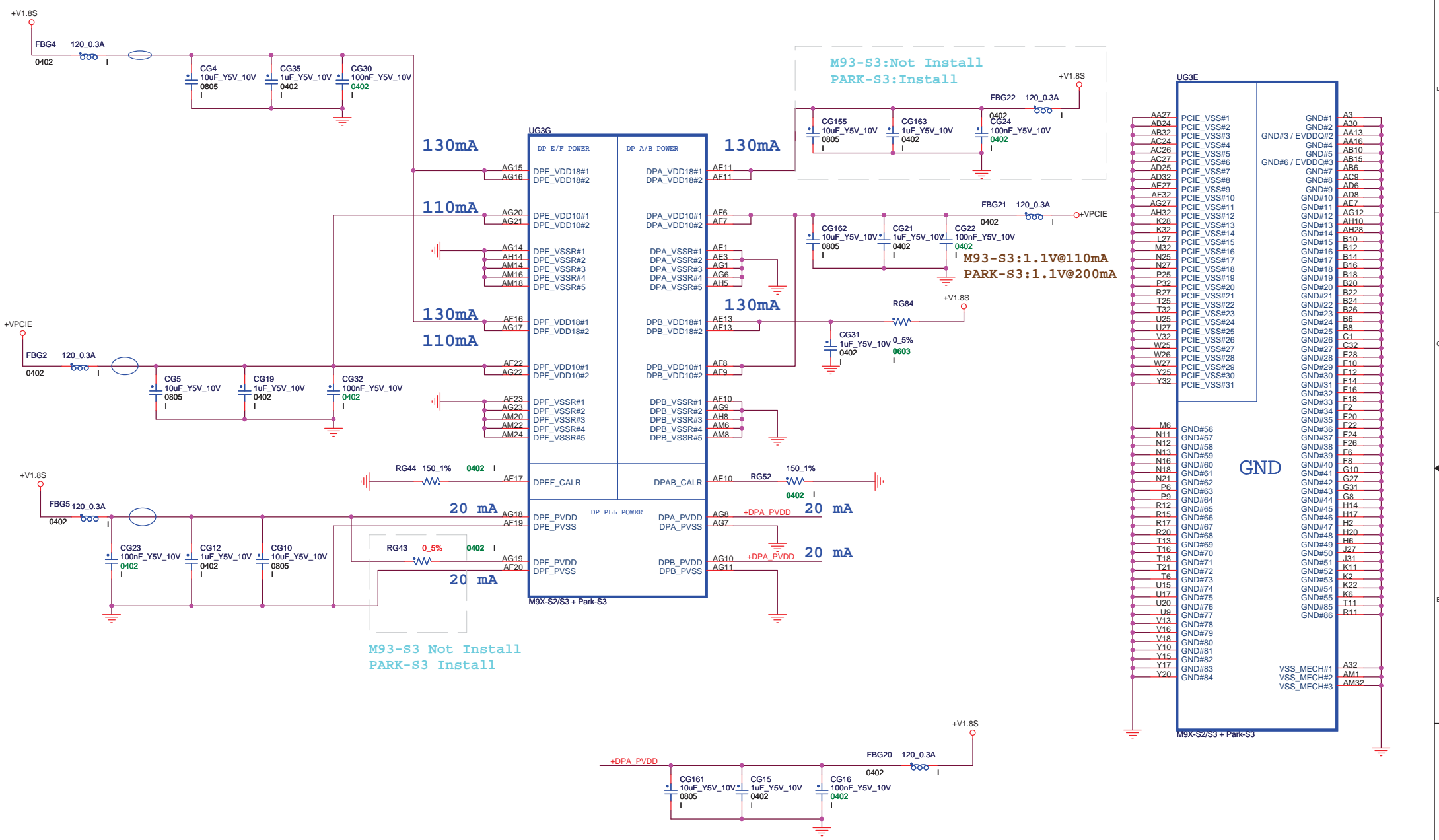
M93-S3 Not Install  
PARK-S3 Install

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Title: **VGA (DDR3) 4/6**

Size: Document Number  
Custom **PM** Rev: **0.1**

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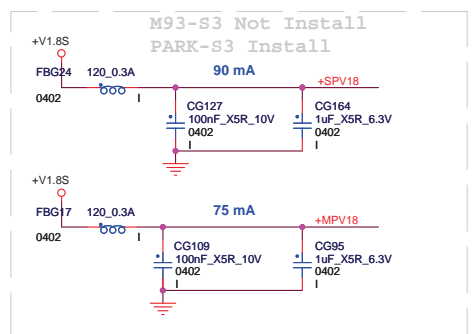
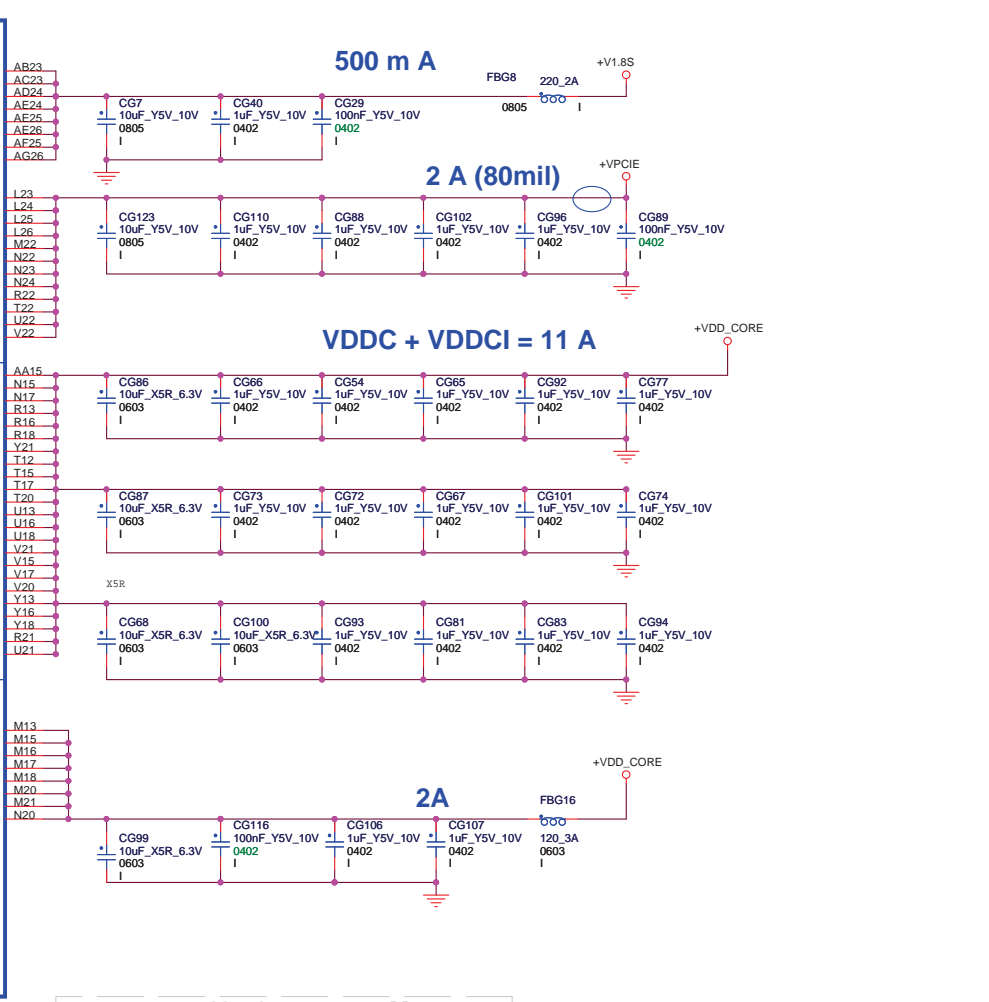
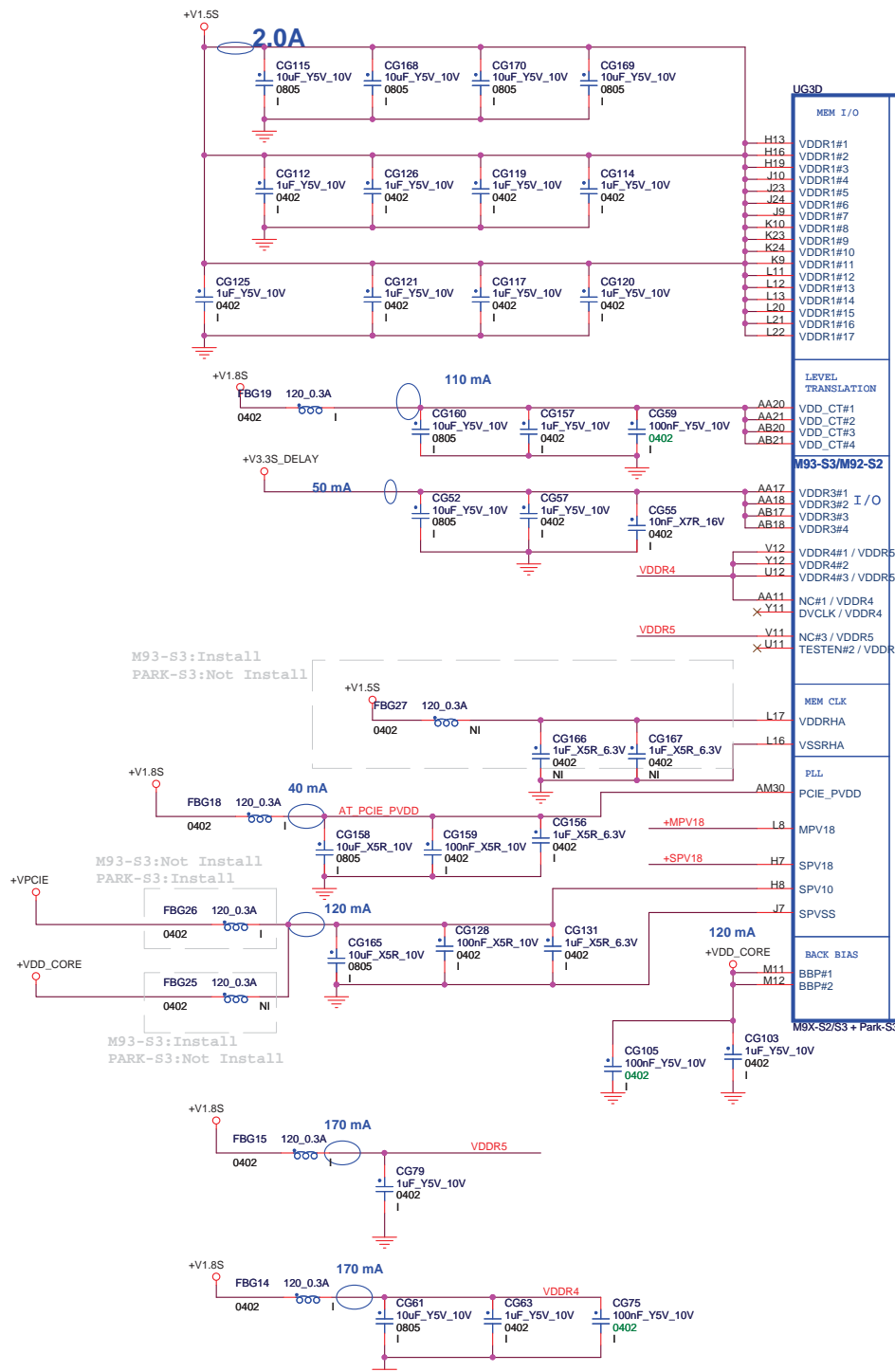
AA27	PCIE_VSS#1	GND#1	A3
AB24	PCIE_VSS#2	GND#2	A30
AB32	PCIE_VSS#3	GND#3 / EVDDQ#2	AA13
AC24	PCIE_VSS#4	GND#4	AA16
AC26	PCIE_VSS#5	GND#5	AB10
AC27	PCIE_VSS#6	GND#6 / EVDDQ#3	AB9
AD25	PCIE_VSS#7	GND#7	AC9
AD32	PCIE_VSS#8	GND#8	AD6
AE27	PCIE_VSS#9	GND#9	AD8
AF32	PCIE_VSS#10	GND#10	AE7
AG27	PCIE_VSS#11	GND#11	AG12
AH32	PCIE_VSS#12	GND#12	AH10
K28	PCIE_VSS#13	GND#13	AH28
K32	PCIE_VSS#14	GND#14	B10
L27	PCIE_VSS#15	GND#15	B12
M32	PCIE_VSS#16	GND#16	B14
N25	PCIE_VSS#17	GND#17	B16
N27	PCIE_VSS#18	GND#18	B18
P25	PCIE_VSS#19	GND#19	B20
P32	PCIE_VSS#20	GND#20	B22
R27	PCIE_VSS#21	GND#21	B24
T25	PCIE_VSS#22	GND#22	B26
T32	PCIE_VSS#23	GND#23	B6
U25	PCIE_VSS#24	GND#24	B8
U27	PCIE_VSS#25	GND#25	C1
V32	PCIE_VSS#26	GND#26	C32
W25	PCIE_VSS#27	GND#27	E28
W26	PCIE_VSS#28	GND#28	F10
W27	PCIE_VSS#29	GND#29	F12
Y25	PCIE_VSS#30	GND#30	F14
Y32	PCIE_VSS#31	GND#31	F16
		GND#32	F18
		GND#33	F2
		GND#34	F20
		GND#35	F22
		GND#36	F24
		GND#37	F26
		GND#38	F6
		GND#39	F8
		GND#40	G10
		GND#41	G27
		GND#42	G31
		GND#43	G8
		GND#44	H14
		GND#45	H17
		GND#46	H2
		GND#47	H20
		GND#48	H6
		GND#49	J27
		GND#50	J31
		GND#51	K11
		GND#52	K2
		GND#53	K22
		GND#54	K6
		GND#55	T11
		GND#56	R11
		GND#57	
		GND#58	
		GND#59	
		GND#60	
		GND#61	
		GND#62	
		GND#63	
		GND#64	
		GND#65	
		GND#66	
		GND#67	
		GND#68	
		GND#69	
		GND#70	
		GND#71	
		GND#72	
		GND#73	
		GND#74	
		GND#75	
		GND#76	
		GND#77	
		GND#78	
		GND#79	
		GND#80	
		GND#81	
		GND#82	
		GND#83	
		GND#84	
		VSS_MECH#1	A32
		VSS_MECH#2	AM1
		VSS_MECH#3	AM32

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Title: **VGA (POWER) 5/6**

Size	Document Number	Rev
Custom	PM	0.1

Page Modified: Wednesday, August 26, 2009 18:38:11 (UTC/GMT) Sheet 30 of 68

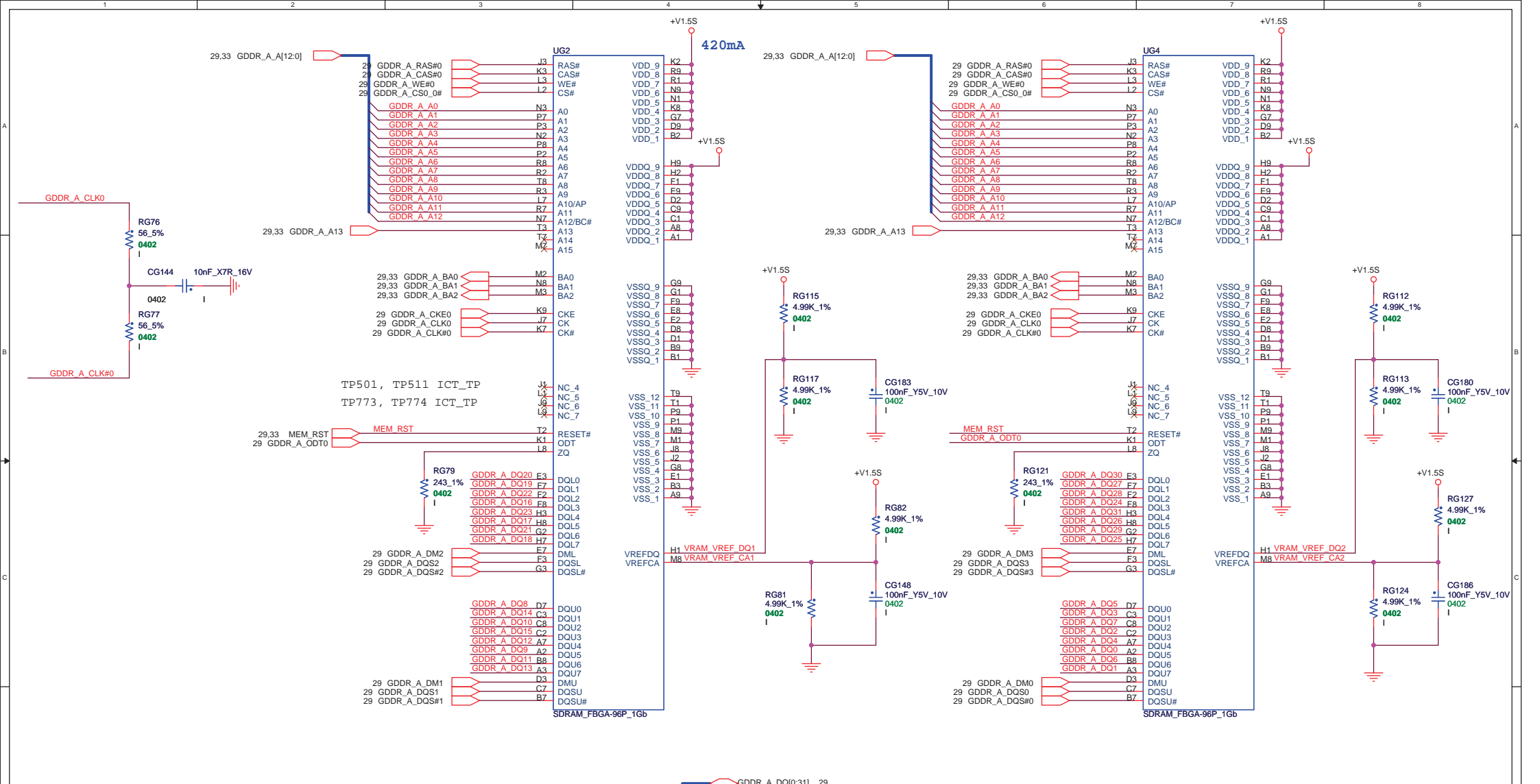


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Title: **VGA (POWER) 6/6**

Size	Document Number	Rev
Custom	PM	0.1

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GDDR\_A\_DQ[0:31] 29

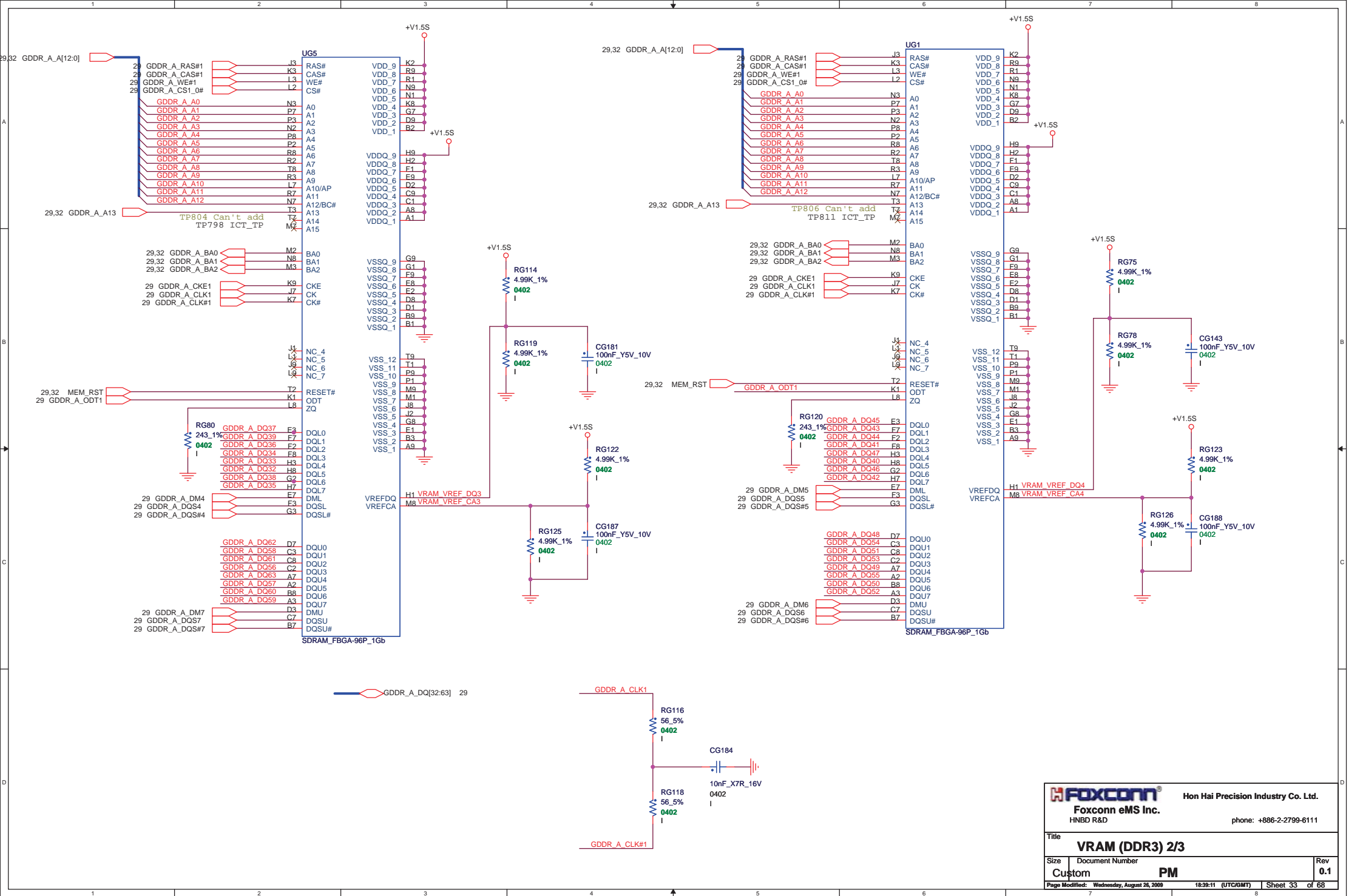
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
**Foxconn eMS Inc.**  
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Title: **VRAM (DDR3) 1/3**

Size	Document Number	Rev
Custom	<b>PM</b>	0.1

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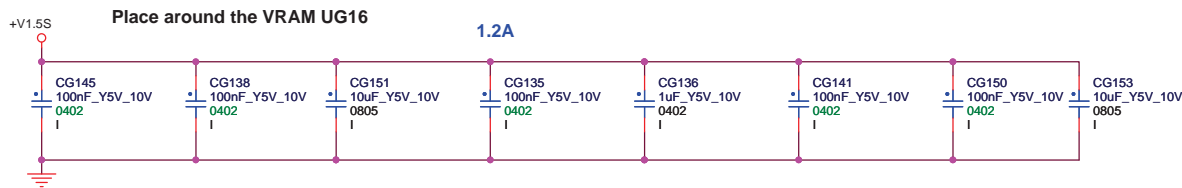
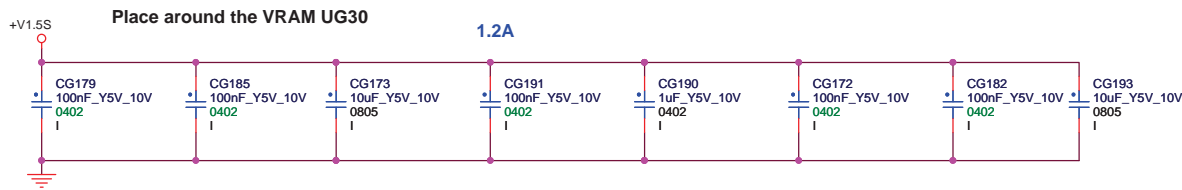
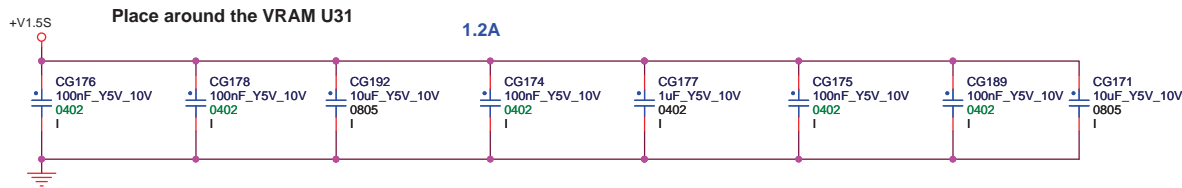
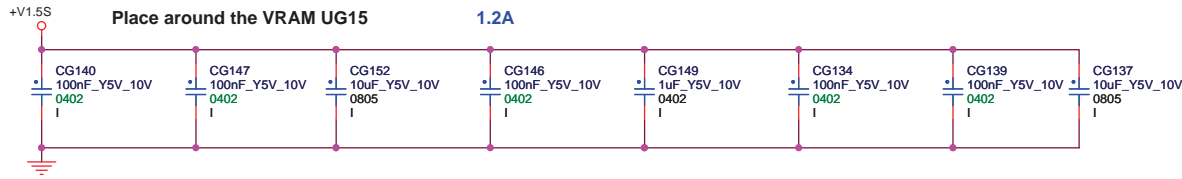



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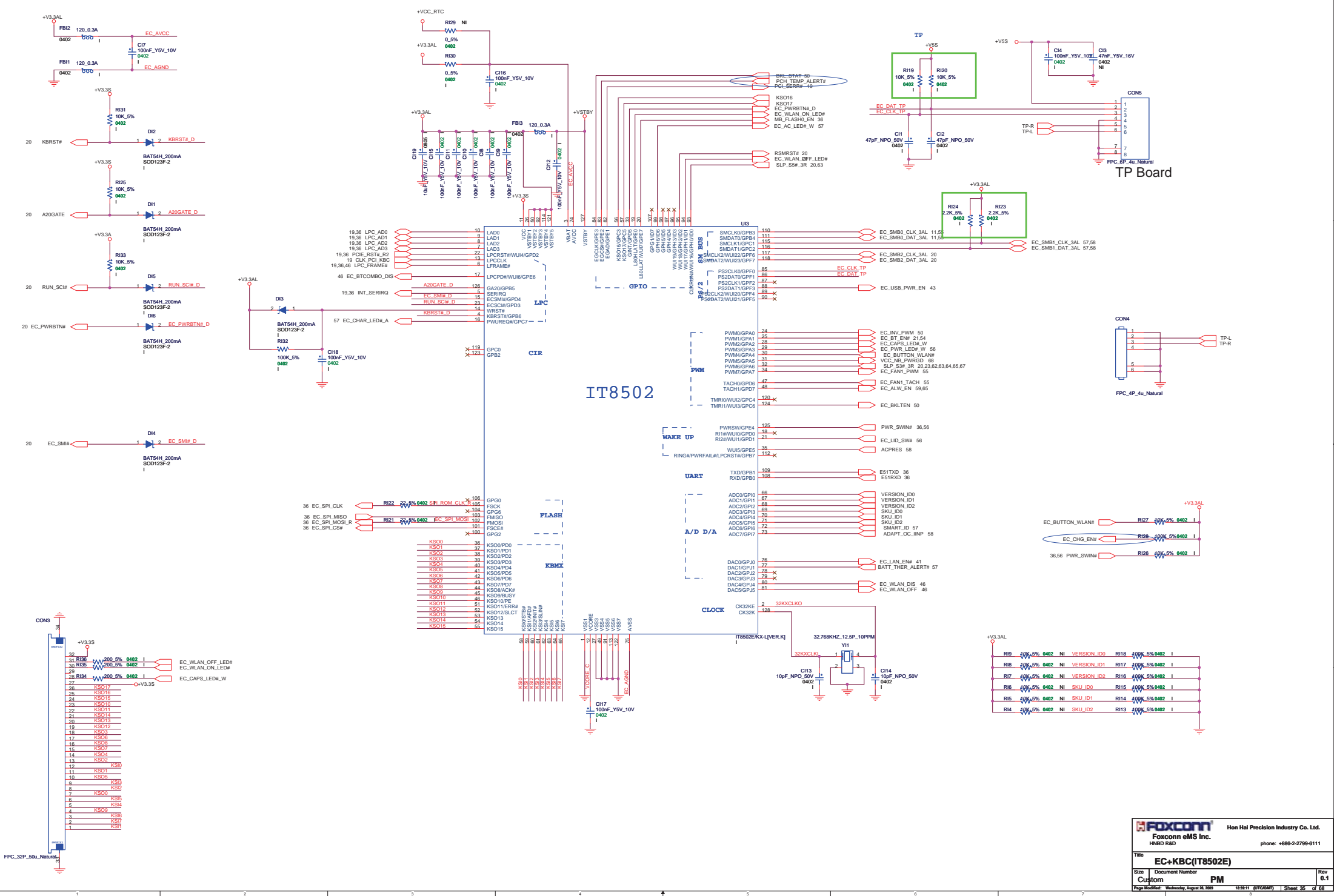
Title: **VRAM (DDR3) 2/3**

Size	Document Number	Rev
Custom	PM	0.1

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		Hon Hai Precision Industry Co. Ltd.	
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Title			
<b>VRAM (BYPASS) 3/3</b>			
Size	Document Number		Rev
Custom	PM		0.1
Page Modified: Wednesday, August 26, 2009		18:38:11 (UTC/GMT)	Sheet 34 of 68



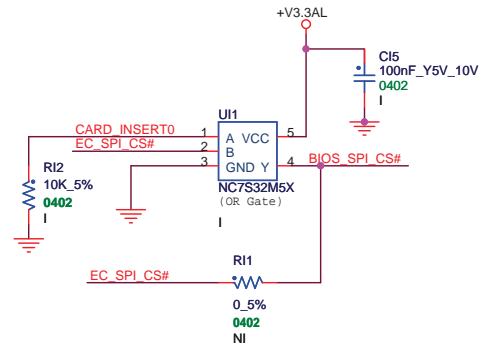
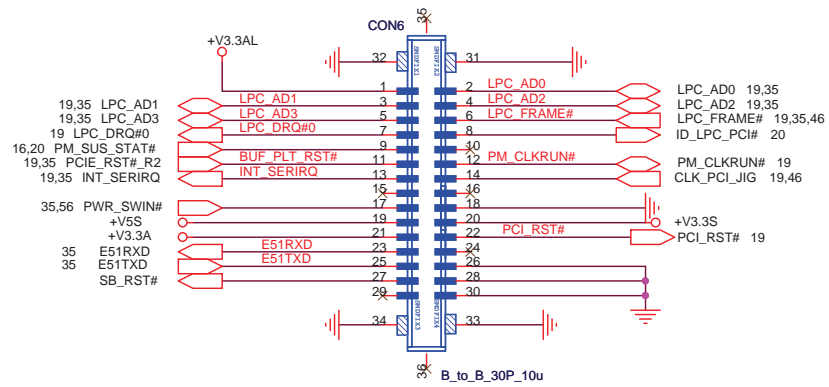
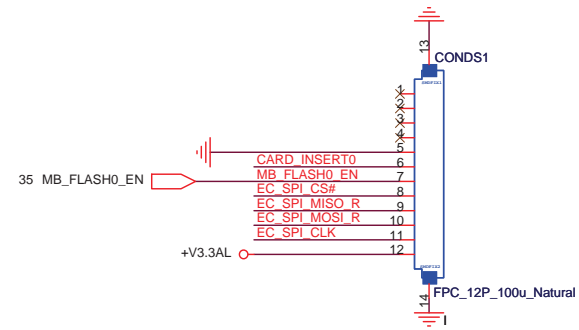
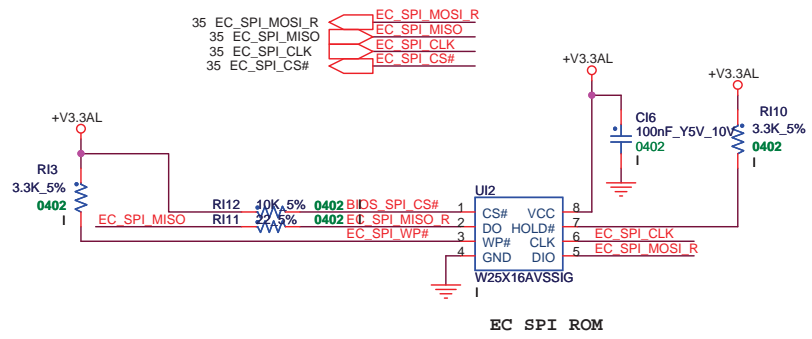
IT8502

**Foxconn** Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc.  
 HNBD R&D phone: +886-2-2799-6111

Title: **EC+KBC(IT8502E)**

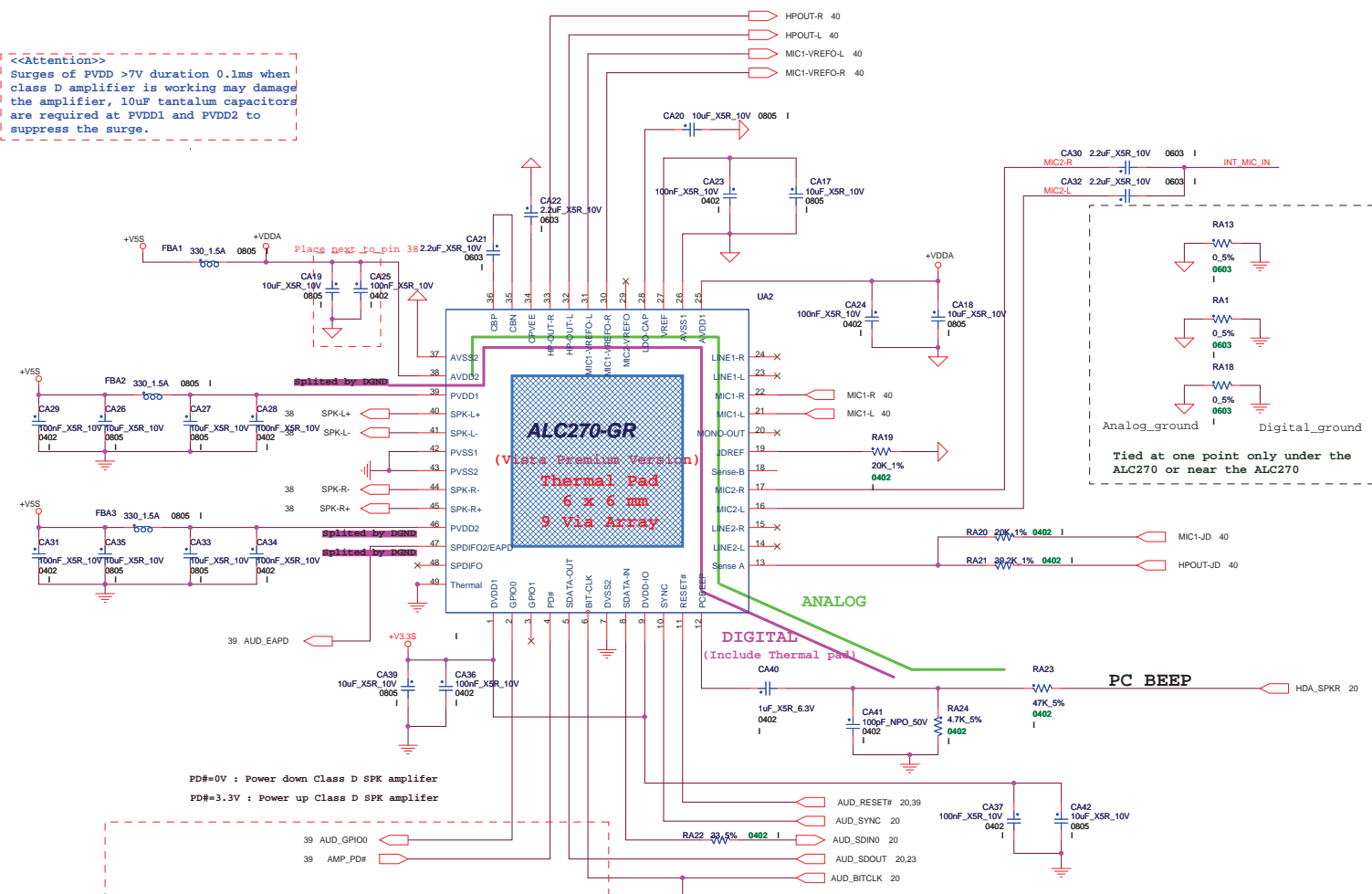
Size: Custom Document Number: PM Rev: 0.1

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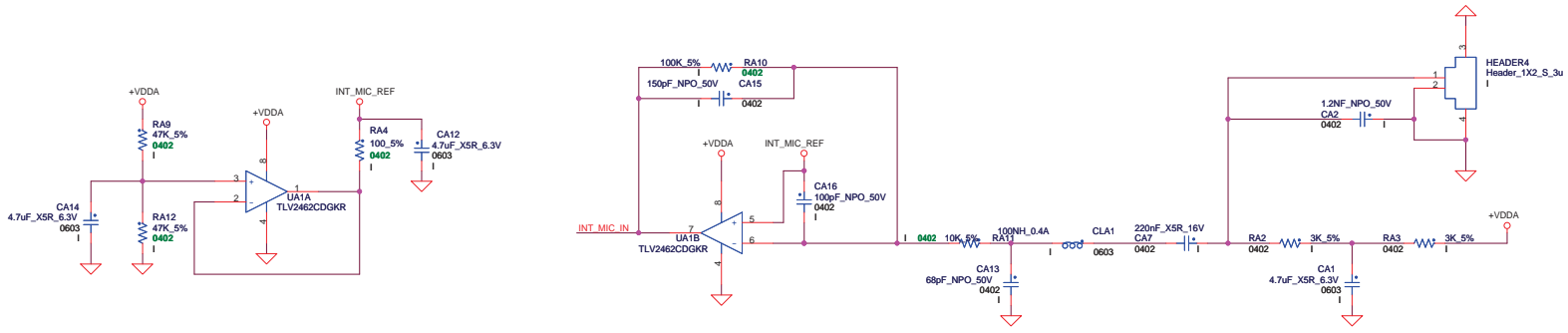
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNB D R&D	
		phone: +886-2-2799-6111	
Title <b>Flash ROM/SPI</b>			
Size	Document Number		Rev
B	<b>PM</b>		<b>0.1</b>
Page Modified: Wednesday, August 26, 2009		18:39:11 (UTC/GMT)	Sheet 36 of 68

<<Attention>>  
 Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

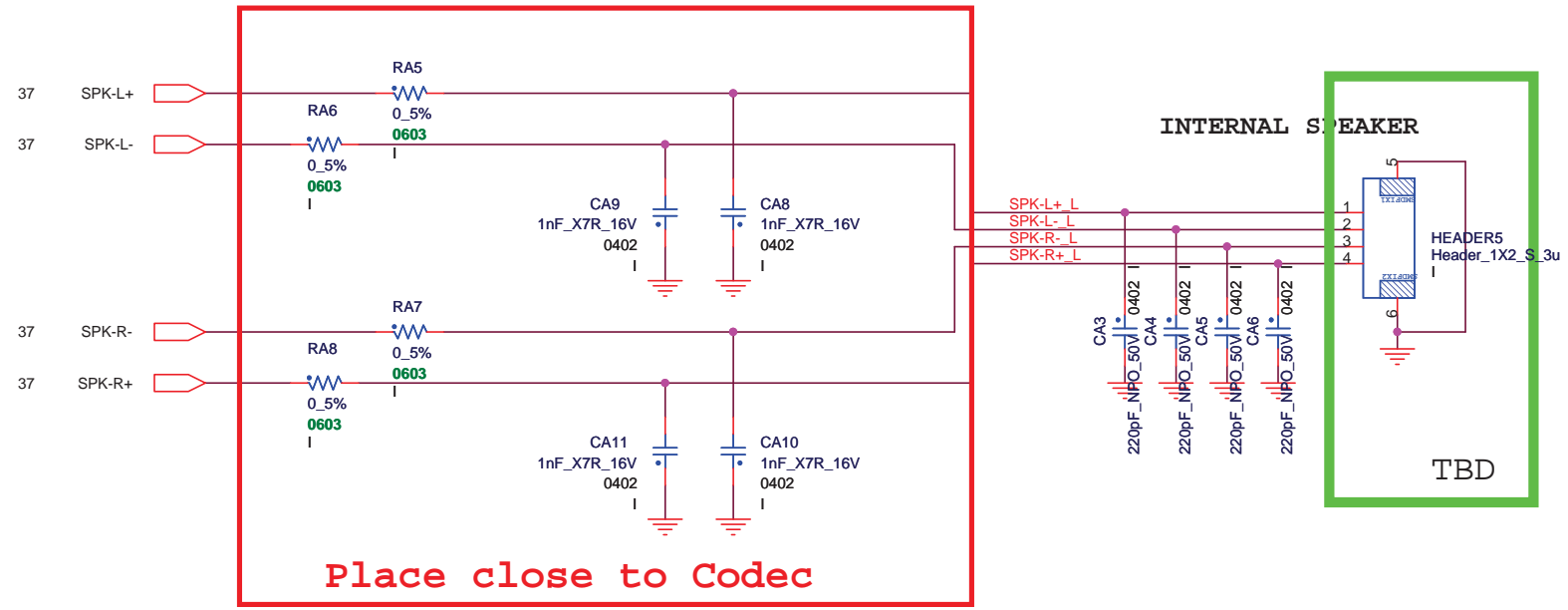


PD# = 0V : Power down Class D SPK amplifier  
 PD# = 3.3V : Power up Class D SPK amplifier

<<Attention>>  
 For power\_on/off de-pop circuit and system booting warning signal: Please system BIOS Engineer Note :  
 1. If you want the system make warning signal after power on, please let EC\_MUTE# High first.  
 2. When you want to exit your Bios Programming Code, please let the EC\_MUTE# Low. (The programming is different from before .)



<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
Title		ALC270 Audio CODEC	
Size	Document Number	Rev	0.1
C	PM		
Page Modified: Wednesday, August 28, 2009		18:38:11 (UTC+0800) Sheet 37 of 68	

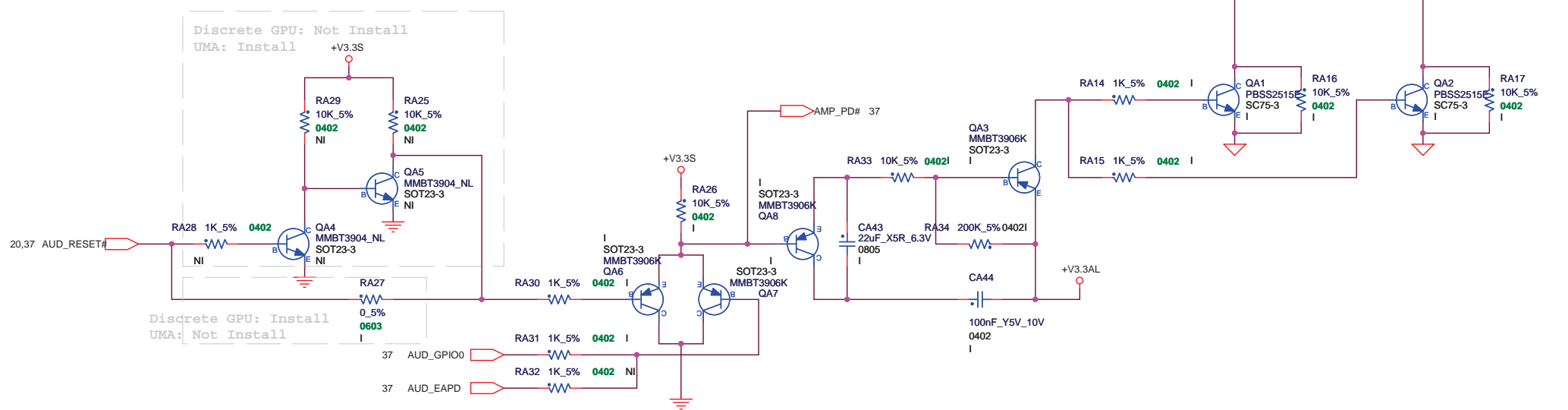


Place close to Codec

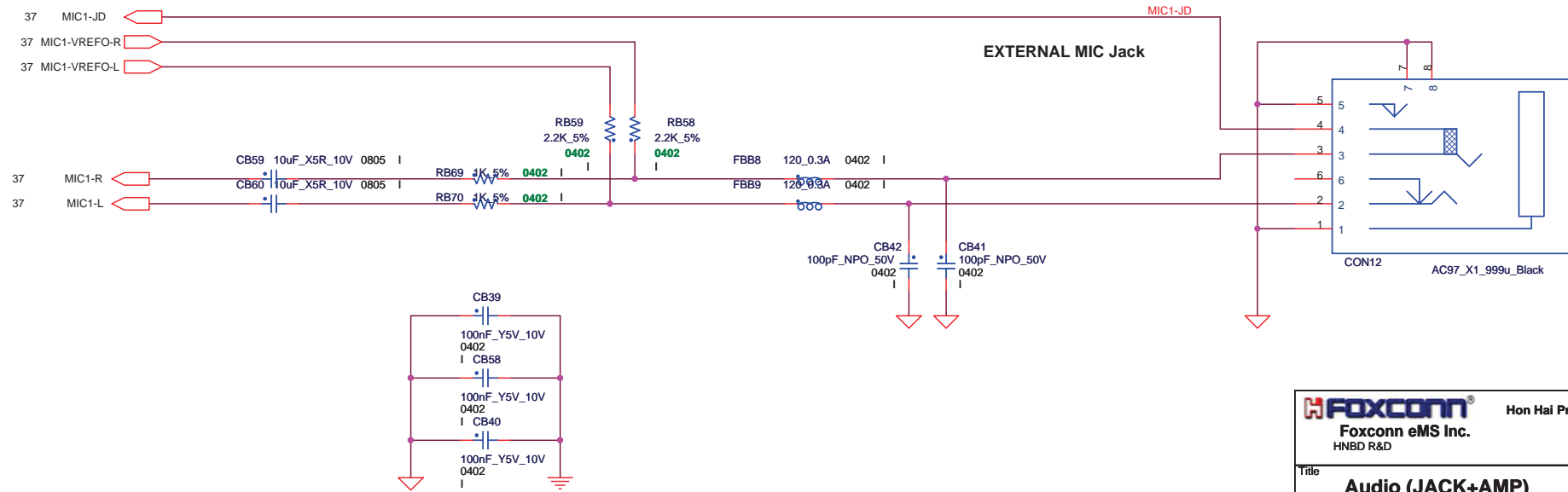
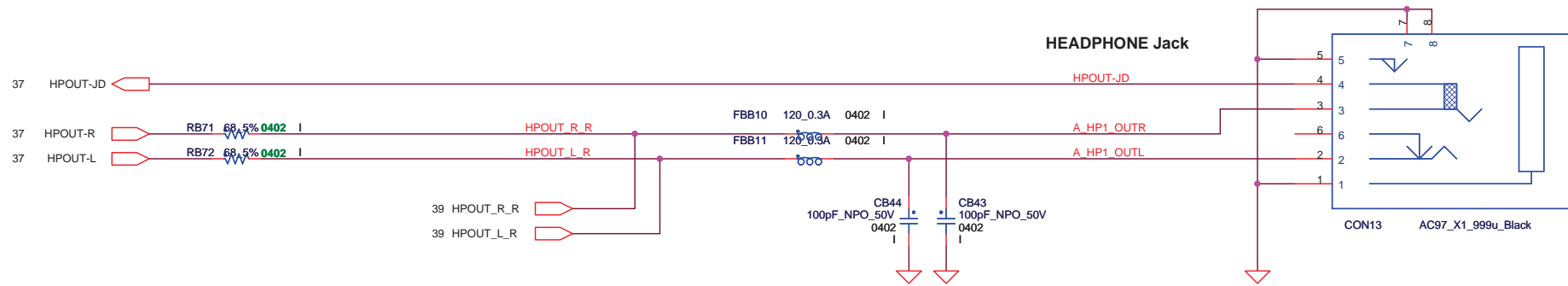
INTERNAL SPEAKER

TBD

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Title <b>Audio (SPKR+AMP)</b>				
Size	Document Number			Rev
Custom	PM			0.1
Page Modified: Wednesday, August 26, 2009		18:39:11 (UTC/GMT)		Sheet 38 of 68

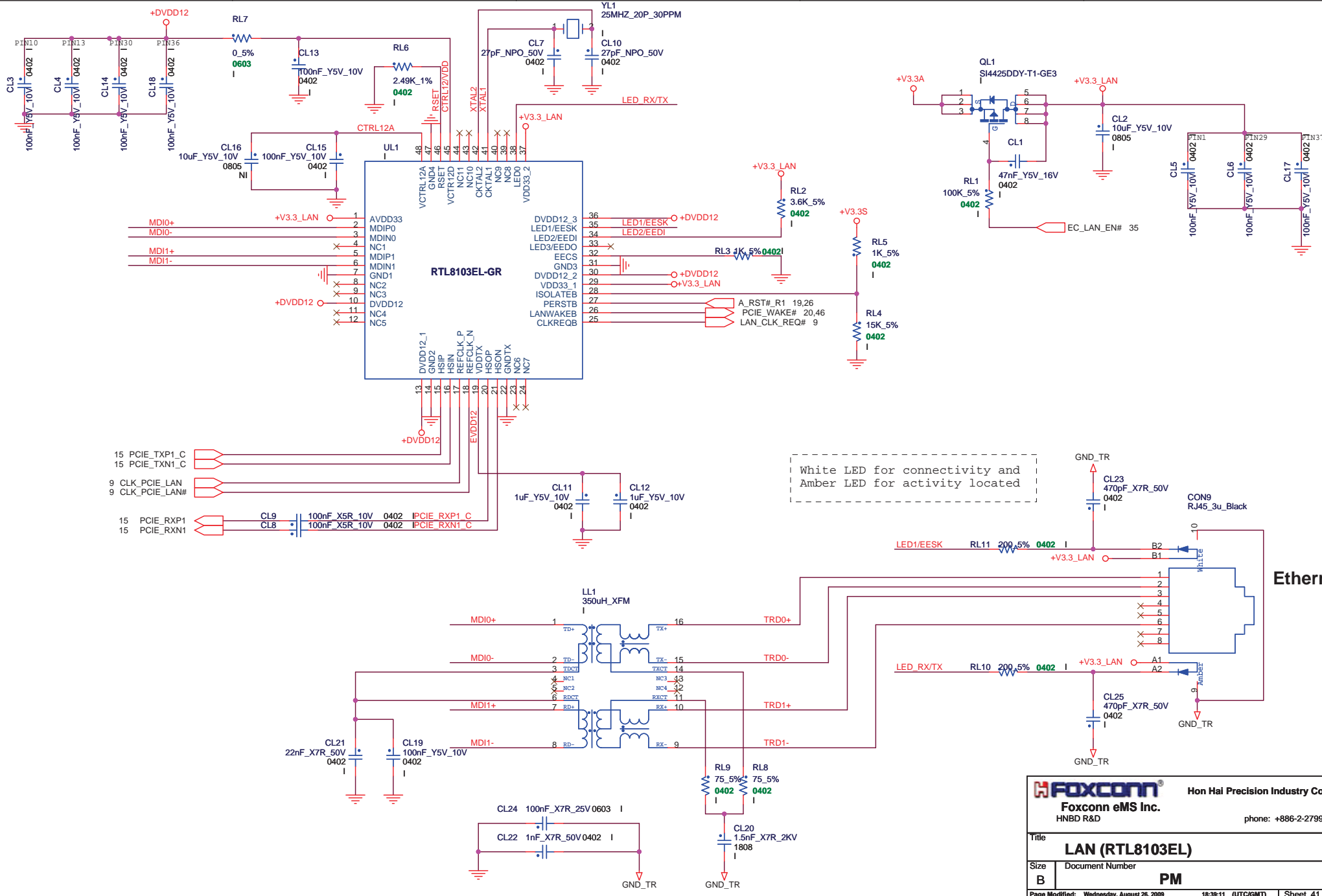


		Hon Hai Precision Industry Co. Ltd. <b>Foxconn eMS Inc.</b> HNBD R&D	
		phone: +886-2-2799-6111	
<b>Title</b> Audio (MUTE)			
<b>Size</b> B	<b>Document Number</b> PM		<b>Rev</b> 0.1
Page Modified: Wednesday, August 26, 2009		18:39:11 (UTC/GMT)	Sheet 39 of 68



		<b>Hon Hai Precision Industry Co. Ltd.</b>	
<b>Foxconn EMS Inc.</b>		HNB D R&D	
		phone: +886-2-2799-6111	
<b>Title</b> <b>Audio (JACK+AMP)</b>			
<b>Size</b> <b>B</b>	<b>Document Number</b> <b>PM</b>		<b>Rev</b> <b>0.1</b>
Page Modified: Wednesday, August 26, 2009 18:39:11 (UTC/GMT) Sheet 40 of 68			

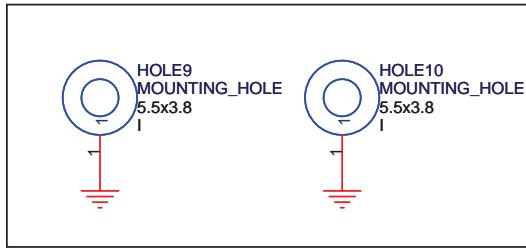




White LED for connectivity and Amber LED for activity located

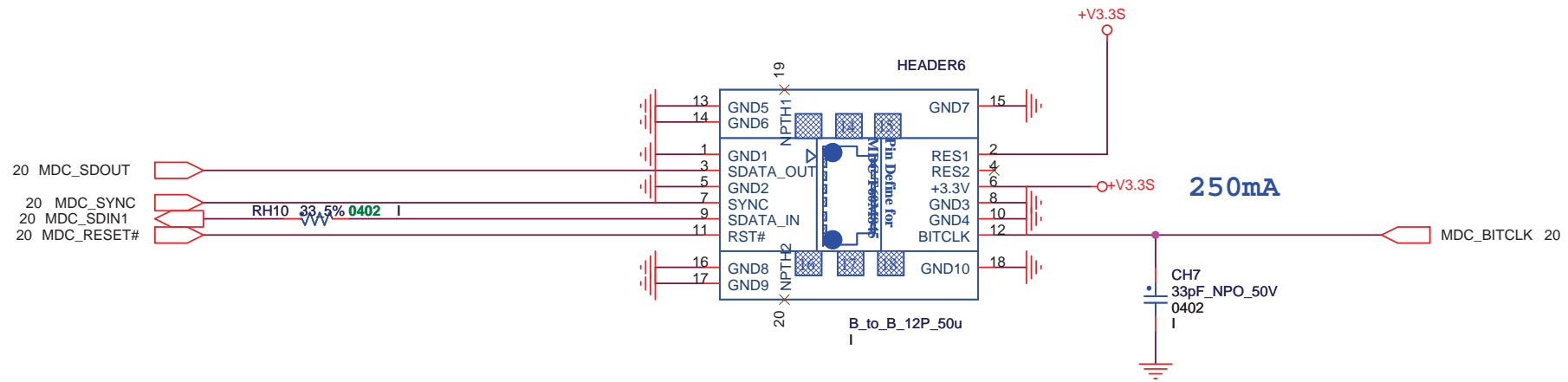
Ethernet

		<b>Hon Hai Precision Industry Co. Ltd.</b>	
<b>Foxconn eMS Inc.</b>		HNB D R&D	
		phone: +886-2-2799-6111	
<b>Title</b> <b>LAN (RTL8103EL)</b>			
<b>Size</b> <b>B</b>	<b>Document Number</b> <b>PM</b>	<b>Rev</b> <b>0.1</b>	
Page Modified: Wednesday, August 26, 2009 18:39:11 (UTC/GMT) Sheet 41 of 68			

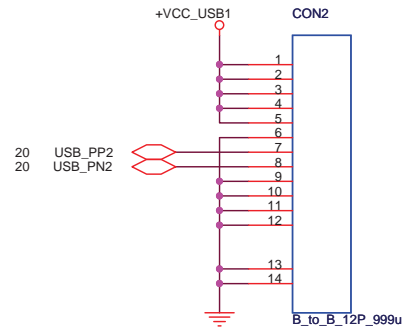
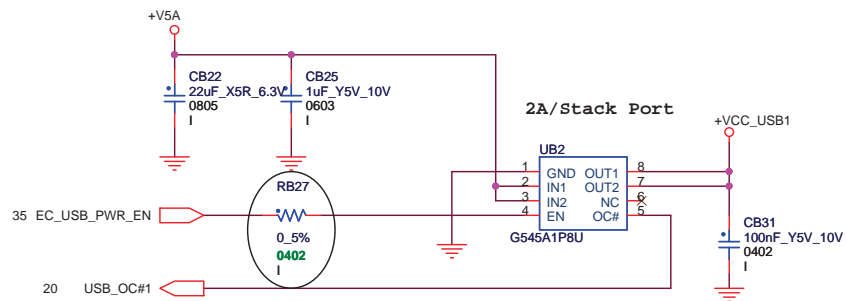
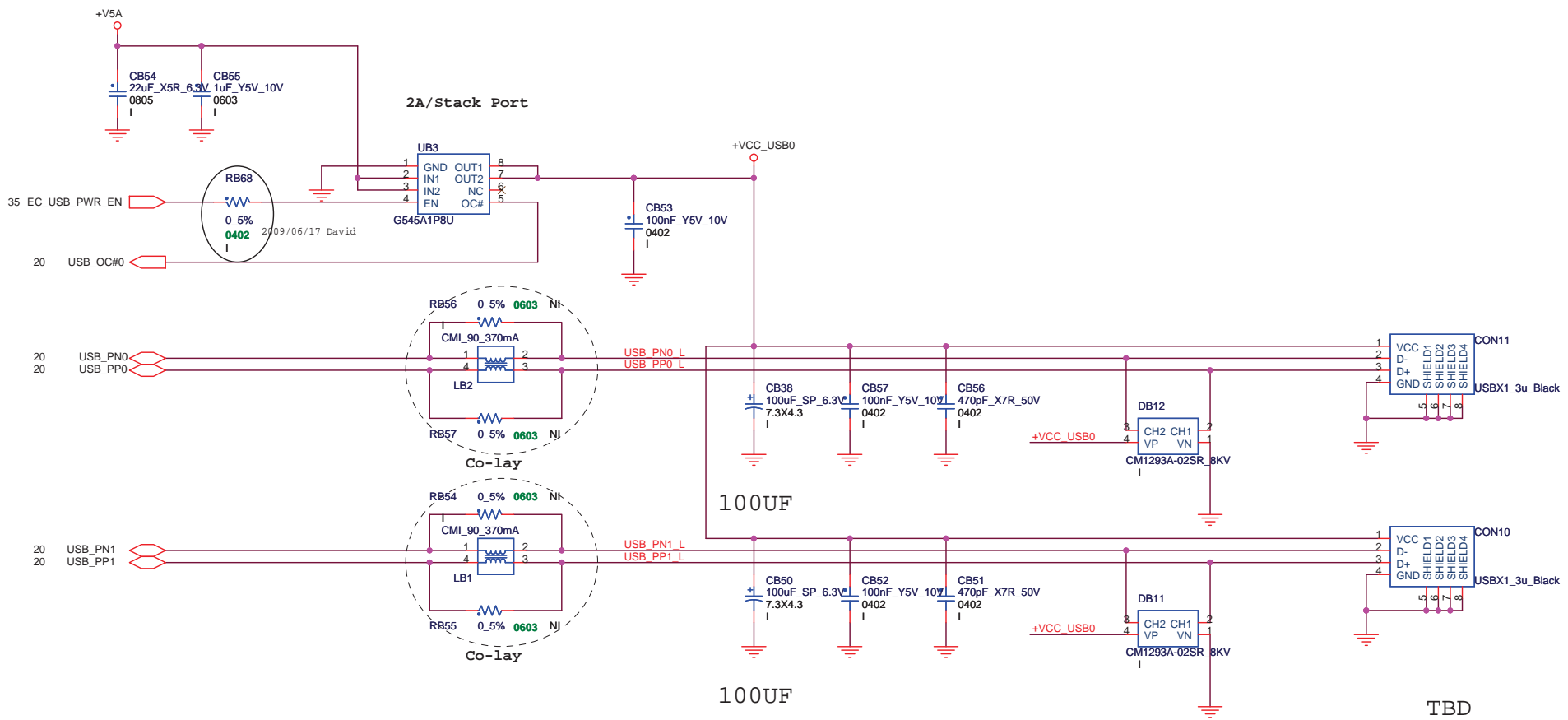


MDC CONN.

Option



		<b>Hon Hai Precision Industry Co. Ltd.</b>	
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		phone: +886-2-2799-6111	
Title <b>RJ11</b>			
Size	Document Number		Rev
Custom	PM		0.1
Page Modified: Wednesday, August 26, 2009		18:39:11 (UTC/GMT)	Sheet 42 of 68



Need to change footprint

		Hon Hai Precision Industry Co. Ltd.	
Foxconn EMS Inc.		HNB D R&D	
		phone: +886-2-2799-6111	
Title <b>USB2 &amp; USB DB</b>			
Size <b>B</b>	Document Number <b>PM</b>	Rev <b>0.1</b>	
Page Modified: Wednesday, August 26, 2009 18:39:11 (UTC/GMT) Sheet 43 of 68			

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A

 <b>Hon Hai Precision Industry Co. Ltd.</b>			
<b>Foxconn eMS Inc.</b>			
HNBD R&D	phone: +886-2-2799-6111		
Title			
<b>USBx2</b>			
Size	Document Number	Rev	
<b>B</b>	<b>PM</b>	<b>0.1</b>	
Page Modified: Wednesday, August 26, 2009		18:39:11 (UTC/GMT)	Sheet 44 of 68

5

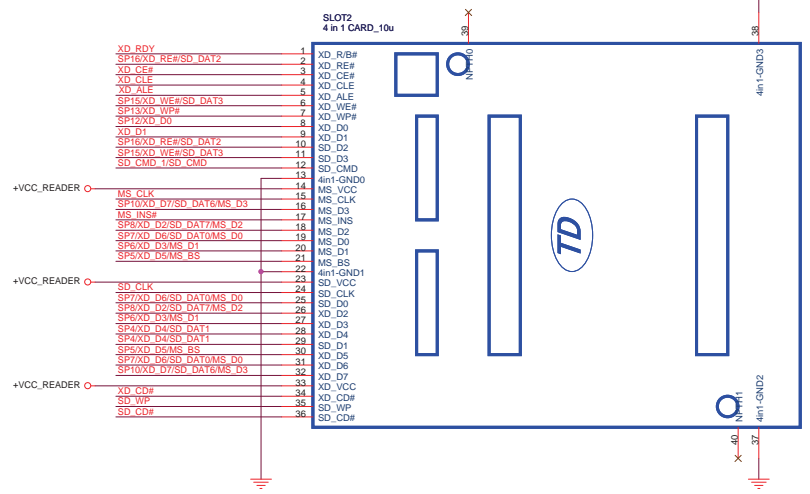
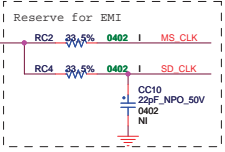
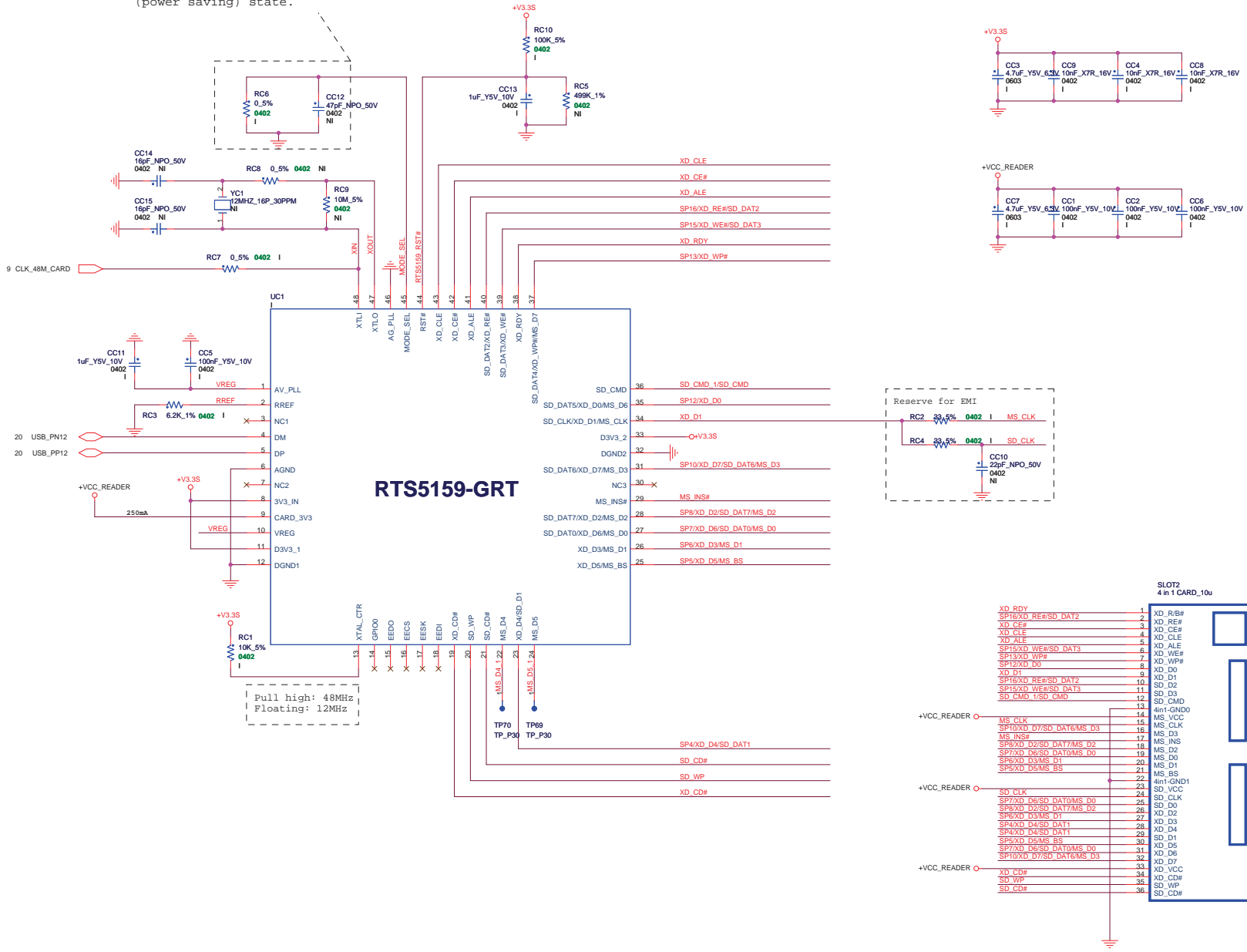
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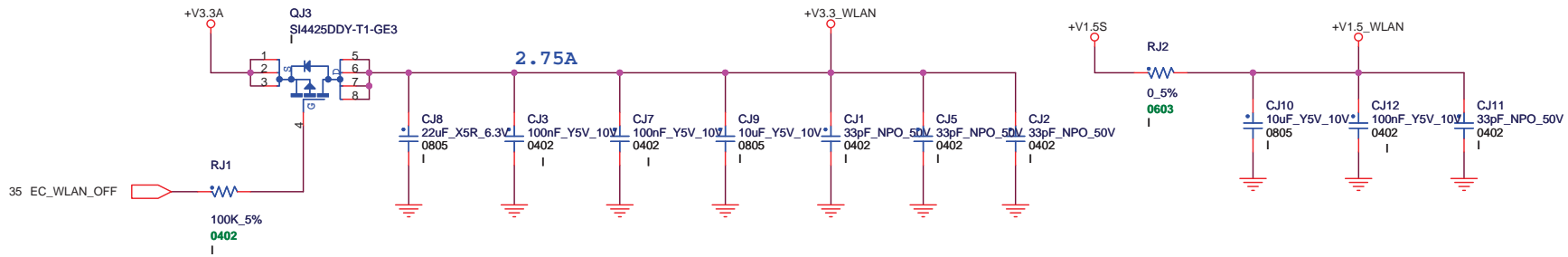
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2

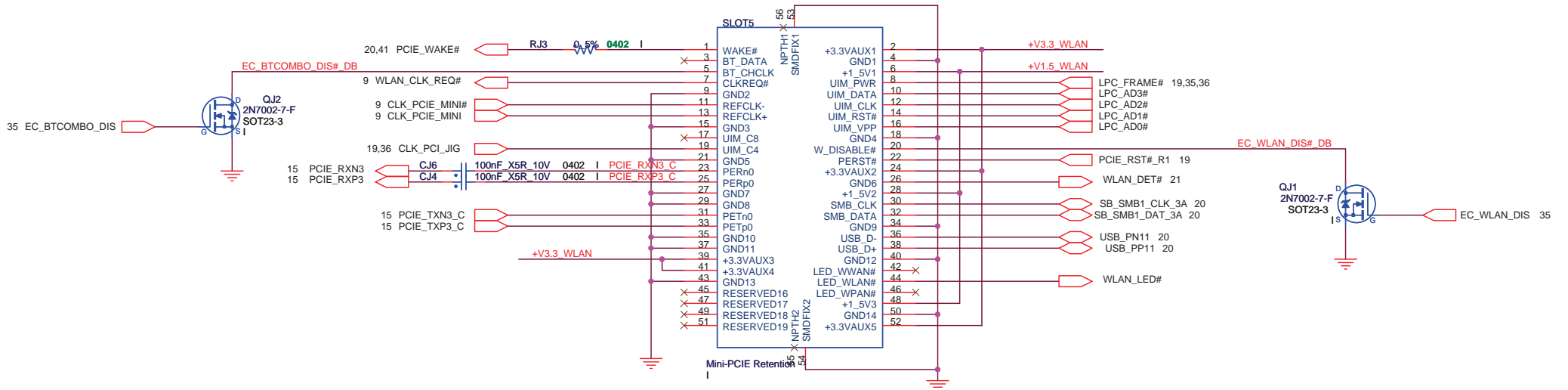
1

D3 mode: (R:0 ohm ; C:NC)  
 If user remove memory card from socket, RTS5159 will terminate USB bus connection and enter D3 (power saving) state.

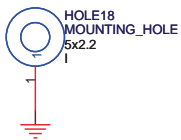




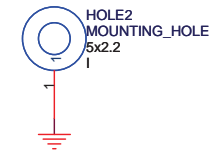
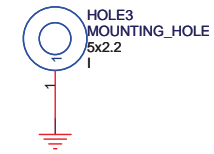
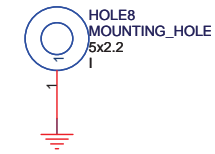
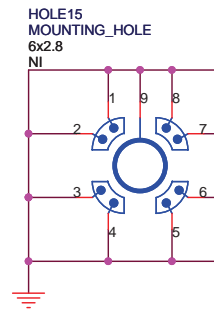
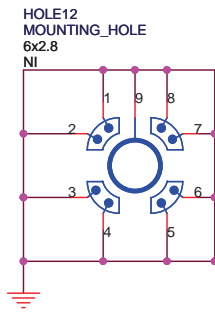
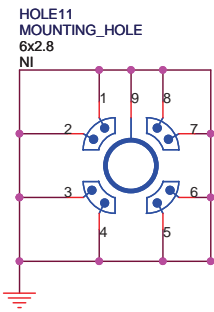
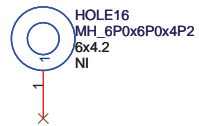
+1\_5V=>0.5A Peak/0.375A Normal  
 +3\_3VAux=>2.75A Peak/1.1A Normal



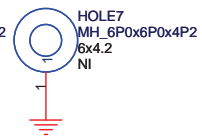
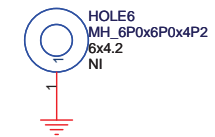
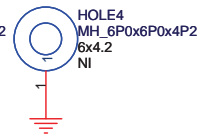
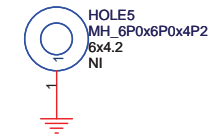
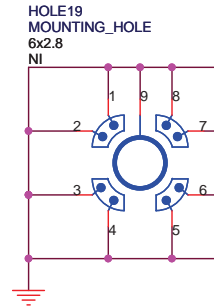
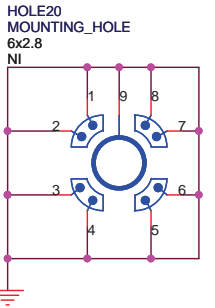
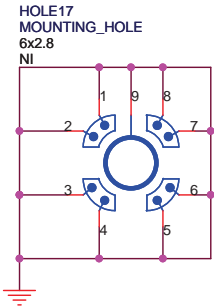
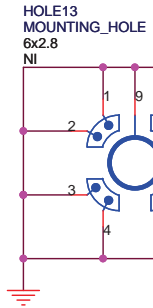
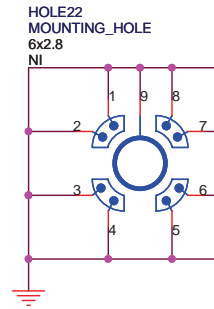
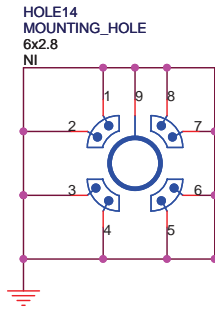
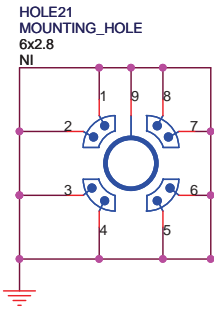
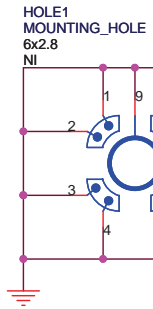
Half Mini Card for WLAN



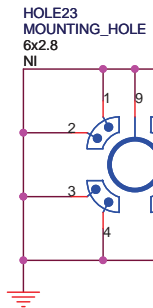
		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D	
		phone: +886-2-2799-6111	
Title <b>WLAN Mini-PCIE Card</b>			
Size <b>B</b>	Document Number <b>PM</b>	Rev <b>0.1</b>	
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For GPU use

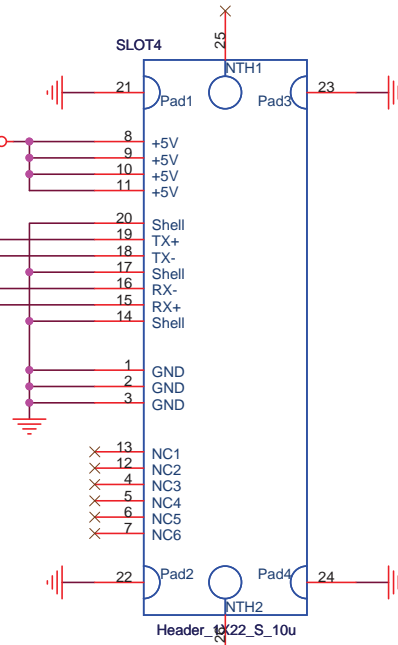
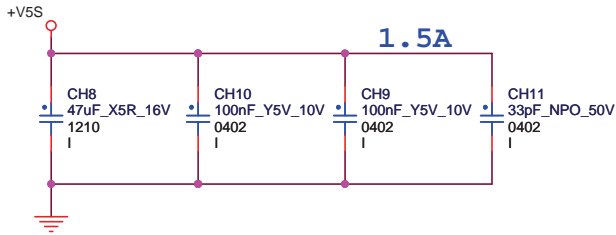
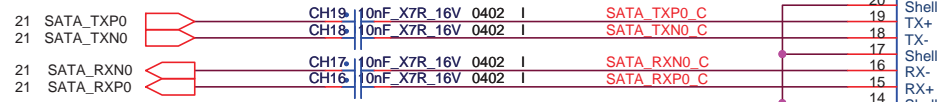


For CPU use

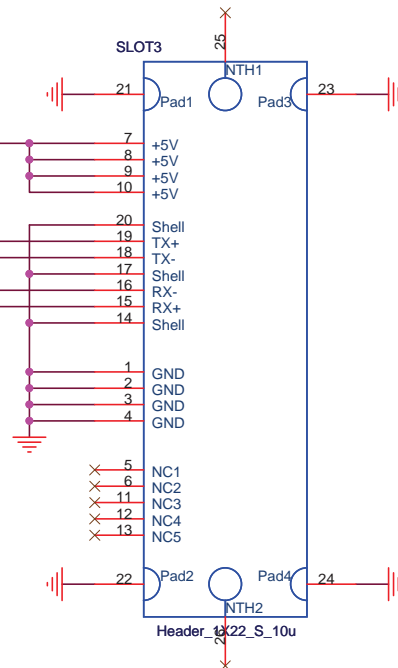
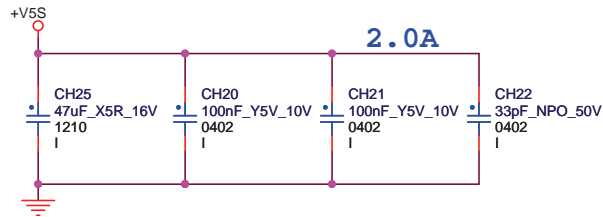
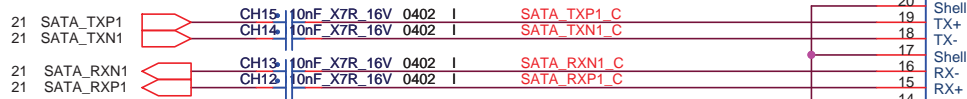


		Hon Hai Precision Industry Co. Ltd.	
Foxconn EMS Inc.		HNBD R&D	
		phone: +886-2-2799-6111	
Title			
<b>MOUNTING HOLE</b>			
Size	Document Number	Rev	
Custom	PM	0.1	
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# SATA HDD CONN



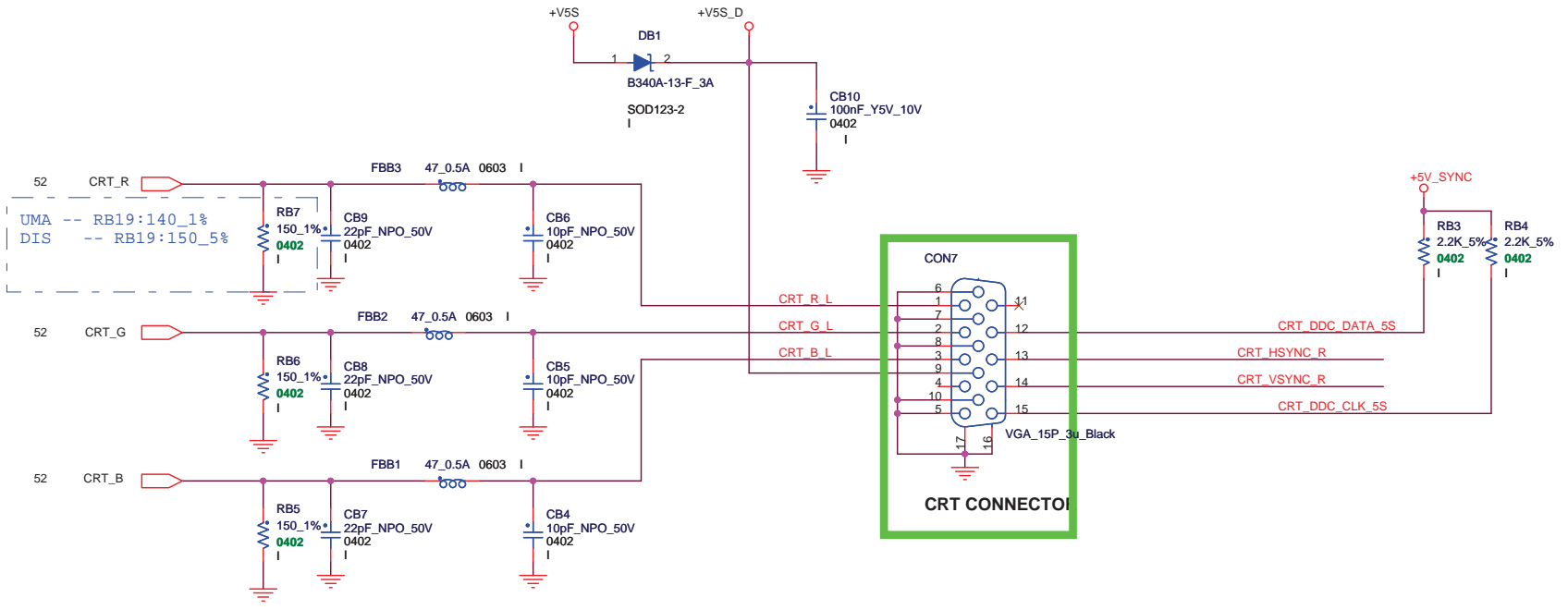
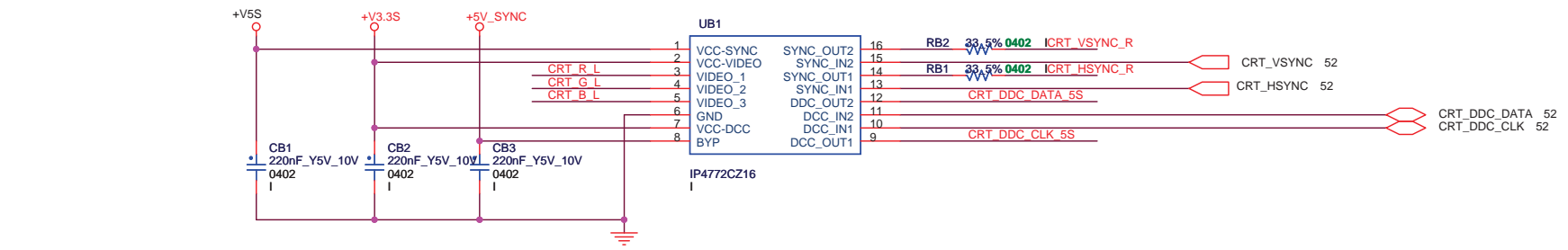
# SATA ODD CONN



Power pin current  
max. 1300 mA (less 2ms)

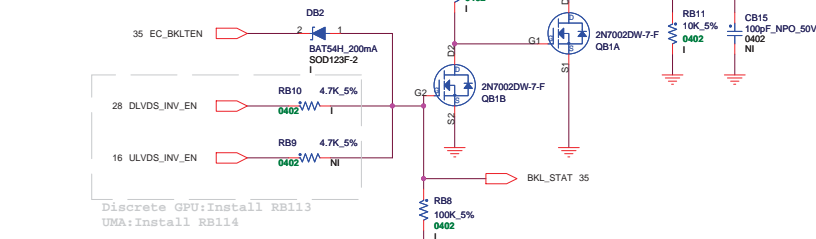
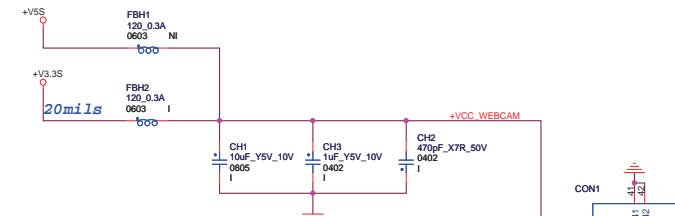
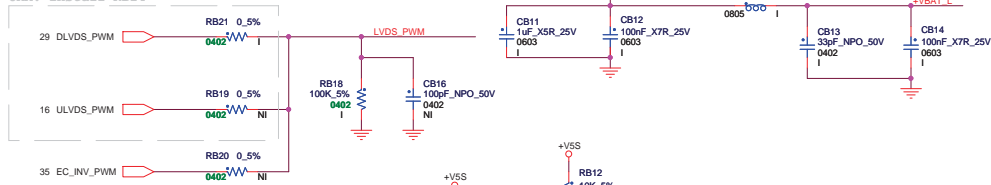
		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D	
		phone: +886-2-2799-6111	
Title <b>SATA HDD/ODD</b>			
Size	Document Number		Rev
Custom	PM		0.1
Page Modified: Wednesday, August 26, 2009		18:39:11 (UTC/GMT)	Sheet 48 of 68



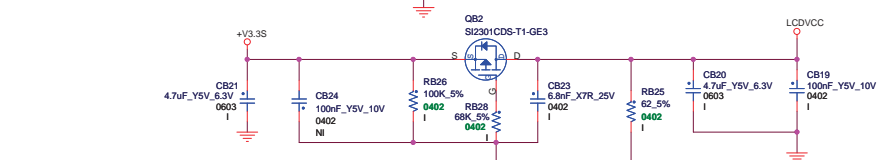


		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +886-2-2799-6111	
Title <b>CRT</b>			
Size <b>B</b>	Document Number <b>PM</b>		Rev <b>0.1</b>
Page Modified: Wednesday, August 26, 2009 18:39:11 (UTC/GMT) Sheet 49 of 68			

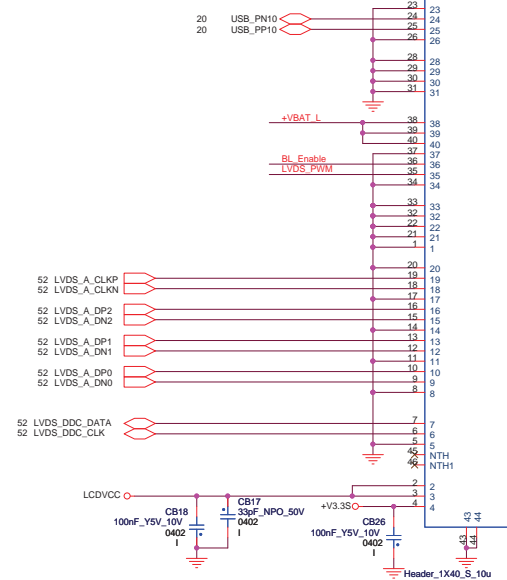
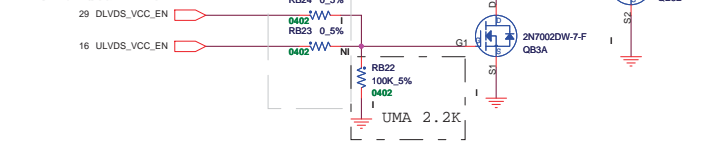
Discrete GPU: Install RB22  
UMA: Install RB24



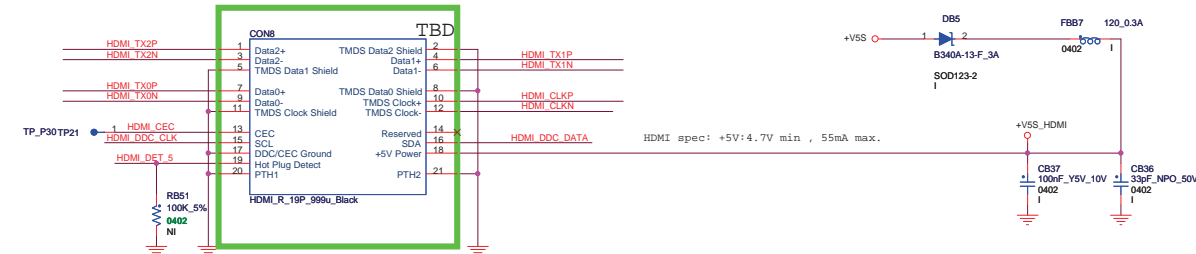
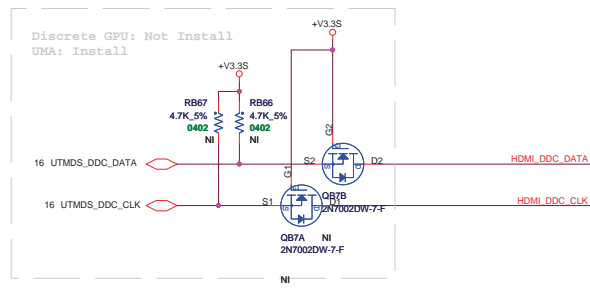
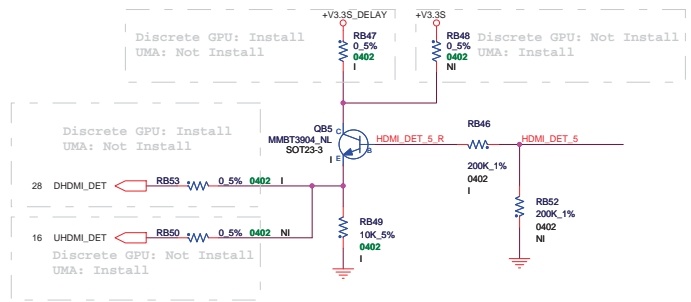
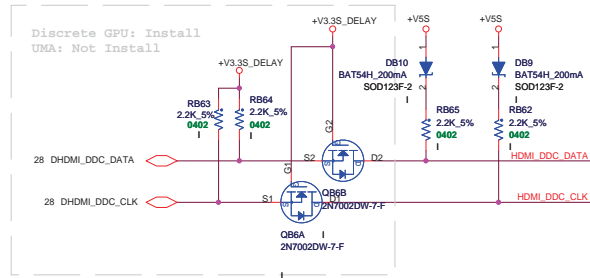
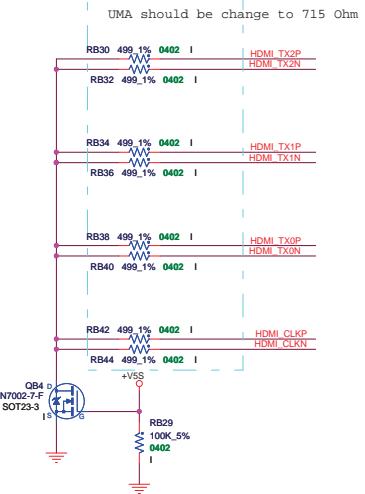
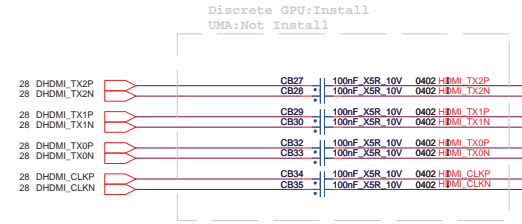
Discrete GPU: Install RB113  
UMA: Install RB114

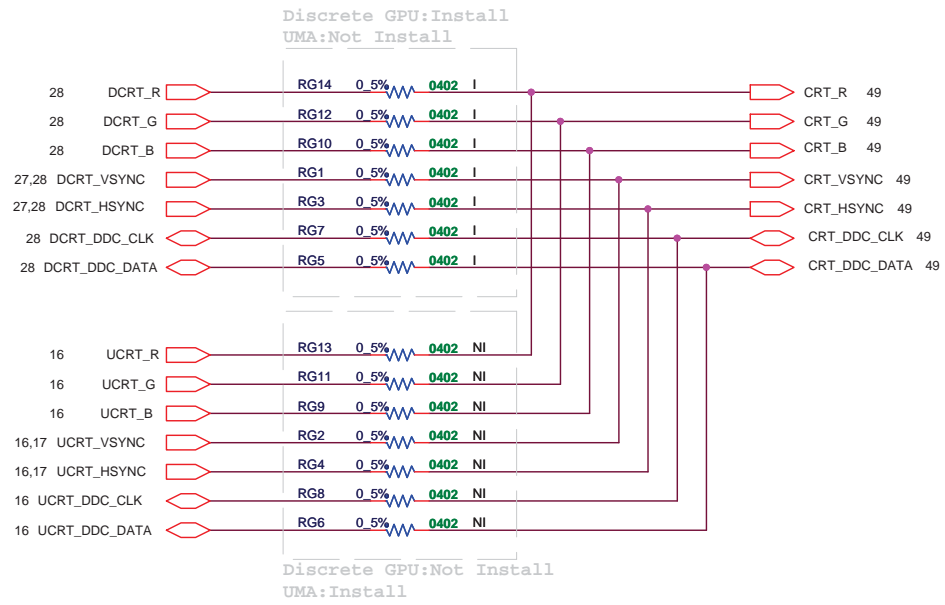


Discrete GPU: Install RB36  
UMA: Install RB37

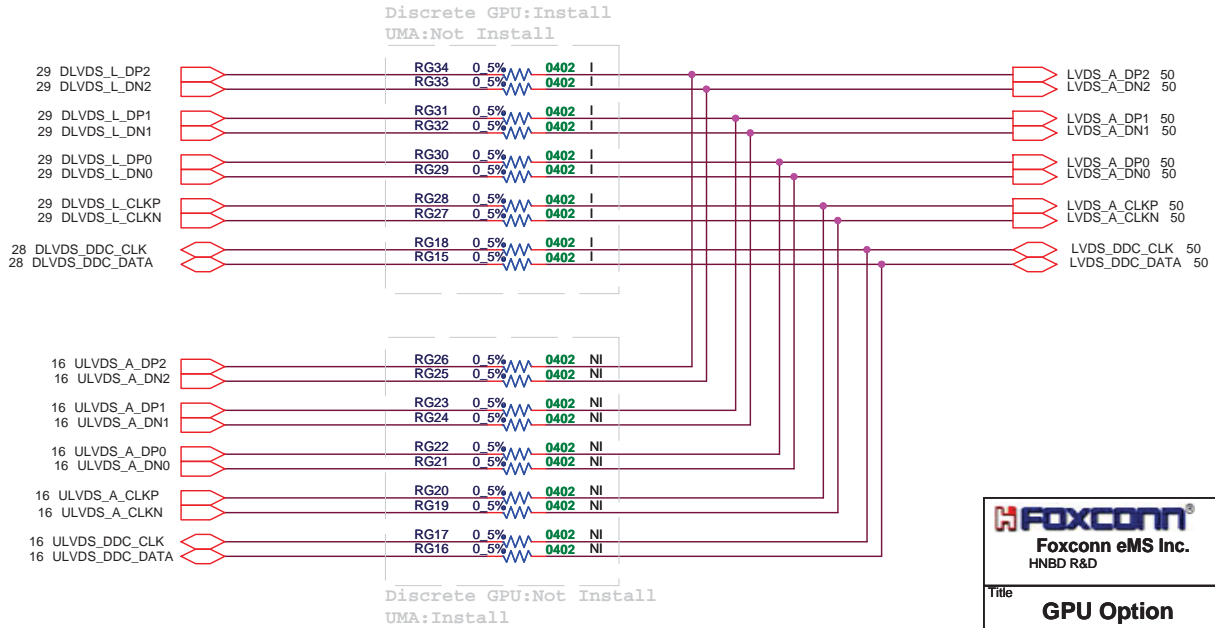


<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
HNBD R&D		phone: +886-2-2799-6111	
<b>LVDS</b>			
Size	Document Number	Rev	0.2
C	PM		
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**CRT**



**LVDS**

**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc.  
 HNBD R&D phone: +886-2-2799-6111

Title: **GPU Option**

Size: <b>B</b>	Document Number: <b>PM</b>	Rev: <b>0.2</b>
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		<b>Hon Hai Precision Industry Co. Ltd.</b>	
<b>Foxconn eMS Inc.</b>		phone: +886-2-2799-6111	
HNBD R&D			
Title <b>Camera</b>			
Size	Document Number		Rev
Custom	PM		0.1
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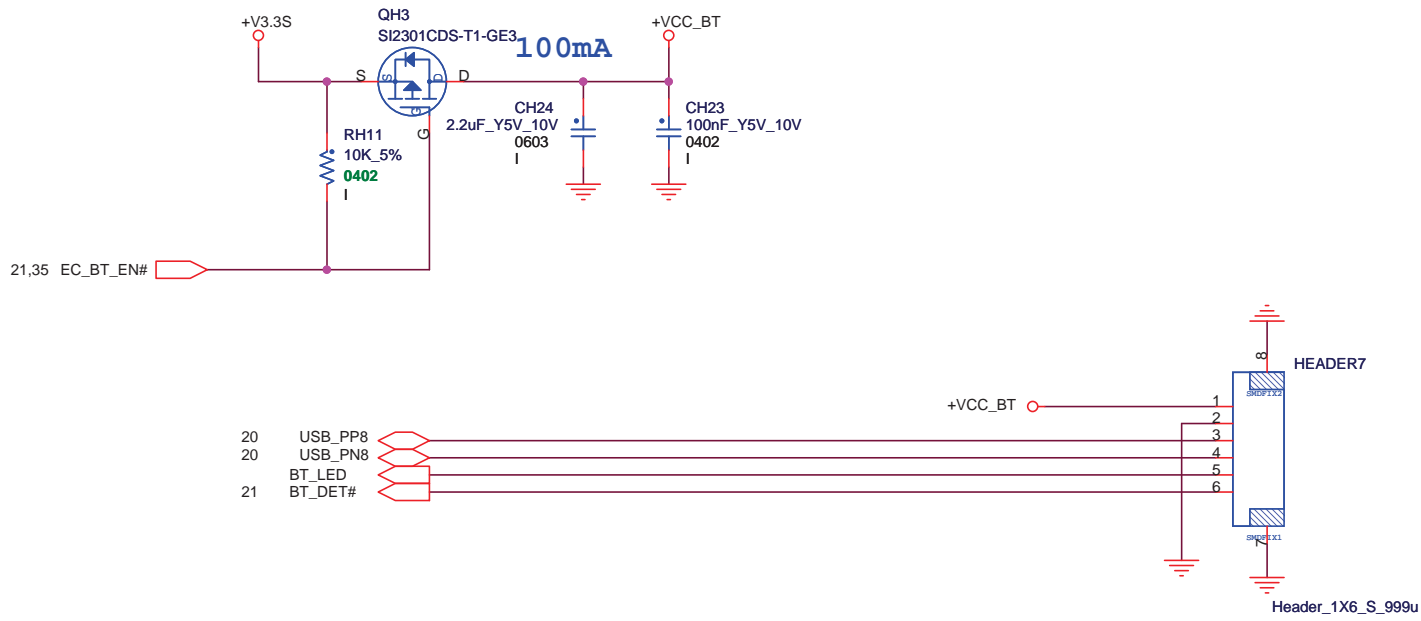
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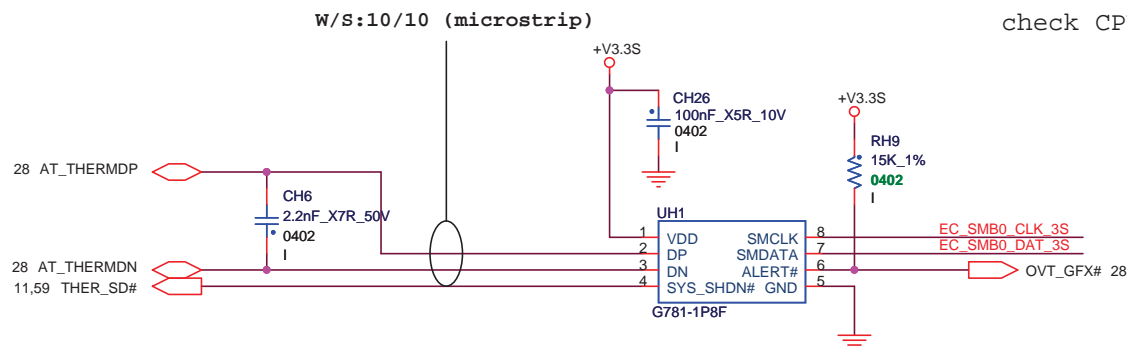
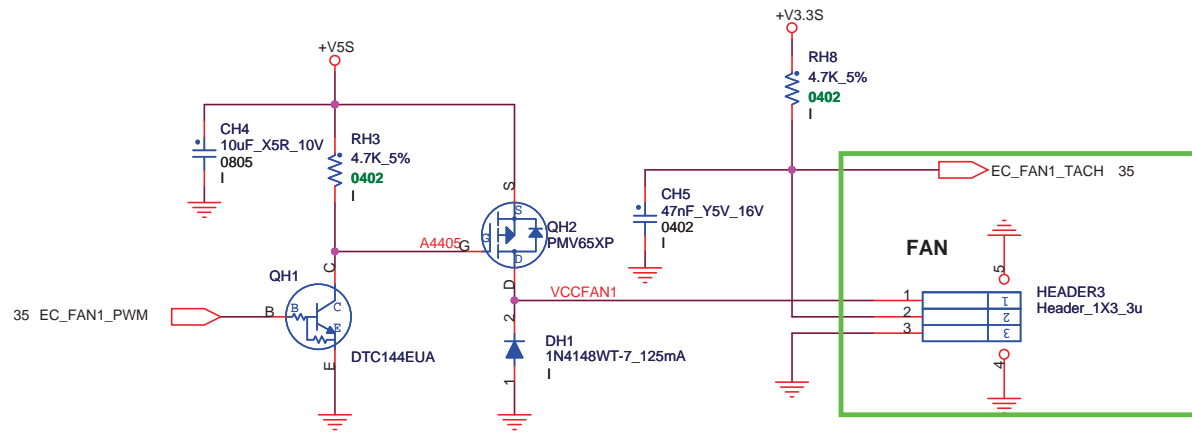
1



- 20 USB\_PP8
- 20 USB\_PN8
- BT\_LED
- 21 BT\_DET#

## Bluetooth CONN.

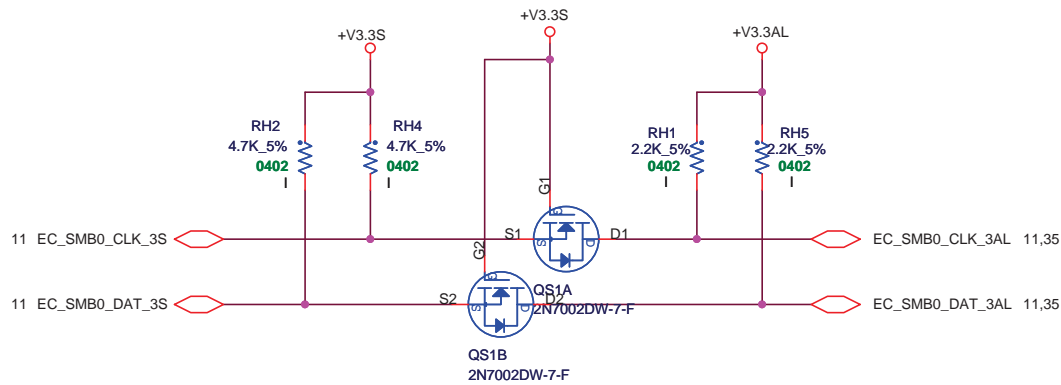
		<b>Hon Hai Precision Industry Co. Ltd.</b>	
<b>Foxconn eMS Inc.</b>		HNBD R&D	
		phone: +886-2-2799-6111	
<b>Title</b> <b>Bluetooth</b>			
<b>Size</b> Custom	<b>Document Number</b> <b>PM</b>		<b>Rev</b> <b>0.1</b>
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Place Thermal-Sensor near GMCH.

SMBus Address: 98H  
CPU/VGA Thermal-Sensor

check CPU hardware shutdown temp



SYS\_SHDN Threshold Temperature

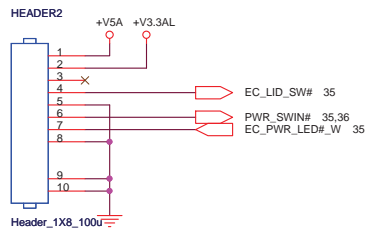
SYS_SHD PULL-UP / ALERT PULL-UP	SYS_SHDN Threshold Temperature					
	4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%
4.7K OHM ±10%	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM ±10%	78°C	84°C	90°C	96°C	102°C	108°C
10K OHM ±10%	79°C	85°C	91°C	97°C	103°C	109°C
15K OHM ±10%	80°C	86°C	92°C	98°C	104°C	110°C
22K OHM ±10%	81°C	87°C	93°C	99°C	105°C	111°C
33K OHM ±10%	82°C	88°C	94°C	100°C	106°C	112°C

**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
**Foxconn eMS Inc.** HNBD R&D phone: +886-2-2799-6111

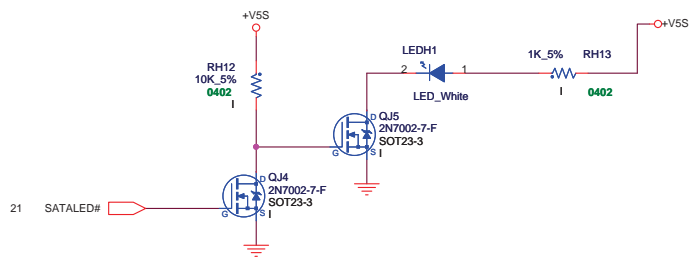
Title: **FAN/Thermal Sensor**


Size: Document Number **Custom PM** Rev **0.1**

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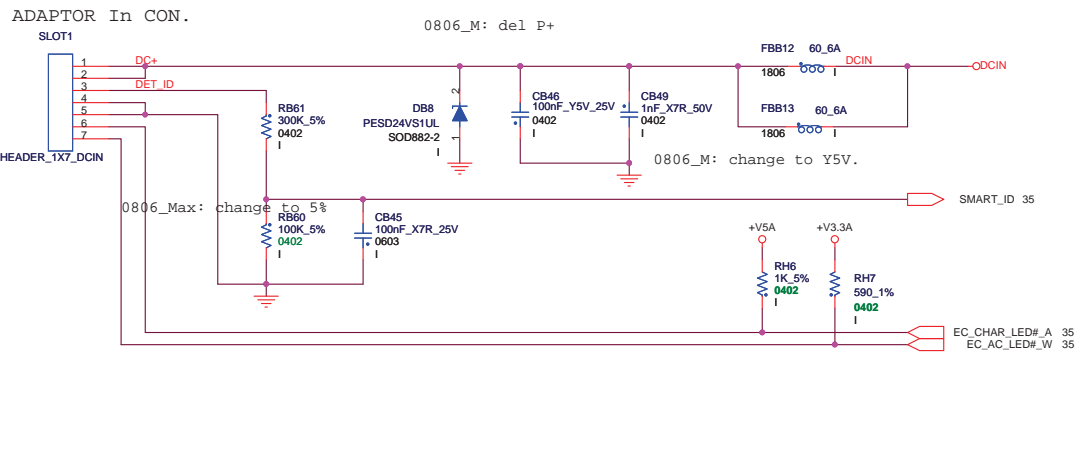


### HDD/ODD Status LED



 <b>Foxconn eMS Inc.</b>		Hon Hai Precision Industry Co. Ltd.	
HNBD R&D		phone: +886-2-2799-6111	
Title <b>Power Button Board/LED</b>			
Size	Document Number	Rev	
Custom	<b>PM</b>	<b>0.1</b>	
Page Modified: Wednesday, August 26, 2009 18:38:11 (UTC/GMT) Sheet 56 of 68			

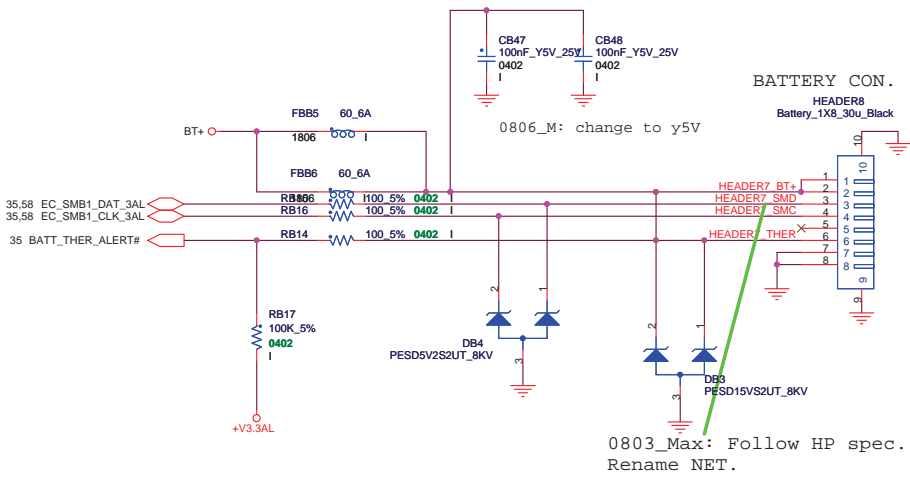




0803\_Max: Modify for new proposal.YB.

Pin No	Pin Define	AWG	Color
1	DC+	22	Red
2	DC+	22	Red
3	Detect (ID)	28	White
4	DC-	22	Black
5	DC-	22	Black
6	LED-	28	Black
7	LED+	28	yellow

0806\_Max: EE: check LED+/- ???



Pin No.	Symbol	Comments
1	B ATT+	B att+, Battery Positive Terminal.
2	B ATT+	B att+, Battery Positive Terminal.
3	SMD	SMBus data interface I/O pin..
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	B att-, Battery Negative Terminal
8	GND	B att-, Battery Negative Terminal

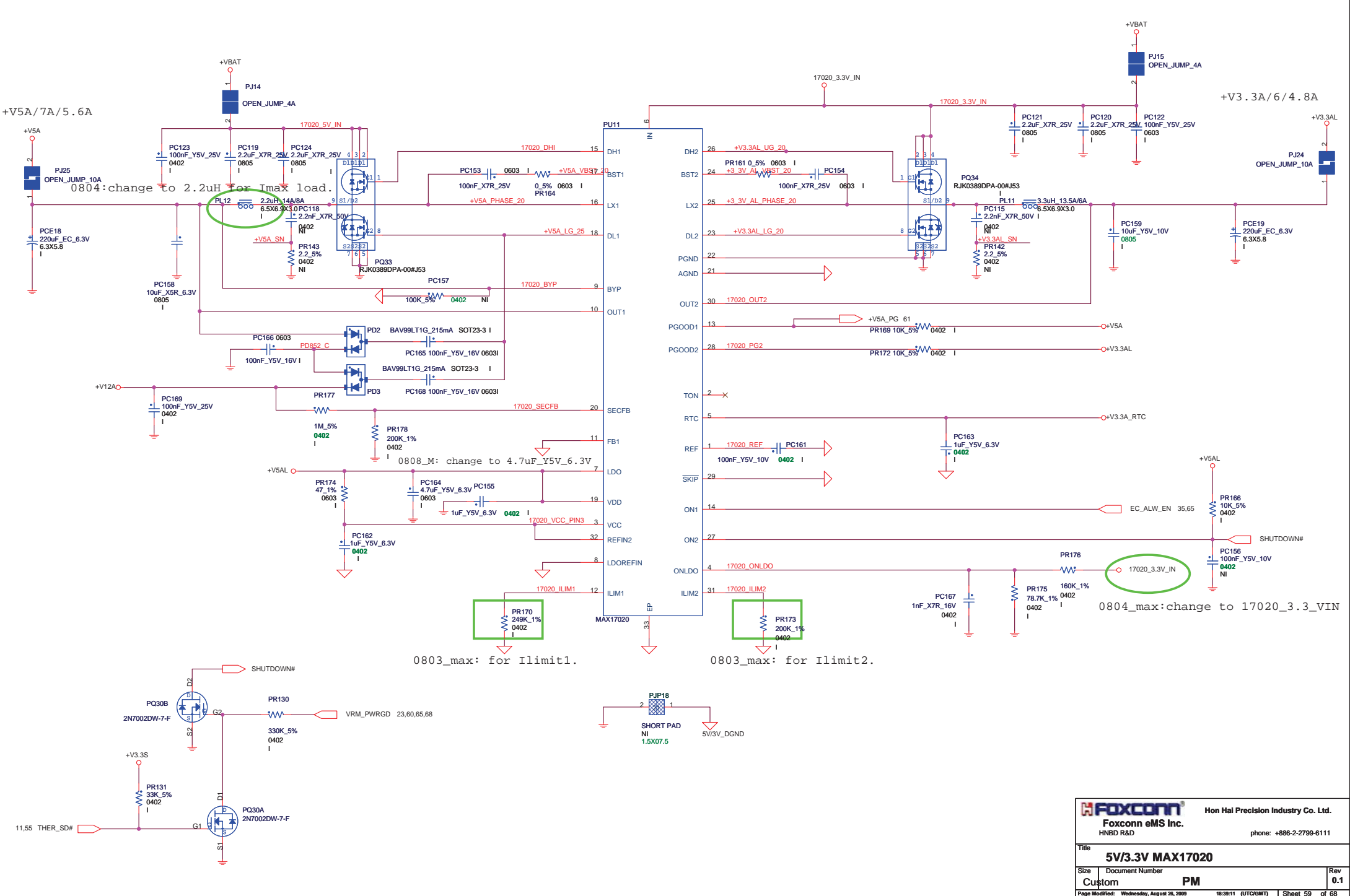
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc.  
 HNBD R&D phone: +886-2-2799-6111

Title: **PWR\_DCIN & Battery**

Size: Custom Document Number: PM Rev: 0.1

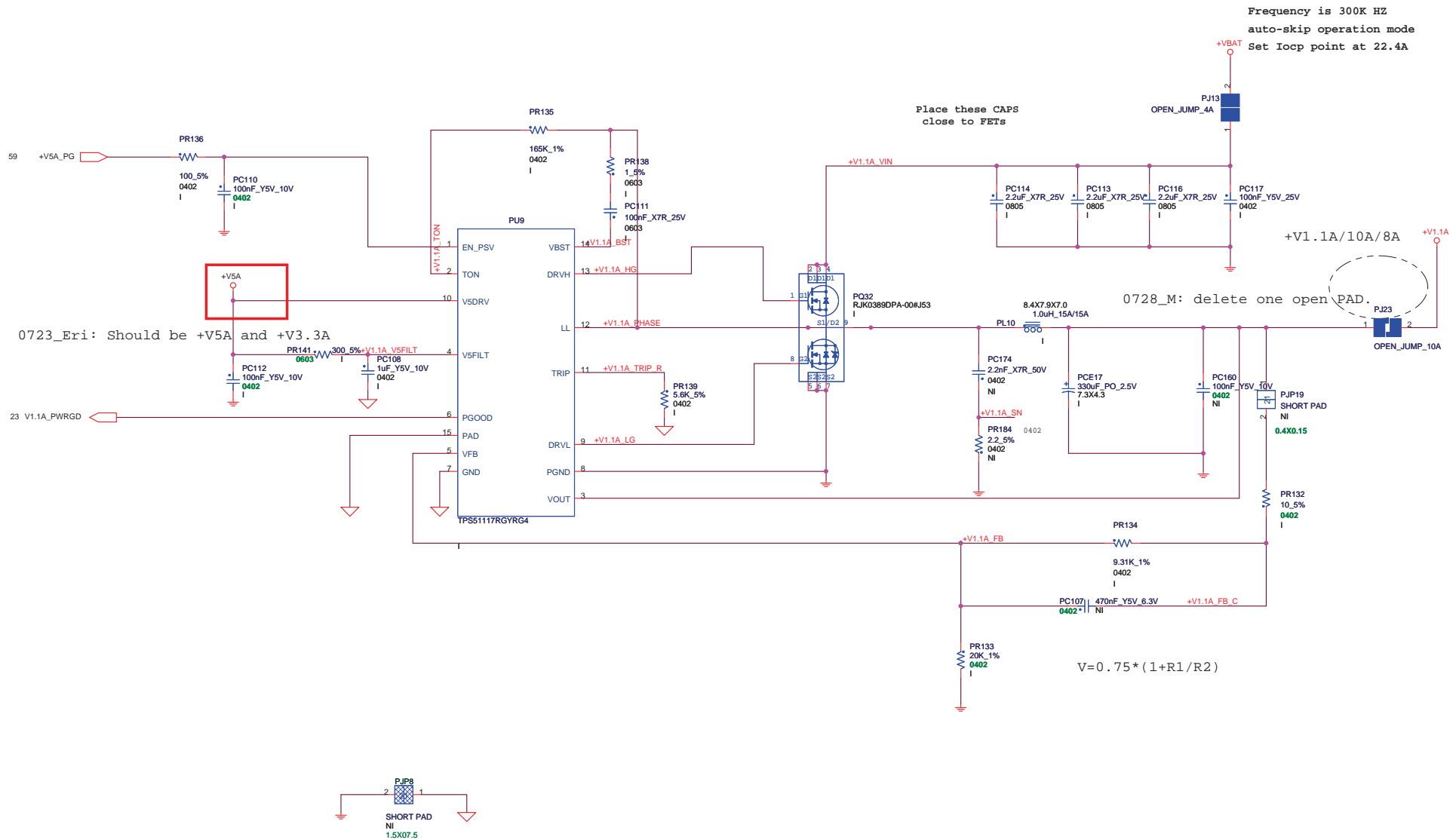
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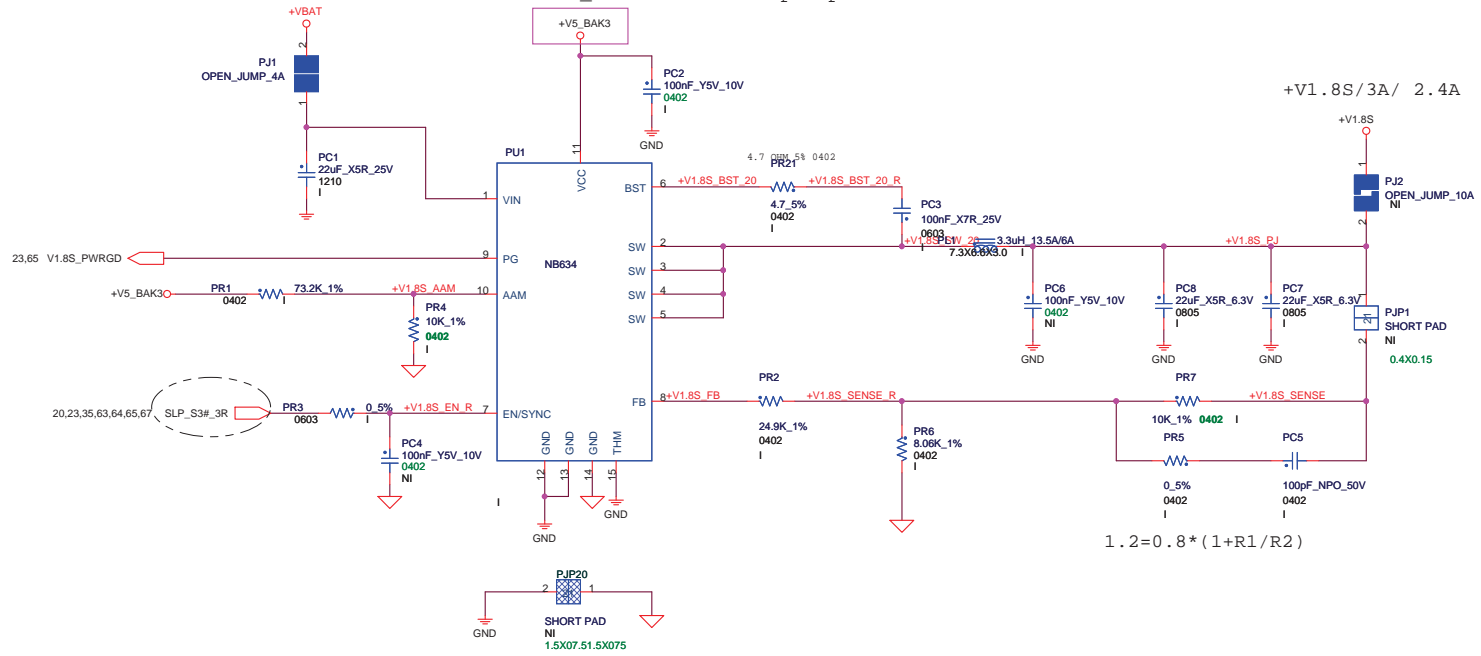
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
HNB D R&D		phone: +886-2-2799-6111	
Title: <b>5V/3.3V MAX17020</b>			
Size	Document Number	Rev	
Custom	PM	0.1	
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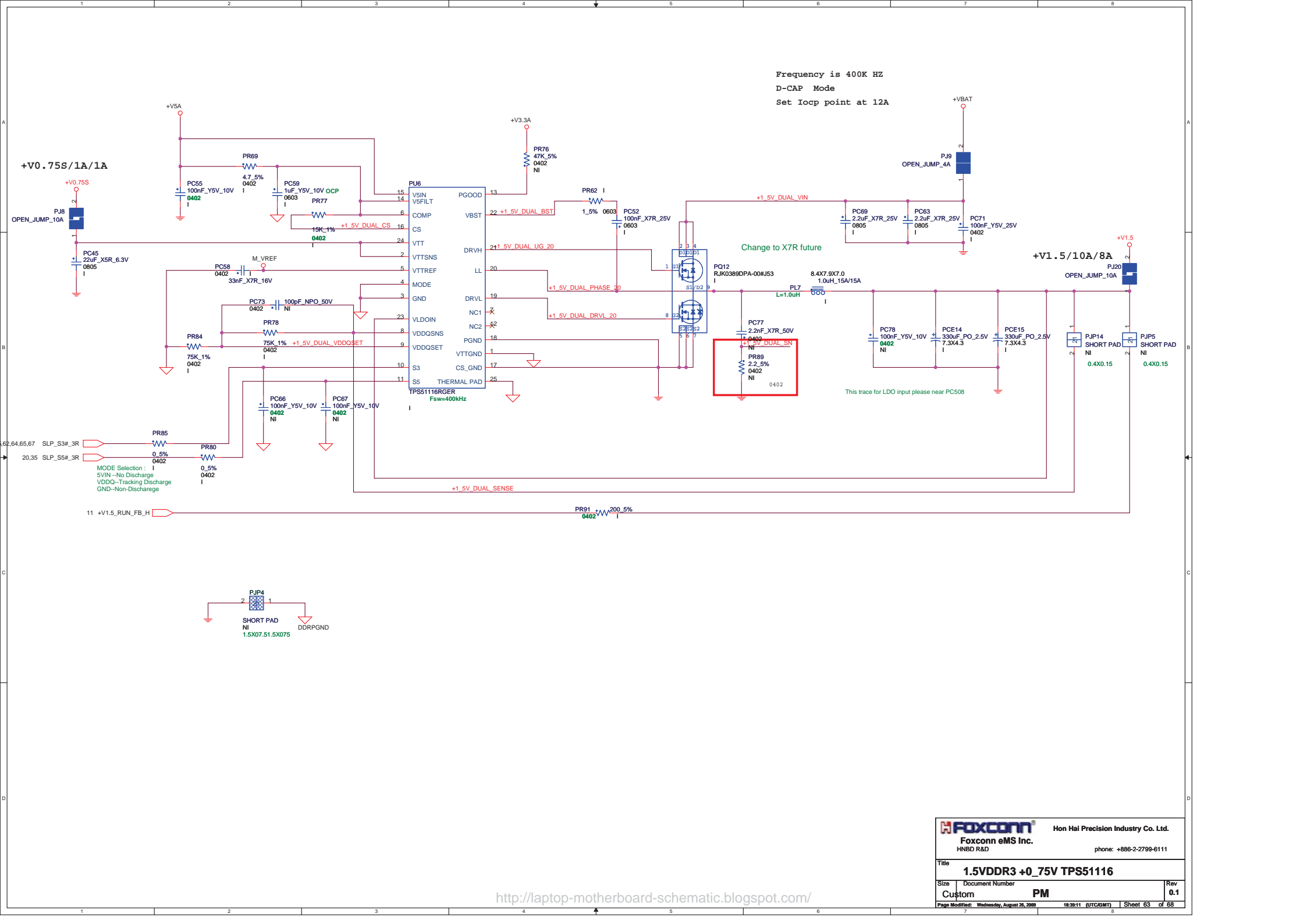


<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +886-2-2799-6111	
Title			
<b>+V1.1A TPS5117</b>			
Size	Document Number	Rev	
Custom	<b>PM</b>	<b>0.1</b>	
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0724\_Max: This is output power. 5V 5mA.



		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D	
		phone: +886-2-2799-6111	
Title <b>V1.8S NB634</b>			
Size	Document Number	Rev	
Custom	PM	0.1	
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Frequency is 400K HZ  
 D-CAP Mode  
 Set Iocp point at 12A

+V0.75S/1A/1A

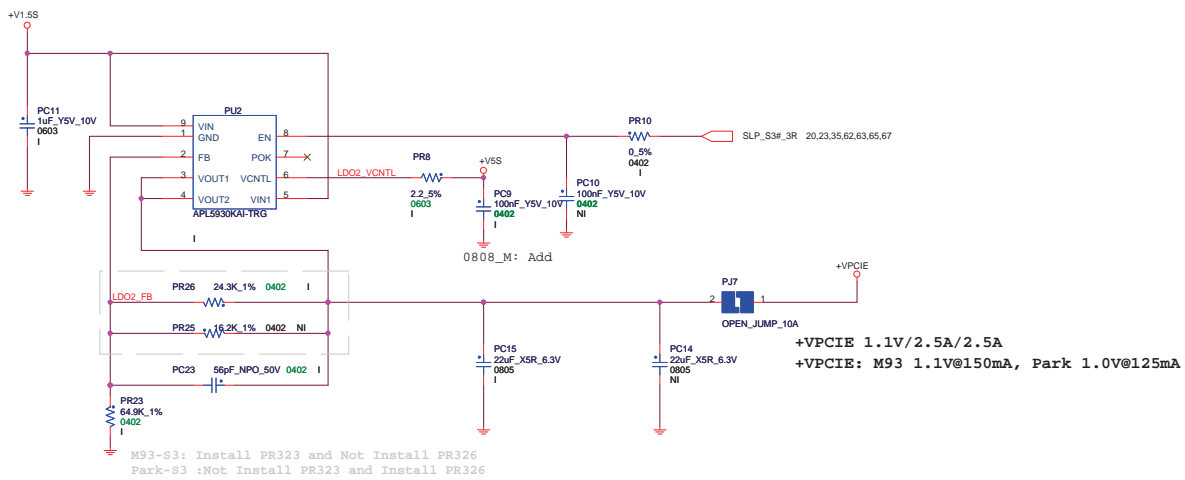
+V1.5/10A/8A

MODE Selection : I  
 5VIN --No Discharge  
 VDDQ--Tracking Discharge  
 GND--Non-Discharge

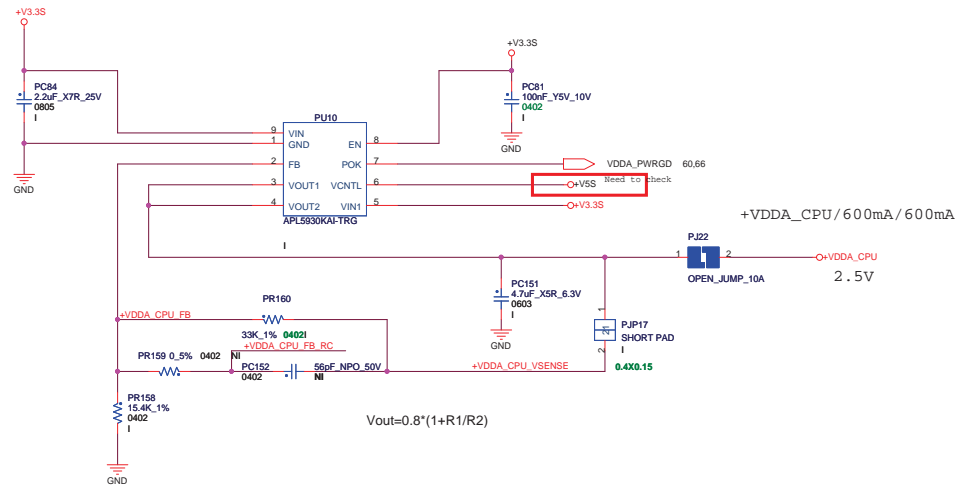
PJP4  
 SHORT PAD  
 NI  
 1.5X07.51.5X075

Change to X7R future

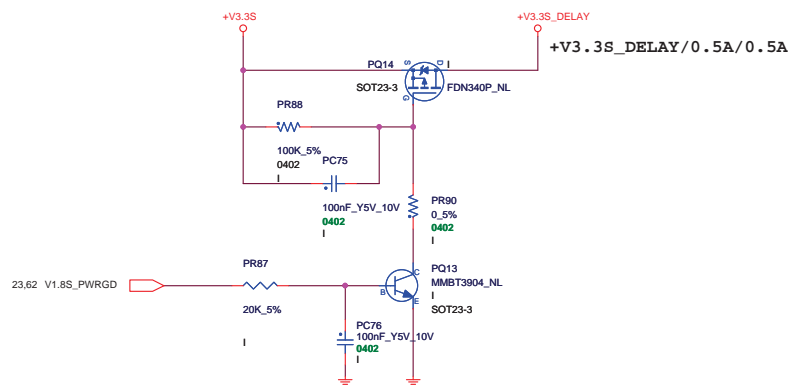
This trace for LDO input please near PC508



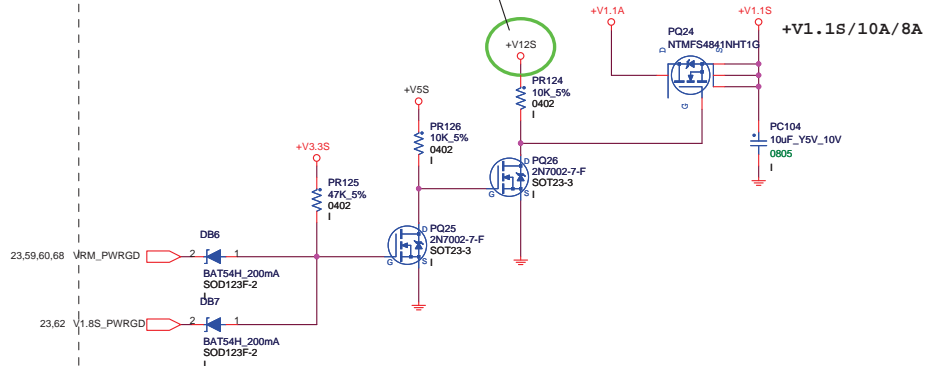
Dis ONLY, For Graphic Power



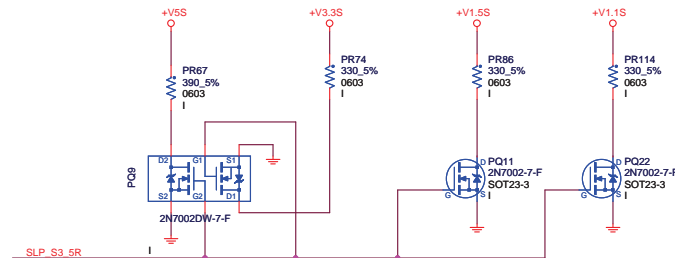
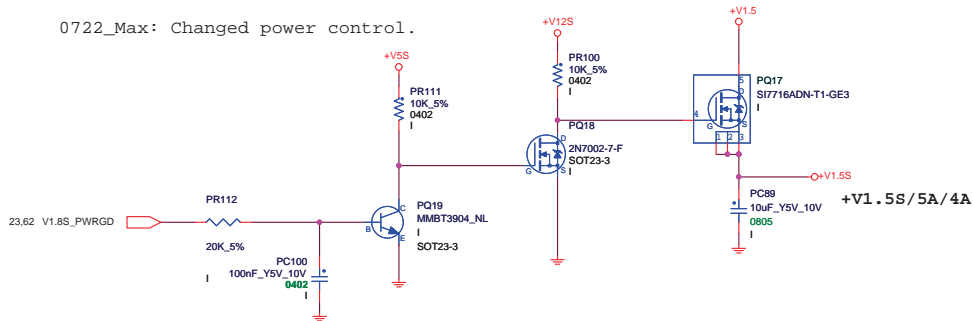




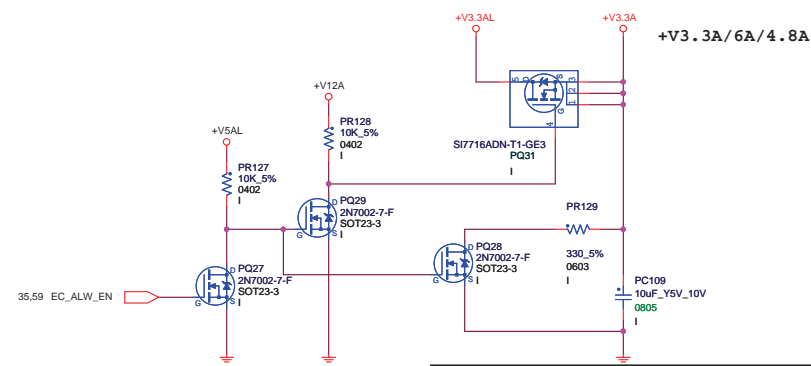
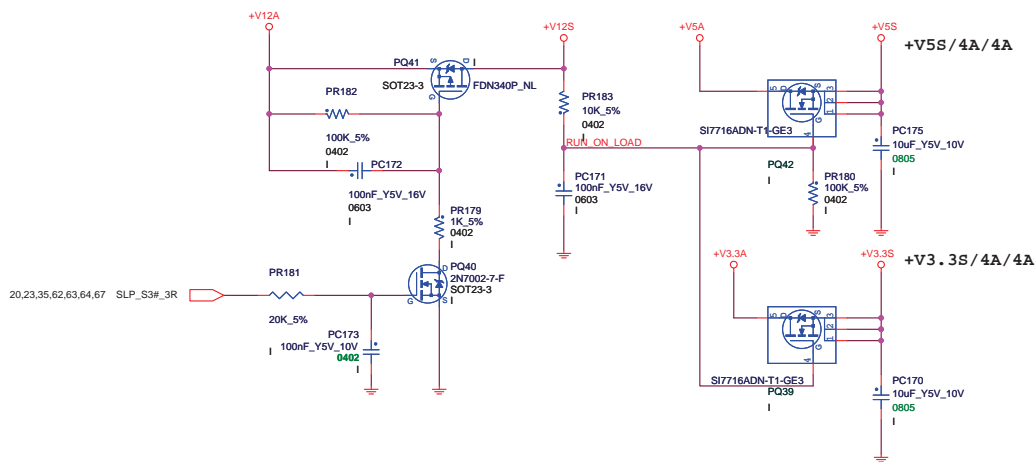
0803\_Max: change to +V12S



0722\_Max: Changed power control.

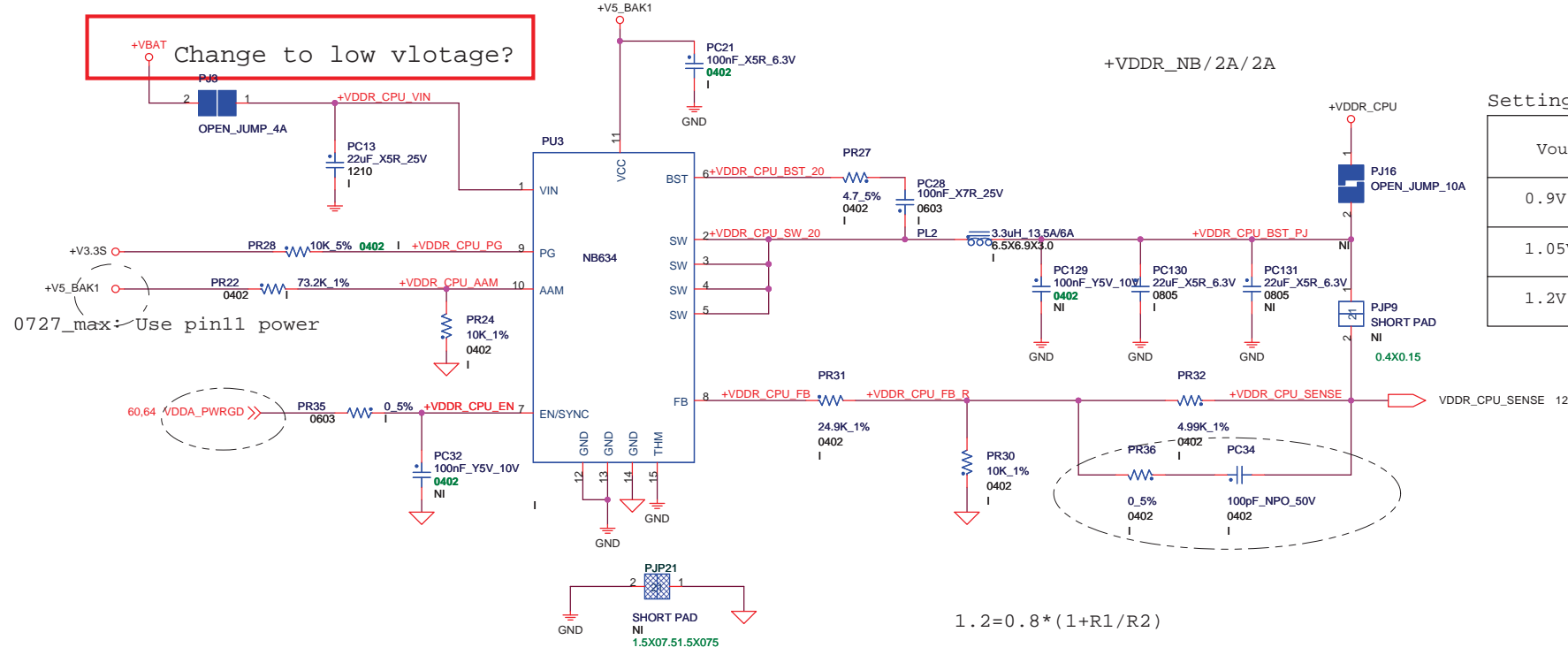


0803\_Max: Changed value to 3904.



**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
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 HNBD R&D phone: +886-2-2798-6111

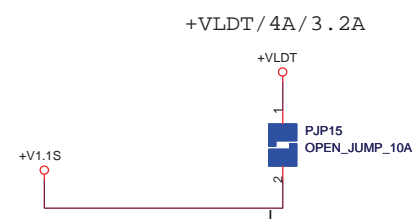
Title		
<b>PWR_Others power plane</b>		
Size	Document Number	Rev
Custom	PM	0.1
Page Modified: Wednesday, August 26, 2009 16:28:11 (UTC+8MT) Sheet 65 of 68		



Setting table.

Vout	PR663	PR666
0.9V	4.99K	39K
1.05V	4.99K	15.8K
1.2V	4.99K	10K

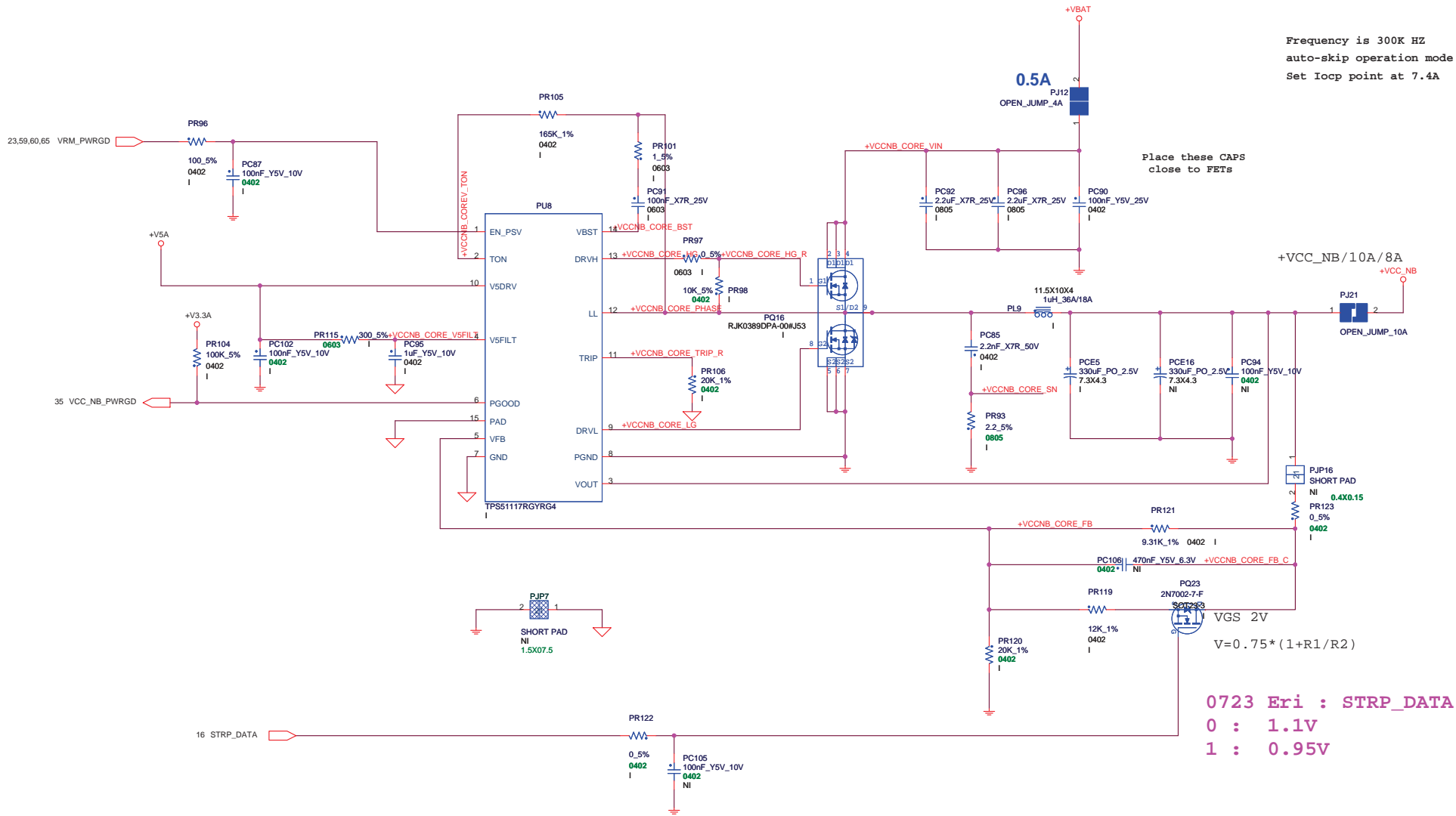
$$1.2 = 0.8 * (1 + R1/R2)$$



0727\_max Use pin11 power

Change to low vlotage?





Frequency is 300K HZ  
 auto-skip operation mode  
 Set Iocp point at 7.4A

Place these CAPS  
 close to FETs

0723 Eri : STRP\_DATA  
 0 : 1.1V  
 1 : 0.95V

$$V = 0.75 * (1 + R1/R2)$$