


GIGABYTE GA-8I848P Schematics

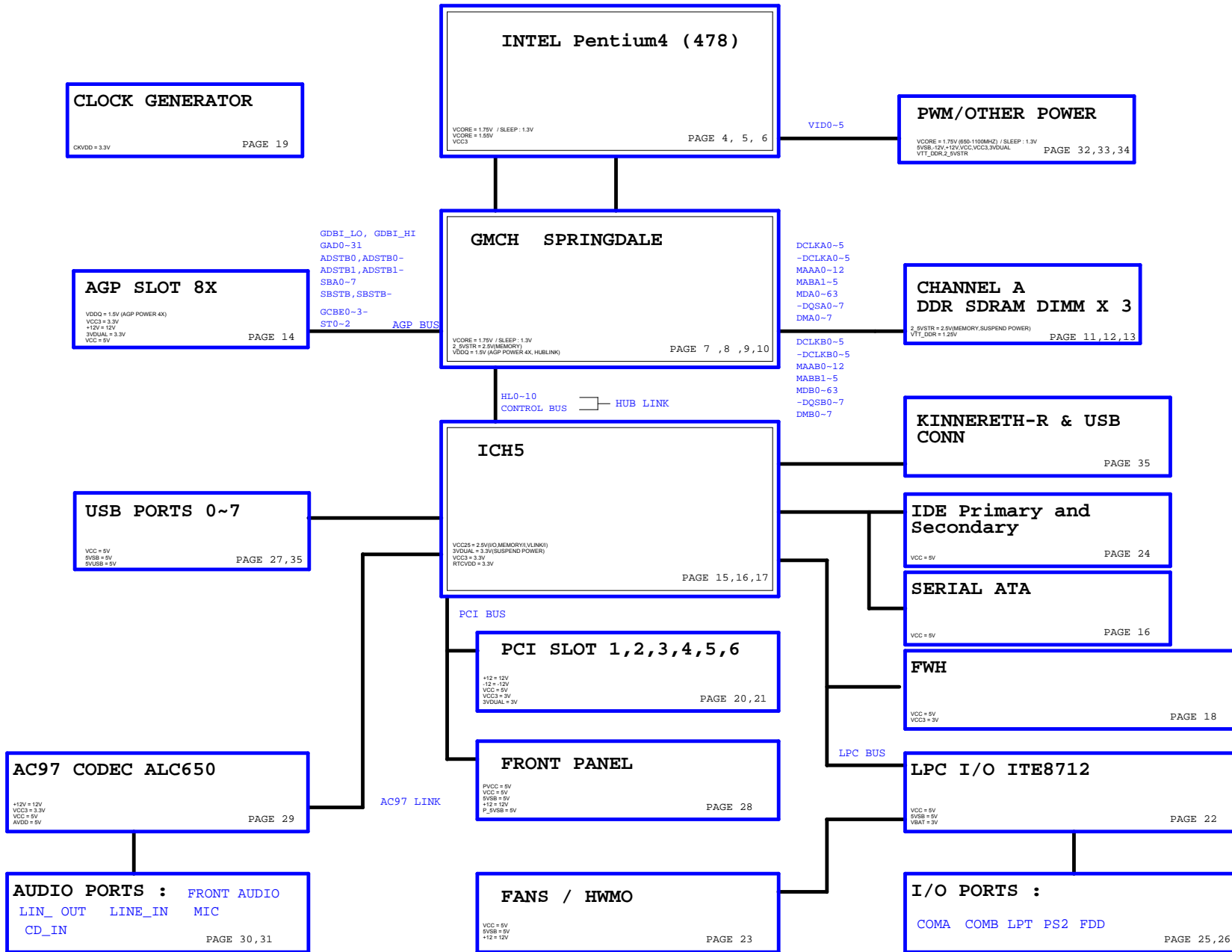
Revision 2.01

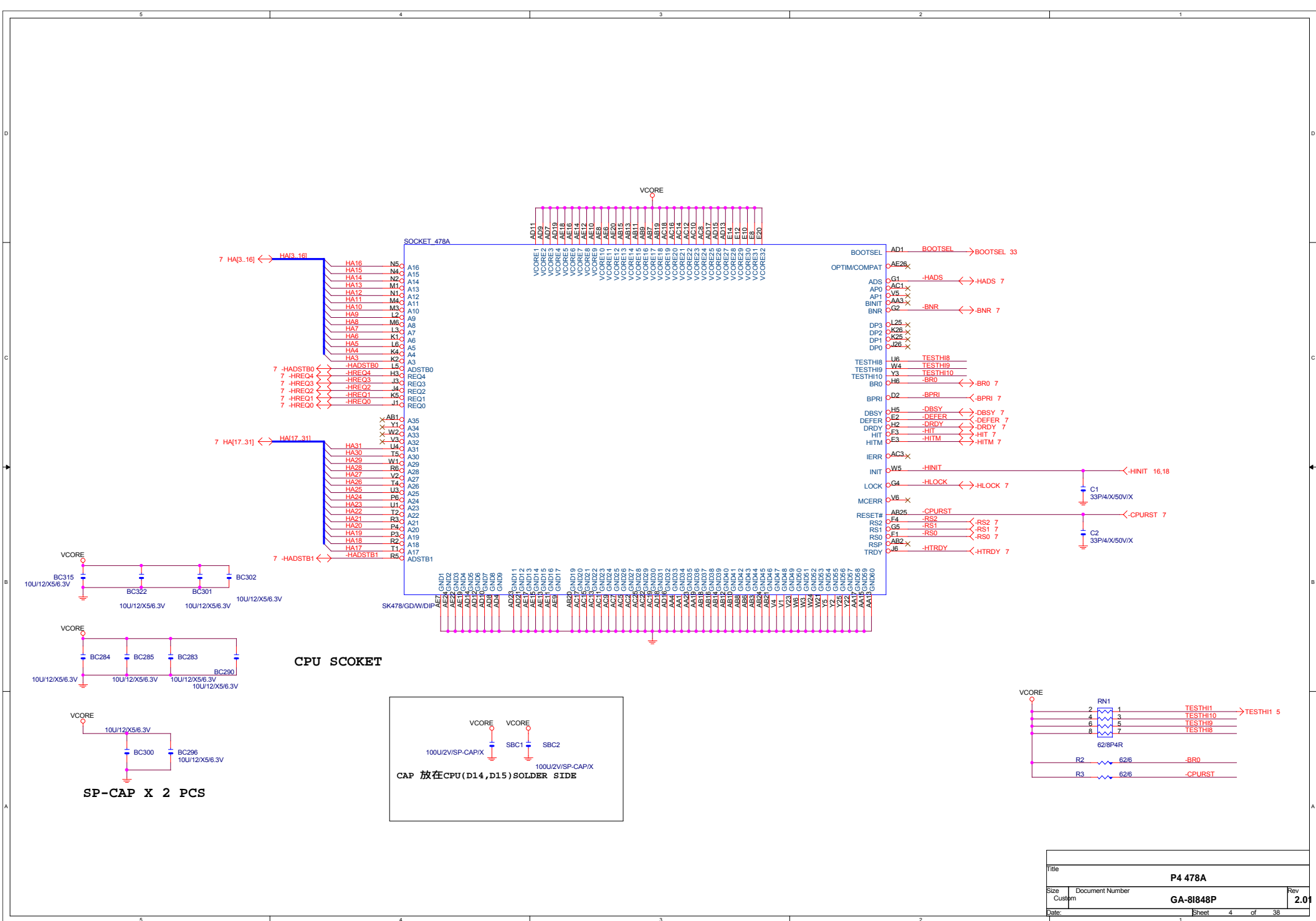
SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3 CHANNEL A
13	DDR TERMINATION
14	AGP
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	FWH
19	ICS952603 CLOCK GEN
20	PCI1_2
21	PCI3_4
22	PCI5_6

SHEET	TITLE
23	CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712
26	COM_LPT
27	IDE
28	FAN/HWMO
29	KB_PS2
30	FPANEL
31	USB CONN
32	DDR POWER
33	VCORE POWER
34	ATX, OTHERS POWER
35	KINNERETH-R LNA(CSA-1)
36	KINNERETH-R LNA(CSA-2)
37	KINNERETH-R LNA(CSA-3)

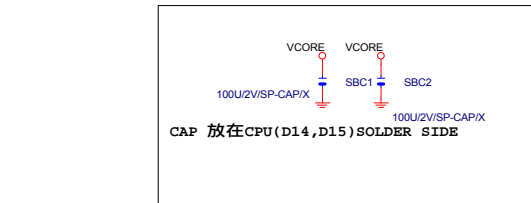
		COMPONENT SIDE (1 oz. Copper) VCC SIDE (1 oz. Copper) GND SIDE (1 oz. Copper) SOLDER SIDE (1 oz. Copper)
GIGABYTE CORP.		
Title: COVER SHEET		
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BLOCK DIAGRAM



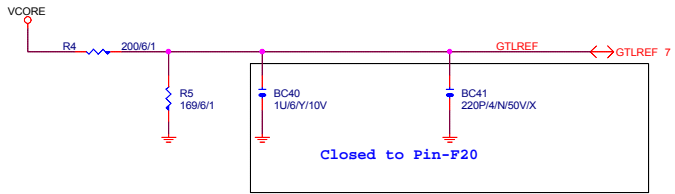


CPU SOCKET

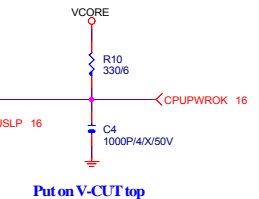
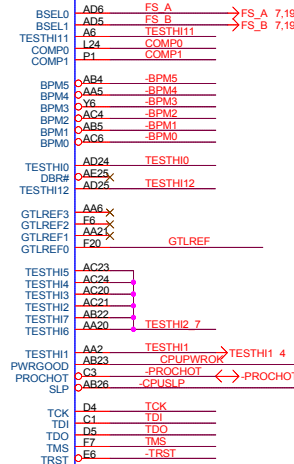
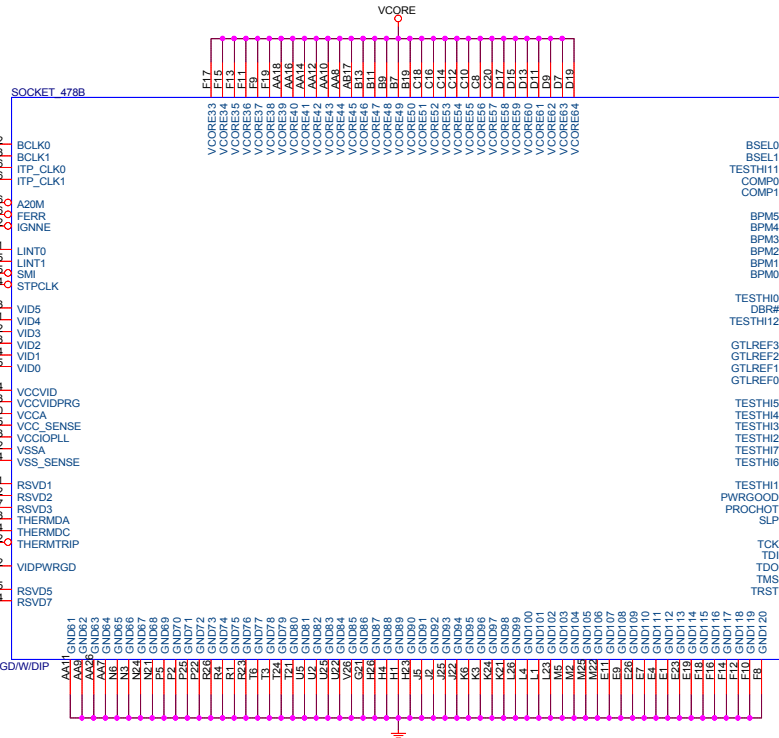
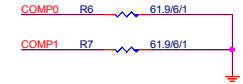


SP-CAP X 2 PCS

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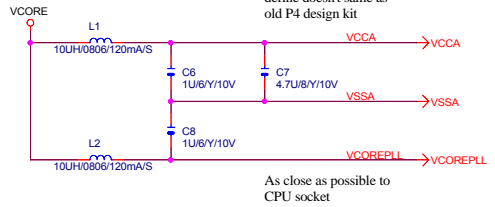


Place outside of CPU socket



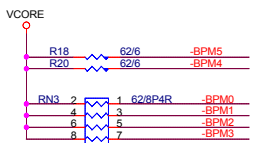
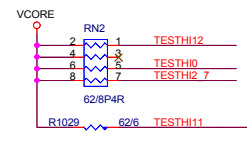
Put on V-CUT top

Note:
VCCA & VCCOREPLL
define doesn't same as
old P4 design kit

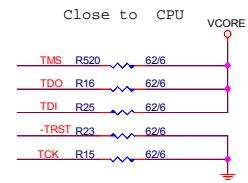


As close as possible to CPU socket

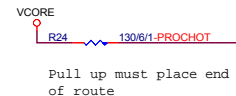
Trace width doesn't less than 12 Mil



Close to CPU

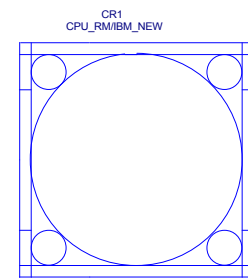
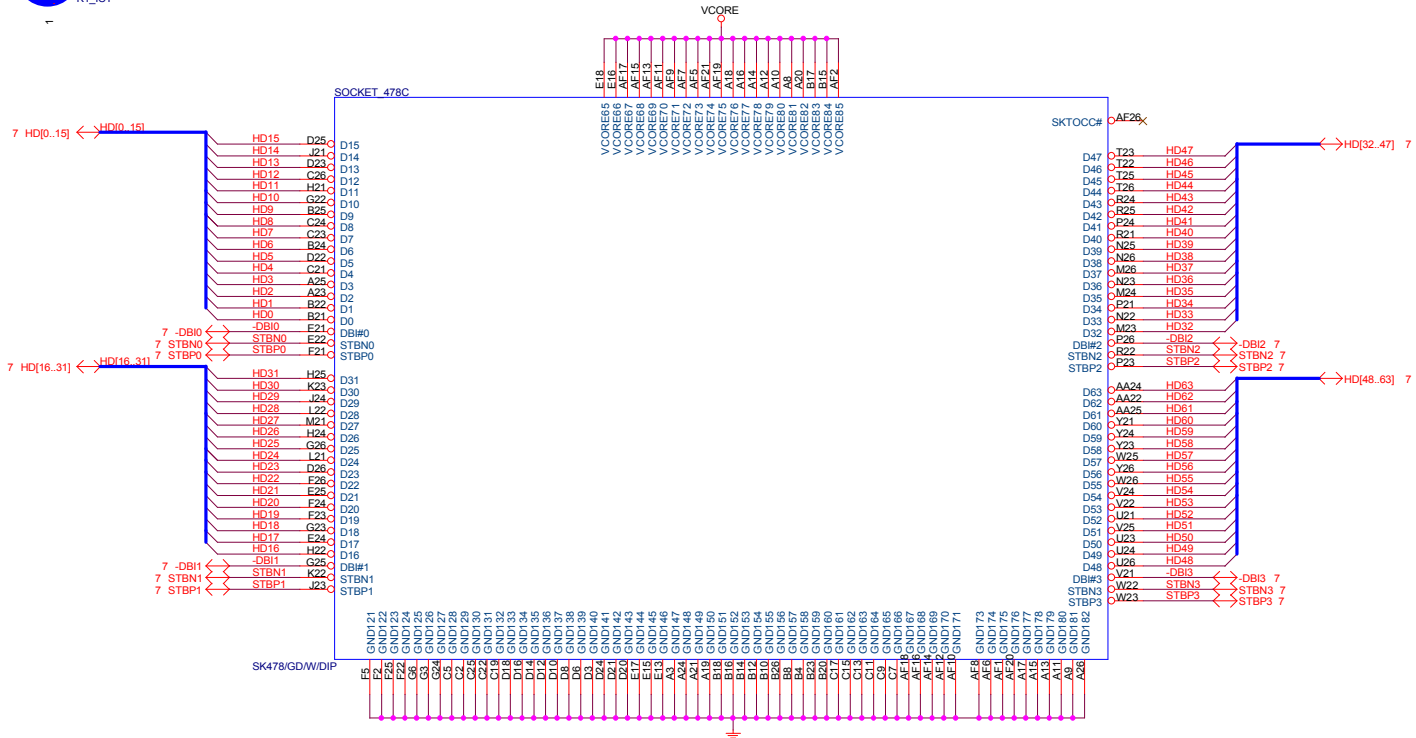
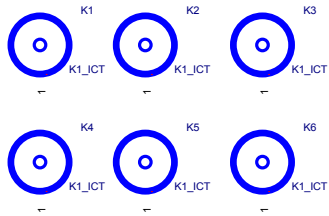


Close to CPU

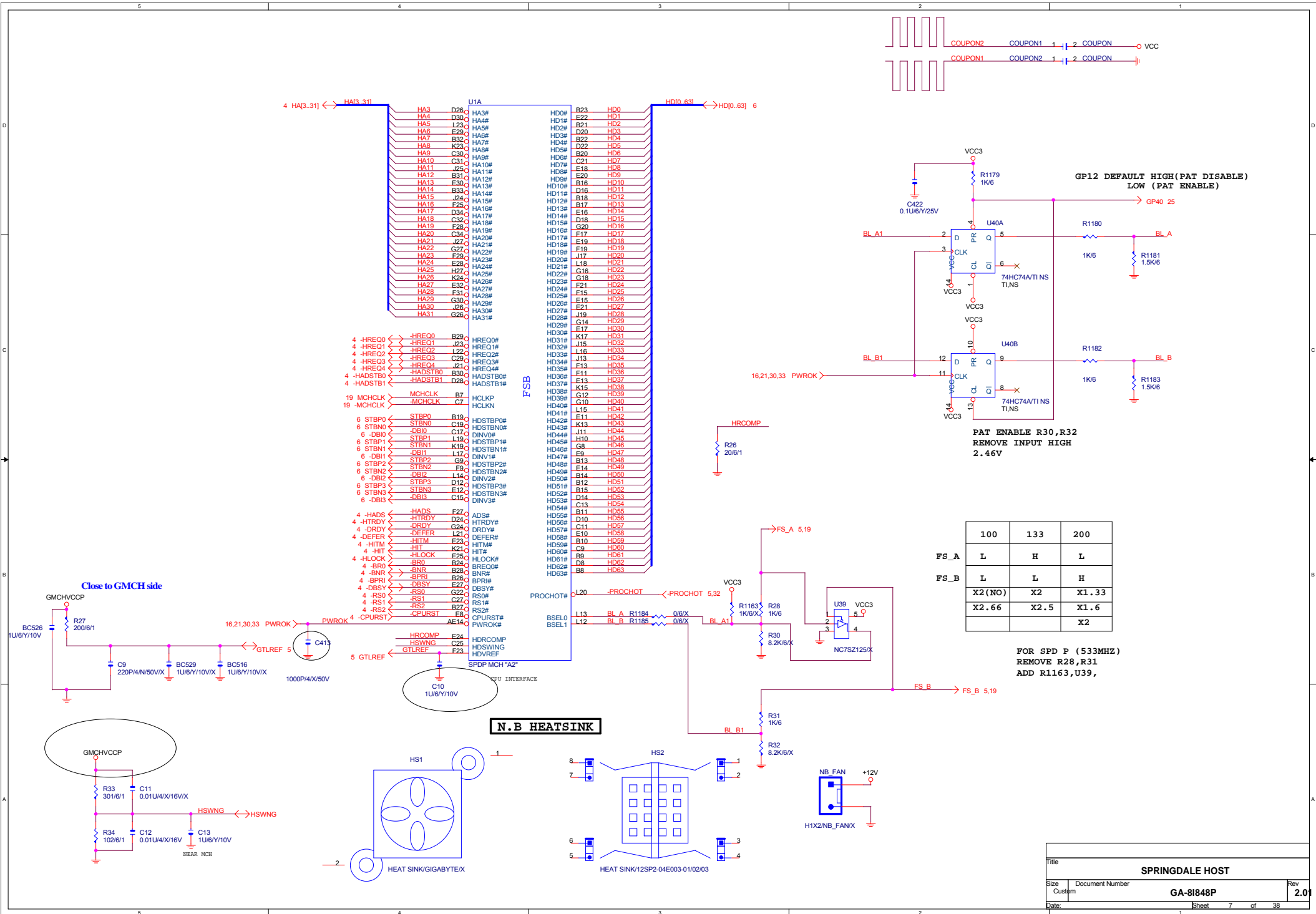


Pull up must place end of route

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P4 478B		
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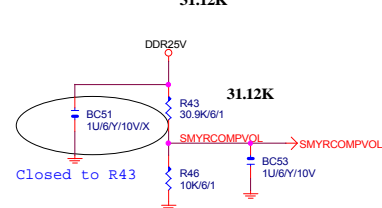
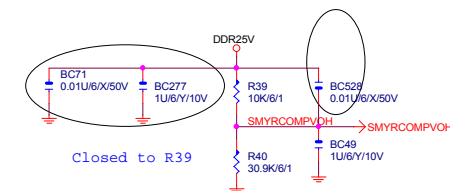
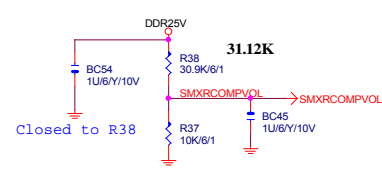
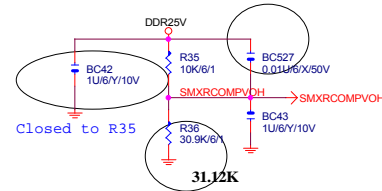
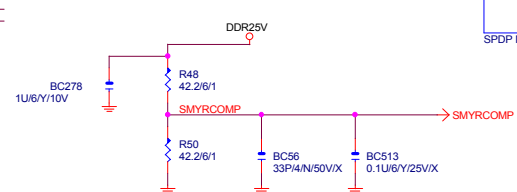
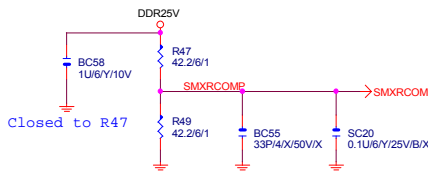
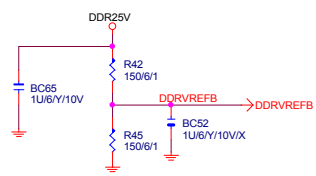
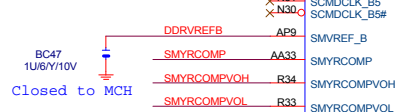
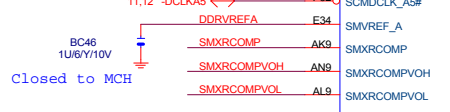
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U1B		U1C	
11,12,13 MAAA[0..12]	MAAA0..121	SDQS_A0	AN11 DQSA0
11,12,13 MABA[1..5]	MABA1..51	SDM_A0	AP12 MDA0
11,12,13 DMA[0..7]	MDA10..71	SDQ_A0	AP10 MDA0
11,12,13 MDA[0..63]	MDA10..631	SDQ_A1	AP11 MDA1
11,12,13 DQSA[0..7]	DQSA10..71	SDQ_A2	AP12 MDA2
		SDQ_A3	AP13 MDA3
		SDQ_A4	AP10 MDA4
		SDQ_A5	AL10 MDA5
		SDQ_A6	AL12 MDA6
		SDQ_A7	AP13 MDA7
		SDQS_A1	AP15 DQSA1
		SDM_A1	AP16 DMA1
		SDQ_A8	AP14 MDA8
		SDQ_A9	AM14 MDA9
		SDQ_A10	AL18 MDA10
		SDQ_A11	MDA11
		SDQ_A12	AL14 MDA12
		SDQ_A13	AN15 MDA13
		SDQ_A14	AP18 MDA14
		SDQ_A15	AM18 MDA15
		SDQS_A2	AP23 DQSA2
		SDM_A2	AM24 DMA2
		SDQ_A16	AP22 MDA16
		SDQ_A17	AM22 MDA17
		SDQ_A18	AL24 MDA18
		SDQ_A19	AN27 MDA19
		SDQ_A20	AP21 MDA20
		SDQ_A21	AL22 MDA21
		SDQ_A22	AP25 MDA22
		SDQ_A23	AP27 MDA23
		SDQS_A3	AM30 DQSA3
		SDM_A3	AM33 DMA3
		SDQ_A24	AP28 MDA24
		SDQ_A25	AP29 MDA25
		SDQ_A26	AP33 MDA26
		SDQ_A27	AM33 MDA27
		SDQ_A28	AM28 MDA28
		SDQ_A29	AM29 MDA29
		SDQ_A30	AM31 MDA30
		SDQ_A31	AN34 MDA31
		SDQS_A4	AF34 DQSA4
		SDM_A4	AF31 DMA4
		SDQ_A32	AH32 MDA32
		SDQ_A33	AS34 MDA33
		SDQ_A34	AF32 MDA34
		SDQ_A35	AD32 MDA35
		SDQ_A36	AH31 MDA36
		SDQ_A37	AC33 MDA37
		SDQ_A38	AE34 MDA38
		SDQ_A39	AD34 MDA39
		SDQS_A5	V34 DQSA5
		SDM_A5	W33 DMA5
		SDQ_A40	AC34 MDA40
		SDQ_A41	AB31 MDA41
		SDQ_A42	V32 MDA42
		SDQ_A43	V31 MDA43
		SDQ_A44	AD31 MDA44
		SDQ_A45	AB32 MDA45
		SDQ_A46	U34 MDA46
		SDQ_A47	U33 MDA47
		SDQS_A6	M32 DQSA6
		SDM_A6	M34 DMA6
		SDQ_A48	T34 MDA48
		SDQ_A49	T32 MDA49
		SDQ_A50	K34 MDA50
		SDQ_A51	K32 MDA51
		SDQ_A52	T31 MDA52
		SDQ_A53	P34 MDA53
		SDQ_A54	L34 MDA54
		SDQ_A55	L33 MDA55
		SDQS_A7	H31 DQSA7
		SDM_A7	H32 DMA7
		SDQ_A56	J33 MDA56
		SDQ_A57	H34 MDA57
		SDQ_A58	E33 MDA58
		SDQ_A59	F33 MDA59
		SDQ_A60	K31 MDA60
		SDQ_A61	J34 MDA61
		SDQ_A62	G34 MDA62
		SDQ_A63	F34 MDA63

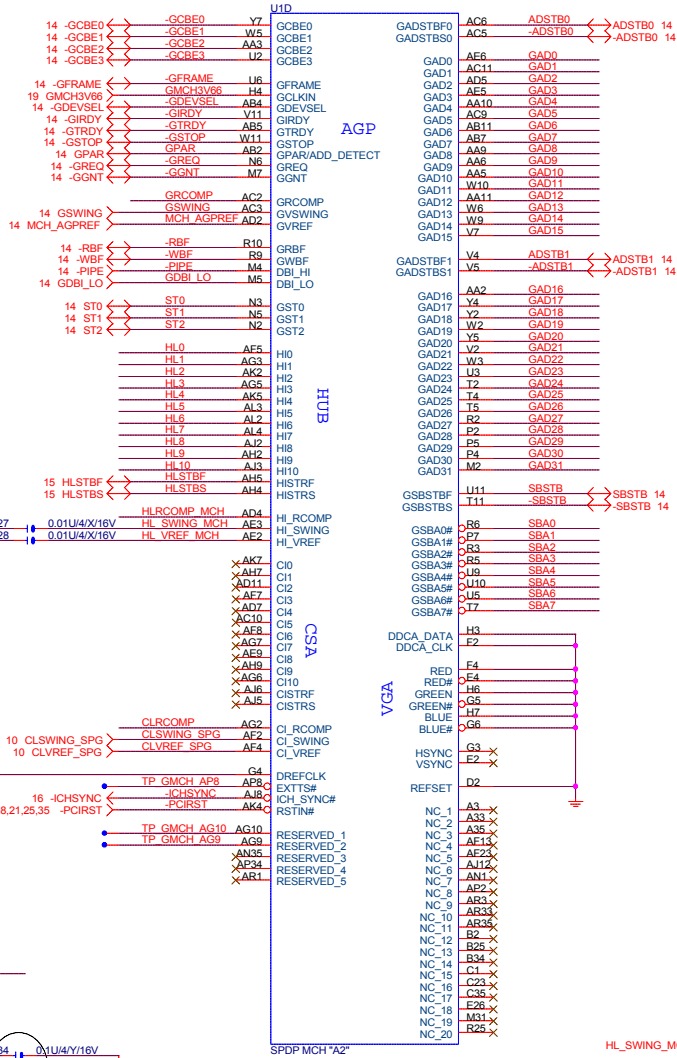
DDR Channel A

DDR Channel B

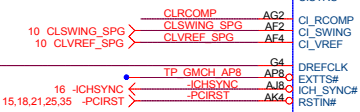
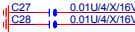


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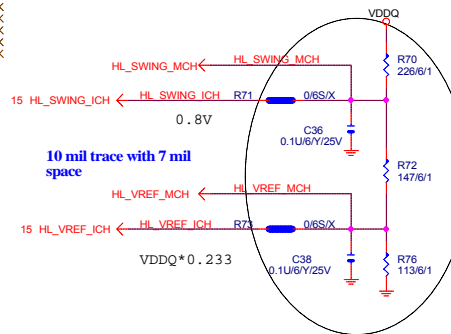
14 GAD[0..31] ↔ GAD[0..31]
 14 SBA[0..7] ↔ SBA[0..7]
 15 HL[0..10] ↔ HL[0..10]



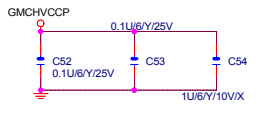
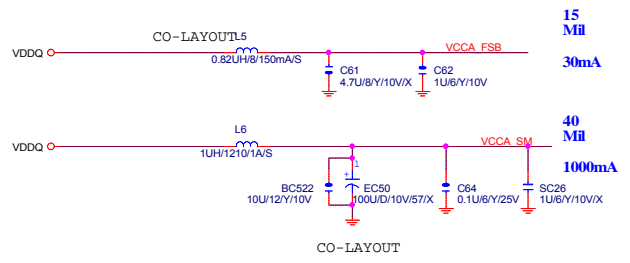
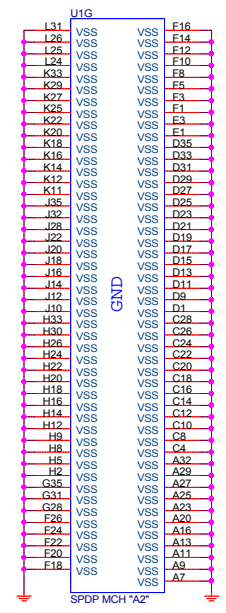
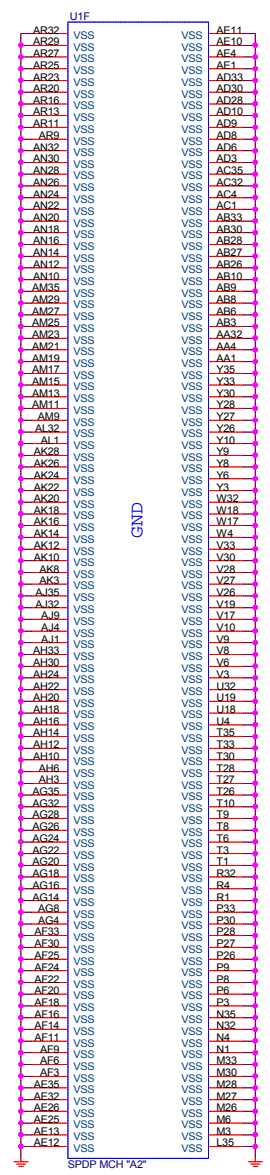
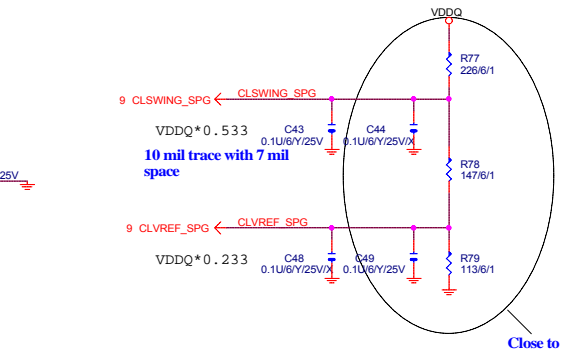
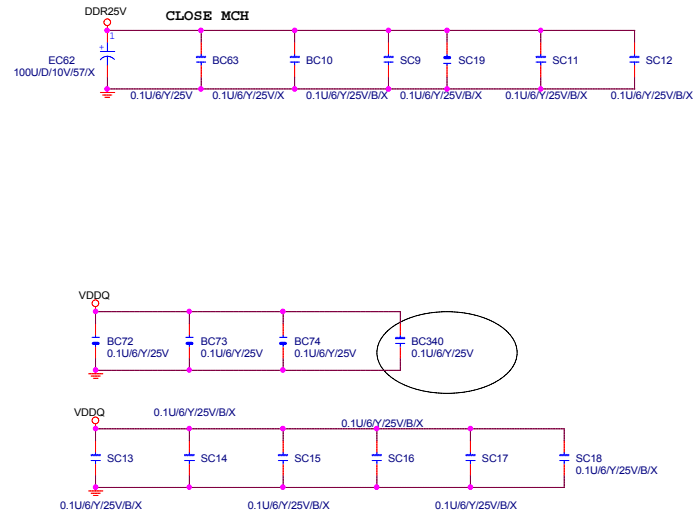
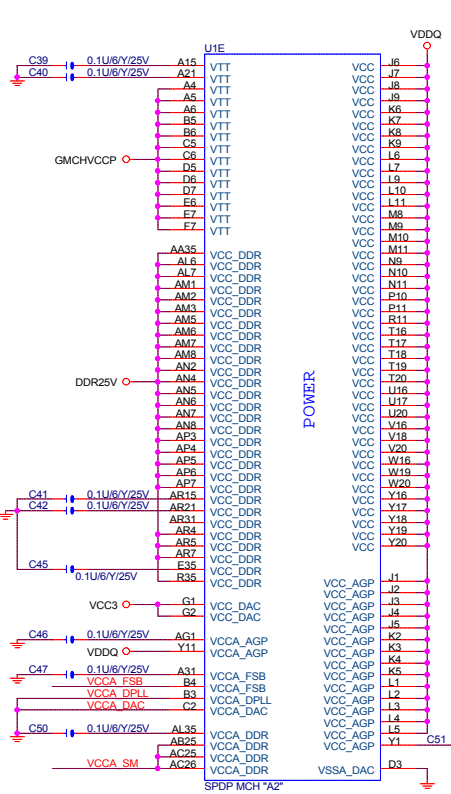
Close to MCH



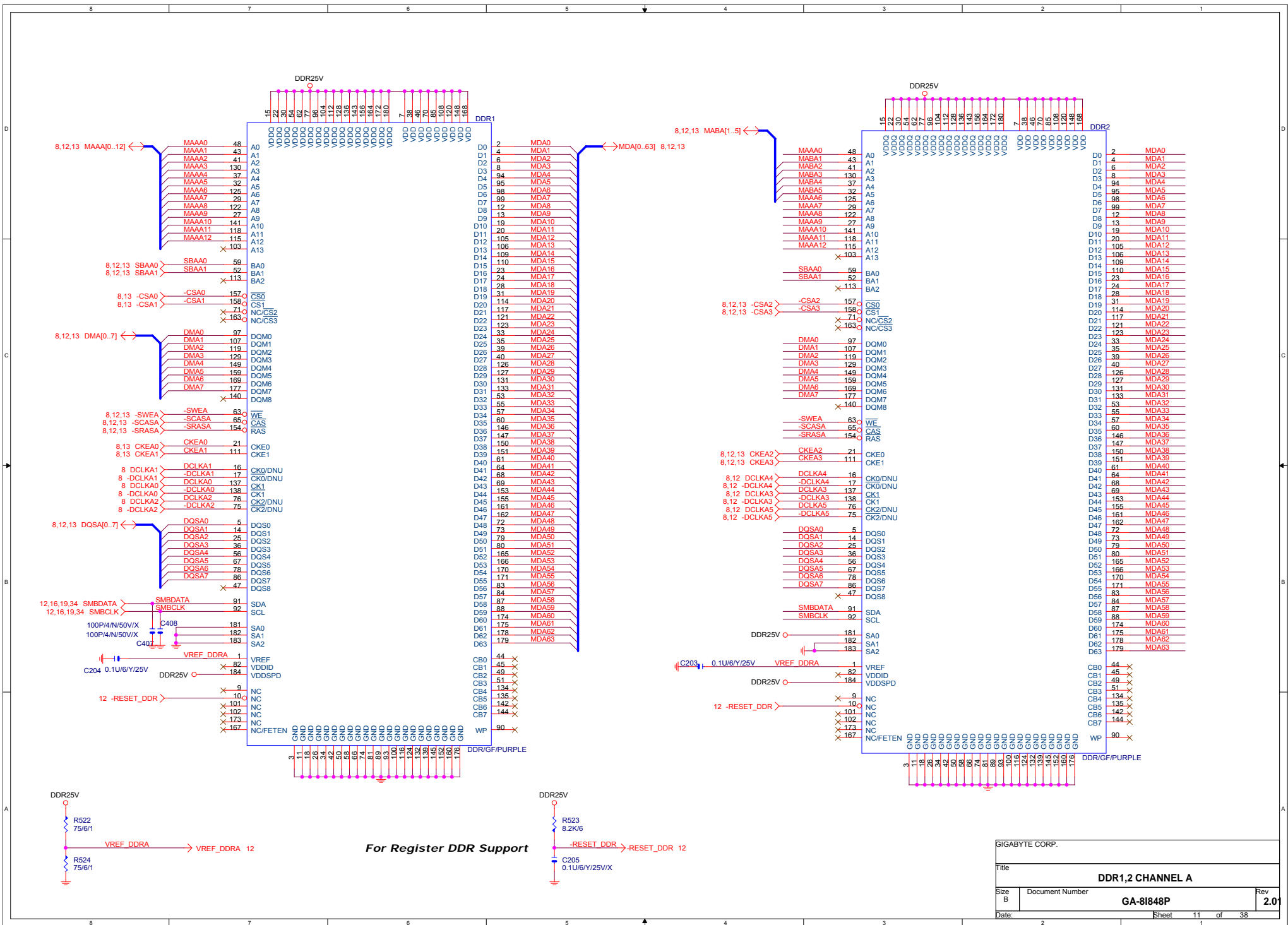
CLOSED TO MCH



Title		
SPRINGDALE AGP,HUB,CSA,VGA		
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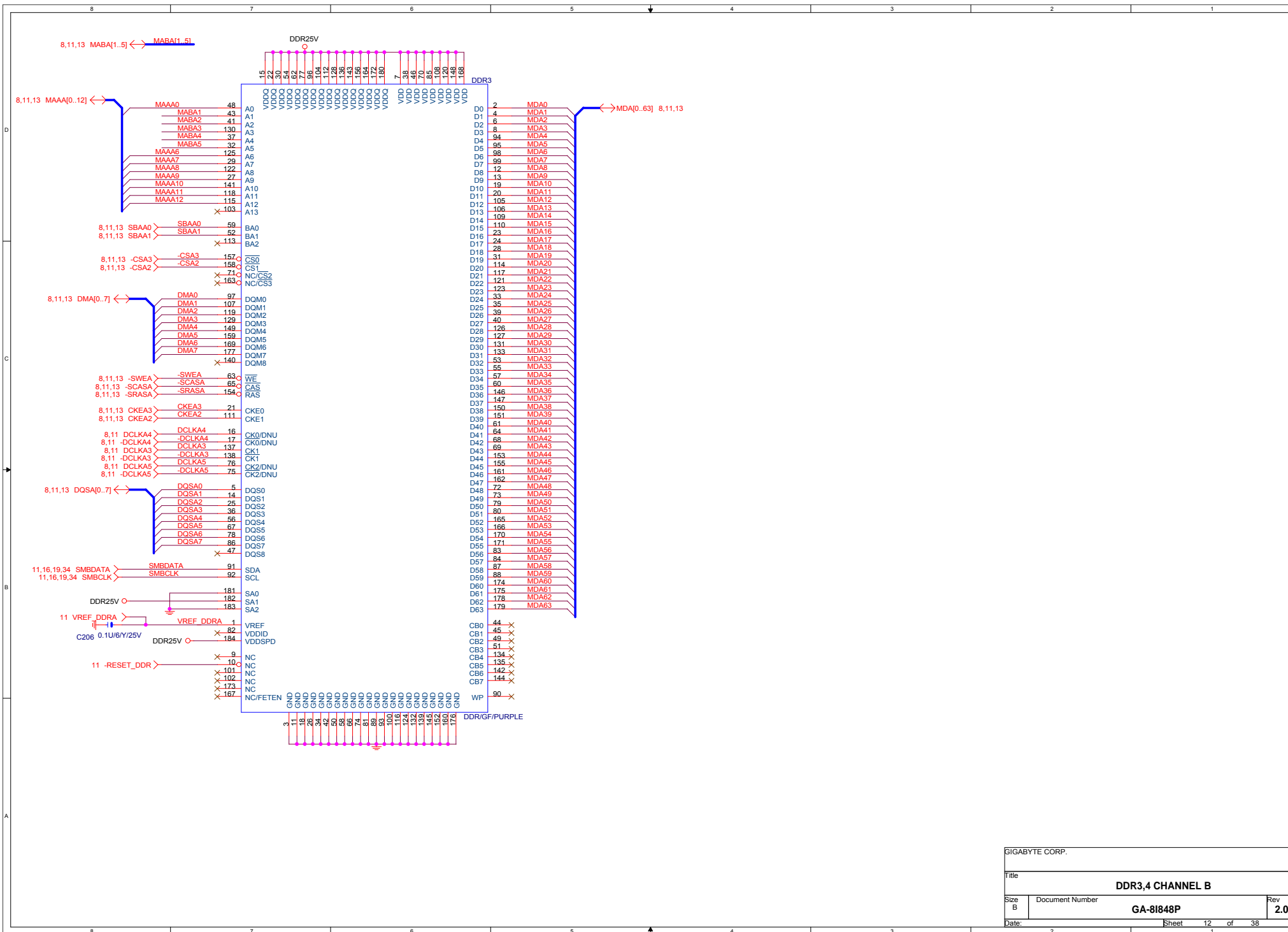


Title			
SPRINGDALE PWR			
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For Register DDR Support

SIGABYTE CORP.		
Title DDR1,2 CHANNEL A		
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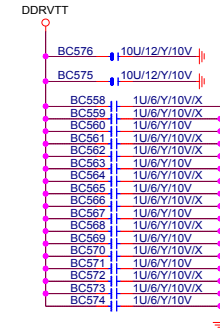
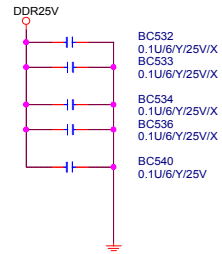
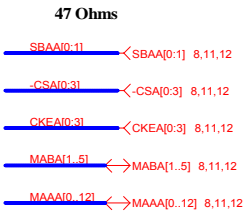
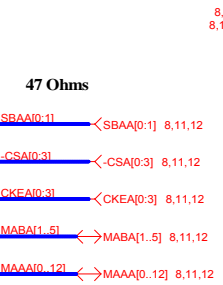
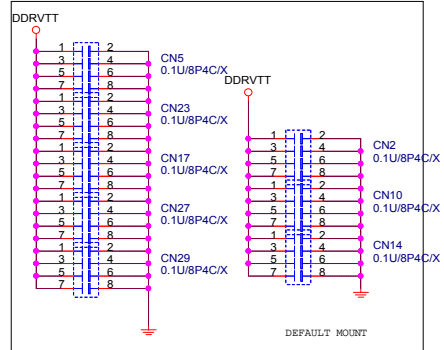
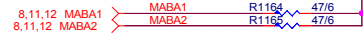
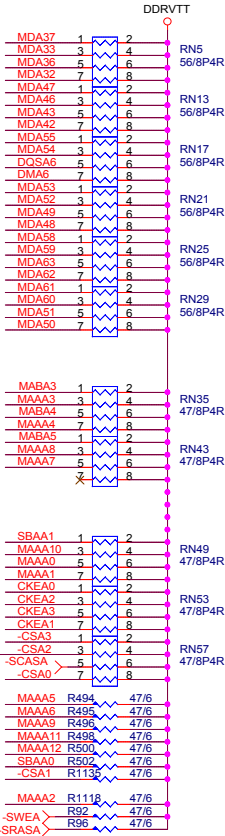
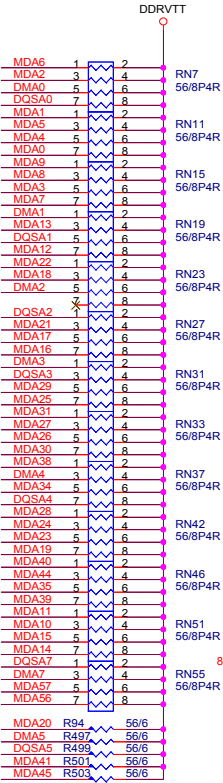
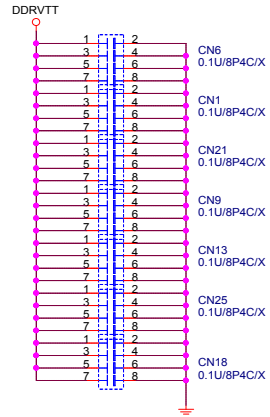


DDRVTT Decouple

DDR TERMINATION CHANNEL A

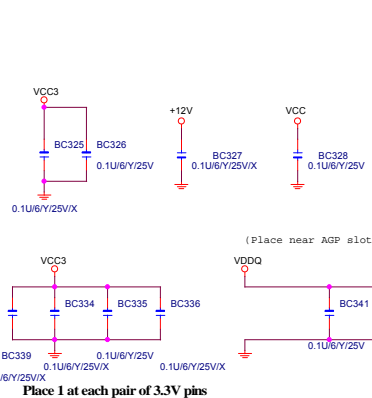
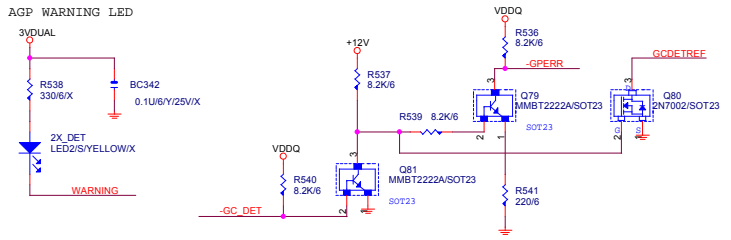
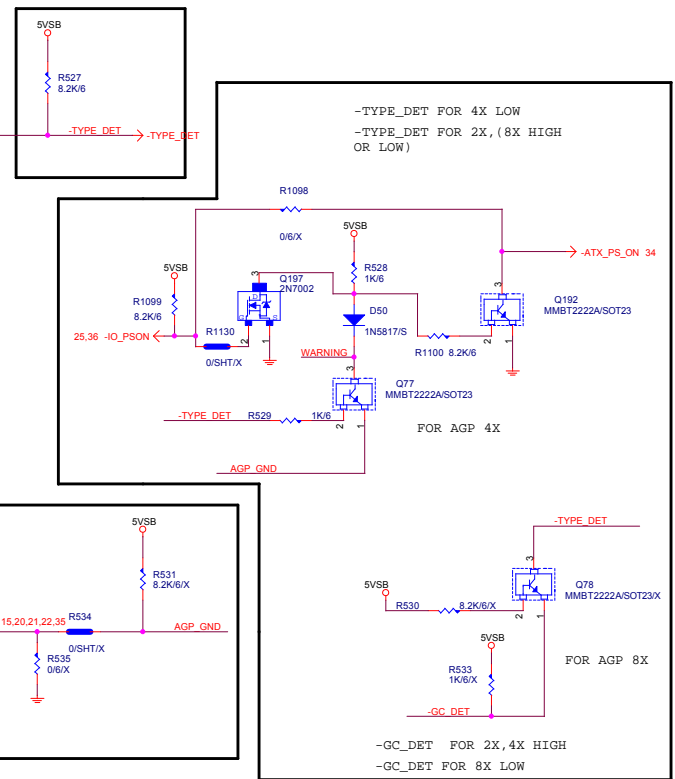
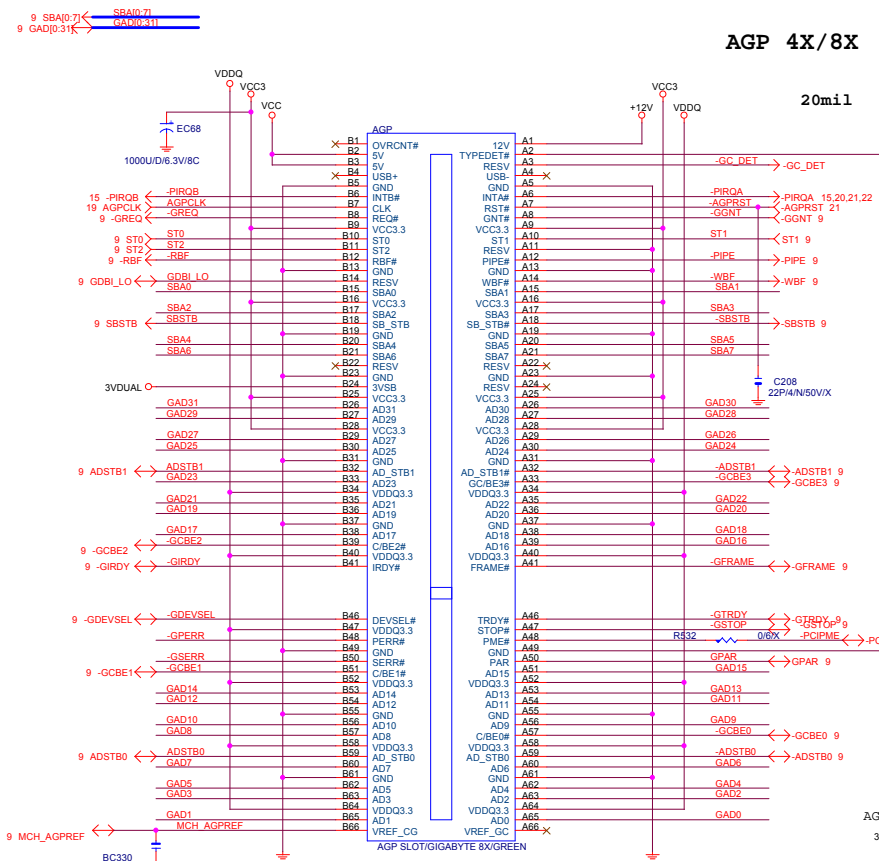
DDRVTT Decouple

CHANNEL B

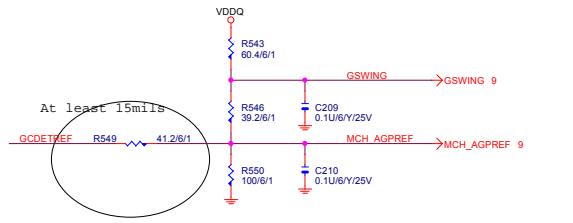


AGP 4X/8X

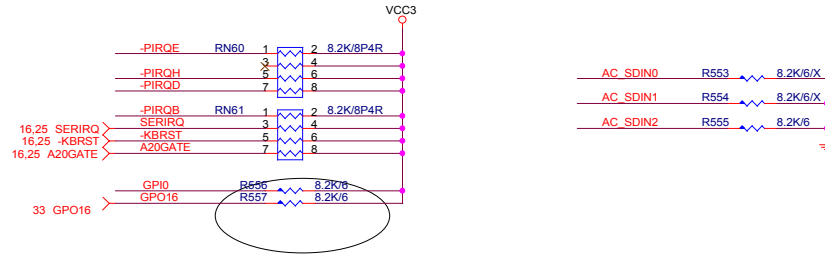
20mil



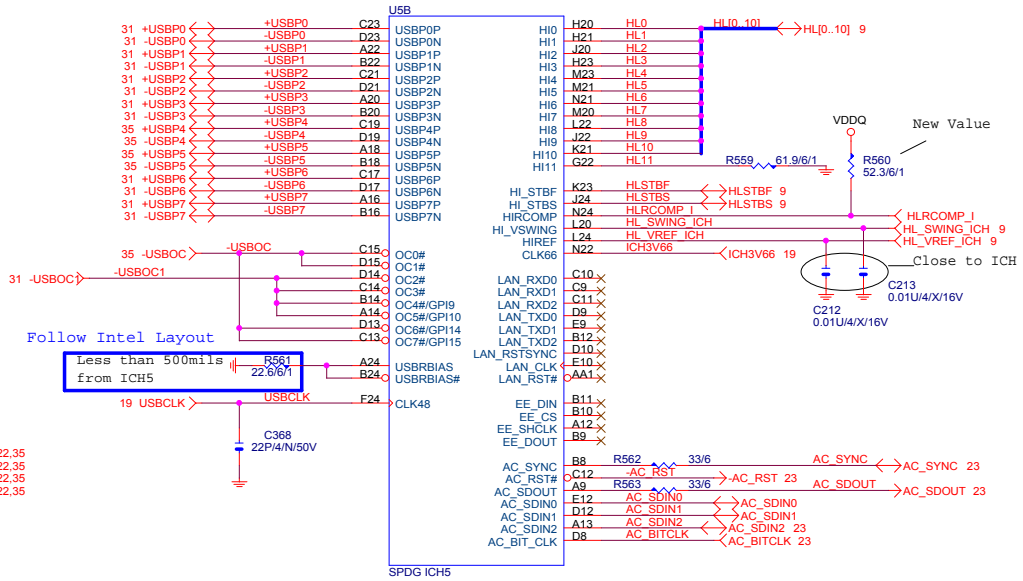
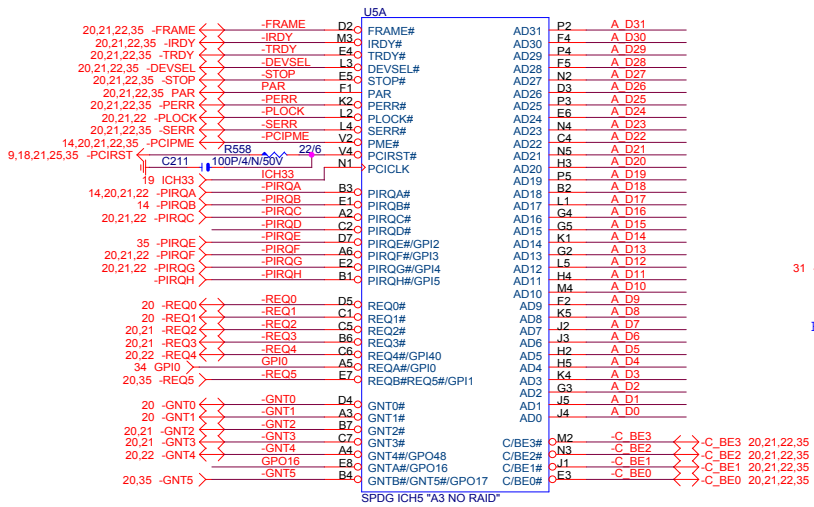
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33

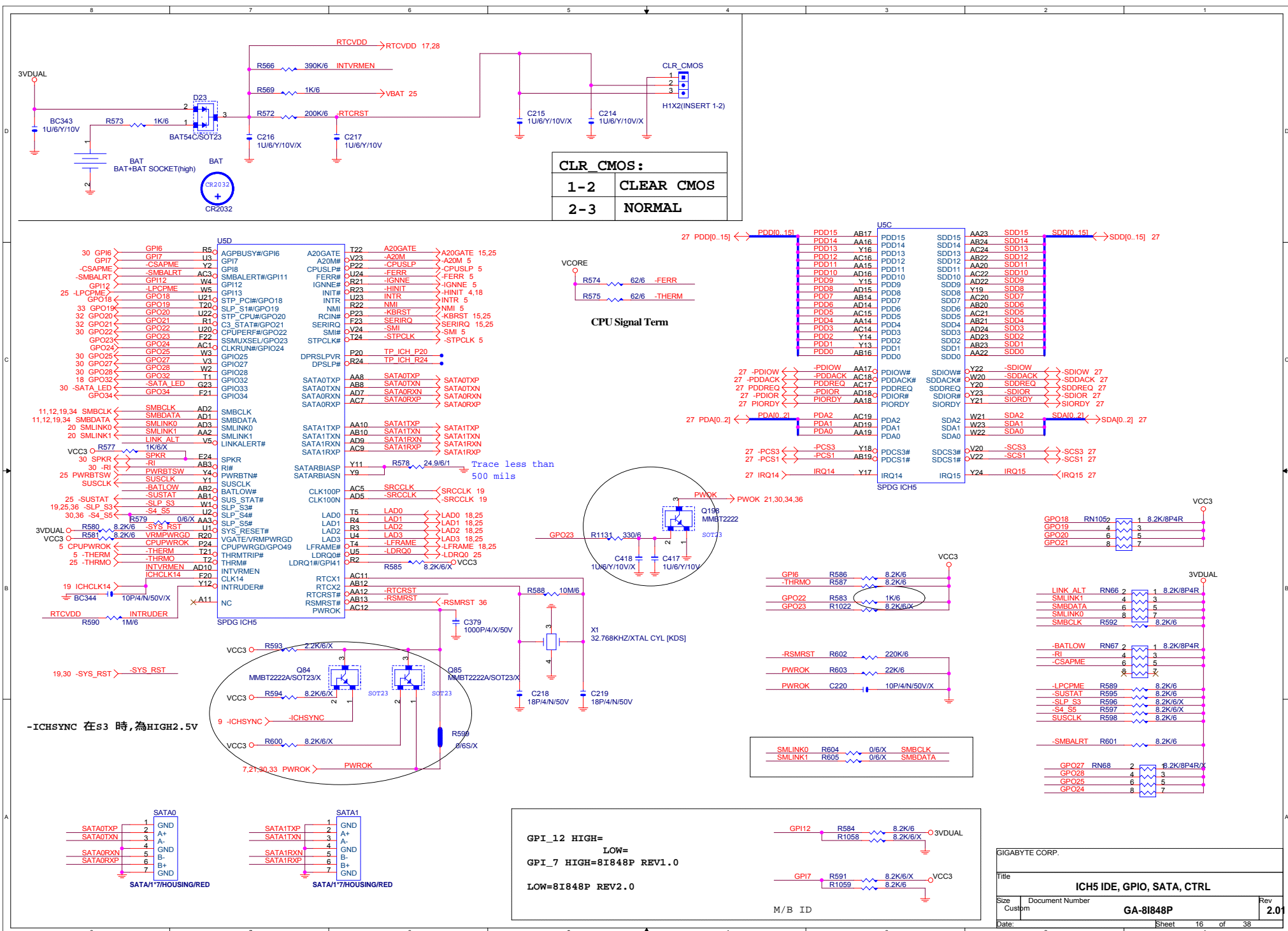


GIGABYTE CORP.		
AGP SLOT		
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A_D0_311 <-> A_D0_31] 20,21,22,35

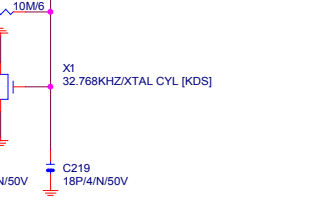
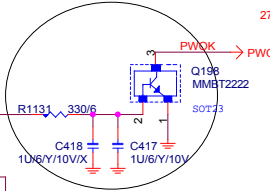
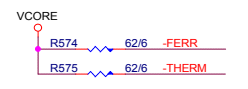




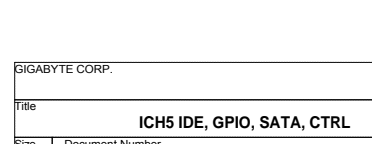
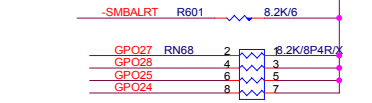
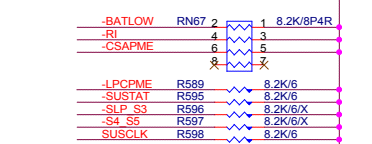
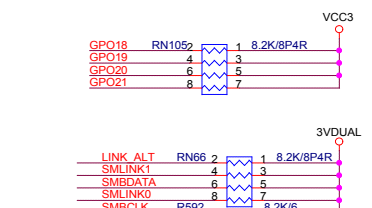
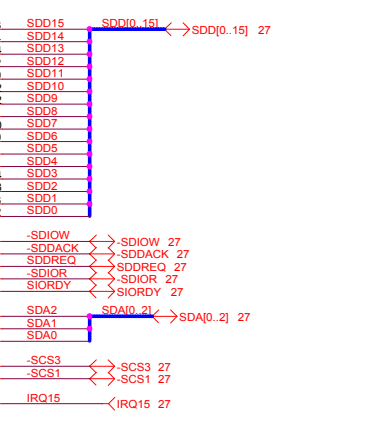
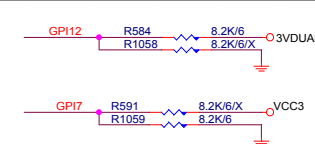
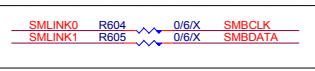
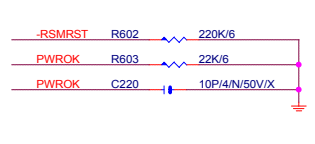
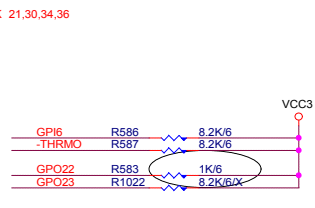
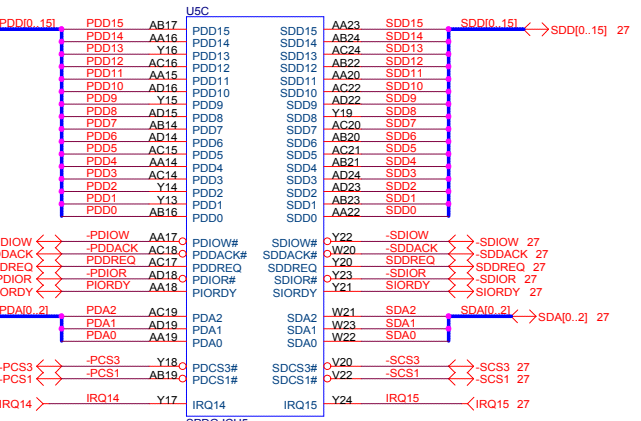
CLR_CMOS :

1-2	CLEAR CMOS
2-3	NORMAL

CPU Signal Term

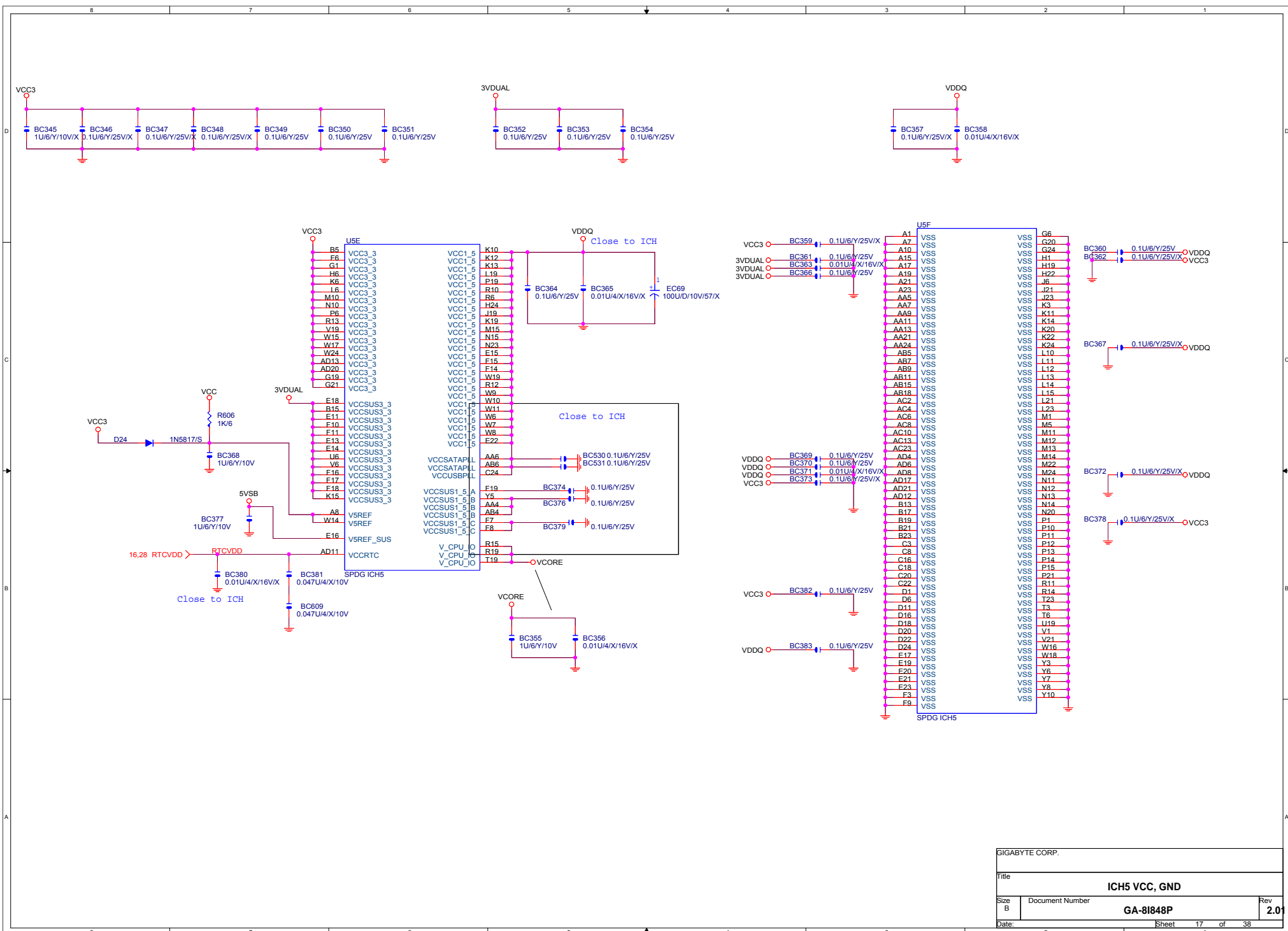


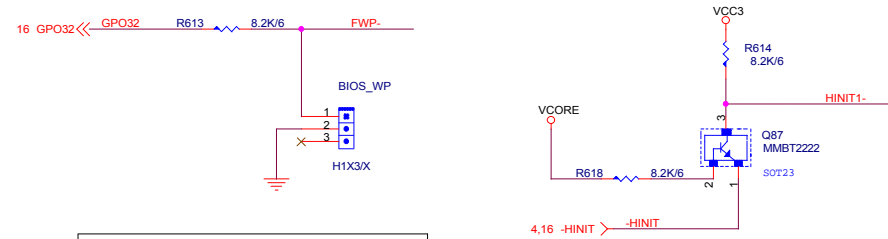
GPI_12 HIGH=
LOW=
GPI_7 HIGH=8I848P REV1.0
LOW=8I848P REV2.0



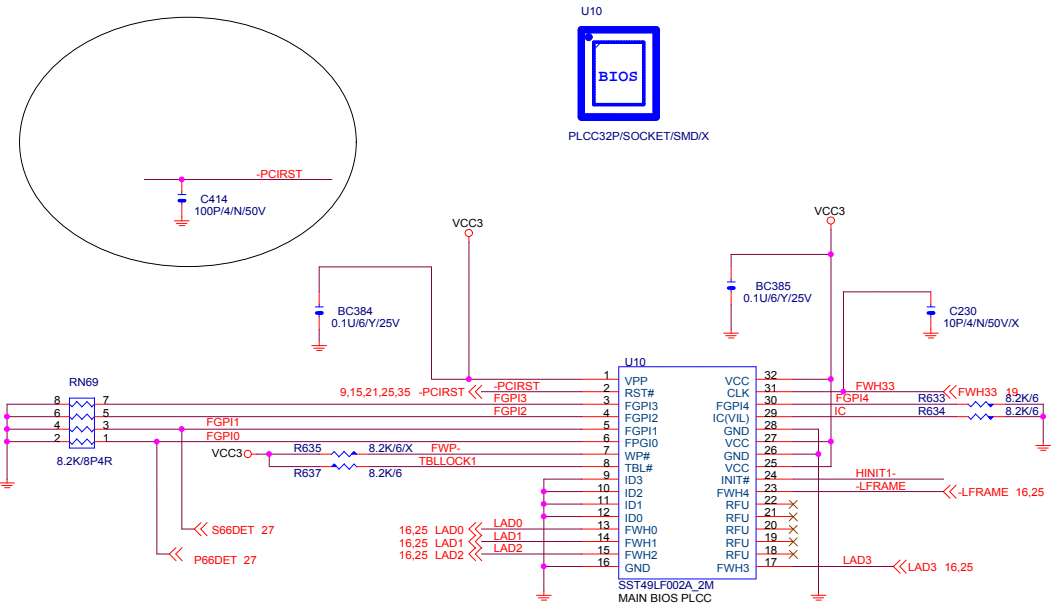
GIGABYTE CORP.

Title			
ICH5 IDE, GPIO, SATA, CTRL			
Size	Document Number	Rev	
Custom	GA-8I848P	2.01	
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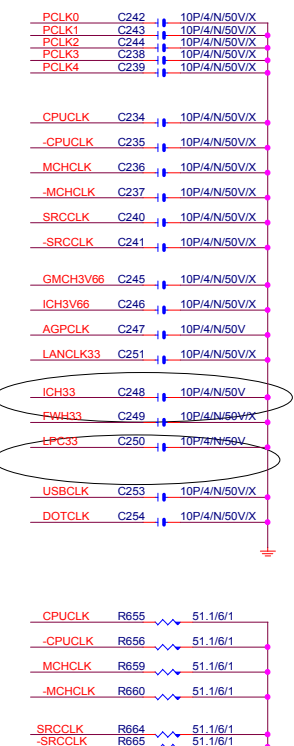
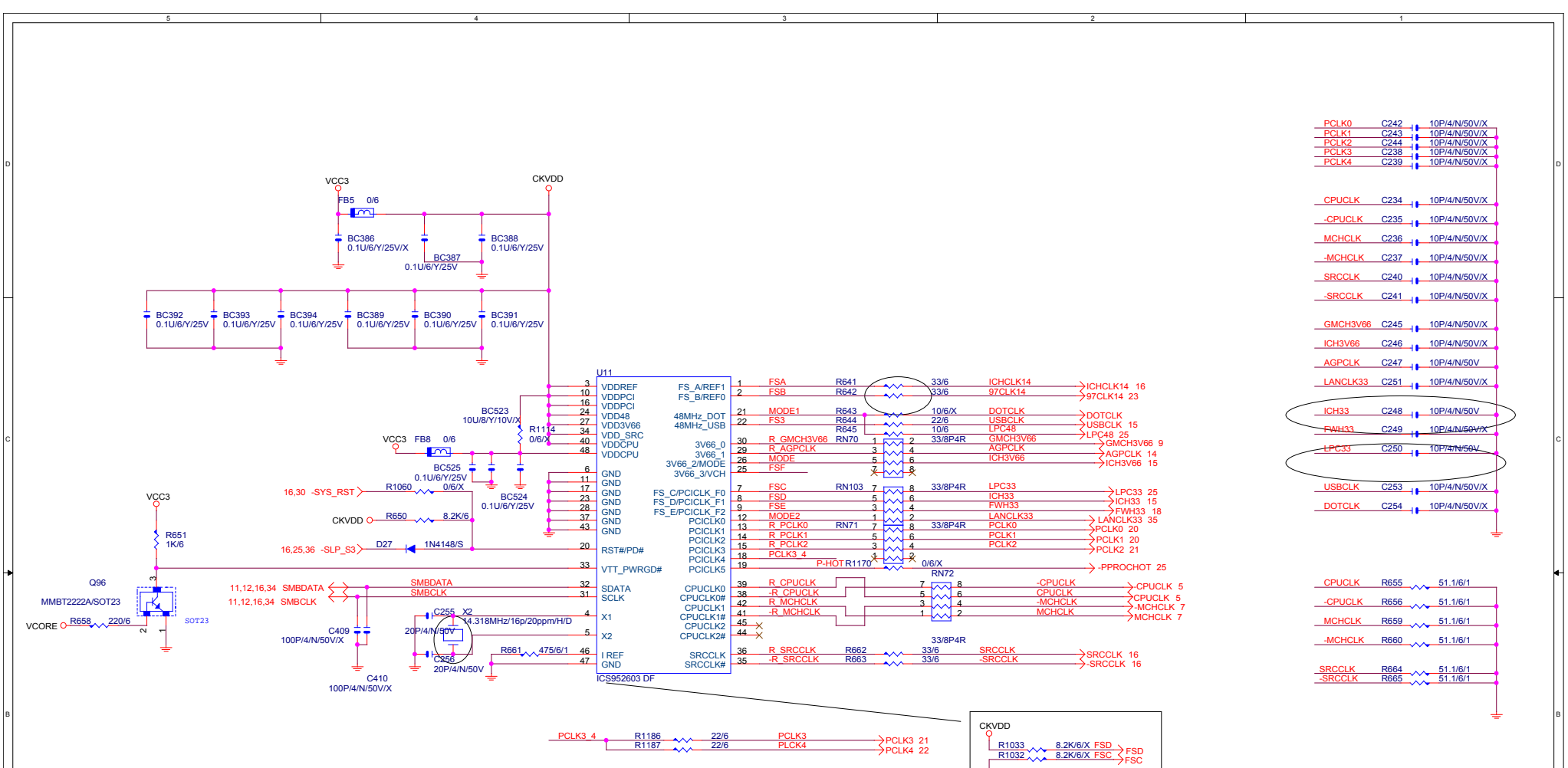


BIOS_WP :	
1-2	WRITE PROTECT
2-3	DISABLE



ADD WINBOUD FWH SEC. SOURCE

GIGABYTE CORP.		
Title		FWH
Size B	Document Number	GA-8I848P
Date:	星期二, 二月 16, 2004	Sheet 18 of 38
		Rev 2.01

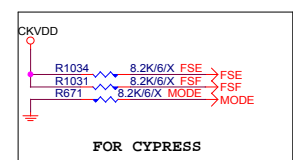
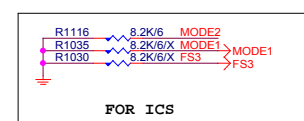
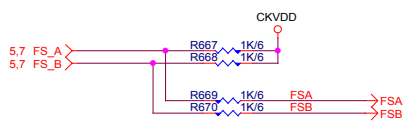
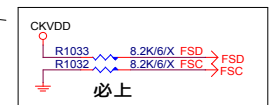
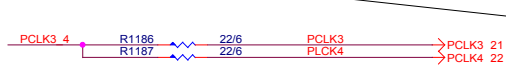


CYPRESS CY28405

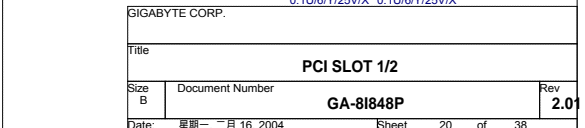
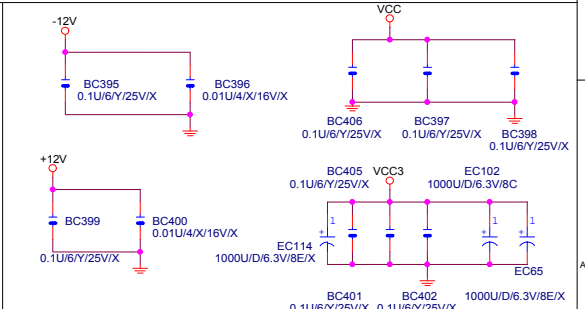
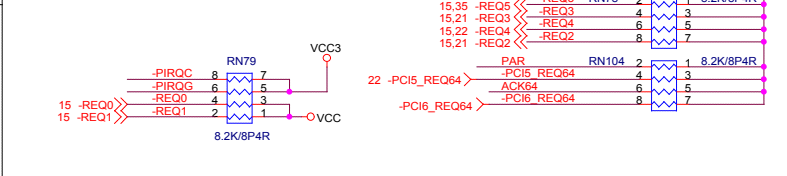
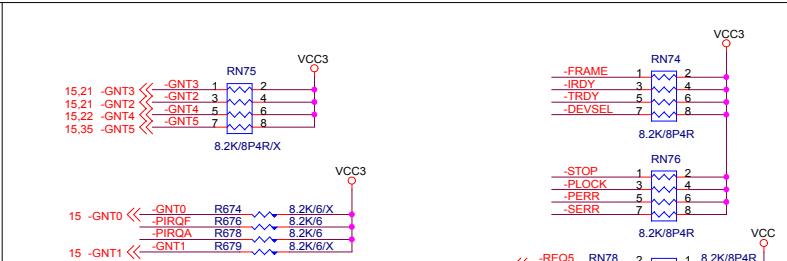
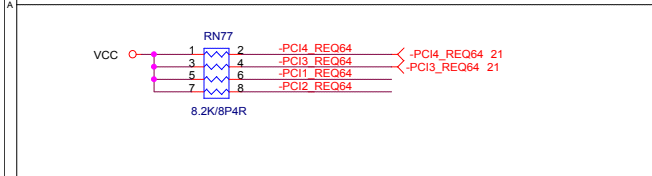
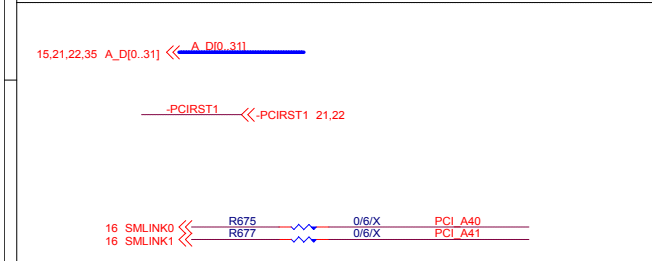
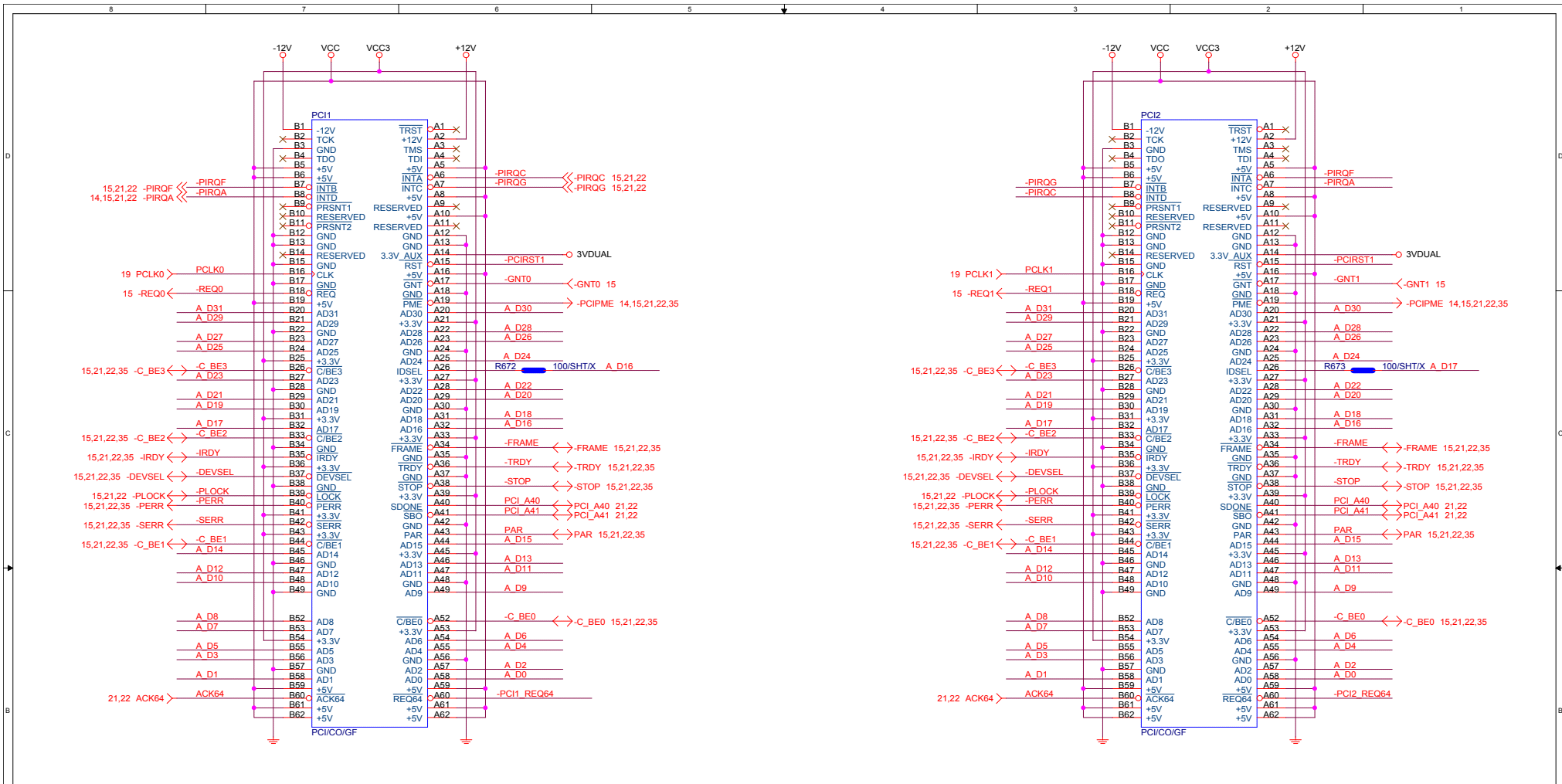
FS_E	FS_D	FS_C	FS_A	FS_B	Clock
1	1	0	0	0	100MHz
1	1	0	1	0	133MHz
1	1	0	1	1	166MHz
1	1	0	0	1	200MHz

ICS952603

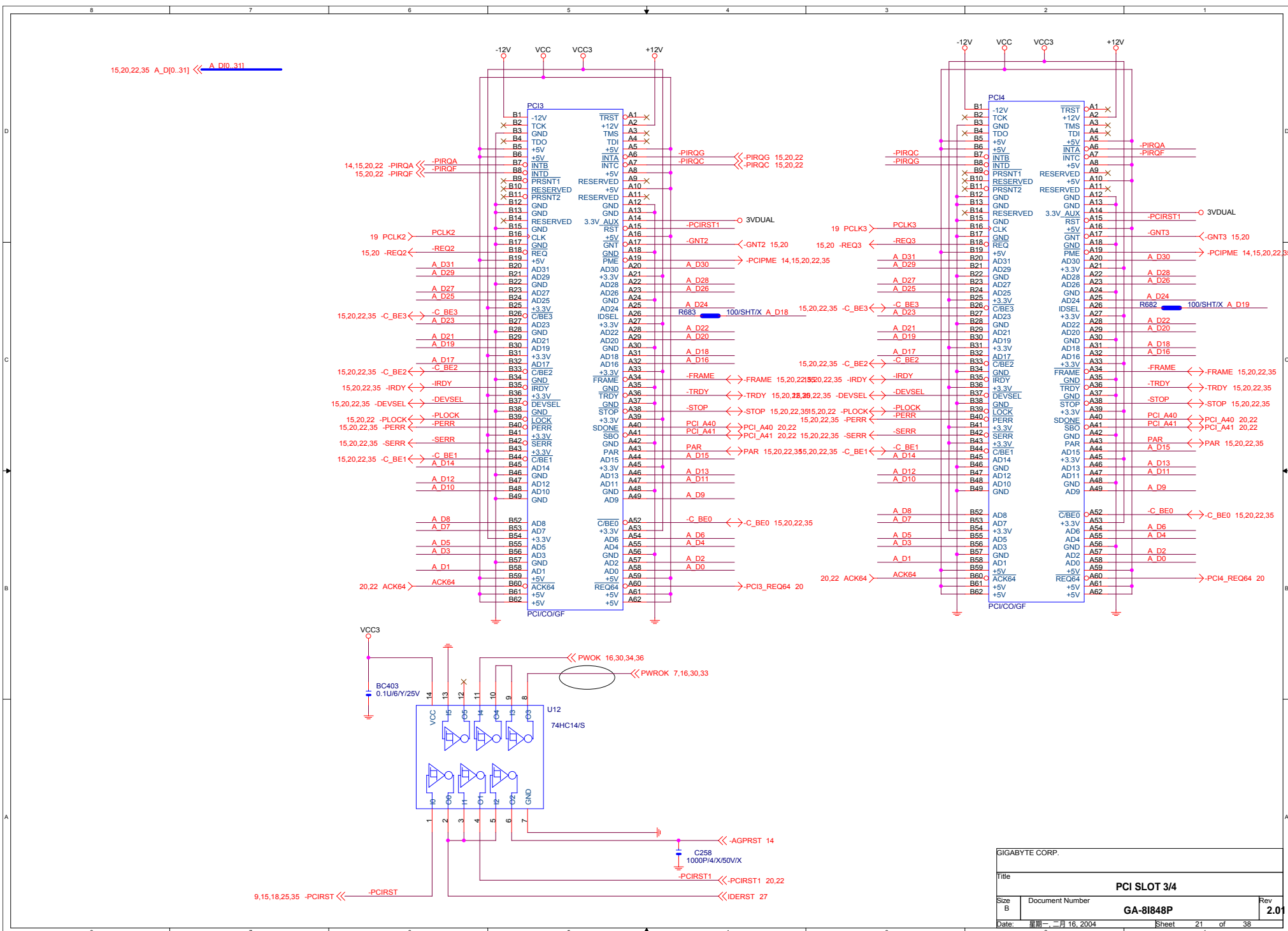
FS_D	FS_3	FS_C	FS_A	FS_B	Clock
1	0	0	0	0	100MHz
1	0	0	1	0	133MHz
1	0	0	1	1	166MHz
1	0	0	0	1	200MHz



CY28405 上 R1031,R1034,R671
 不上R1030,R1035
 ICS952616上R1030,R1035
 不上 R1031,R1034,R671

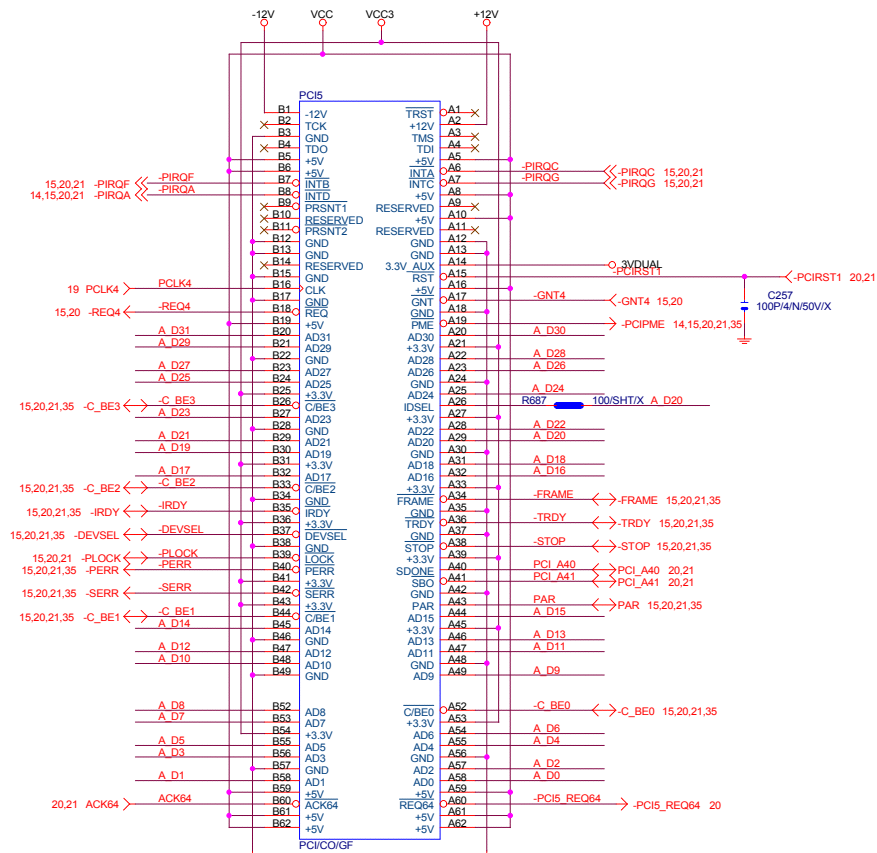


GIGABYTE CORP.			
Title			
PCI SLOT 1/2			
Size	Document Number		Rev
B	GA-81848P		2.01
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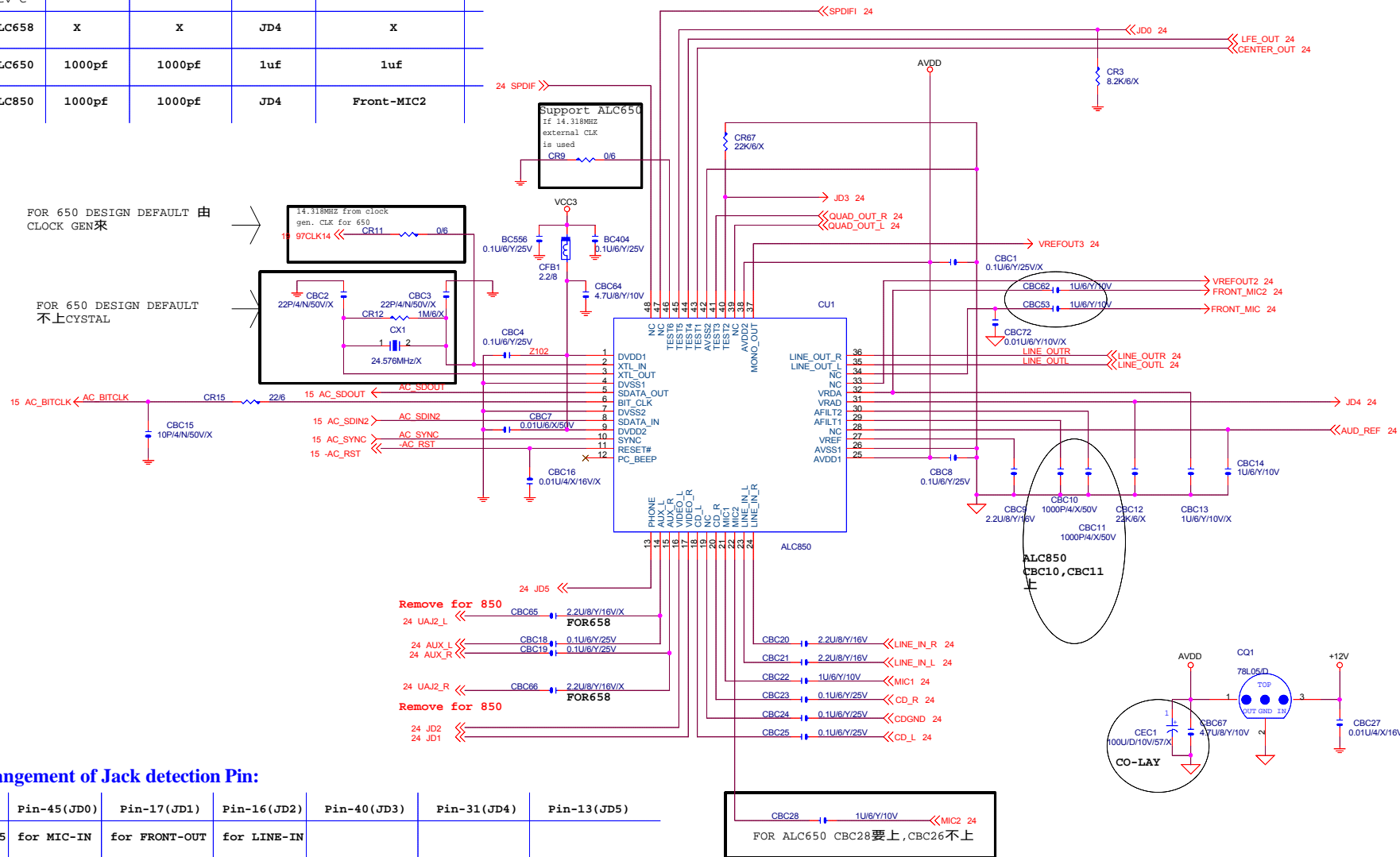
GIGABYTE CORP.		
Title		
PCI SLOT 3/4		
Size	Document Number	Rev
B	GA-81848P	2.01
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15,20,21,35 A_D[0..31] << A_D[0..31]



Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2

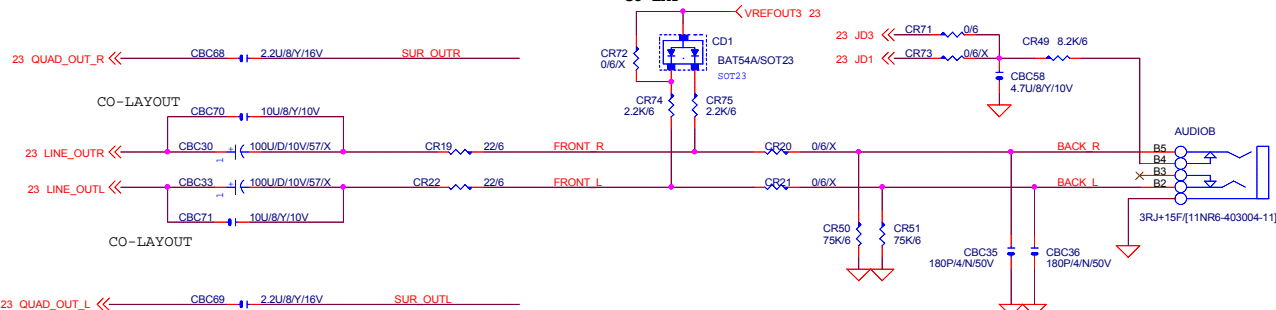


Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

LINE OUT

JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual) 1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



LINE OUT SENSING
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

2x5 header for 850

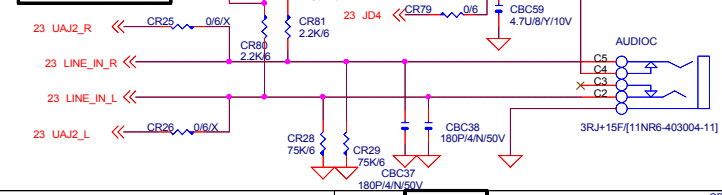
For 850 if JD5 = low AUX-In is configured as input
 For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

For 850 AUX-In is shared to Surr-Back out

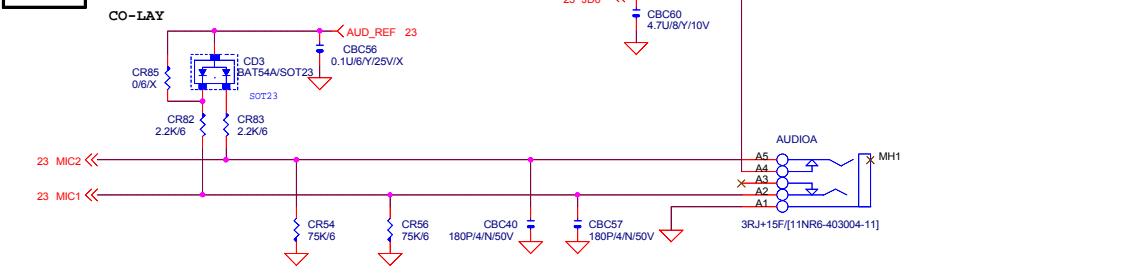
LINE IN SENSING (當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

LINE IN SENSING (當INPUT)
 swing of input signal>-40dbv(10mv)==>line in device active
 swing of input signal<-40dbv(10mv)==>unknown line in device

LINE-IN



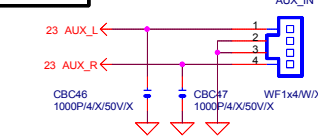
MIC



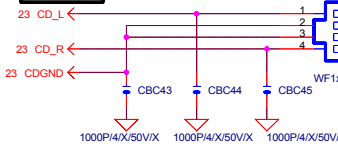
MICROPHONE IN SENSING (當INPUT) (利用vref 偏壓 與CR43,CR32 並聯求出阻抗)
 7.1k ohm>R>2.3k ohm==>microphone in
 R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING (當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

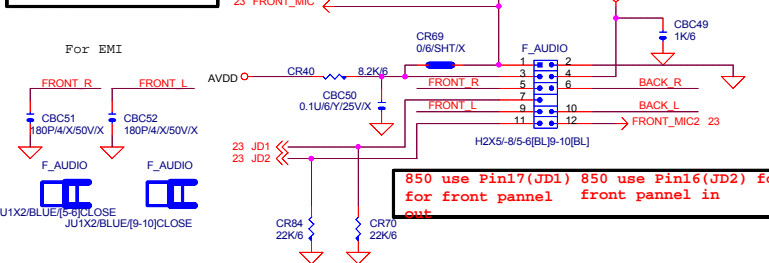
AUX IN DEFAULT NO POP



CD IN

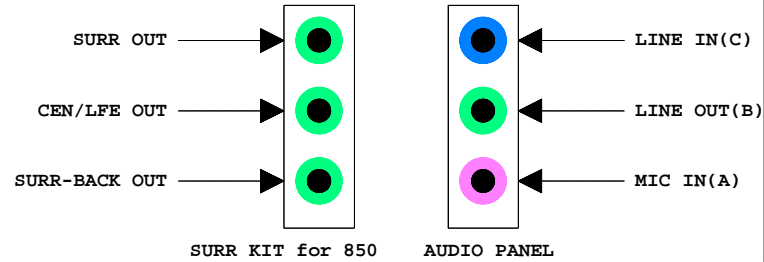
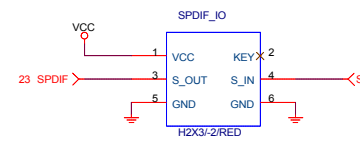


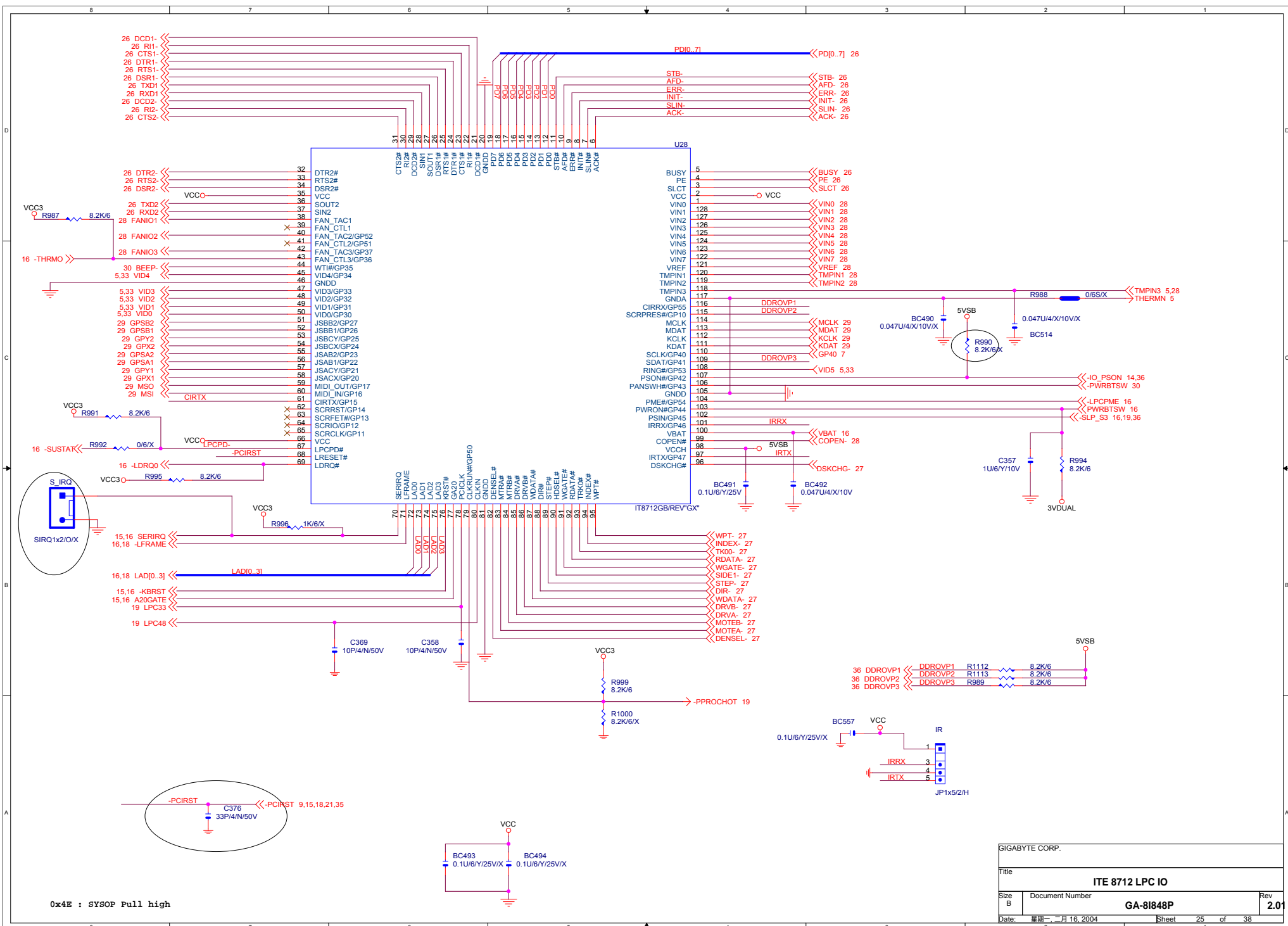
INTEL FRONT AUDIO



850 use Pin17(JD1) 850 use Pin16(JD2) for front panel front panel in out

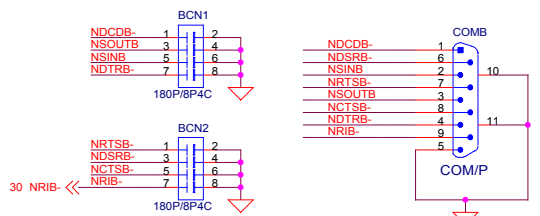
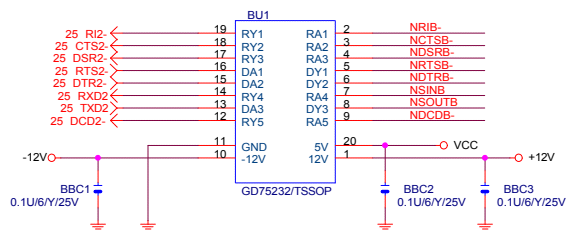
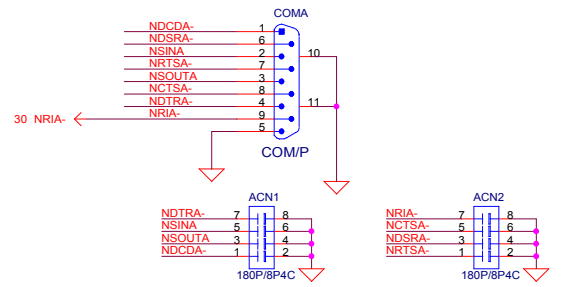
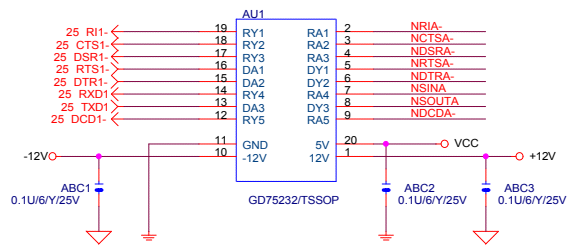
SPDIF_IO





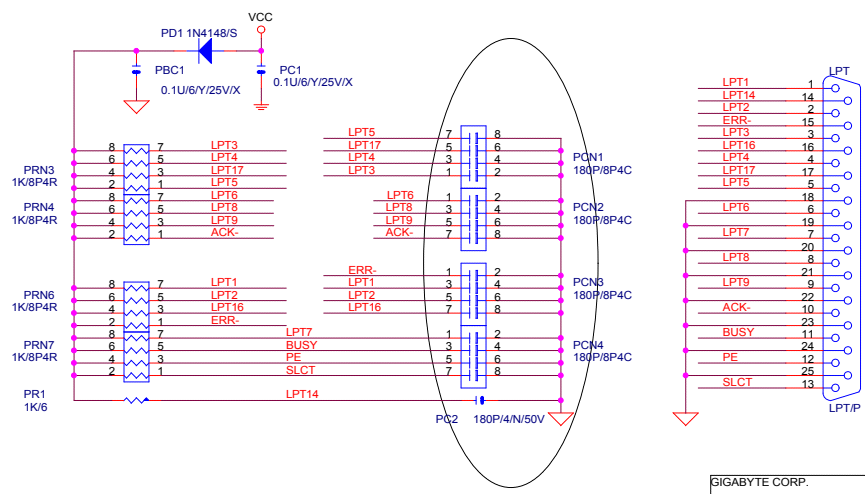
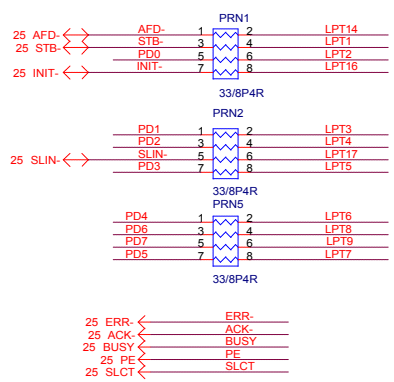
0x4E : SYSOP Pull high

SIGABYTE CORP.		
Title		
ITE 8712 LPC IO		
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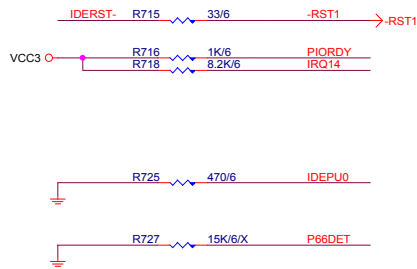
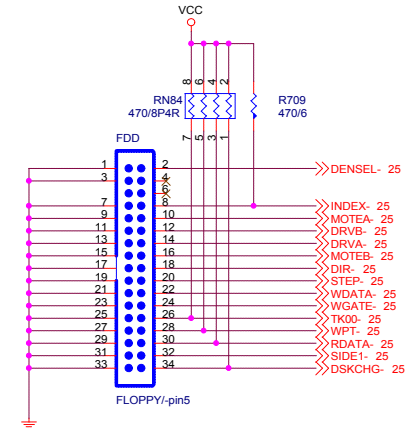
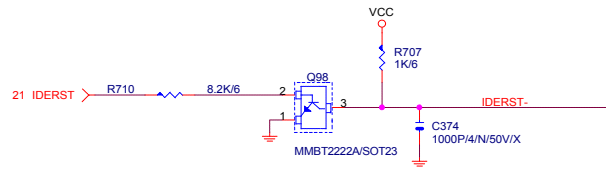


PLACE NEAR VGA_COM CONNECTOR

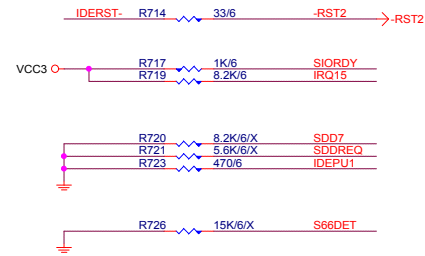
25 PD[0..7] ↔ PD[0..7]



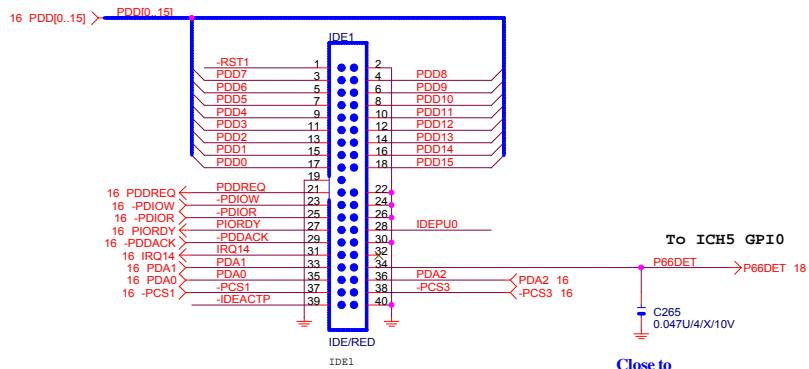
SIGABYTE CORP.		
Title		
COM & IR & LPT PORT & FLOOPY		
Size	Document Number	Rev
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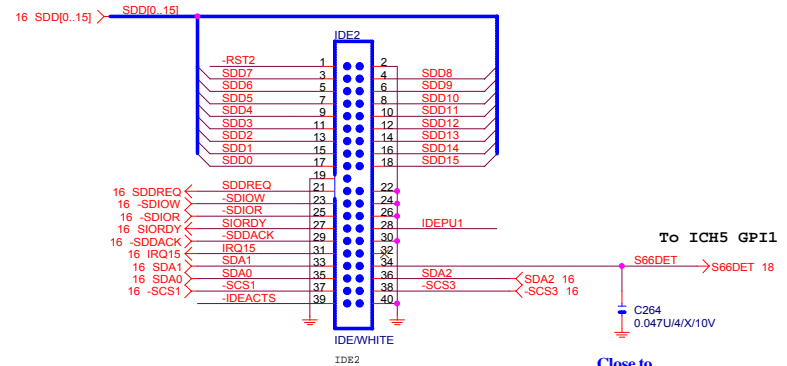
PRIMARY IDE CONNECTOR



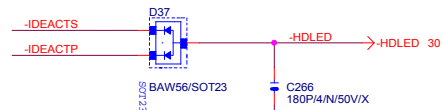
SECONDARY IDE CONNECTOR



Close to connector

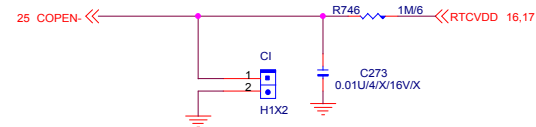
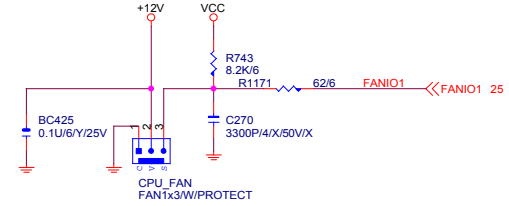
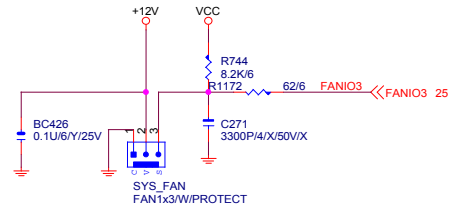
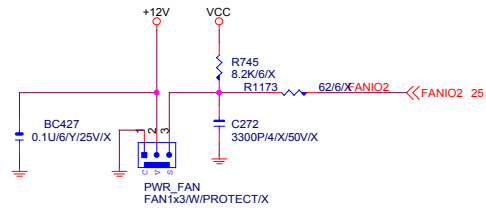
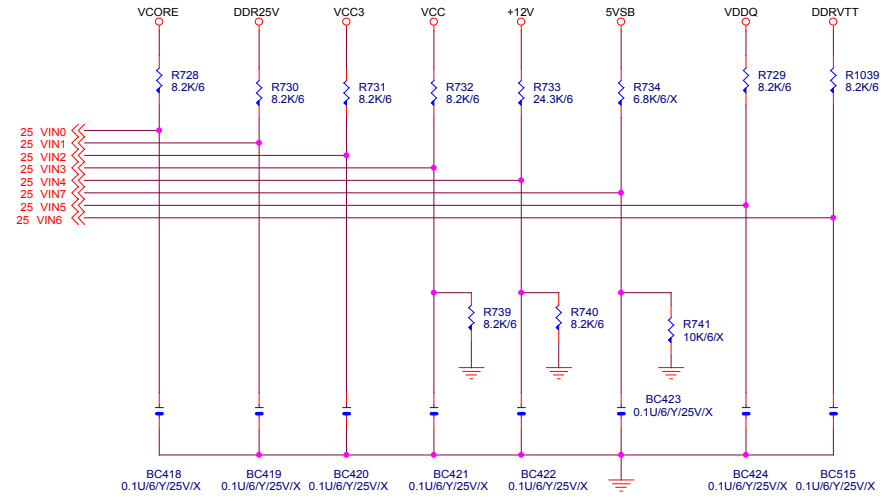
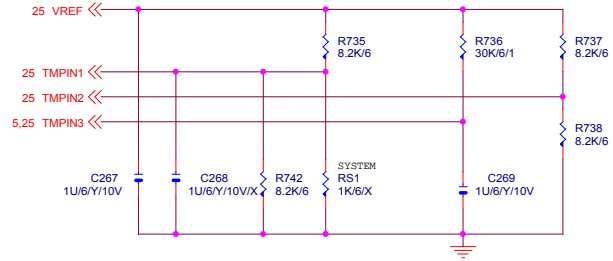


Close to connector

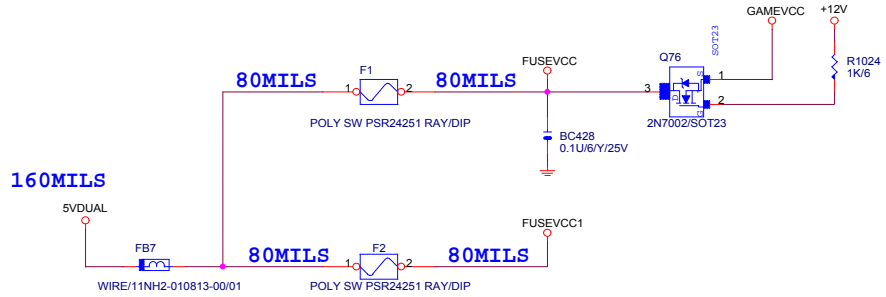


GIGABYTE CORP.		
Title		
IDE CONNECTOR		
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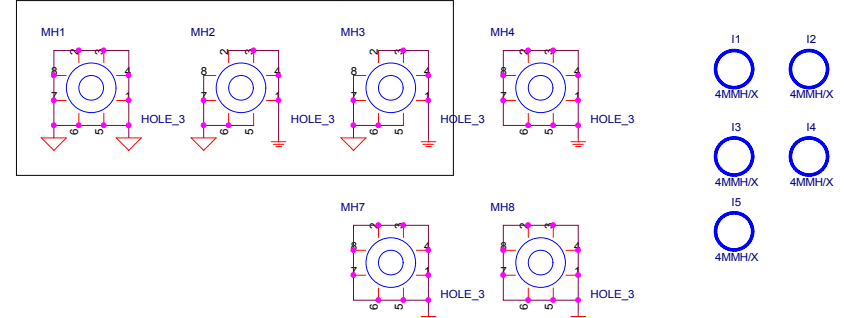
Hardware Monitor circuits



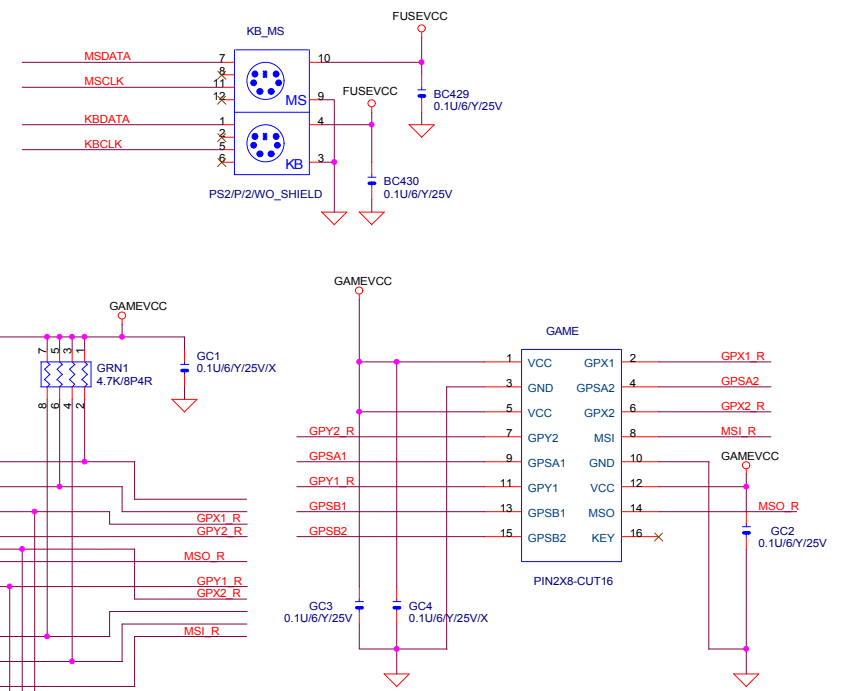
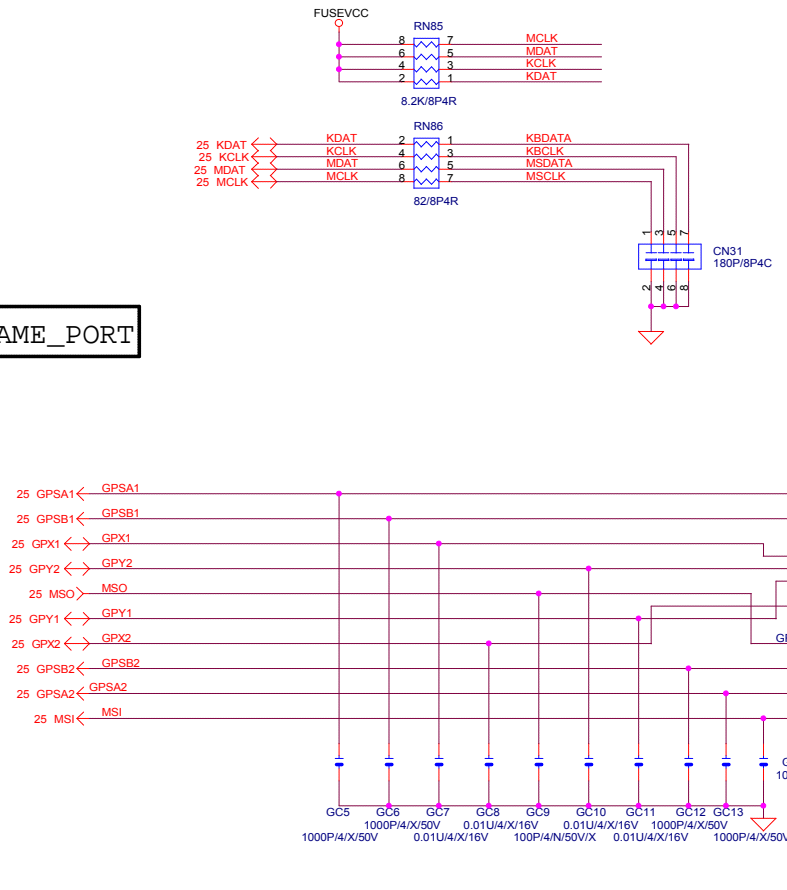
SIGABYTE CORP.		
Title		
FAN/HWMO		
Size B	Document Number GA-81848P	Rev 2.01
Date: 星期一, 二月 16, 2004	Sheet 28	of 38



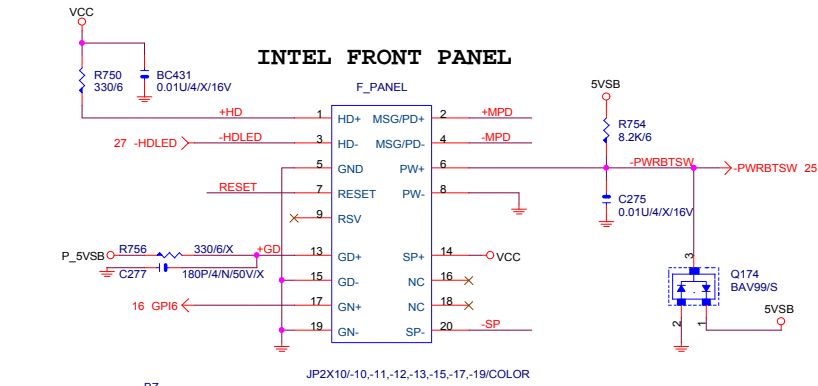
ATX AGND 與 GND 切割必須有三個



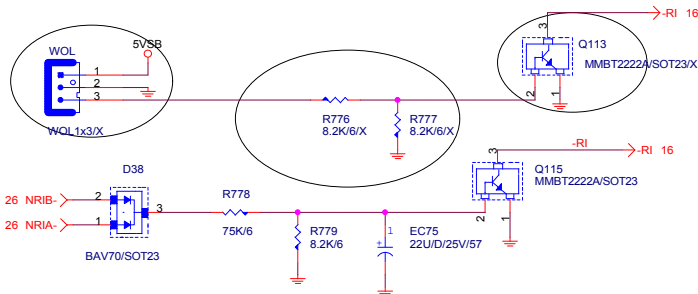
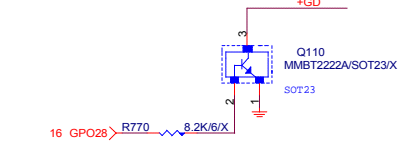
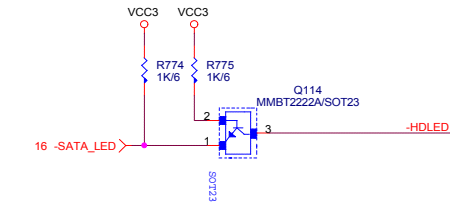
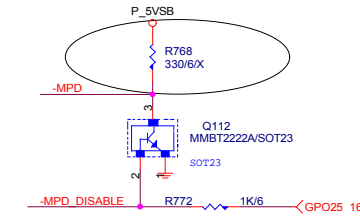
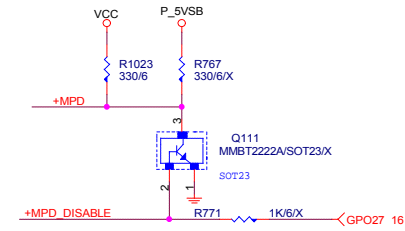
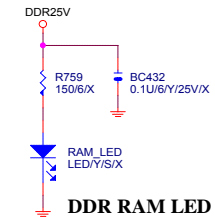
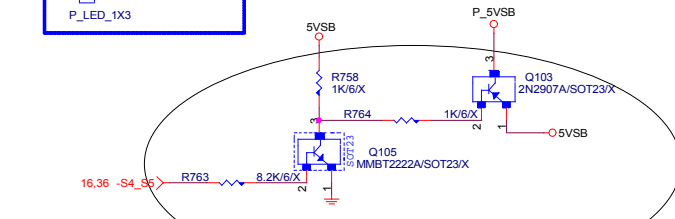
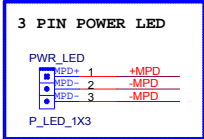
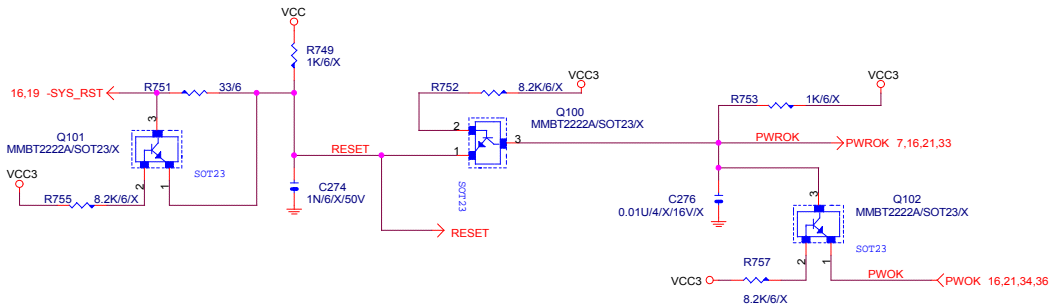
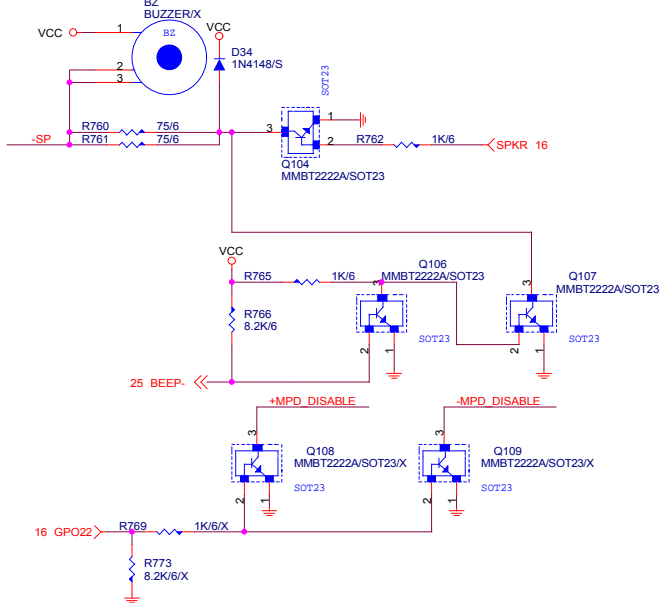
GAME_PORT



INTEL FRONT PANEL

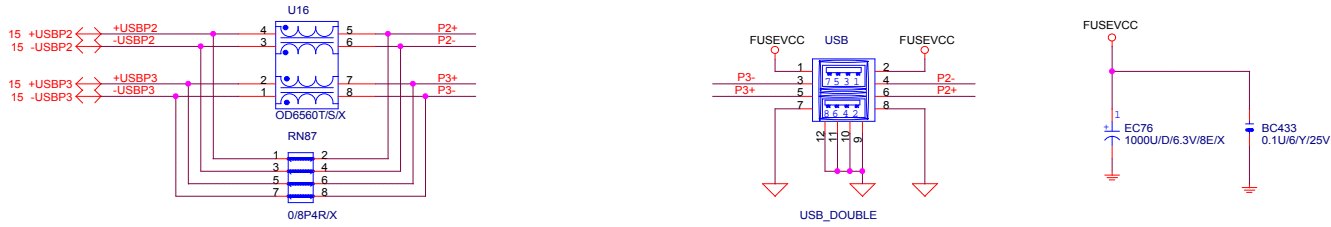


JP2X10/-10,-11,-12,-13,-15,-17,-19/COLOR

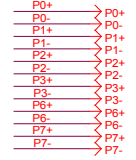
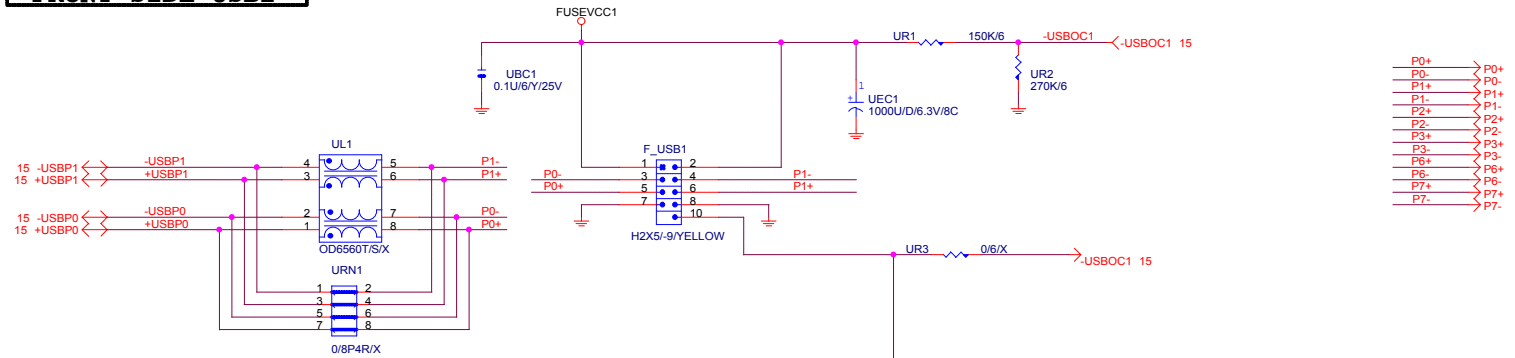


GIGABYTE CORP.		
Title		
PANEL & STR LED & RI		
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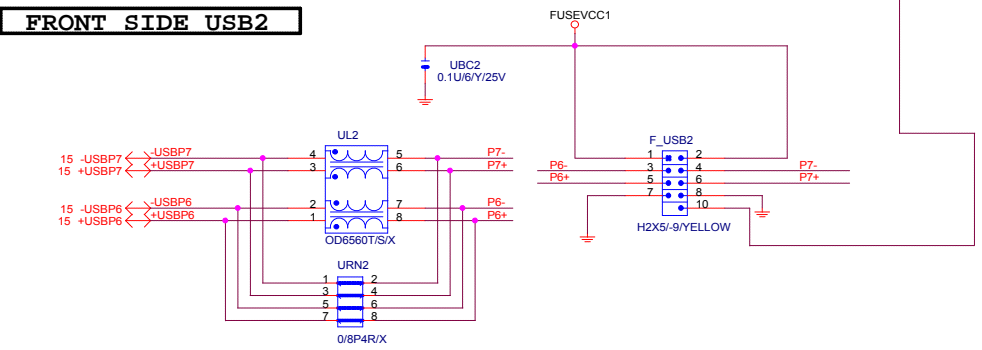
REAR USB



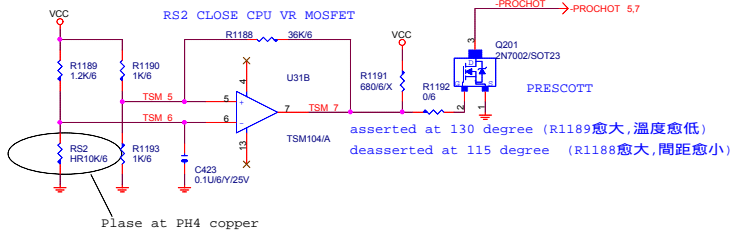
FRONT SIDE USB1



FRONT SIDE USB2

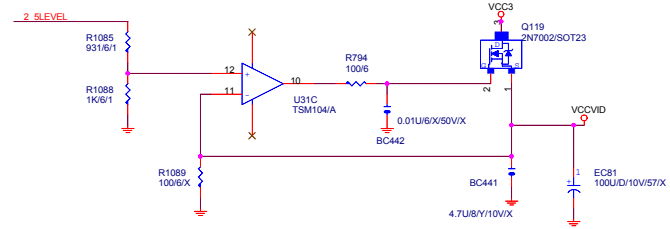
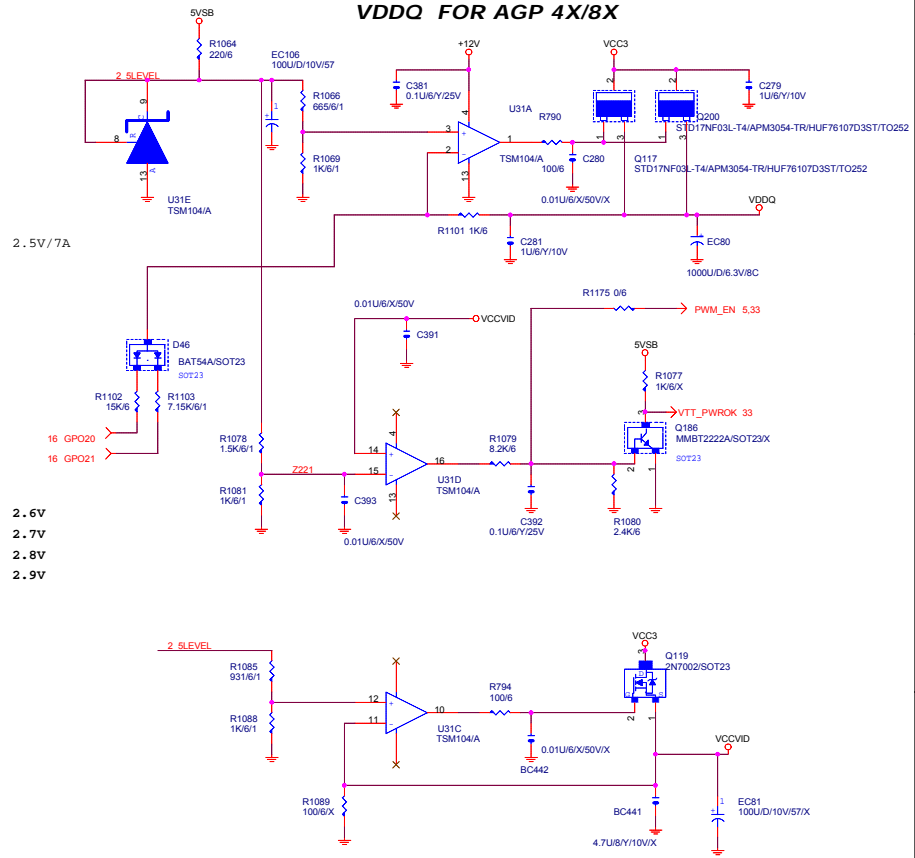


DDR25V FOR DDR DIMM & NB

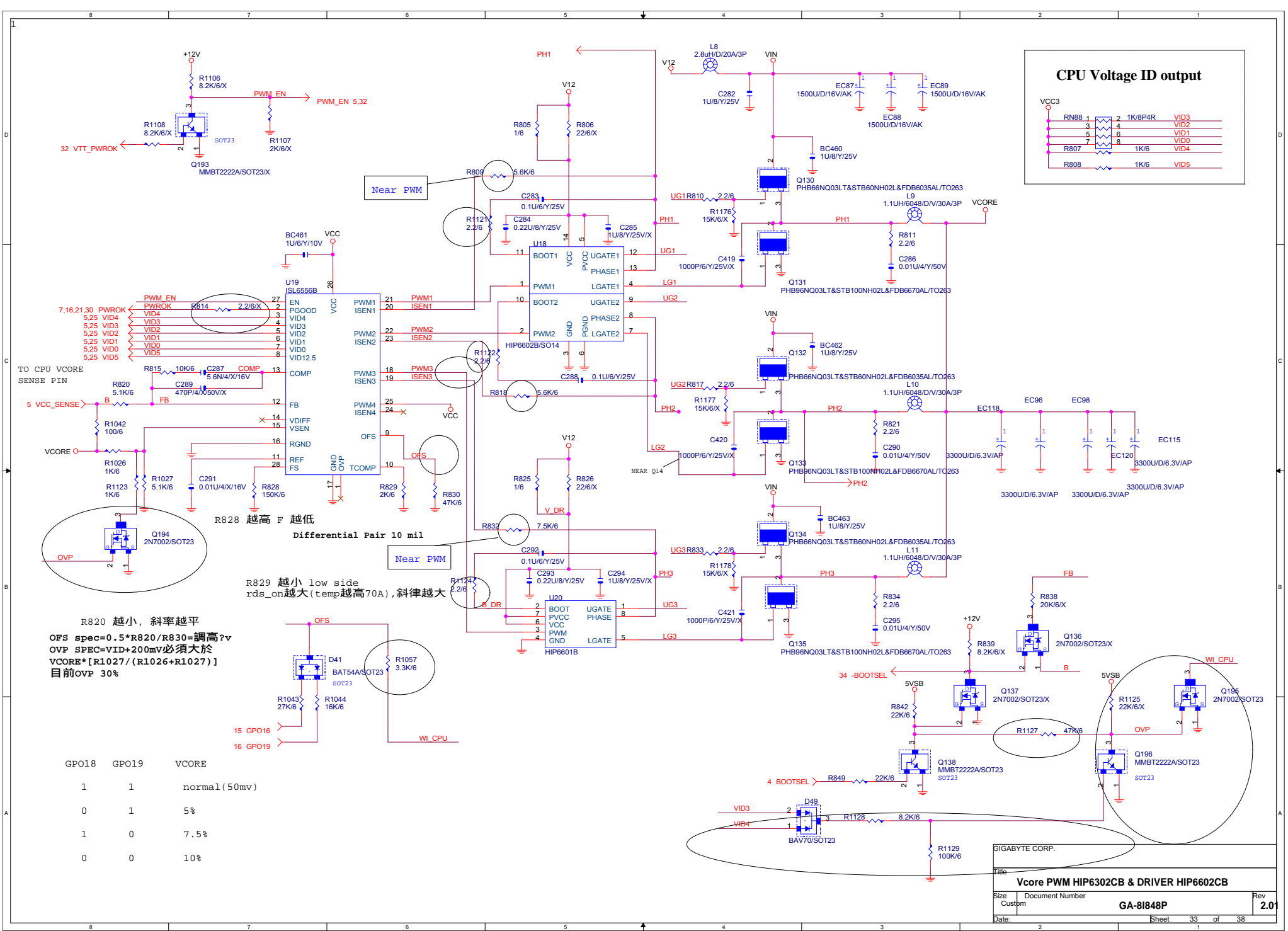
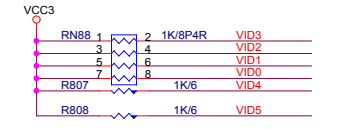


DDROVP1	DDROVP2	
1	1	2.6V
0	1	2.7V
1	0	2.8V
0	0	2.9V

VDDQ FOR AGP 4X/8X



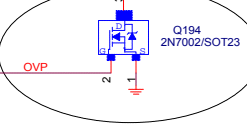
CPU Voltage ID output



7.16,21,30 PWROK
5.25 VID4
5.25 VID3
5.25 VID2
5.25 VID1
5.25 VID0
5.25 VID5

TO CPU Vcore
SENSE PIN
5 VCC_SENSE

Vcore
R1026 1K/6
R1027 5.1K/6
R1123 1K/6
R820 5.1K/6
R815 10K/6
R828 越高 F 越低

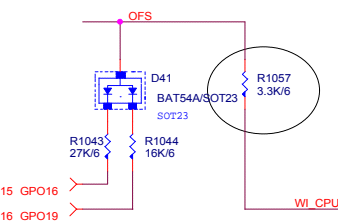


R820 越小, 斜率越平
OFS spec=0.5*R820/R830=調高?V
OVP SPEC=VID+200mV必須大於
Vcore*[R1027/(R1026+R1027)]
目前OVP 30%

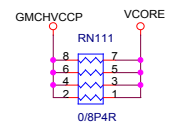
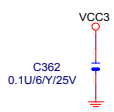
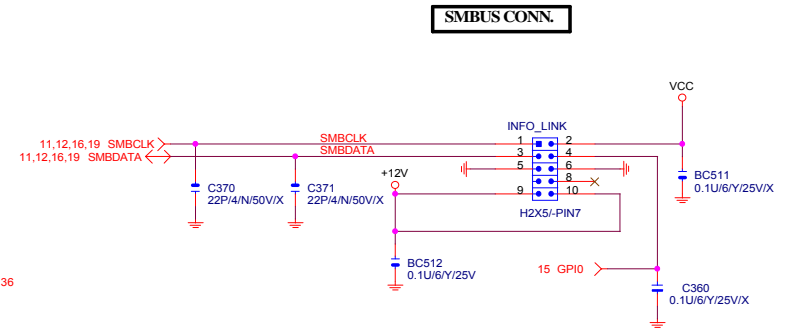
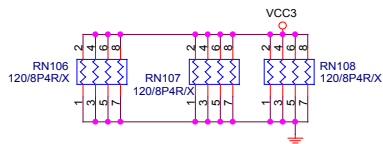
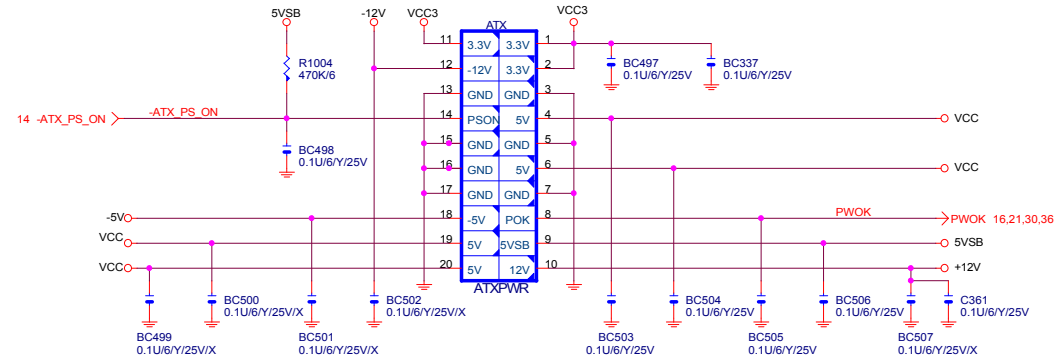
GPO18	GPO19	Vcore
1	1	normal (50mv)
0	1	5%
1	0	7.5%
0	0	10%

Differential Pair 10 mil

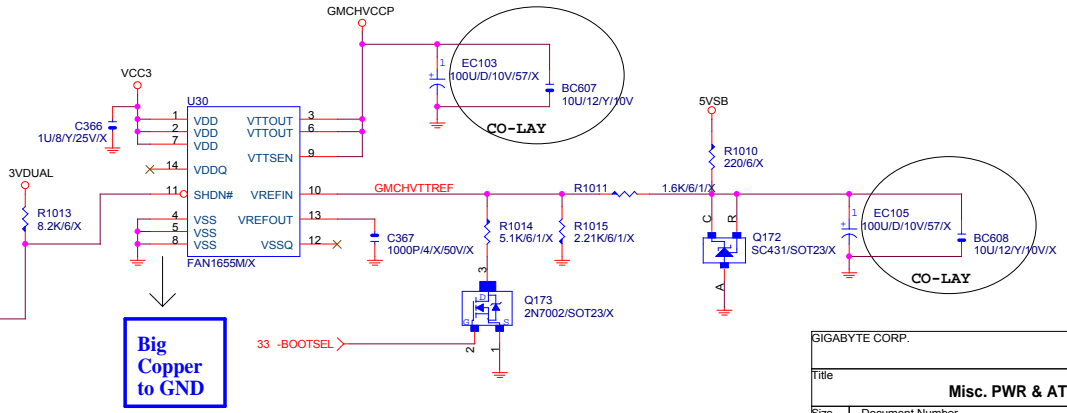
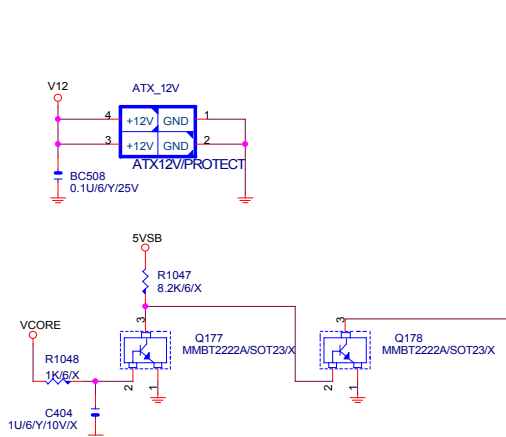
R829 越小 low side
rds_on 越大 (temp 越高 70A), 斜率越大



ATX POWER CONNECTOR



Northwood:+1.45V
Prescott:+1.225V

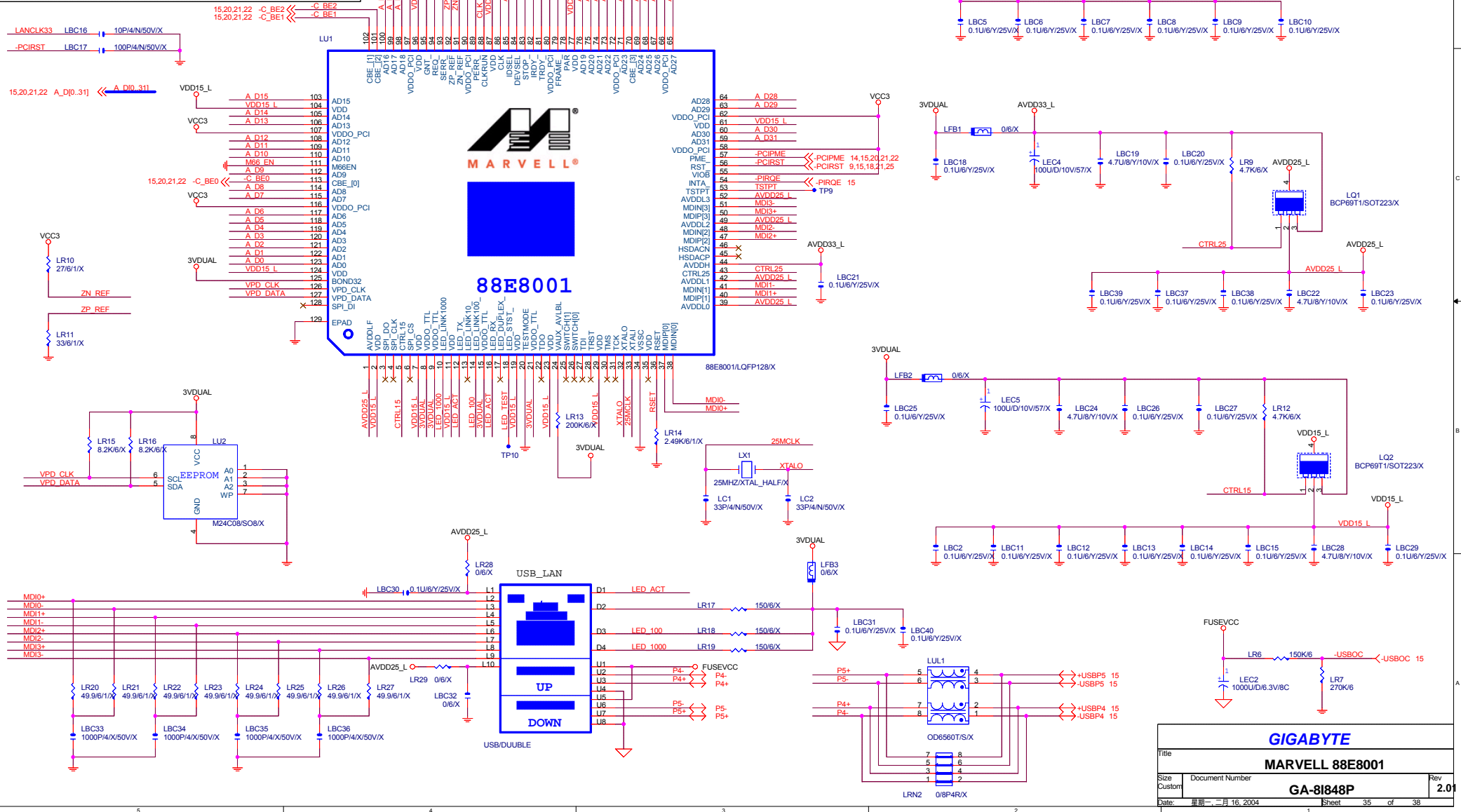


Big Copper to GND

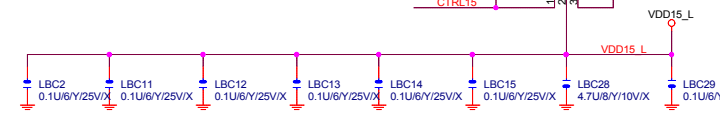
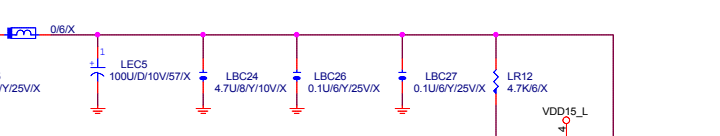
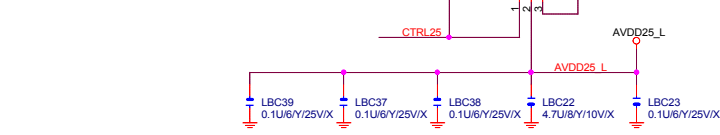
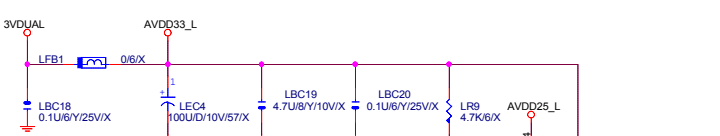
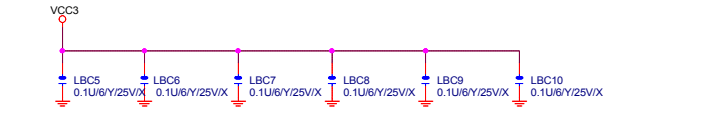
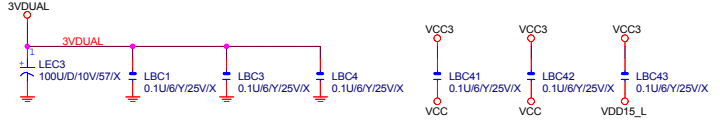
GIGABYTE CORP.		
Title		
Misc. PWR & ATX CONN.		
Size B	Document Number	Rev
	GA-8I848P	2.01
Date:	Sheet 34	of 38

Layout Check 注意事項

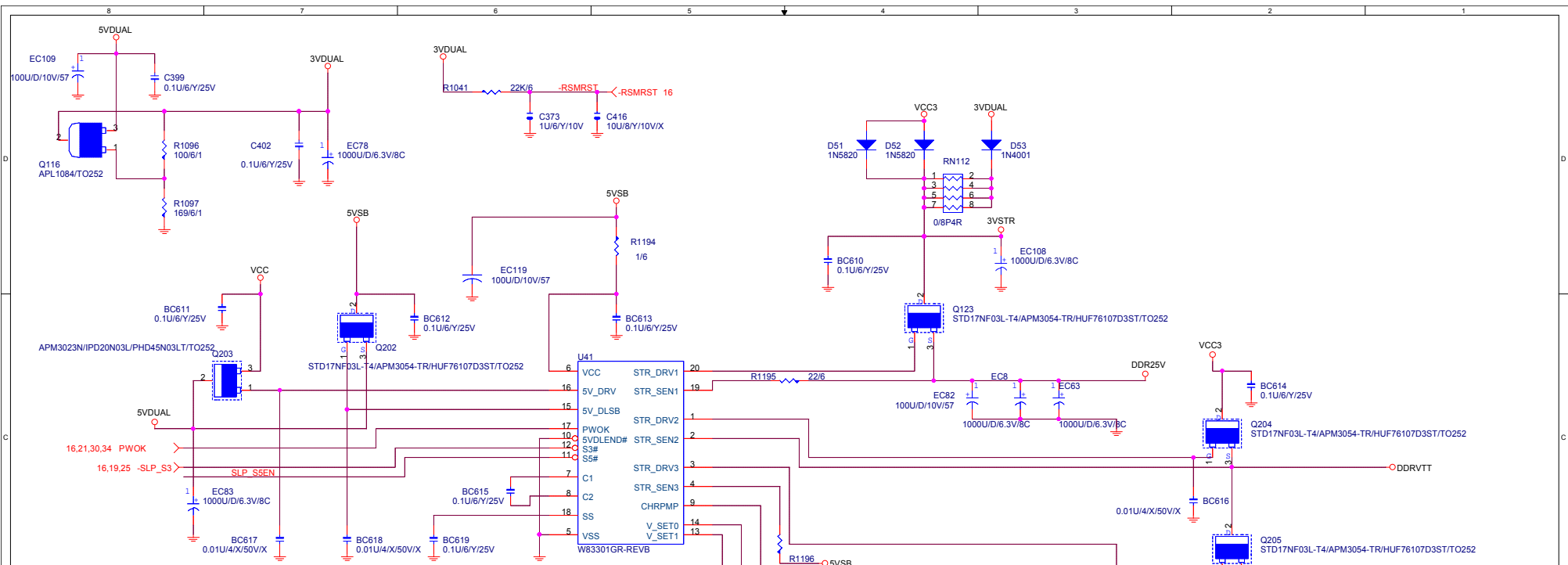
1. LU1 PIN129 需下內層GND,打 12 VIA
2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8, 每對之間保持 40mil



POWER DECOUPLING CAP.



GIGABYTE		
MARVELL 88E8001		
Title	Document Number	Rev
	GA-81848P	2.01
Date	日期: 二月 16, 2004	Sheet 35 of 38

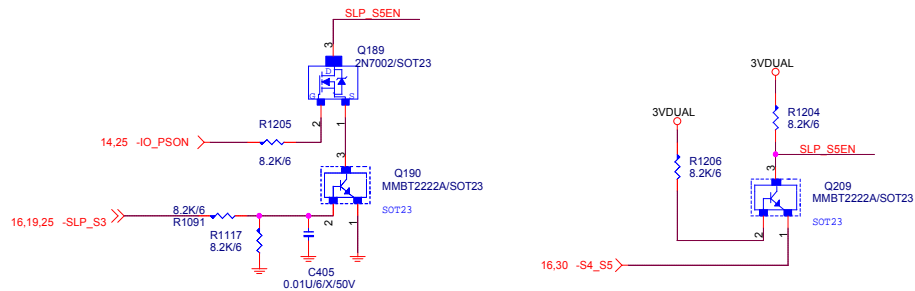


1.25V VTT_DDR LINEAR SOLUTION

DDROVP1, DDROVP2, DDROVP3 RESUME WELL DEFAULT HIGH

	DDROVP2	DDROVP1	DDROVP3	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V
2.8V	HIGH	HIGH	LOW	2.5V	0V

FOR 2.8V BIOS PROGRAMMING 時須先PROGRAMMING 2.5V後再PROGRAMMING 2.8V



GIGABYTE GA-8I848P PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT	
PCI SLOT1	16	C,F,G,A	PCLK0	REQ0-	GNT0-	
PCI SLOT2	17	F,G,A,C	PCLK1	REQ1-	GNT1-	
PCI SLOT3	18	G,A,C,F	PCLK2	REQ2-	GNT2-	
PCI SLOT4	19	A,C,F,G	PCLK3	REQ3-	GNT3-	
PCI SLOT5	20	C,F,G,A	PCLK4	REQ4-	GNT4-	
LAN (Marvell)	25	E	LANCLK33	-REQ5 (REQB#)	-GNT5 (GNTB#)	

GIGABYTE CORP.		
Title		
PCI ROUNT LIST		
Size	Document Number	Rev
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GIGABYTE GA-8I848P GPIO LIST

SHEET

TITLE

GPIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CASPME.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL,-SMBALERT.
GPI12	I	PULL 8.2K TO VCC3,M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3,PANEL S3 POWER LED.

SHEET

TITLE

GPIP	I/O	FUNCTION
GPO16		PULL 8.2K TO VCC3
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, LAN 100/10 DETECT.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GPO28		PULL 8.2K TO 3VDUAL